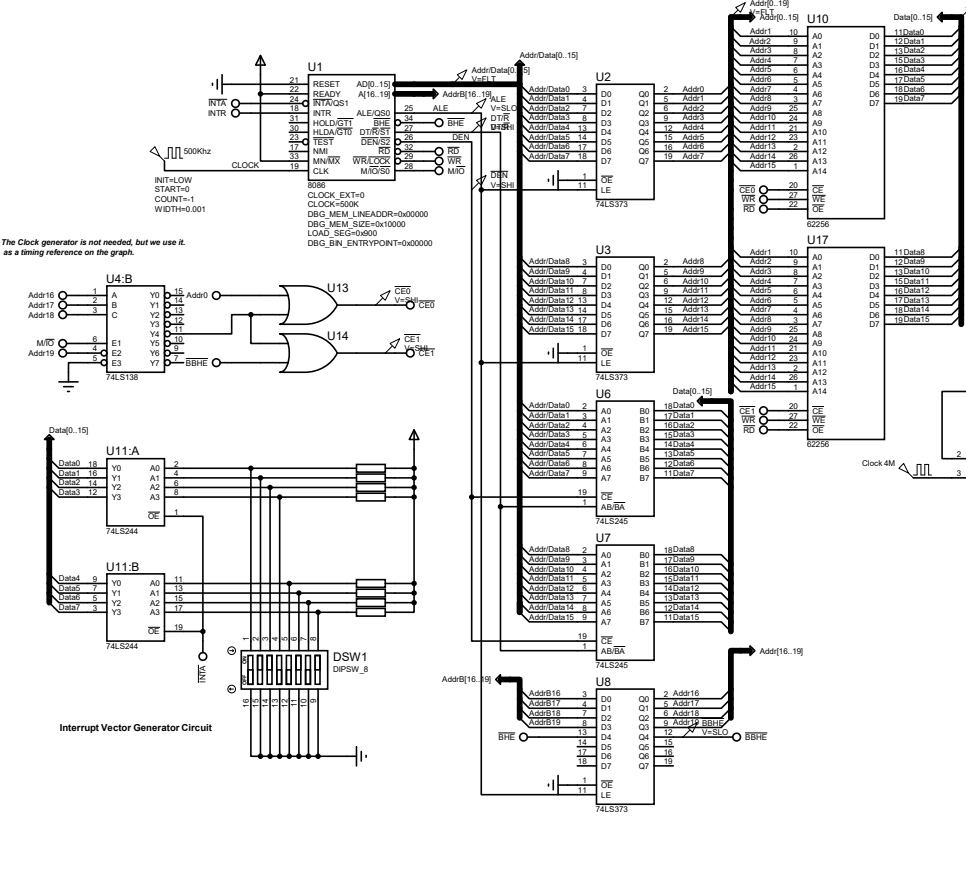
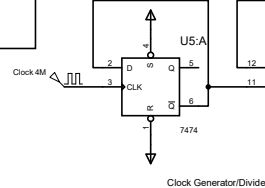


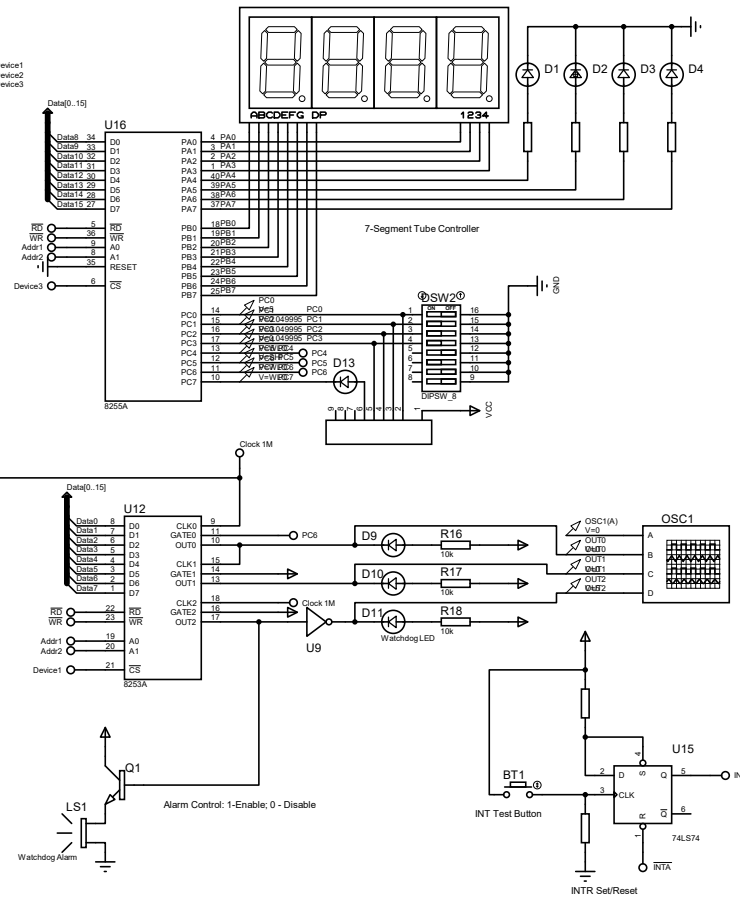
The Clock generator is not needed, but we use it as a timing reference on the graph.



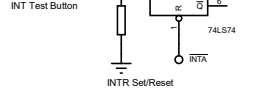
I/O Space Port Address Decoder Circuit



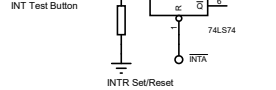
Clock Generator/Divider



7-Segment Tube Controller



Alarm Control: 1-Enable, 0-Disable

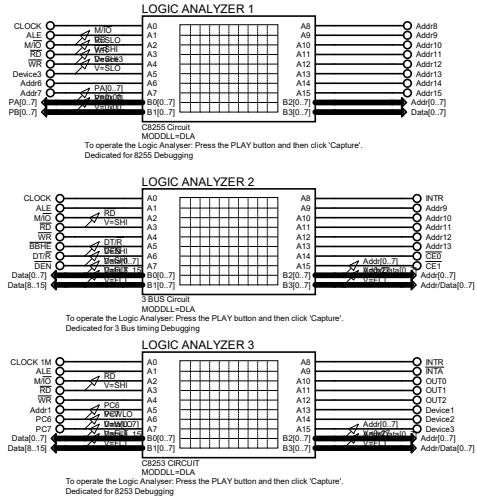


Watchdog Alarm

Debugging facilities

The equipment here help you debug the system software and hardware cooperation.

The Digital Graph illustrates the signal timing for your reference.



To operate the Logic Analyzer: Press the PLAY button and then click 'Capture'. Dedicated for 8255 Debugging

To operate the Logic Analyzer: Press the PLAY button and then click 'Capture'. Dedicated for 3 Bus timing Debugging

To operate the Logic Analyzer: Press the PLAY button and then click 'Capture'. Dedicated for 8253 Debugging

