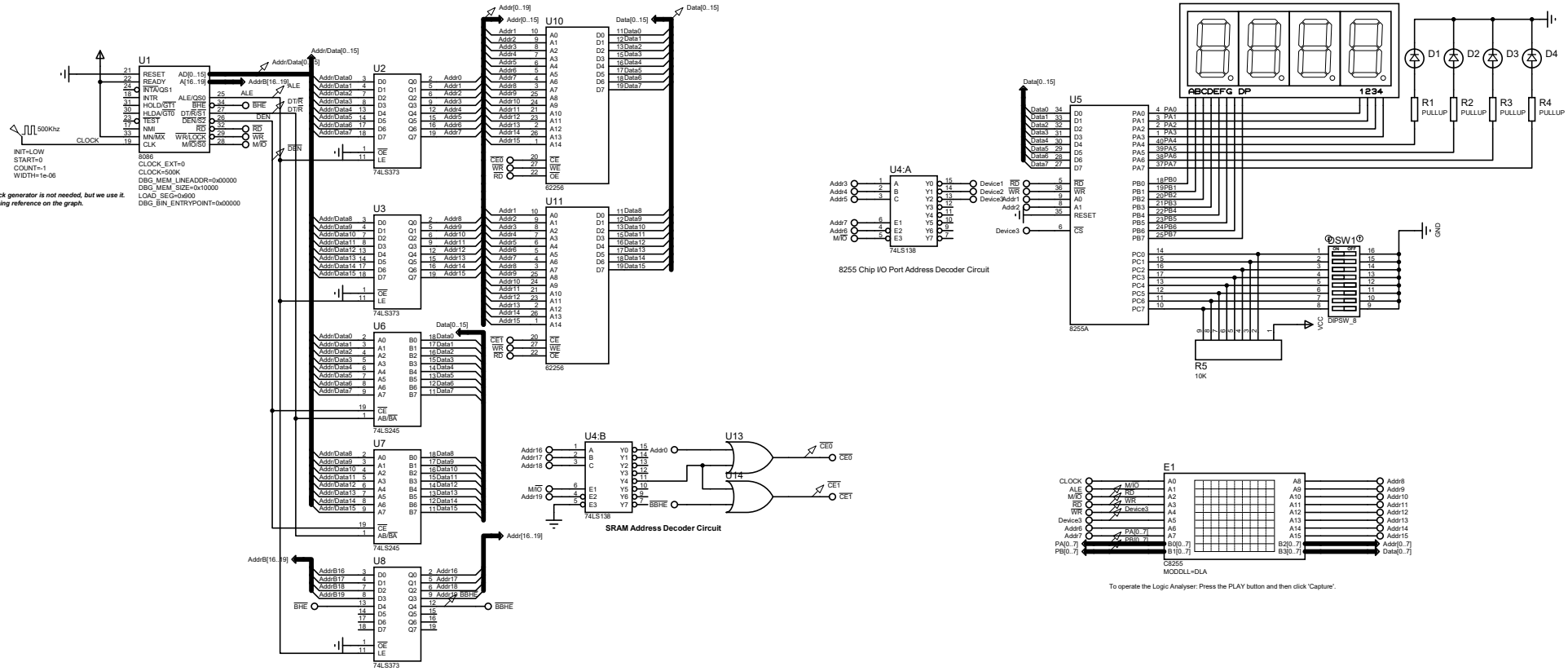
U1
8086
CLOCK_EXT=0
CLOCK=500K
DBG_MEM_LINEADDR=0x00000
DBG_MEM_SIZE=0x10000
LOAD_SEG=0x900
DBG_BIN_ENTRYPOINT=0x00000
500Khz
CLOCK
INIT=LOW
START=0
COUNT=-1
WIDTH=1e-06
The Clock generator is not needed, but we use it. as a timing reference on the graph.
U2
U3
U6
U7
U8
U10
U11
74LS373
74LS245
62256
U4:A
74LS138
8255 Chip I/O Port Address Decoder Circuit
U5
8255A
DSW1
DIPSW_8
R5
10K
D1
D2
D3
D4
R1
R2
R3
R4
PULLUP
U4:B
U13
U14
SRAM Address Decoder Circuit
E1
C8255
MODDLL=DLA
To operate the Logic Analyser: Press the PLAY button and then click 'Capture'.
E2
3BUS
MODDLL=DLA
To operate the Logic Analyser: Press the PLAY button and then click 'Capture'.
C8255 DIGITAL ANALYSIS
500Khz
ALE
M/IO
Addr/Data[0..15]
Addr[0..19]
Data[0..15]
RD
WR
DT/R
DEN
CE1
CE0
Device3
BBHE
PA[0..7]
PB[0..7]
FE
00
3F
300u
350u
400u
450u
500u
550u
600u
650u
700u
750u
800u
850u