NYCU EE-VLSI 2022

Lab1: A CMOS multiplexer: Hspice Simulation

Due at 2022/10/28 12:00

I. CMOS Driving Strength

Please measure the rising time***(Tr)*** of example inverter in 3 different capacitive loading, i.e. *10fF*, *20fF*, and *30fF*.

Rising time is defined as the timing change of voltage *from 0.2v to 1.6v.*

(Hint: you can use Hspice command *.alter* and *.measure* to generate the output voltage curve, and **display it on 1 graph**, then measure the output rising time.)

- Given an input of falling edge and observe the rising output of inverter. (wp&wn=0.24u)
- Input spec: Von: 1.8v Vss: 0v Vfall: 0.1n

Questions:

1. What do you observe the difference of output rising time when altering the output load? Please explain it in detail.
2. How to improve the driving capability of an inverter when the next stage's input capacitance is large? What is the side effect of your method?

II. CMOS Transfer Characteristics

Fig 2.26(c) is an inverter operating at beta ratio 1, please test the example inverter (output loading 10f) and find out the width ratio of the PMOS and NMOS when the inverter working on this point C(both Vin and Vout are Vdd/2). Also, please demonstrate VTC of inverter with width ratio beta 2 and 0.5. Please display the DC transfer curve like Fig 2.26(c). (Hint: you can use the hspice command .dc)

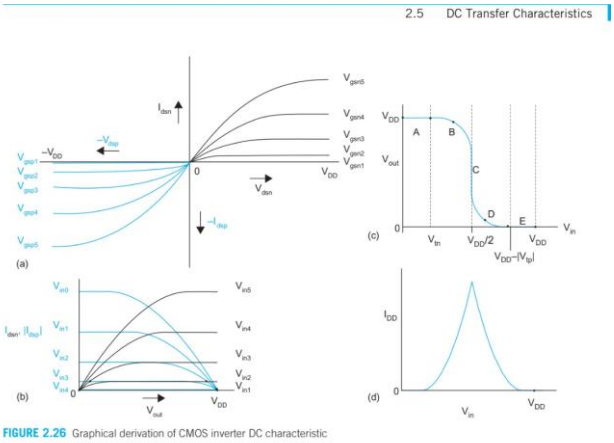

FIGURE 2.26 Graphical derivation of CMOS inverter DC characteristic

Questions:

1. Compare the results of beta 2, 0.5, and your finding width ratio, what do you observe? Is that the same as the beta ratio that textbook suggests, i.e. 2, for your decision in PMOS width? What is the main reason leading to this?
2. Observe the current in Fig 2.26(d), what's the reason we want to keep the PMOS size to let the inverter work on this point C? (Hint: you can mention in these perspectives, power, speed, or noise margin)

III. CMOS Logic Gate Design

Please Design a CMOS 2:1MUX with a tristate buffer. The design specifications are given as follows:

- Circuit name: MUX (MUX.sp)
- Input port: A, B, SEL, EN
- Output port: Y
- Please name your MUX circuit in following order :

.subckt MUX A B SEL EN Y

The specification is described as the following:

- ✓ Rise time and fall time of input signal: **0.1ns**
- ✓ Supply voltage: **1.8V**
- ✓ Output loading of Y: **10fF**
- ✓ ***Bonus: Attach D flip-flop after MUX (+10%) (MUX_seq.sp)***

  Note:

  1. You can modify clock rate as you wish in this part, but just make sure the logic output value corrects.
  2. Please change input value (into multiplexer) at clock negative edge, and check output value (out of D flip-flop) at next clock negative edge.

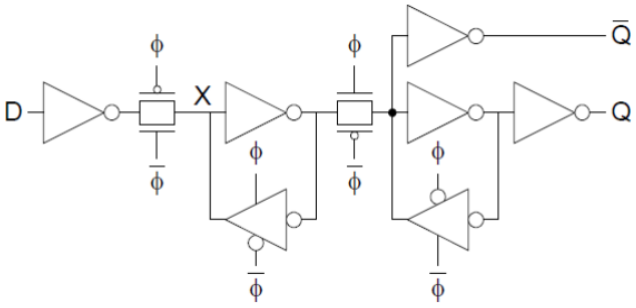

Fig.1 Schematic of D Flip-Flop (positive trigger)

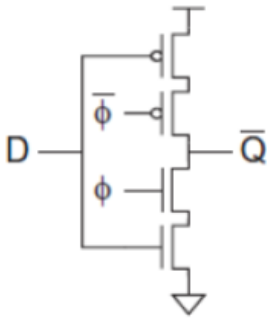

Fig.2 Schematic of tristate INV

Questions:

1. Explain why there are glitches in MUX combinational circuit sometimes, and how to fix it. Is it harmful for your overall design?

2. Explain how you decide MOSFETs' width with fixed channel length in your circuit (Hint: explain with mobility of PMOS NMOS, prove it with HSPICE)?

IV. Grading Policy:

1. code: 20%
2. Report: 80% (include all the following items)
   (1) Summary of your structure
   (2) Output waveform with at least nine different setting (three different output loading * three different MOS width) for the multiplexer. What you observe?
   (3) Describe how you measure the average power, propagation delay, rise, and fall time. You should show your code, e.g. propagation delay:
   .meas tran tprop trig v(?) val='?' rise=? targ v(?) val='?' rise=?
   (4) Answer all the questions

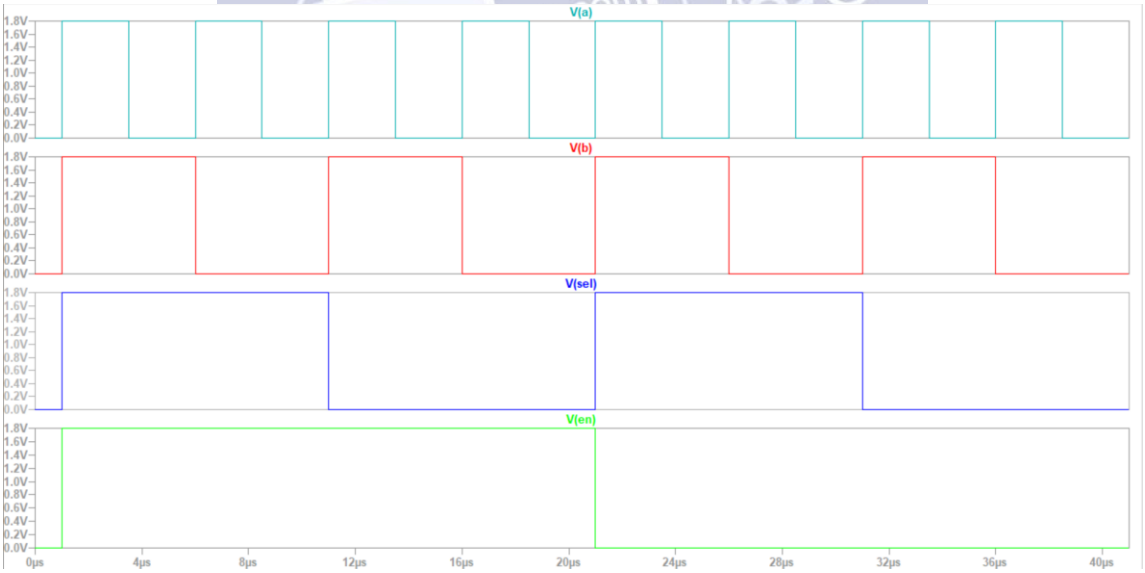

Fig. 3 Example of input signals for MUX

Note:

1. Copy the files to your own account：
   "tar -xvf ~vlsita01/HW1.tar"
2. Enjoy the fun from this assigned work
3. Accept late homework within 1 week (till 2022/11/5 12:00), and your total score will be*0.7.