NCTU EE-VLSI 2022

HW02: multiplexer Standard Cell Layout

Due at 2022/12/19 12:00

I. Layout dependent parasitic:

Use the inverter in HW02/Example. Follow the steps in Layout_tutorial.pdf

Please build up a buffer with 2 inverter shared diffusion and without shared diffusion. Compare the propagation delay, rising time , falling time, area and power for each other.

What's your observation in post-sim, is that the same as the lecture?

(You should check DRC/LVS by yourself, and attached your layout with ruler in report.)
(You can determine W/L by yourself, but it should be reasonable for comparison.)

II. Long metal wire:

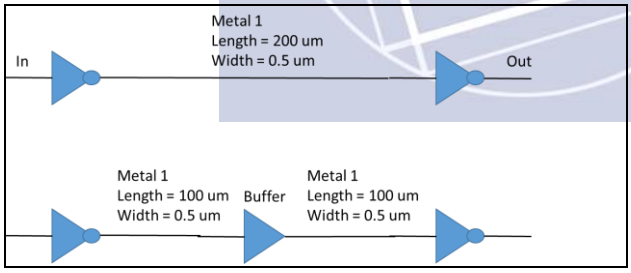
Use the inverter in HW02/Example. Please draw a layout with following circuit.

Compare the propagation delay(post-sim) for a long metal line with and without buffer.

What's your observation, is that the same as the lecture? What's the reason?

(You should check DRC/LVS by yourself, and attached your layout with ruler in report.)

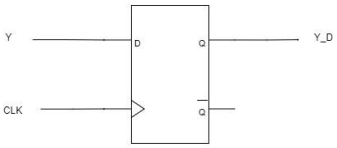
(You can determine W/L by yourself, but it should be reasonable for comparison.)

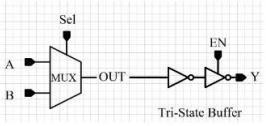


III. Logic gate

Enter the folder in HW02/Exercise, please design a multiplexer with a tristate buffer.
Then, attach D flip-flop after multiplexer. The design specifications are given as follows:

1. Circuit name: MUX (MUX_seq.sp)
2. Input port: A, B, SEL, EN CLK
3. Output port: Y_D
4. Please name your MUX circuit in following order :
   .subckt MUX A B SEL EN Y_D CLK

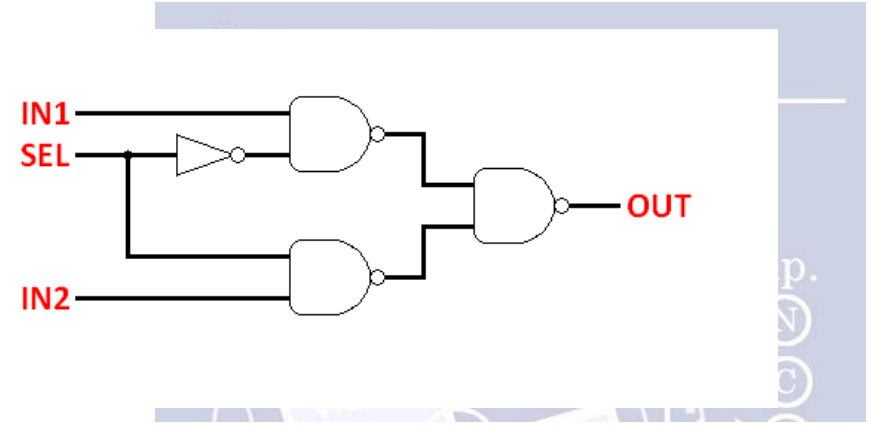




5. Multiplexer output must be A when SEL=0, and be B when SEL=1.
6. Input signal must follow fig.3 input signal with A period=5us tdelay=1us and rise fall time =0.1ns, do not modify the input signal, or you will fail the demo.
7. Use the code below to generate input signal

```
V1 A 0 PULSE(0 1.8 1u 0.1n 0.1n 2.5u 5u)
V2 B 0 PULSE(0 1.8 1u 0.1n 0.1n 5u 10u)
V3 SEL 0 PULSE(0 1.8 1u 0.1n 0.1n 10u 20u)
V4 EN 0 PULSE(0 1.8 1u 0.1n 0.1n 20u 40u)
V5 CLK 0 PULSE(0 1.8 0.3u 0.1n 0.1n 0.5u 1u)
```

8. MUX, DFF, and Tristate INV should be only used by the following schematic below. Anyone used different architecture would fail the demo.



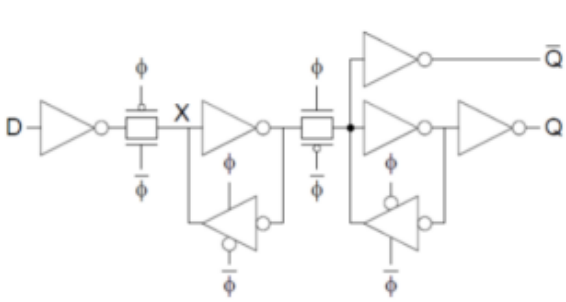


Fig.1 Schematic of D Flip-Flop (positive trigger)

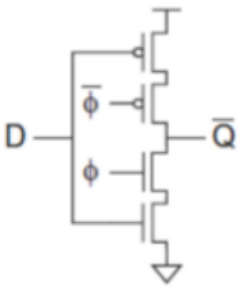


Fig.2 Schematic of tristate INV

The specification is described as the following:

1. Output loading of Y_D: 10fF
2. Supply voltage: 1.8V
3. Pre-simulation (Hspice):
   worst case needs to meet following requirements (TT corner)
   (1) Longest rise and fall time of node Y: < 0.6ns
   (2) Maximum propagation delay, i.e. input to Y< 1ns
   (3) Average power: 0~100uw (with given pattern) in 0~30us

(Note that timing for Trise, Tfall, Tprop is specified to output of MUX(node Y), not output of DFF(Y_D).)

Any violation of above SPEC will fail the demo.

4. Layout style and restriction:

   This design will be requested to follow the standard cell layout and the layout shape of MUX is shown as follows:

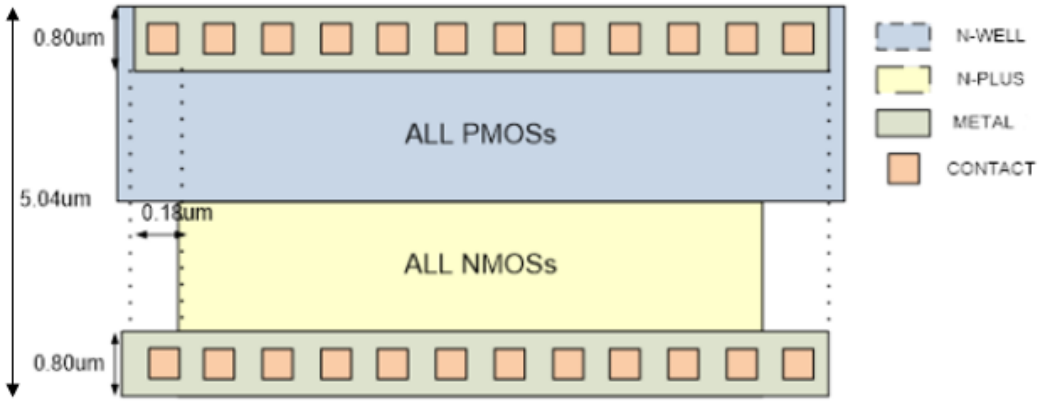


Fig.1 Layout shape

5. The specifications of layout:
   (1) The whole layout shape (except NWell) has to be fixed in layout height.
   (2) The layout height should be fixed to be 5.04um.
   (3) The metal width of VDD & GND rails should be fixed to be 0.8um.
   (4) Power rails should be placed at the top (VDD) and bottom (GND) of your layout design.
   (5) All PMOSs and NMOSs should be limited to locate in opposite parts.
   (6) About usage of metal, only metal 1~metal 3 are allowed.
   (7) Please use static CMOS logic gates
   (8) If your DFF need to be reset before use, please reset, TA will not check the signal before 1us.

Discussion:

1. How to reduce your area of layout? What are advantages and disadvantages of reducing area?
2. Summary of your structure including whole layout of multiplexer
3. List rise time, fall time and propagation delay of all conditions with highlighting of the worst case, and average power

IV. Grading Policy:

1. **Layout dependent parasitic (20%)**
2. **Long metal wire (20%)**
3. **Logic gate (60%)**
   - **i.** Layout spec check (10%) (attached layout with ruler in report)
   - **ii.** DRC, LVS (16%) (8% for each) (attached result in report)
   - **iii.** Post-sim waveform correctness (24%) (attached waveform in report)
   - **iv.** Performance (15%) (Area ranking, those who fail the above will not be included)
   - **v.** Discussion (5%)

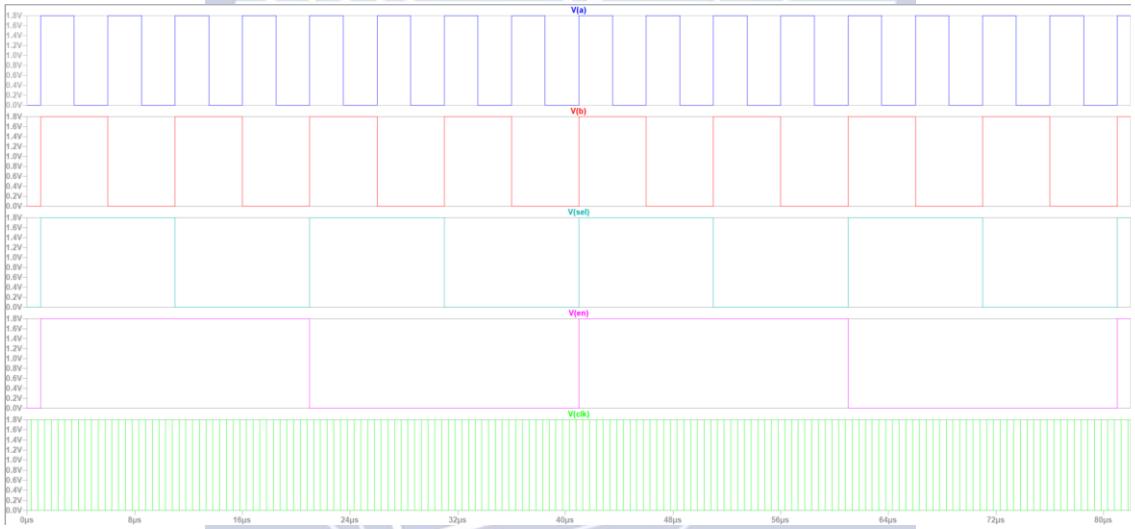


Fig. 3 Input signals

Note:

1. Copy the files to your own account：
   "tar -xvf ~vlsita01/HW02.tar"
2. You need to hand in the following files on New E3:

File	Description
studentID_MUX_seq.gds	From LVS directory.
studentID_ MUX_seq.sp	Pre-sim design.
studentID_report.pdf	PDF format, others are forbidden

3. Naming error rules: (You will get 5-point penalty if you break any of the following rules)
   (1) File names are consistent with the table above. DON'T submit compressed files.
   (2) Please use P_18_G2 and N_18_G2 as MOS model in studentID_MUX_seq.sp
   (3) Do NOT modify port names, MUX A B SEL EN Y_D CLK in your pre-sim file and layout.

4. Any question about HW02 should be posted on Facebook group, rather than directly send emails to TA.
5. Enjoy the fun from this assigned work

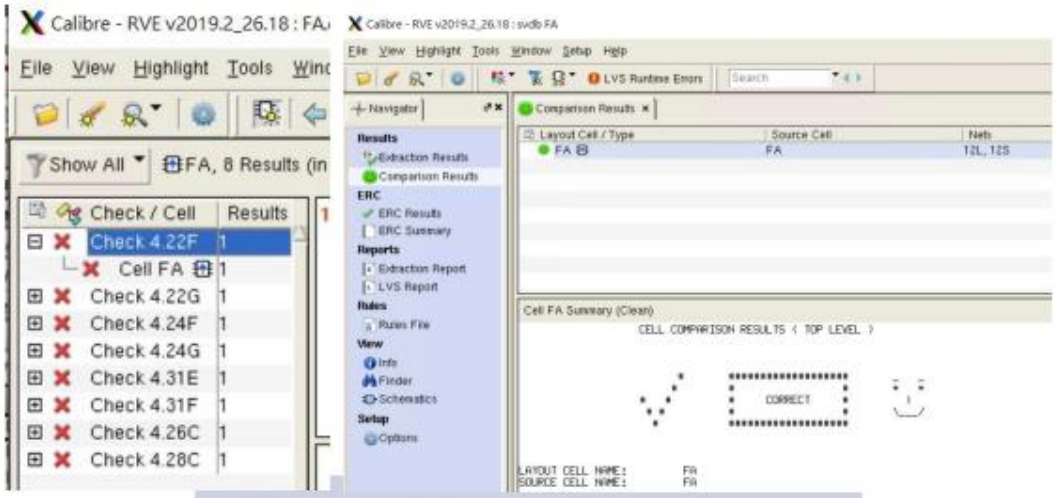


Fig2. right DRC and LVS result