PIPELINING DEMONSTRATION

Step 1 — Set switch SW [9:8] = 10: This displays the retired PC.

As the CPU executes instructions, every instruction retiring from the WB stage increments the PC. Because the processor is pipelined, a new PC appears every clock cycle unless the pipeline stalls. This shows multiple instructions are active at once.

LEDs cycle extremely fast — showing continuous WB completion.

Step 2 — Set switch SW [9:8] = 11: [retire_valid] [register being written]

Every WB-stage write shows up on the LEDs. Because this happens nearly every cycle, we can see that the CPU is retiring instructions continuously, proving pipelining is active.

LEDs flickering with register numbers, proving the WB stage is firing repeatedly.

Step 3 — Press reset (KEY0)

Reset flushes the pipeline. You'll see the retirement PC return to 0 and register writes restart. The behavior changes instantly, demonstrating pipeline flush.

Step 4 — Watch what happens on pipeline stalls

During multiply, there are branches in every iteration. The pipeline flushes IF/ID and ID/EX. You'll see the PC LEDs pause or jump — that's the pipeline flushing due to control hazards.

Flashing that pauses briefly during branches → PROOF of pipeline bubble insertion.

Continuous instruction retirement: LED PC increments every cycle

Pipeline stalls visible: LED PC pauses during hazards in multiply loop

Register writebacks every cycle: LED register-number activity in mode 11

Pipeline flushing: during branch/jump, PC on LEDs jumps, register writes pause for one cycle