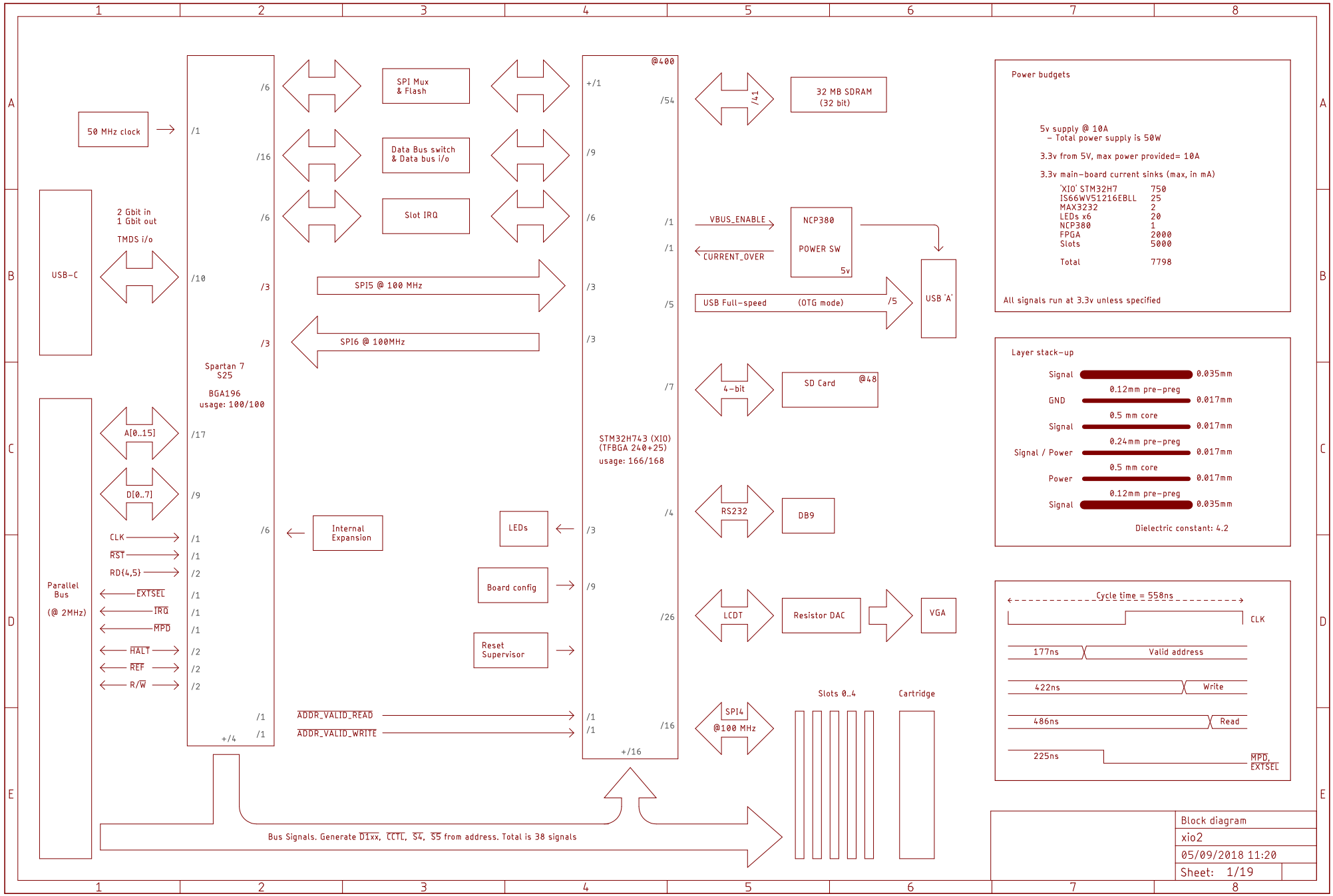


Power budgets

5v supply @ 10A
– Total power supply is 50W

3.3v from 5V, max power provided= 10A

3.3v main-board current sinks (max, in mA)

'XIO' STM32H7	750
IS66WV51216EBLL	25
MAX3232	2
LEDs x6	20
NCP380	1
FPGA	2000
Slots	5000
Total	7798

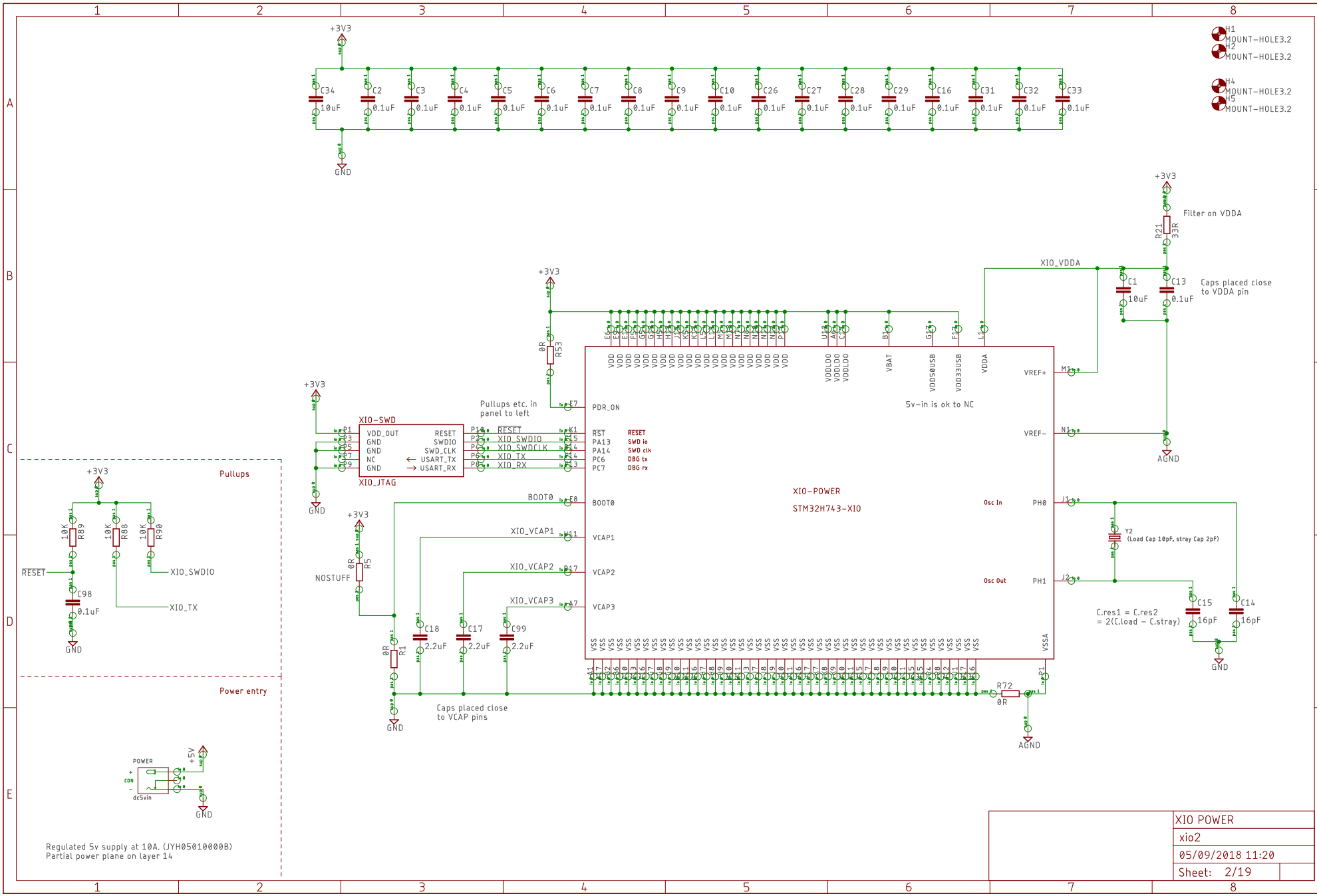
All signals run at 3.3v unless specified

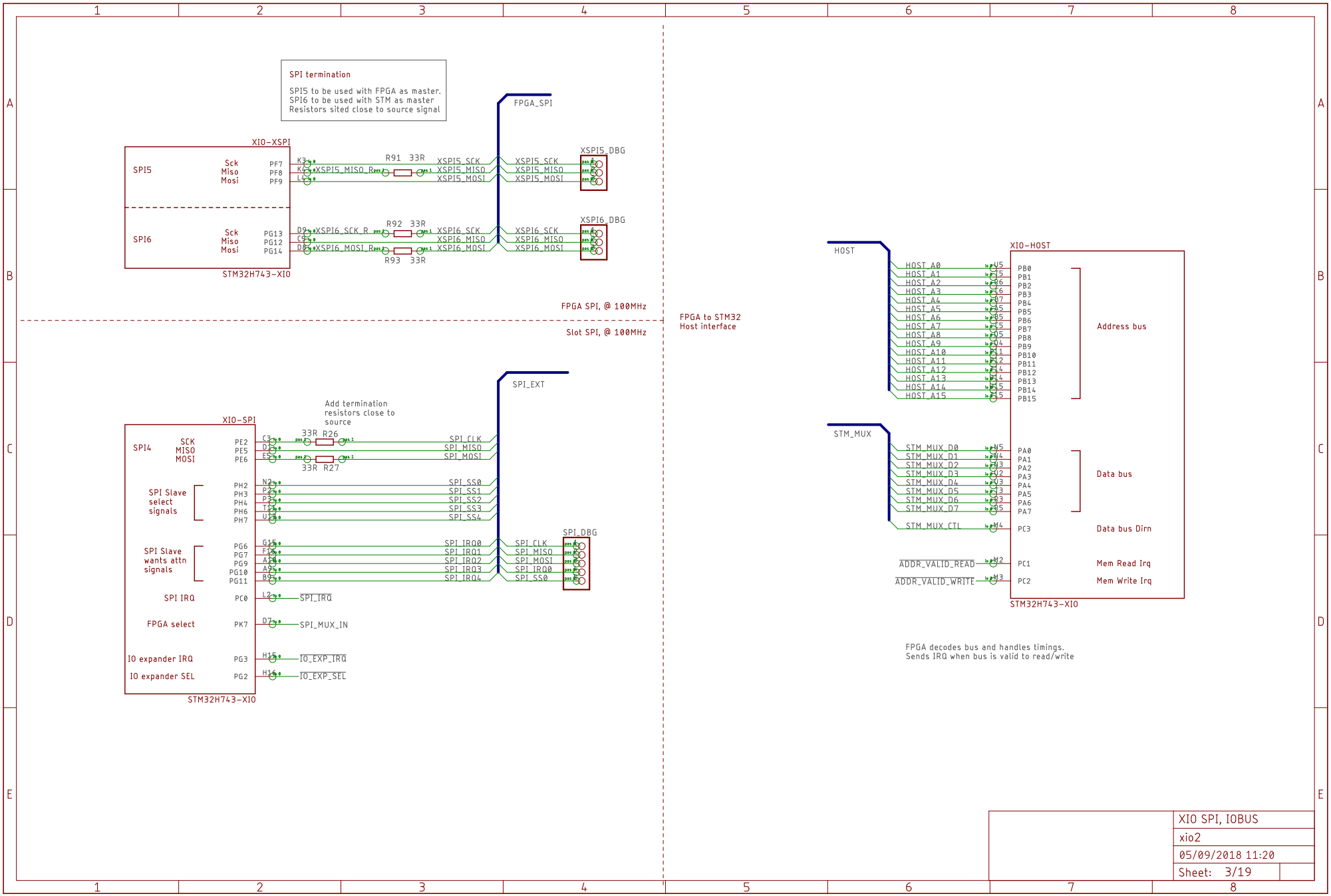
Layer stack-up

Signal		0.035mm
	0.12mm pre-preg	
GND		0.017mm
	0.5 mm core	
Signal		0.017mm
	0.24mm pre-preg	
Signal / Power		0.017mm
	0.5 mm core	
Power		0.017mm
	0.12mm pre-preg	
Signal		0.035mm

Dielectric constant: 4.2

Block diagram	
xio2	
05/09/2018 11:20	
Sheet: 1/19	


+3V3
C34 10uF
C2 0.1uF
C3 0.1uF
C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C26 0.1uF
C27 0.1uF
C28 0.1uF
C29 0.1uF
C16 0.1uF
C31 0.1uF
C32 0.1uF
C33 0.1uF
GND
H1 MOUNT-HOLE3.2
H2 MOUNT-HOLE3.2
H4 MOUNT-HOLE3.2
H5 MOUNT-HOLE3.2
Filter on VDDA
R21 33R
XIO_VDDA
C1 10uF
C13 0.1uF
Caps placed close to VDDA pin
AGND
R53 0R
Pullups etc. in panel to left
5v-in is ok to NC
XIO-SWD
VDD_OUT
GND
NC
RESET
SWDIO
SWD_CLK
USART_TX
USART_RX
XIO_JTAG
XIO_SWDIO
XIO_SWDCLK
XIO_TX
XIO_RX
PDR_ON
RST
PA13
PA14
PC6
PC7
SWD io
SWD clk
DBG tx
DBG rx
BOOT0
XIO_VCAP1
XIO_VCAP2
XIO_VCAP3
VCAP1
VCAP2
VCAP3
XIO-POWER
STM32H743-XIO
VREF+
VREF-
VBAT
VDD50USB
VDD33USB
VDDA
VSSA
Osc In
Osc Out
PH0
PH1
Y2 (Load Cap 10pF, stray Cap 2pF)
C15 16pF
C14 16pF
C.res1 = C.res2 = 2(C.load - C.stray)
NOSTUFF
R5 0R
R1 0R
C18 2.2uF
C17 2.2uF
C99 2.2uF
Caps placed close to VCAP pins
R72 0R
Pullups
10K R89
10K R88
10K R90
RESET
C98 0.1uF
Power entry
POWER
dc5vin
+5V
Regulated 5v supply at 10A. (JYH05010000B)
Partial power plane on layer 14
XIO POWER
xio2
05/09/2018 11:20
Sheet: 2/19


SPI termination
SPI5 to be used with FPGA as master.
SPI6 to be used with STM as master
Resistors sited close to source signal
FPGA_SPI
XIO-XSPI
SPI5
Sck
Miso
Mosi
PF7
PF8
PF9
R91 33R
XSPI5_SCK
XSPI5_MISO_R
XSPI5_MISO
XSPI5_MOSI
XSPI5_DBG
SPI6
PG13
PG12
PG14
R92 33R
R93 33R
XSPI6_SCK_R
XSPI6_MOSI_R
XSPI6_SCK
XSPI6_MISO
XSPI6_MOSI
XSPI6_DBG
STM32H743-XIO
FPGA SPI, @ 100MHz
Slot SPI, @ 100MHz
FPGA to STM32
Host interface
SPI_EXT
XIO-SPI
SPI4
SCK
MISO
MOSI
PE2
PE5
PE6
Add termination
resistors close to
source
33R R26
33R R27
SPI_CLK
SPI_MISO
SPI_MOSI
SPI Slave
select
signals
PH2
PH3
PH4
PH6
PH7
SPI_SS0
SPI_SS1
SPI_SS2
SPI_SS3
SPI_SS4
SPI_DBG
SPI Slave
wants attn
signals
PG6
PG7
PG9
PG10
PG11
SPI_IRQ0
SPI_IRQ1
SPI_IRQ2
SPI_IRQ3
SPI_IRQ4
SPI IRQ
PC0
SPI_IRQ
FPGA select
PK7
SPI_MUX_IN
IO expander IRQ
PG3
IO_EXP_IRQ
IO expander SEL
PG2
IO_EXP_SEL
STM32H743-XIO
HOST
XIO-HOST
HOST_A0
HOST_A1
HOST_A2
HOST_A3
HOST_A4
HOST_A5
HOST_A6
HOST_A7
HOST_A8
HOST_A9
HOST_A10
HOST_A11
HOST_A12
HOST_A13
HOST_A14
HOST_A15
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PB8
PB9
PB10
PB11
PB12
PB13
PB14
PB15
Address bus
STM_MUX
STM_MUX_D0
STM_MUX_D1
STM_MUX_D2
STM_MUX_D3
STM_MUX_D4
STM_MUX_D5
STM_MUX_D6
STM_MUX_D7
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
Data bus
STM_MUX_CTL
PC3
Data bus Dirn
ADDR_VALID_READ
ADDR_VALID_WRITE
PC1
PC2
Mem Read Irq
Mem Write Irq
STM32H743-XIO
FPGA decodes bus and handles timings.
Sends IRQ when bus is valid to read/write
XIO SPI, IOBUS
xio2
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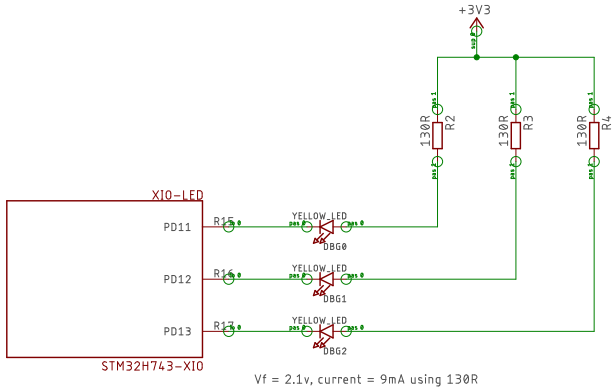
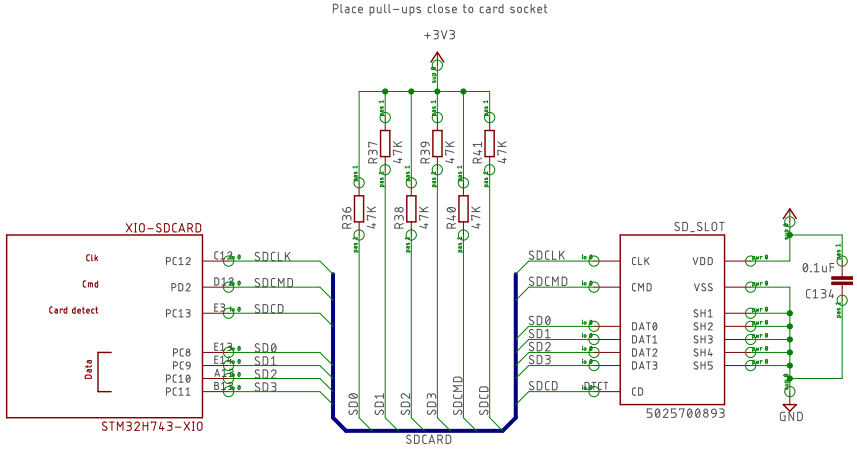
Sheet: 3/19

Debug LEDs

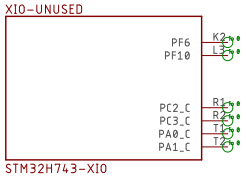


Vf = 2.1v, current = 9mA using 130R

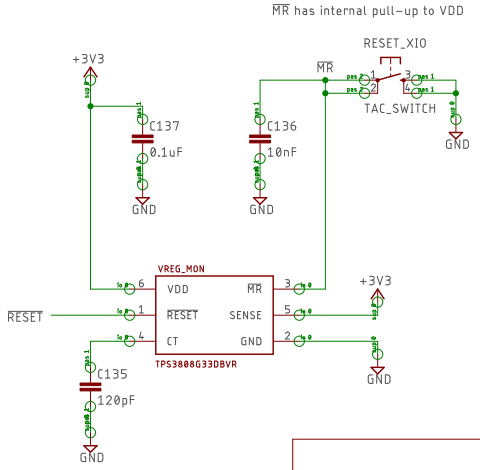
SD Card



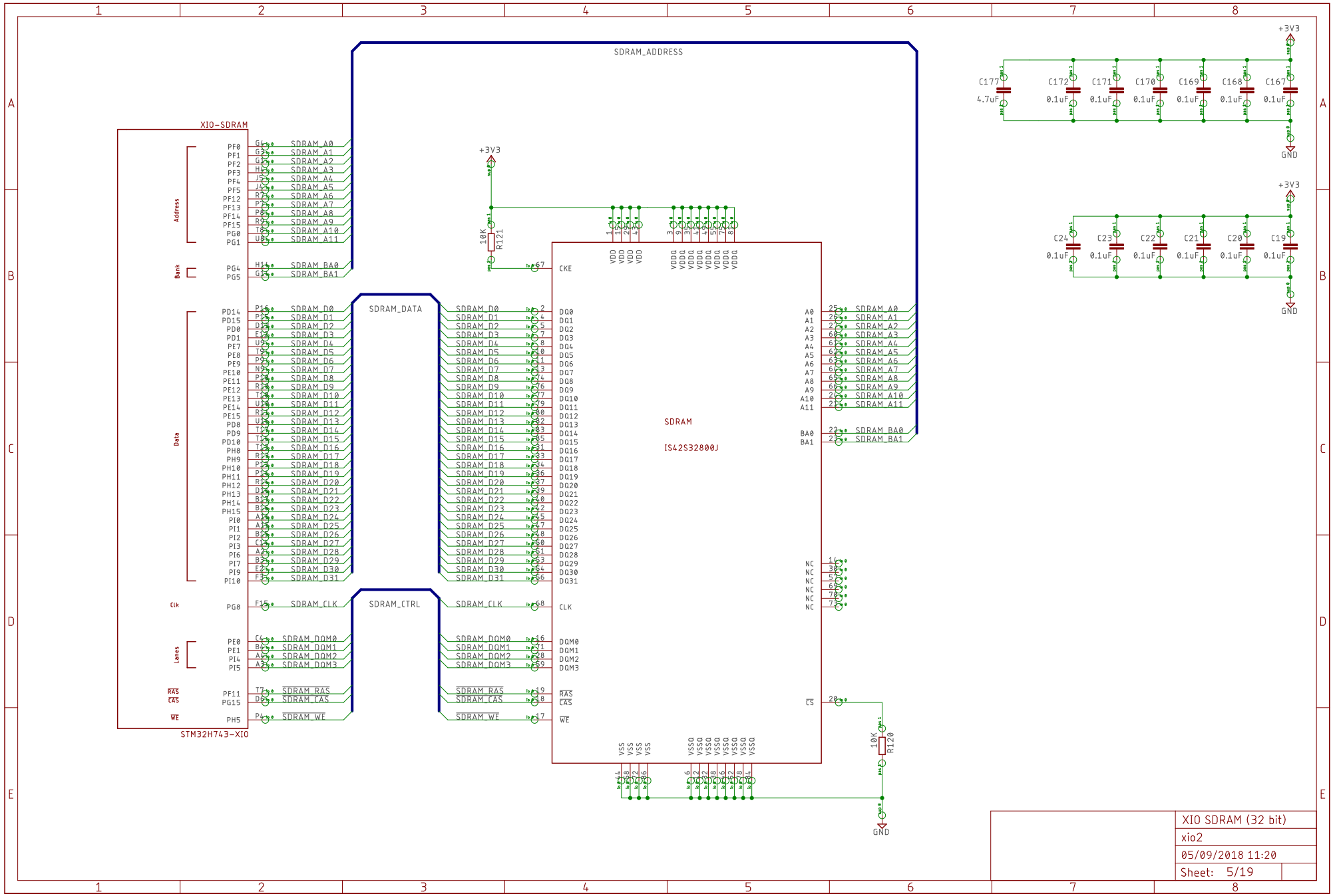
Unused pins



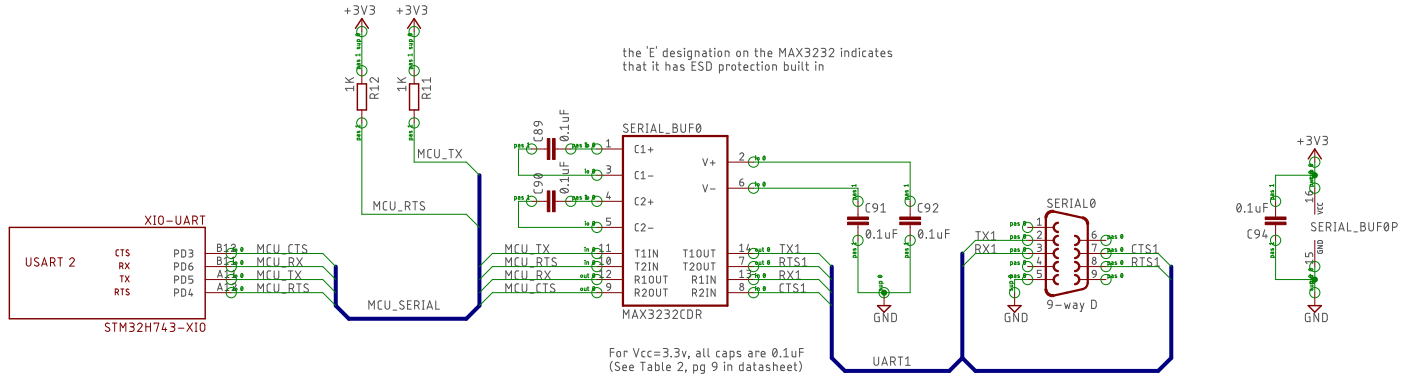
Reset monitor



	Reset, LEDs, SD, unused
	xio2
	05/09/2018 11:20
	Sheet: 4/19

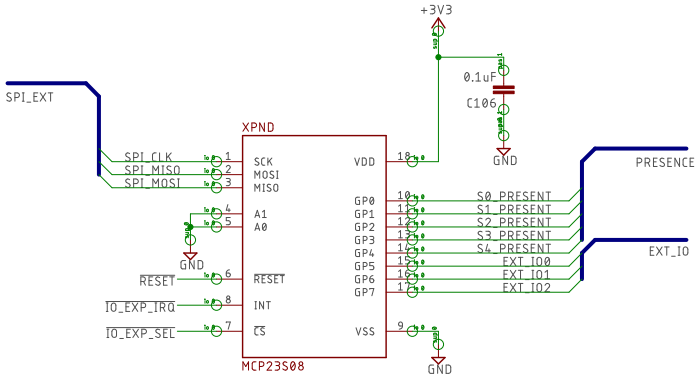


	XIO SDRAM (32 bit)
	xio2
	05/09/2018 11:20
	Sheet: 5/19

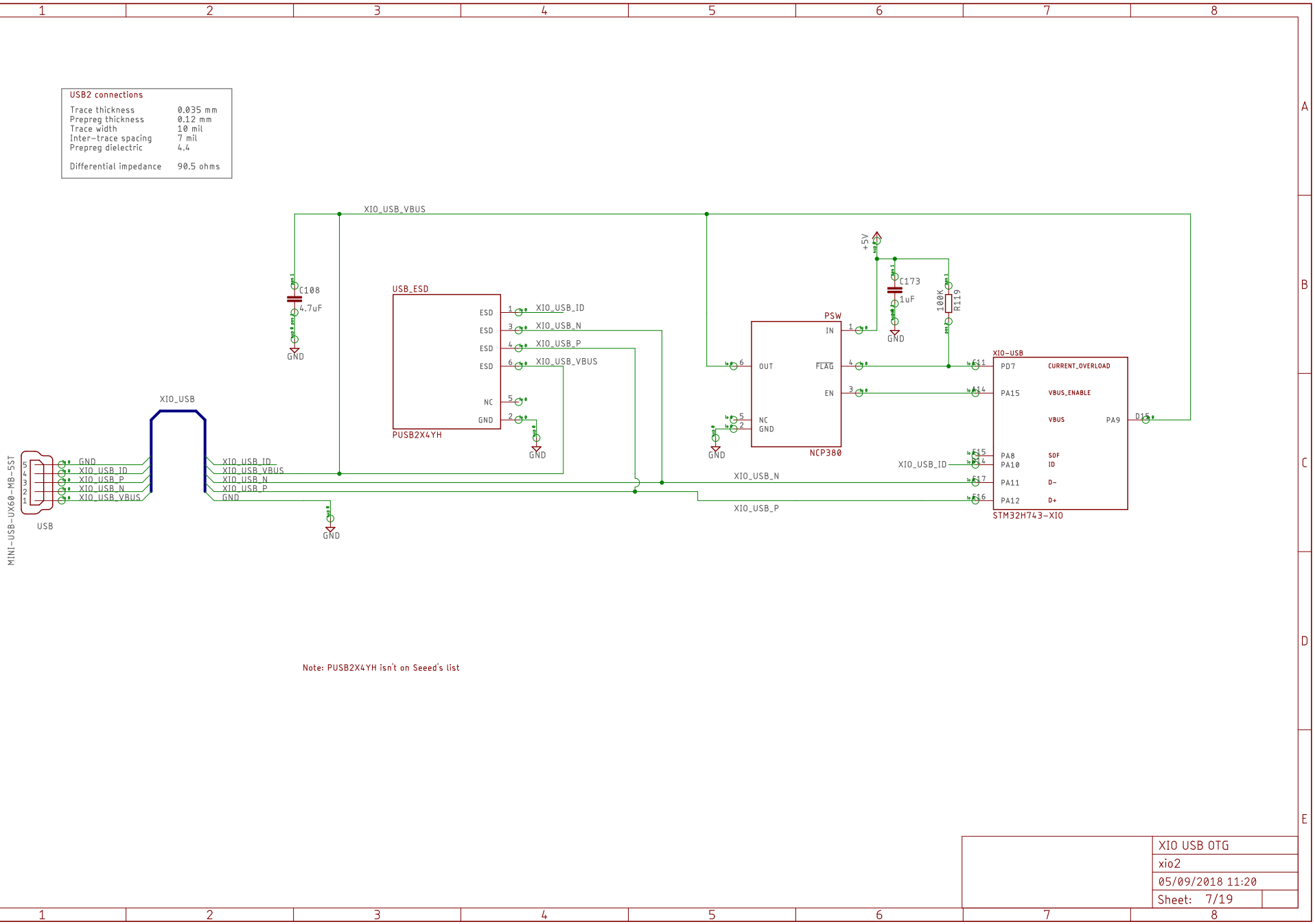


Serial I/O

Slot presence



	Serial IO / Slot presence
	xio2
	05/09/2018 11:20
	Sheet: 6/19


USB2 connections
Trace thickness 0.035 mm
Prepreg thickness 0.12 mm
Trace width 10 mil
Inter-trace spacing 7 mil
Prepreg dielectric 4.4
Differential impedance 90.5 ohms
XIO_USB_VBUS
C108
4.7uF
GND
USB_ESD
ESD
ESD
ESD
ESD
NC
GND
PUSB2X4YH
XIO_USB_ID
XIO_USB_N
XIO_USB_P
XIO_USB_VBUS
+5V
C173
1uF
100K
R119
PSW
IN
OUT
FLAG
EN
NC
GND
NCP380
XIO-USB
PD7
CURRENT_OVERLOAD
PA15
VBUS_ENABLE
VBUS
PA9
PA8
SOF
PA10
ID
PA11
D-
PA12
D+
STM32H743-XIO
XIO_USB
MINI-USB-UX60-MB-5ST
USB
GND
XIO_USB_ID
XIO_USB_P
XIO_USB_N
XIO_USB_VBUS
Note: PUSB2X4YH isn't on Seeed's list
XIO USB OTG
xio2
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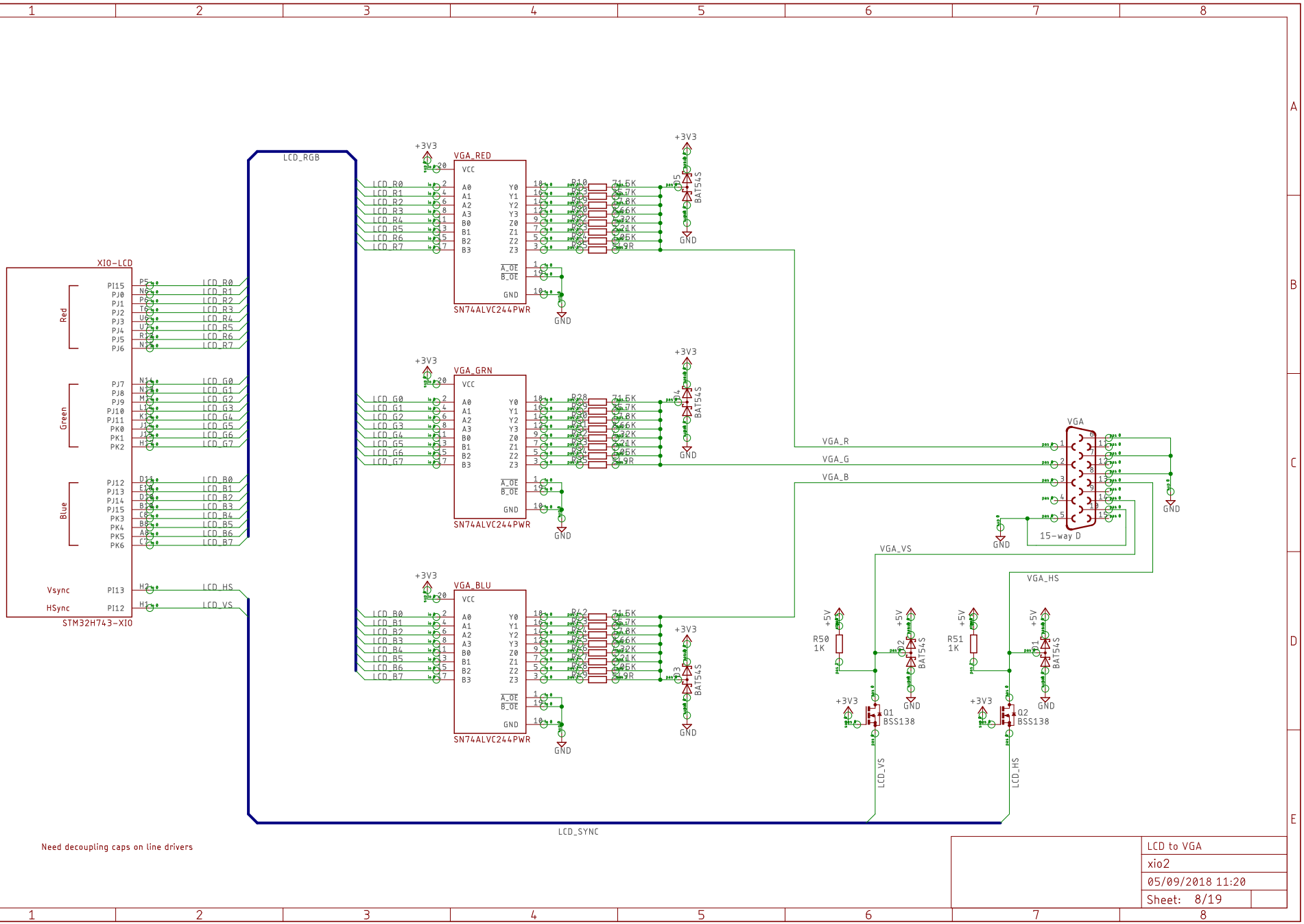
Sheet: 7/19


XIO-LCD
Red
Green
Blue
PI15
PJ0
PJ1
PJ2
PJ3
PJ4
PJ5
PJ6
PJ7
PJ8
PJ9
PJ10
PJ11
PK0
PK1
PK2
PJ12
PJ13
PJ14
PJ15
PK3
PK4
PK5
PK6
Vsync
PI13
HSync
PI12
STM32H743-XIO
LCD_R0
LCD_R1
LCD_R2
LCD_R3
LCD_R4
LCD_R5
LCD_R6
LCD_R7
LCD_G0
LCD_G1
LCD_G2
LCD_G3
LCD_G4
LCD_G5
LCD_G6
LCD_G7
LCD_B0
LCD_B1
LCD_B2
LCD_B3
LCD_B4
LCD_B5
LCD_B6
LCD_B7
LCD_HS
LCD_VS
LCD_RGB
LCD_SYNC
VGA_RED
VGA_GRN
VGA_BLU
SN74ALVC244PWR
+3V3
GND
A_OE
B_OE
R10
R20
R42
74.5K
36.7K
18K
9.66K
5.62K
3.32K
2.21K
1.65K
1.29R
D5
D4
D3
BAT54S
VGA_R
VGA_G
VGA_B
VGA
15-way D
VGA_VS
VGA_HS
R50
R51
1K
+5V
D2
D1
Q1
Q2
BSS138
LCD_VS
LCD_HS
Need decoupling caps on line drivers
LCD to VGA
xio2
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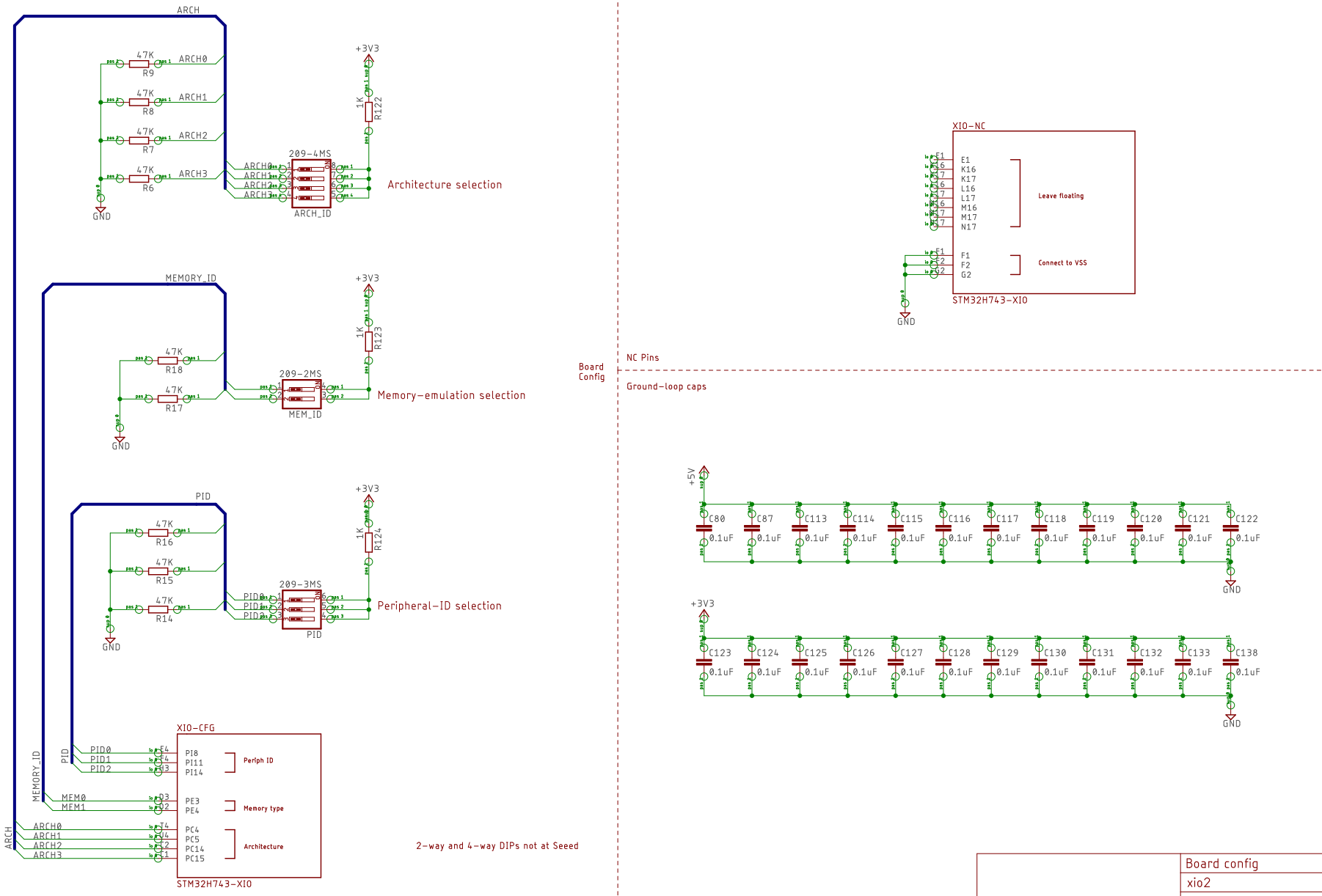
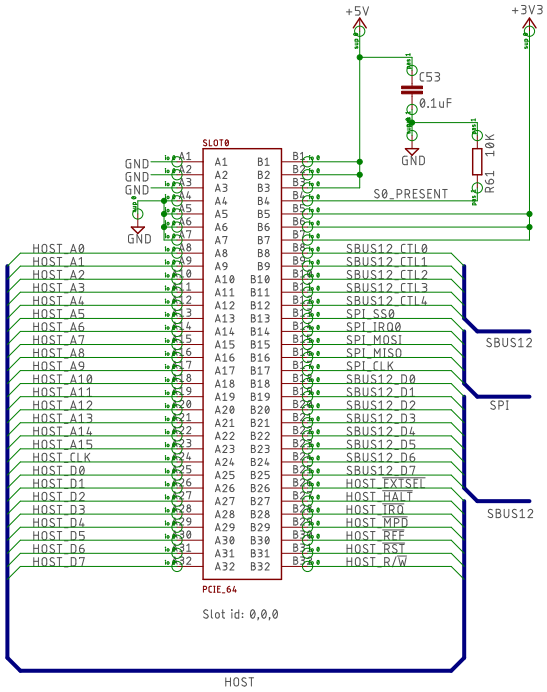
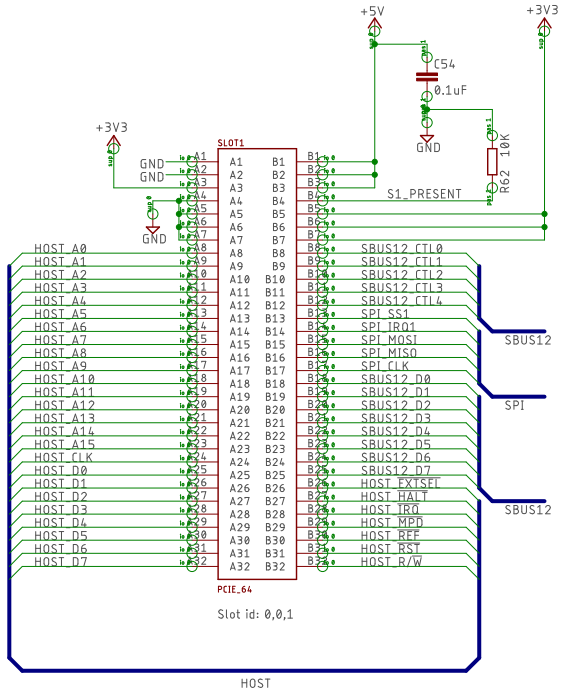
Sheet: 8/19



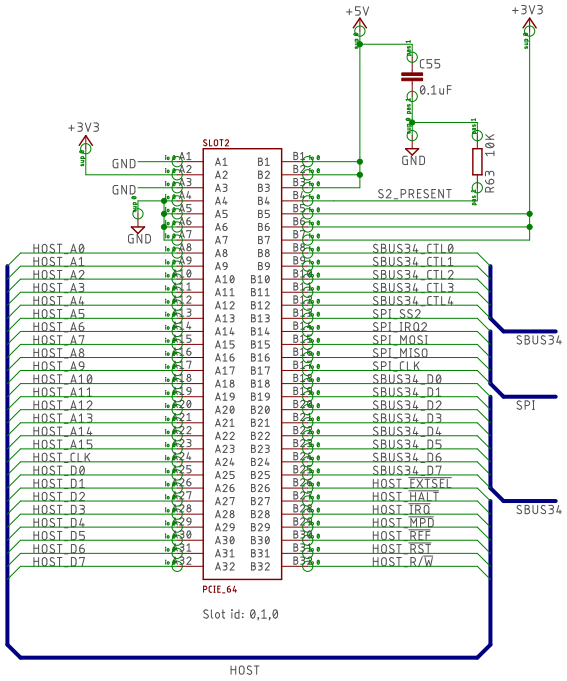
	Board config
	xio2
	05/09/2018 11:20
	Sheet: 9/19

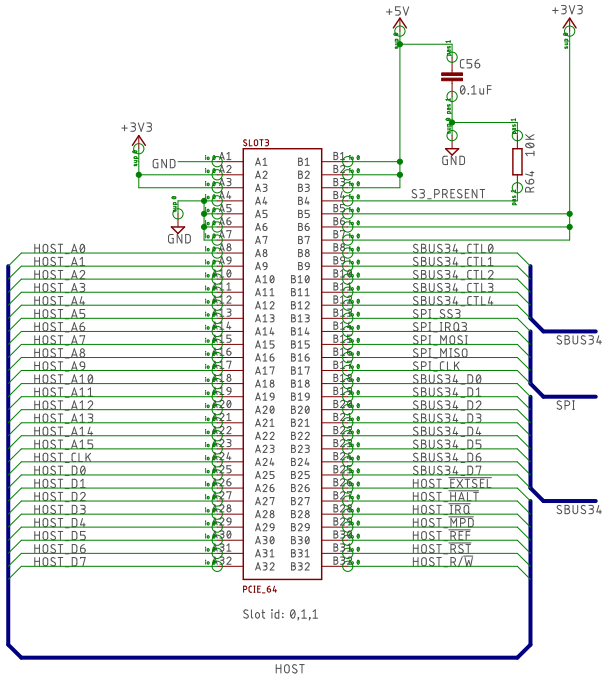




B1,2,3	+5V
B5,6,7	Slot 3.3v
B4	Card-present
A1,2,3	Slot ID
A4,5,6,7	GND

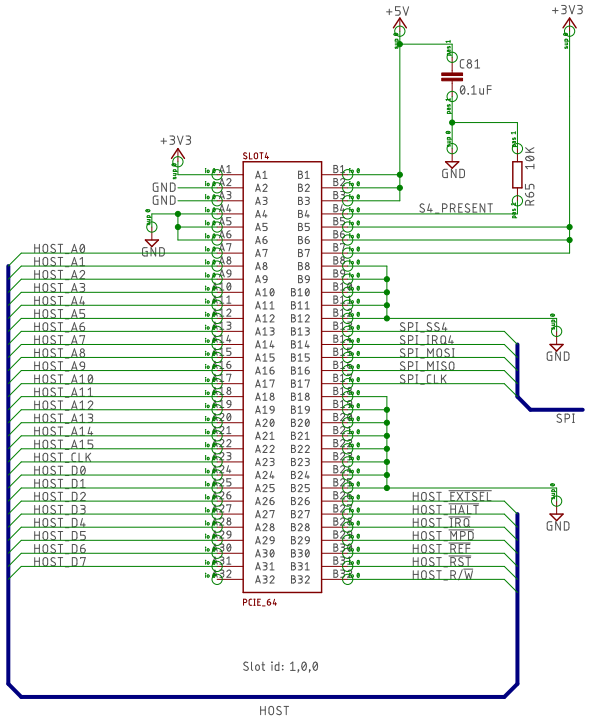
	Slots 0,1
	xio2
	05/09/2018 11:20
	Sheet: 10/19





B1,2,3	+5V
B5,6,7	Slot 3.3v
B4	Card-present
A1,2,3	Slot ID
A4,5,6,7	GND

	Slots 2,3
	xio2
	05/09/2018 11:20
	Sheet: 11/19



B1,2,3	+5V
B5,6,7	Slot 3.3v
B4	Card-present
A1,2,3	Slot ID
A4,5,6,7	GND

	Slot 4
	xio2
	05/09/2018 11:20
	Sheet: 12/19

Power supply notes

Power sequence is
1.0v rail @ 2A, which enables the
1.8v rail @ 1A, which enables the
3.3v rail @ 1A

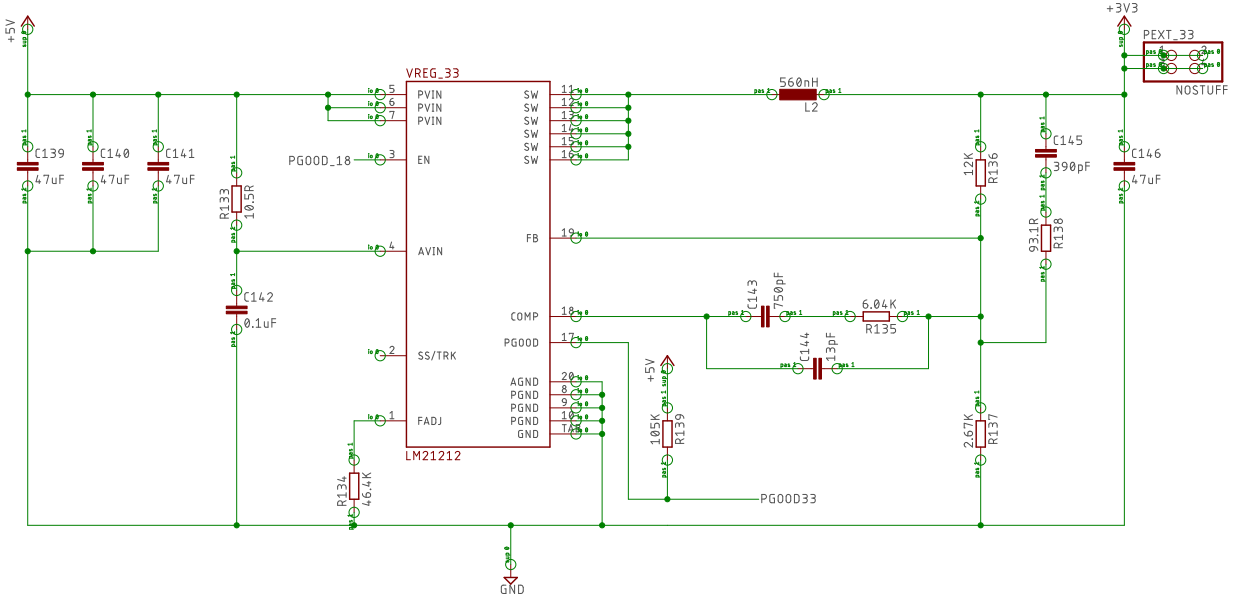
Both 1.8v and 3.3v need no minimum load
All regulators are stable with ceramic caps

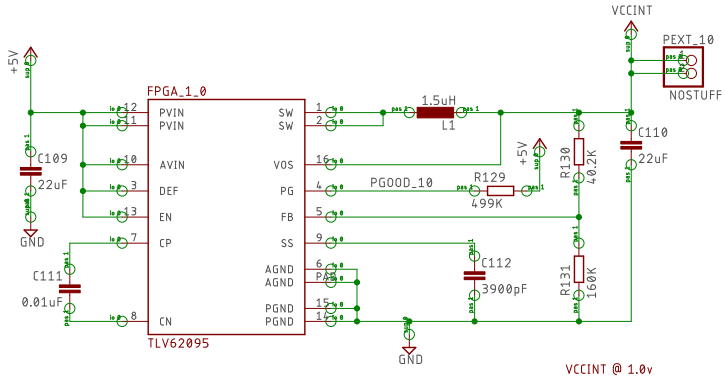
R131 and R130 ought to be at
least 1%, preferably 0.1% resistors

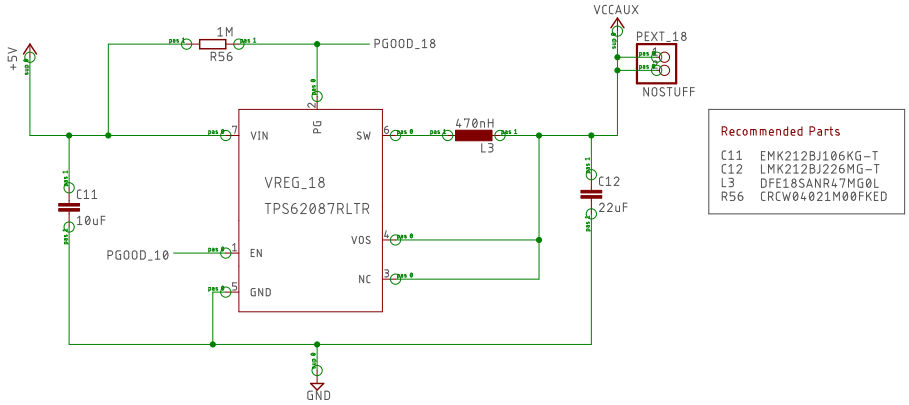
Recommended Parts

C139	GRM32ER60J476ME20L
C140	GRM32ER60J476ME20L
C141	GRM32ER60J476ME20L
C142	GRM155R61C104KA88D
C143	C0603C751K5GACTU
C144	CL21C130JBANNNC
C145	GRM1555C1H391JA01J
C146	GRM32ER60J476ME20L
R133	CRCW040210R5FKED
R134	CRCW040246K4FKED
R135	ERJ-6ENF6041V
R136	RR1220P-123-D
R137	CRCW04022K67FKED
R138	CRCW040293R1FKED
R139	RC0201FR-07105KL
L2	IHLP2525EZERR56M01

Change C139,C140,C141 to 47uF (C146)
Change L2 to 560nH (IHLP2525EZERR56M01)







Recommended Parts

C11	EMK212BJ106KG-T
C12	LMK212BJ226MG-T
L3	DFE18SANR47MG0L
R56	CRCW04021M00FKED

FPGA power supplies	
xio2	
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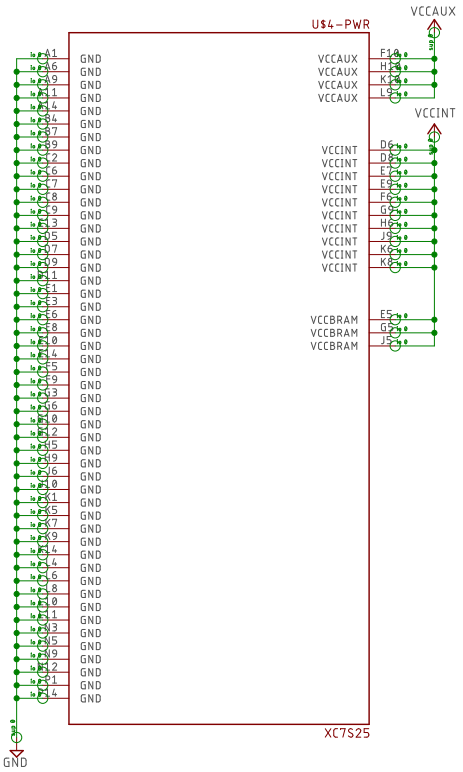
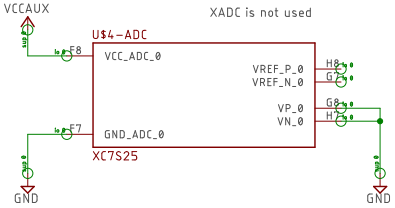
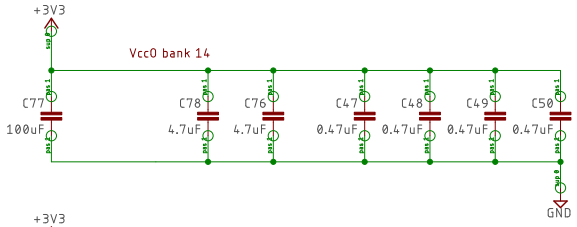
Xilinx-recommended (smaller parts)

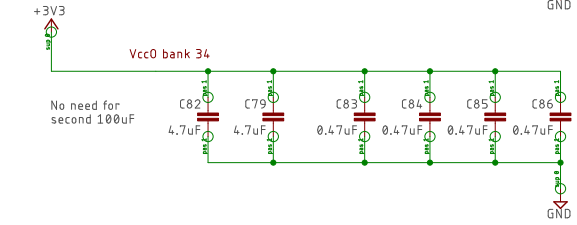
100uF : GRM21BR60J107ME15L (0805)
47uF : GRM21BR60J476ME15L (0805)
4.7uF : GRM155R60J475ME87D (0402)
0.47uF : GRM033R60J474KE90D (0201)

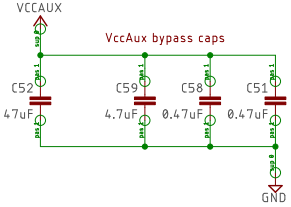
100uF caps can be placed anywhere
others within 2 electrical inches of part

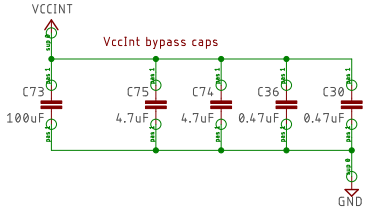


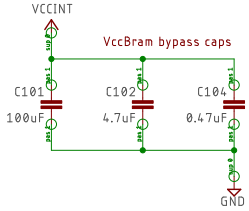












Bypass cap number and
capacitance taken from UG483

FPGA power	
xio2	
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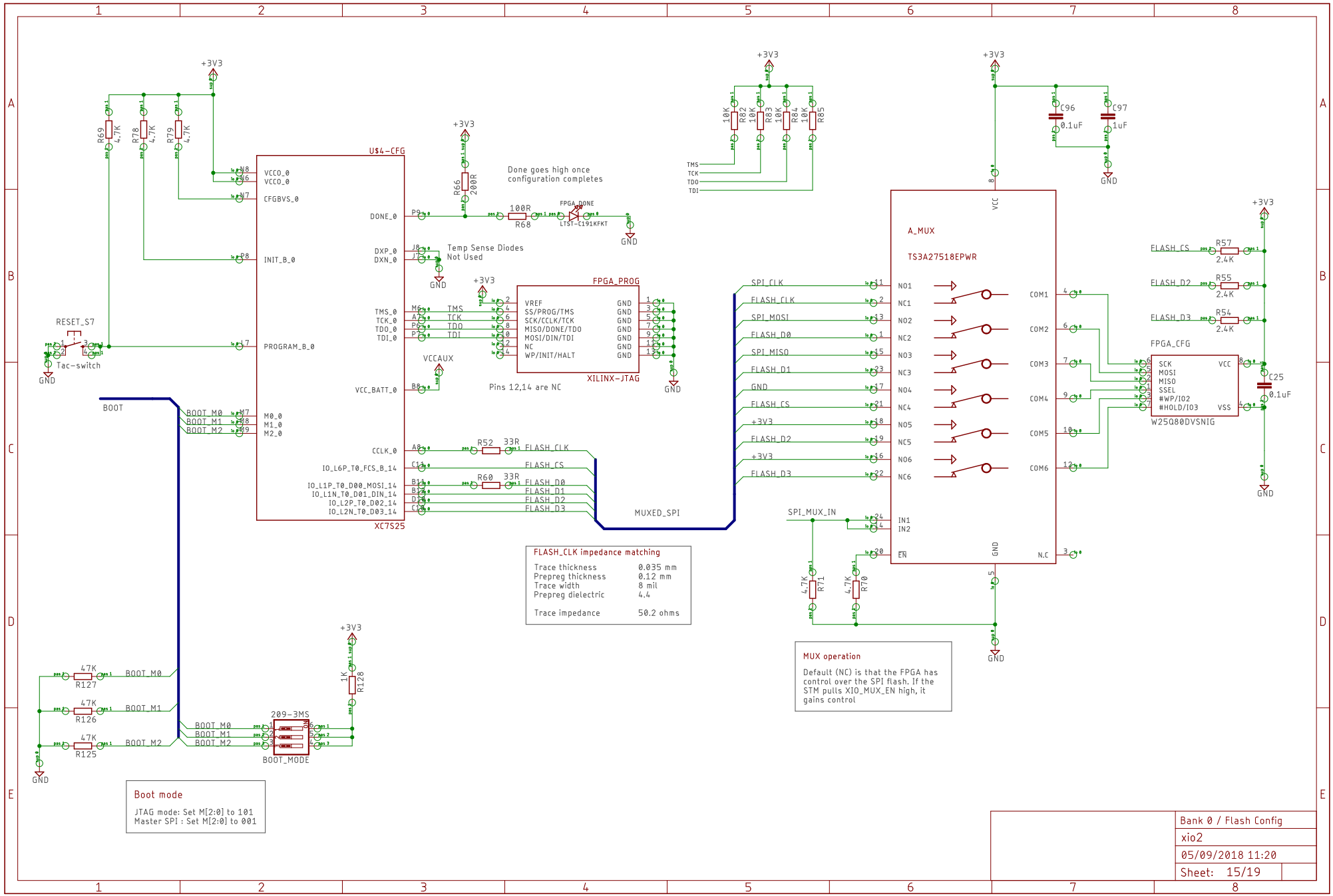
U$4-CFG
XC7S25
VCCO_0
VCCO_0
CFGBVS_0
INIT_B_0
PROGRAM_B_0
DONE_0
DXP_0
DXN_0
VCC_BATT_0
CCLK_0
IO_L6P_T0_FCS_B_14
IO_L1P_T0_D00_MOSI_14
IO_L1N_T0_D01_DIN_14
IO_L2P_T0_D02_14
IO_L2N_T0_D03_14
M0_0
M1_0
M2_0
TMS_0
TCK_0
TDO_0
TDI_0
+3V3
R69 4.7K
R78 4.7K
R79 4.7K
R66 200R
100R R68
FPGA_DONE
LTST-C191KFKT
Done goes high once configuration completes
Temp Sense Diodes Not Used
GND
RESET_S7
Tac-switch
BOOT
BOOT_M0
BOOT_M1
BOOT_M2
R127 47K
R126 47K
R125 47K
209-3MS
BOOT_MODE
R128 1K
Boot mode
JTAG mode: Set M[2:0] to 101
Master SPI : Set M[2:0] to 001
FPGA_PROG
XILINX-JTAG
VREF
SS/PROG/TMS
SCK/CCLK/TCK
MISO/DONE/TDO
MOSI/DIN/TDI
NC
WP/INIT/HALT
VCCAUX
Pins 12,14 are NC
R52 33R
R60 33R
FLASH_CLK
FLASH_CS
FLASH_D0
FLASH_D1
FLASH_D2
FLASH_D3
MUXED_SPI
10K R82
10K R83
10K R84
10K R85
C96 0.1uF
C97 1uF
A_MUX
TS3A27518EPWR
SPI_CLK
FLASH_CLK
SPI_MOSI
FLASH_D0
SPI_MISO
FLASH_D1
FLASH_CS
+3V3
FLASH_D2
+3V3
FLASH_D3
NO1
NC1
NO2
NC2
NO3
NC3
NO4
NC4
NO5
NC5
NO6
NC6
COM1
COM2
COM3
COM4
COM5
COM6
IN1
IN2
EN
N.C
SPI_MUX_IN
R71 4.7K
R70 4.7K
MUX operation
Default (NC) is that the FPGA has control over the SPI flash. If the STM pulls XIO_MUX_EN high, it gains control
FLASH_CS
FLASH_D2
FLASH_D3
R57 2.4K
R55 2.4K
R54 2.4K
FPGA_CFG
SCK
MOSI
MISO
SSEL
#WP/IO2
#HOLD/IO3
VCC
VSS
W25Q80DVSNIG
C25 0.1uF
FLASH_CLK impedance matching
Trace thickness 0.035 mm
Prepreg thickness 0.12 mm
Trace width 8 mil
Prepreg dielectric 4.4
Trace impedance 50.2 ohms
Bank 0 / Flash Config
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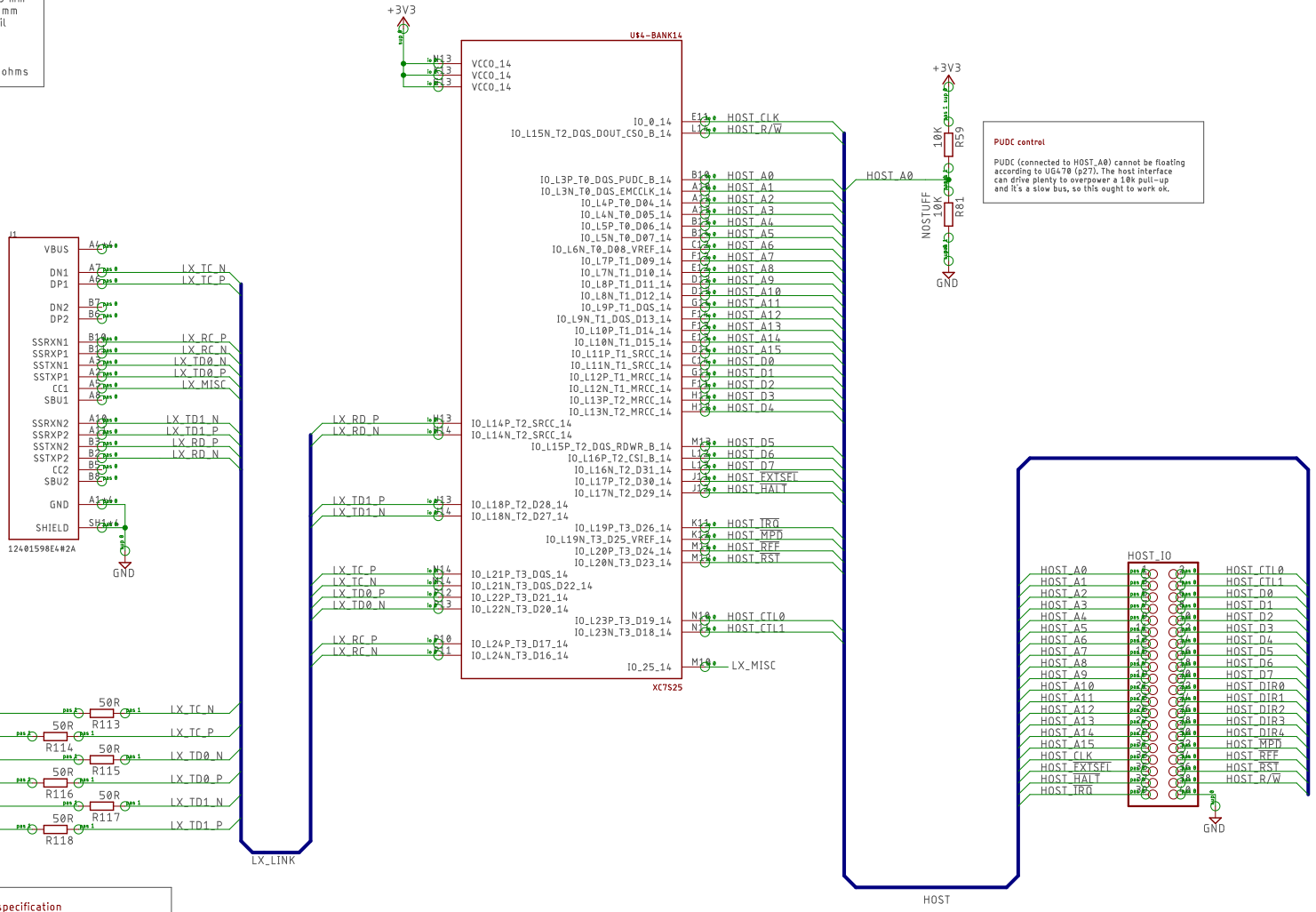
USB3 connections

Trace thickness	0.035 mm
Prepreg thickness	0.12 mm
Trace width	10 mil
Inter-trace spacing	7 mil
Prepreg dielectric	4.4
Differential impedance	90.5 ohms



Pull-up specification

TMDS_33 signalling requires 50R pull-ups to 3.3v on all inputs.

Labels {RX*,TX*} are from perspective of the host board, so need to add pull-ups to TX* lines on this board.

Will dissipate 13.5mA,

	FPGA Bank 14
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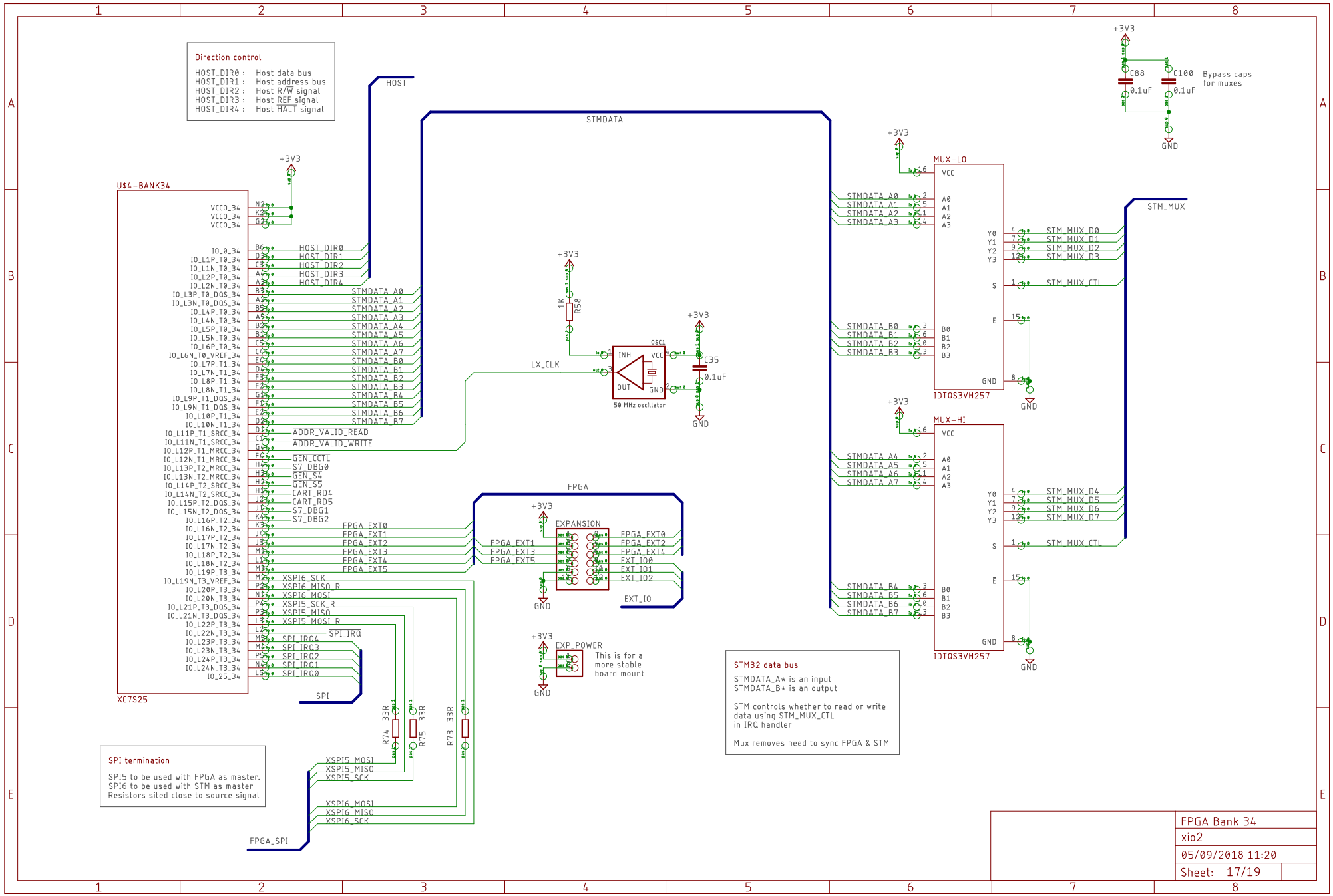
Direction control
HOST_DIR0 : Host data bus
HOST_DIR1 : Host address bus
HOST_DIR2 : Host R/W signal
HOST_DIR3 : Host REF signal
HOST_DIR4 : Host HALT signal
HOST
STMDATA
U$4-BANK34
XC7S25
SPI
FPGA
EXPANSION
EXT_IO
EXP_POWER
This is for a more stable board mount
50 MHz oscillator
LX_CLK
ADDR_VALID_READ
ADDR_VALID_WRITE
GEN_CCTL
S7_DBG0
GEN_S4
GEN_S5
CART_RD4
CART_RD5
S7_DBG1
S7_DBG2
SPI_IRQ
SPI_IRQ4
SPI_IRQ3
SPI_IRQ2
SPI_IRQ1
SPI_IRQ0
XSPI6_SCK
XSPI6_MISO_R
XSPI6_MOSI
XSPI5_SCK_R
XSPI5_MISO
XSPI5_MOSI_R
FPGA_EXT0
FPGA_EXT1
FPGA_EXT2
FPGA_EXT3
FPGA_EXT4
FPGA_EXT5
EXT_IO0
EXT_IO1
EXT_IO2
R74 33R
R75 33R
R73 33R
R58 1K
C35 0.1uF
C88 0.1uF
C100 0.1uF
Bypass caps for muxes
MUX-LO
MUX-HI
IDTQS3VH257
STM_MUX
STM_MUX_D0
STM_MUX_D1
STM_MUX_D2
STM_MUX_D3
STM_MUX_D4
STM_MUX_D5
STM_MUX_D6
STM_MUX_D7
STM_MUX_CTL
SPI termination
SPI5 to be used with FPGA as master.
SPI6 to be used with STM as master
Resistors sited close to source signal
STM32 data bus
STMDATA_A* is an input
STMDATA_B* is an output
STM controls whether to read or write data using STM_MUX_CTL in IRQ handler
Mux removes need to sync FPGA & STM
FPGA Bank 34
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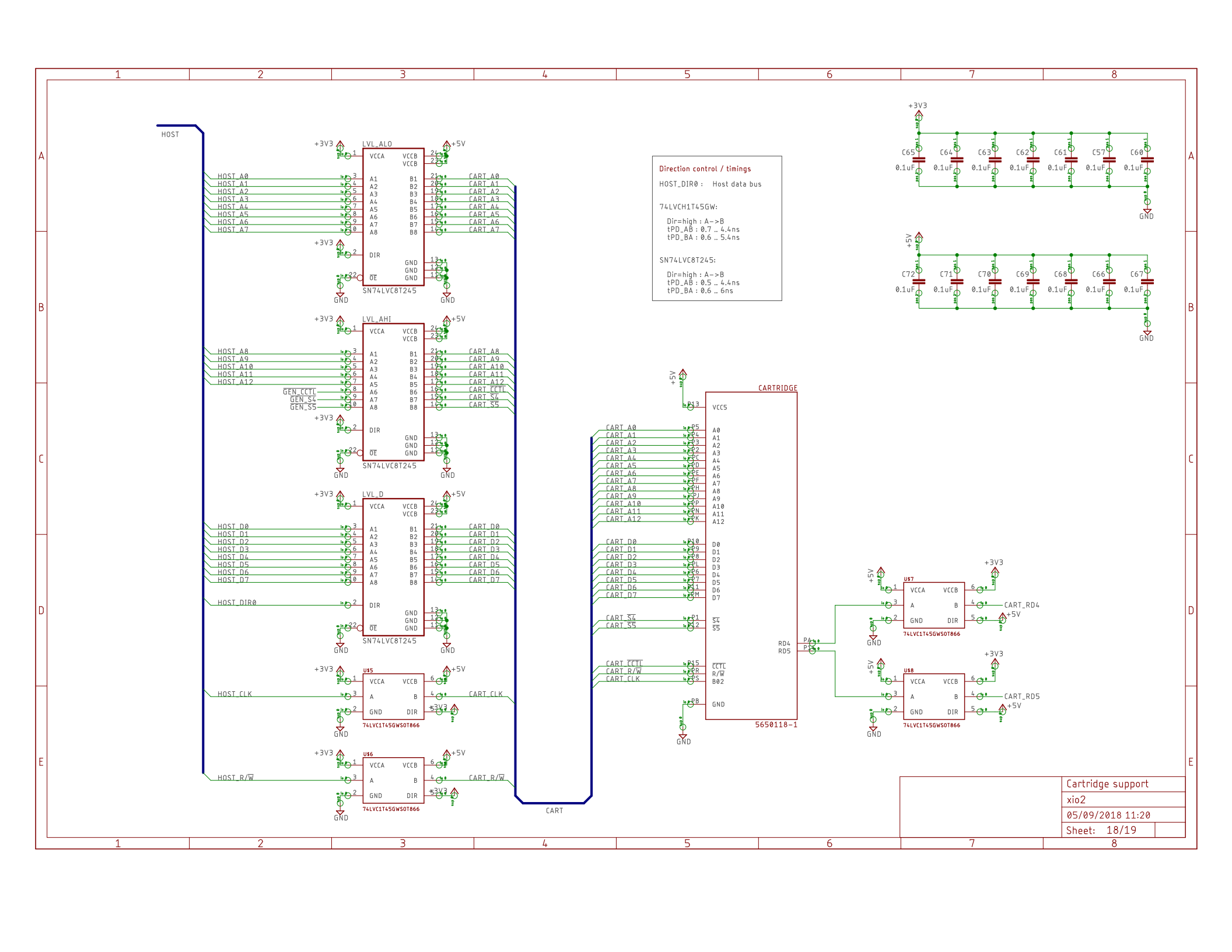
HOST
LVL_AL0
LVL_AHI
LVL_D
SN74LVC8T245
U$5
U$6
74LVC1T45GWSOT866
CART
CARTRIDGE
5650118-1
U$7
U$8
Direction control / timings
HOST_DIR0 : Host data bus
74LVCH1T45GW:
Dir=high : A->B
tPD_AB : 0.7 .. 4.4ns
tPD_BA : 0.6 .. 5.4ns
SN74LVC8T245:
Dir=high : A->B
tPD_AB : 0.5 .. 4.4ns
tPD_BA : 0.6 .. 6ns
Cartridge support
xio2
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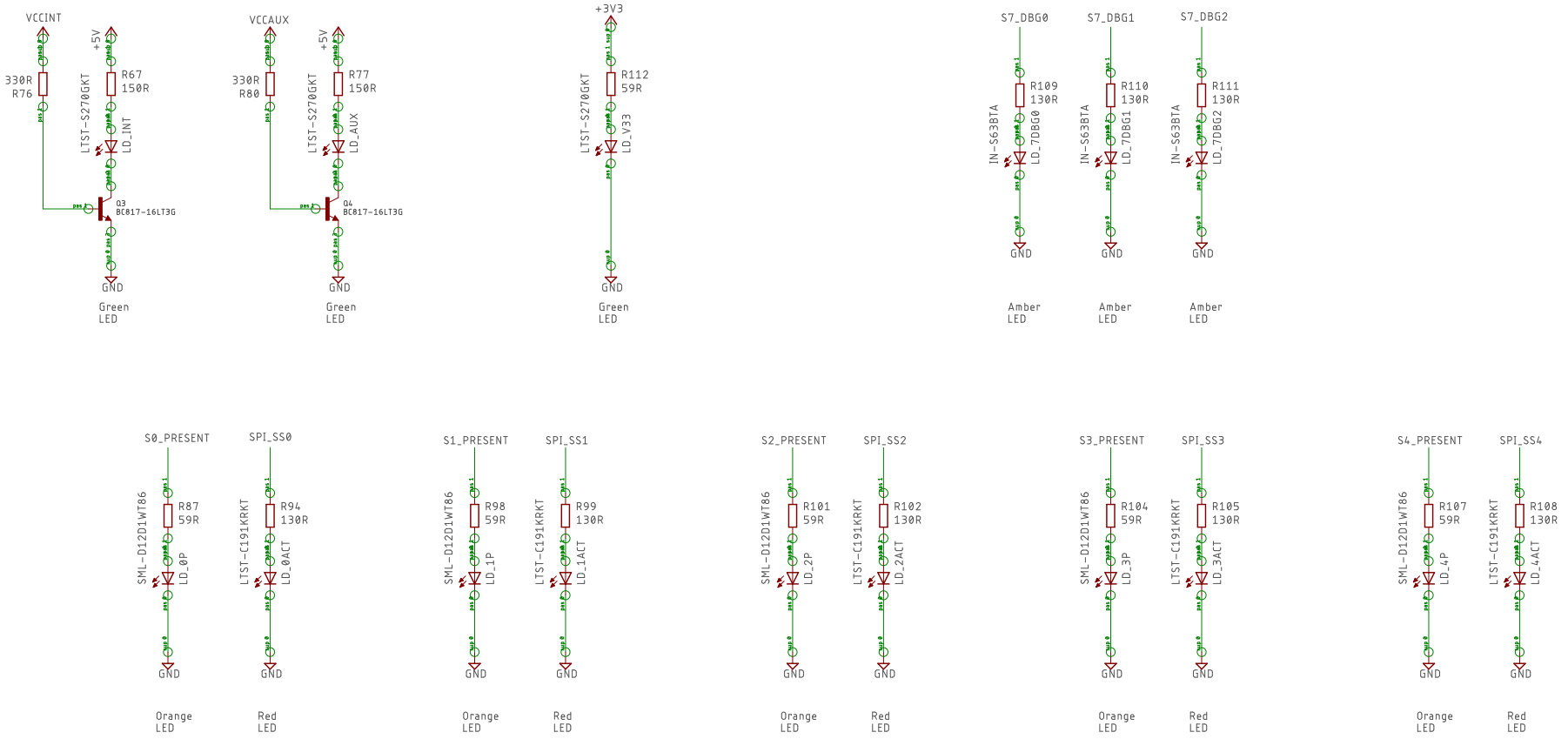

LED resistor values

Green and Orange LEDs are configured for 20mA current

Amber and Red LEDs are configured for 10mA current

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