AD9889A vs. AD9889



- ◆ AD9889A has improved output jitter performance even at extended temp range (-10 to 85C) and wider VDD tolerance (down to 1.68V)
- ◆ AD9889A will operate up to 165MHz
 - Characterized and released up to 80MHz only
- Data to Clock delay adjustment change
 - +/- 1200ps in 400ps steps
 - Register Adjustments
 - ♦ Set R0xBA[7:5] to b000 = -1200pS delay
 b011 = 0 data to clock delay
 b111 = invert clock
- ◆ Other Register Change recommendation
 - ◆ Set R0xA5[7:6] = b11 for proper operation
 - ◆ Set R0x9D = 0x68 for proper operation
- ◆ Only BGA (6X6mm, 0.5mm ball spacing) package available
- ◆ Contains support for SMPTE 274 video mode
- ◆ AD9889A has lower power-down current



AD9889B vs. AD9889A



- ◆ Added Gamut Metadata Packet (GMP) registers (part of HDMI 1.3)
 - GMP packet registers are contained in a secondary register map.
 - The device address for the secondary register map is programmable via register 0xCF of the primary register map. (default = 0x70)
 - Transmission of the GMP data is enabled by 0x44[1] (primary register map)
 - Refer to AD9889B Programming Guide for details
- ◆ Added AVI Info frame bits at registers 0xCD and 0xCE
 - Refer to AD9889B Programming Guide for details
- ◆ Added circuitry to support 4:2:2 to 4:4:4 conversion for modes using pixel repetition.
- ◆ Available in BGA, LFCSP, and LQFP packages
 - 80MHz and 165MHz speed grades available

