Microprocessors & Interfacing

Modes of 8086

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Bus Timing

During T1

- The address of the memory or I/O location is sent out via the address bus and the address/data bus connections.
- Control signals(ALE, DT/R',IO/M',M/IO') are also sent out

During T2,

- The 8086/8088 microprocessors issue the RD' or WR' signal, DEN' , and in the case of a write, the data to be written appear on the data bus.
- The DEN' signal turns on the data bus buffers, if they are present in the system, so the memory or I/O can receive data to be written, or so the microprocessor can accept the data read from the memory or I/O for a read operation

Bus Timing

During T3

- If the bus cycle happens to be a read bus cycle, the data bus is sampled at the end of T3

During T4

- All bus signals are deactivated in preparation for the next bus cycle.
- 8086/8088 samples the data bus connections for data that are read from memory or I/O.
- At the trailing edge of the WR' signal transfers data to the memory or I/O, which activates and writes when the WR' signal returns to a logic 1 level

Signals used during data transfer

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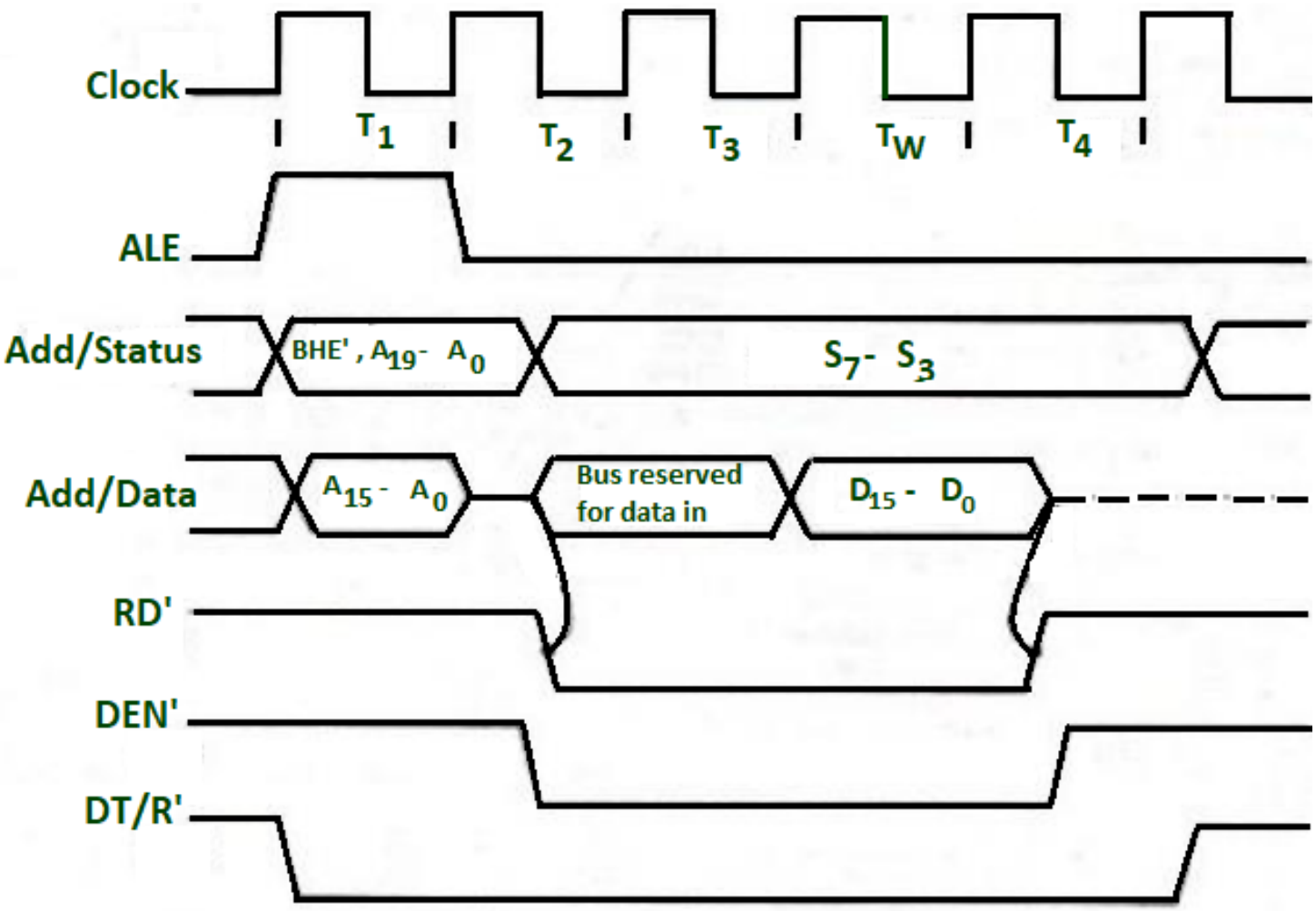
SIGNALS	PURPOSE
AD15 – AD0	Multiplexed Address & Data
A19/S6 – A16/S3	Higher order Address / Status
M/IO’	Indicates mem or I/O Device Access
RD’	Read Operation from Memory/IO
WR’	Write Operation to Memory/IO
ALE	When set – AD0 – AD15-has address
DT/R’	8086 is transmitting/receiving data
DEN’	Enable data buffers

8086 Timing: Reading Data



Bus Timing: Writing Data

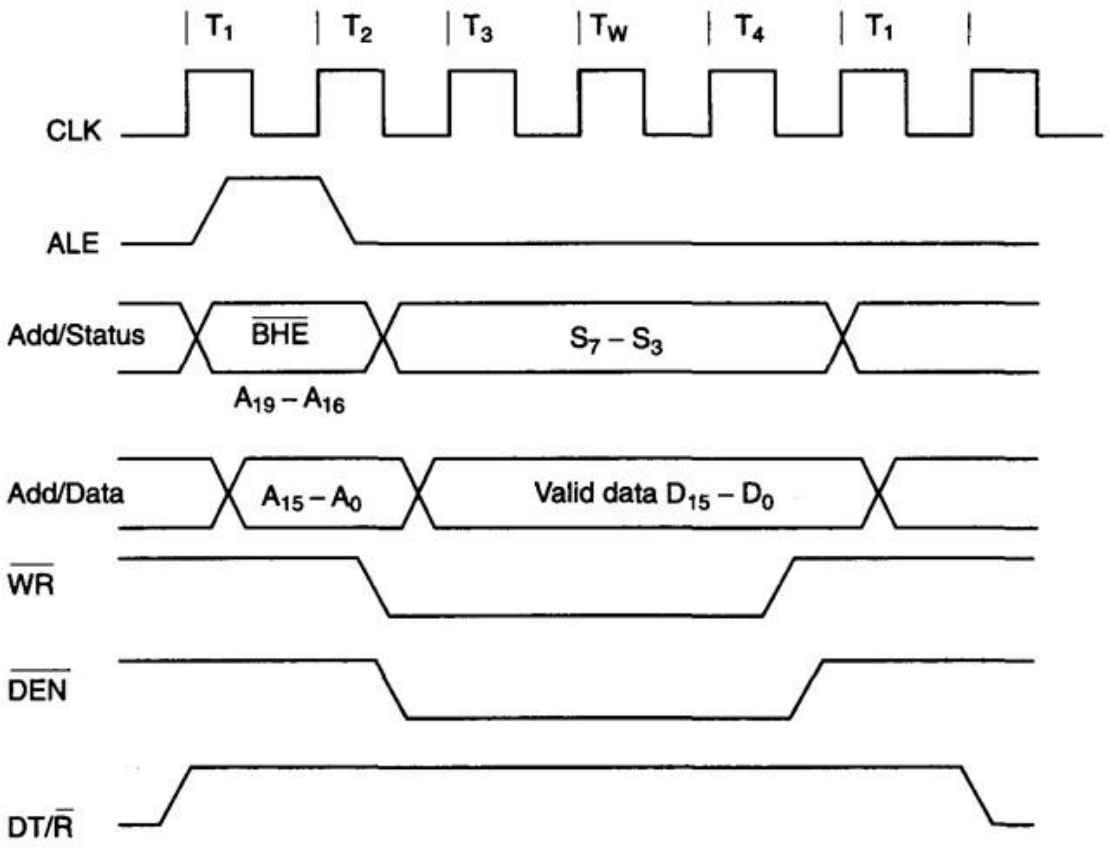


Fig.1.9(b) *Write Cycle Timing Diagram for Minimum Operation*

Ready & Wait State

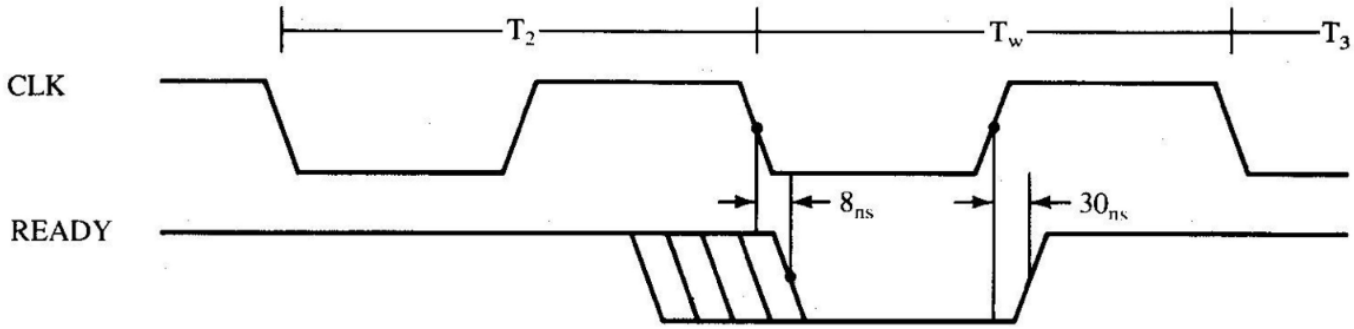
- The READY input causes wait states for slower memory and I/O components.
- Ready Signal- Inserts wait states into the timing.

– if placed at a logic 0, the microprocessor enters into wait states and remains idle

– if logic 1, no effect on the operation

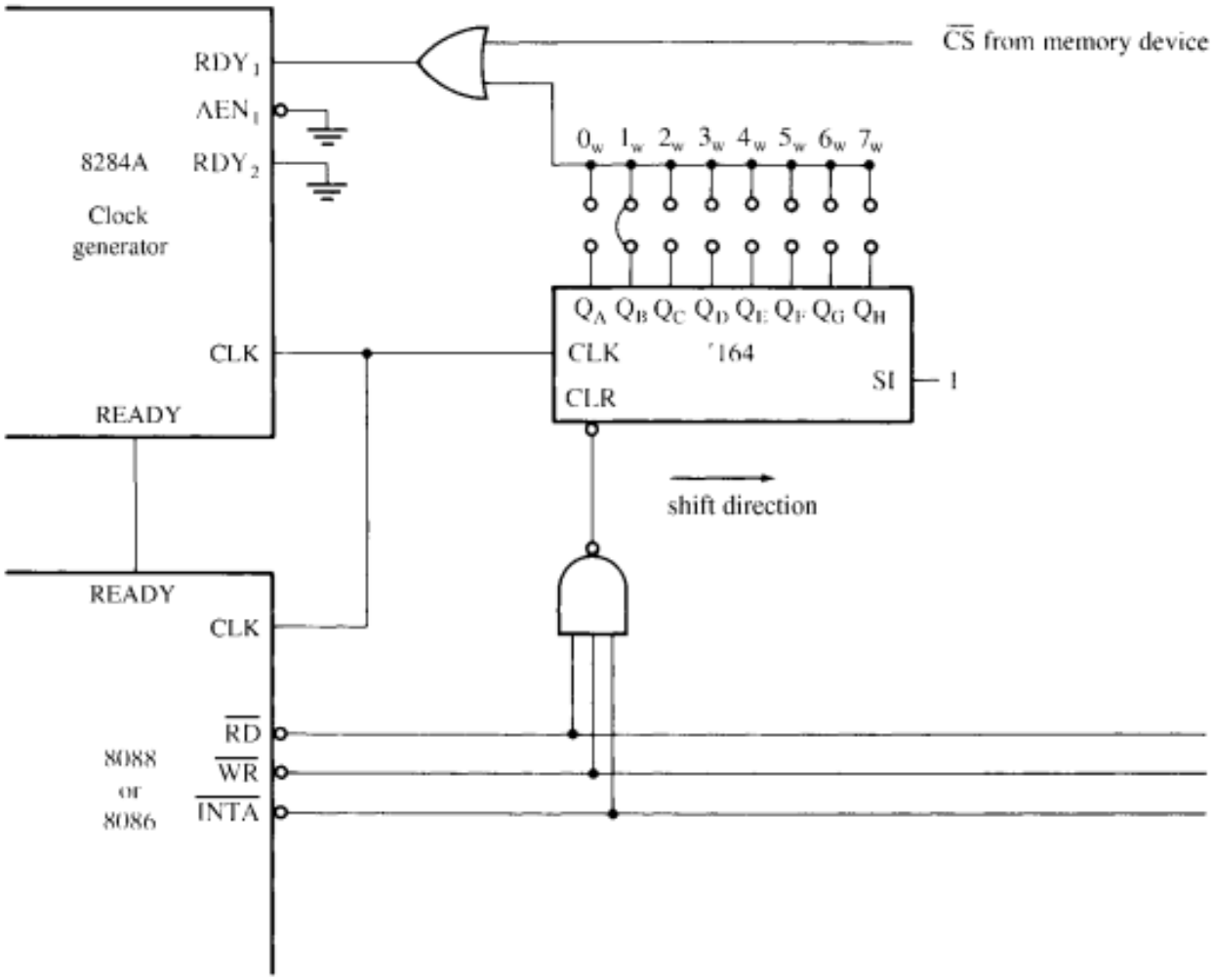
- A wait state (Tw) is an extra clocking period, inserted between T2 and T3 to lengthen the bus cycle.
- If one wait state is inserted, then the memory access time, normally 460 ns with a 5 MHz clock, is lengthened by one clocking period (200 ns) to 660 ns.

8086 READY input timing

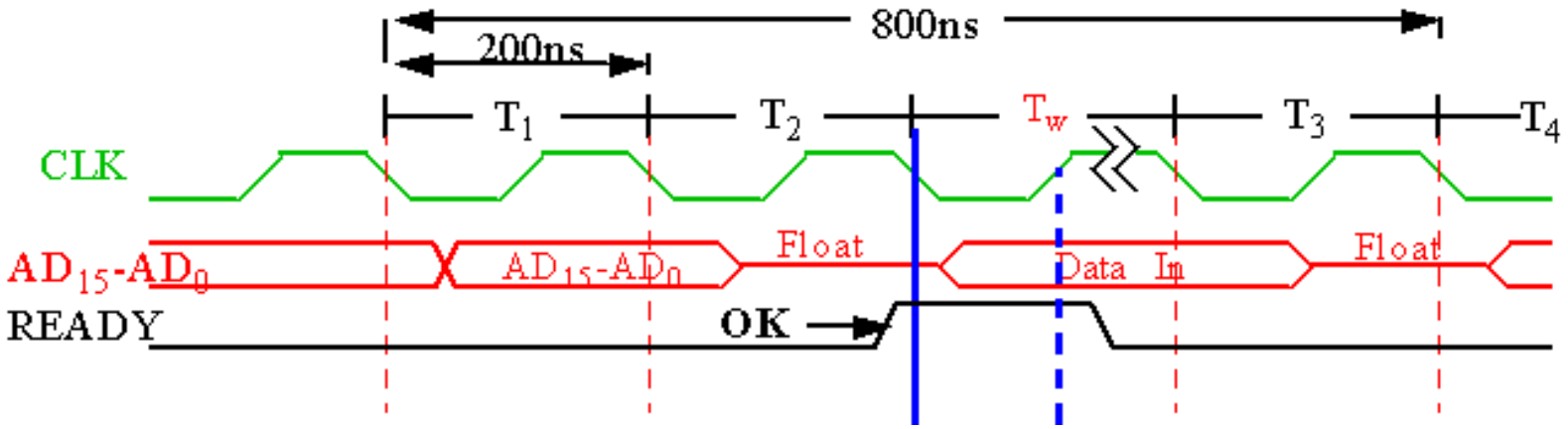


- If READY is logic 0 at the end of T_2, T_3 is delayed and T_w inserted between T_2 and T_3.
- READY is next sampled at the middle of T_w to determine if the next state is T_w or T_3.

Circuit that will cause between 0 an d 7 wait states



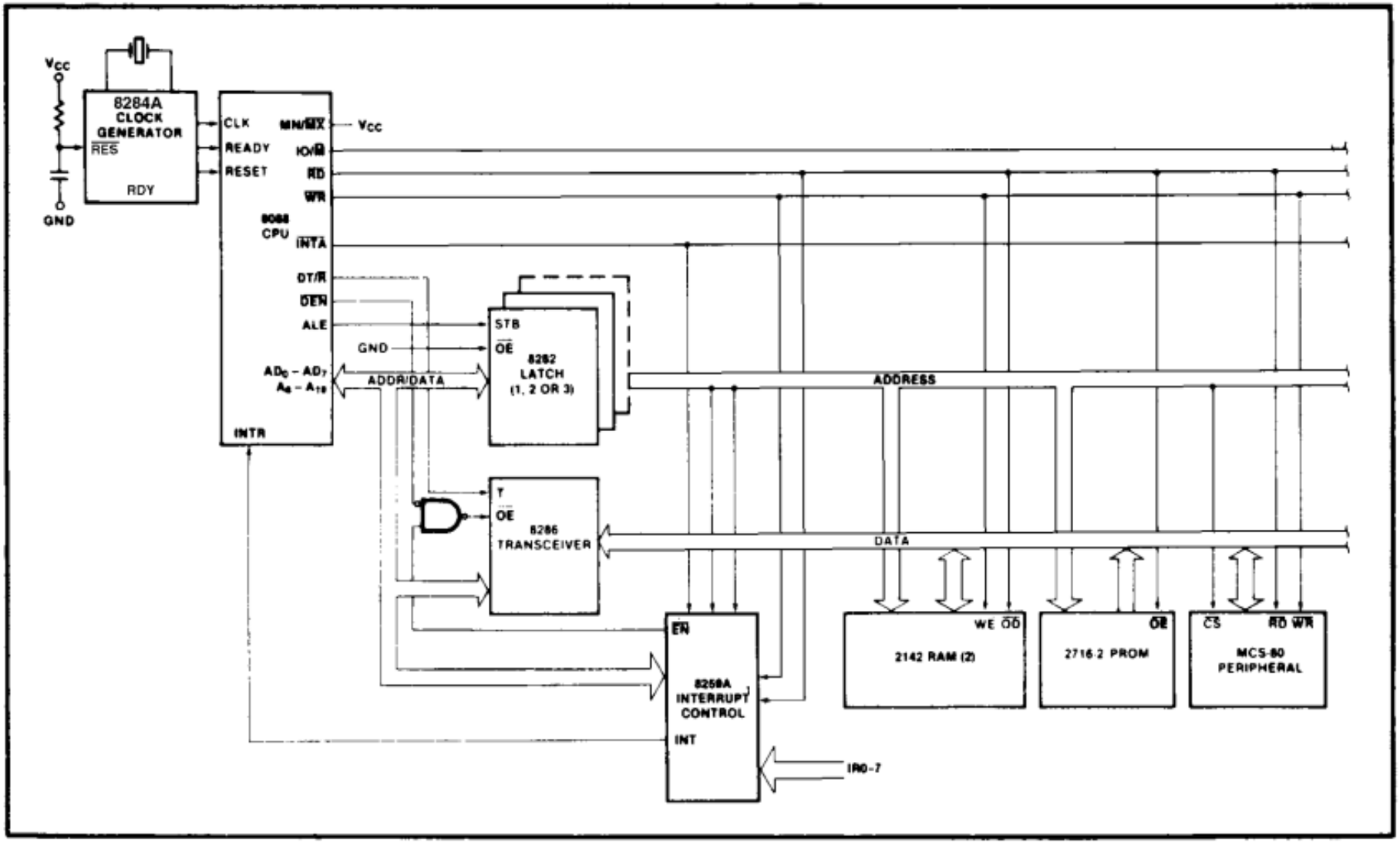
Wait state generation timing



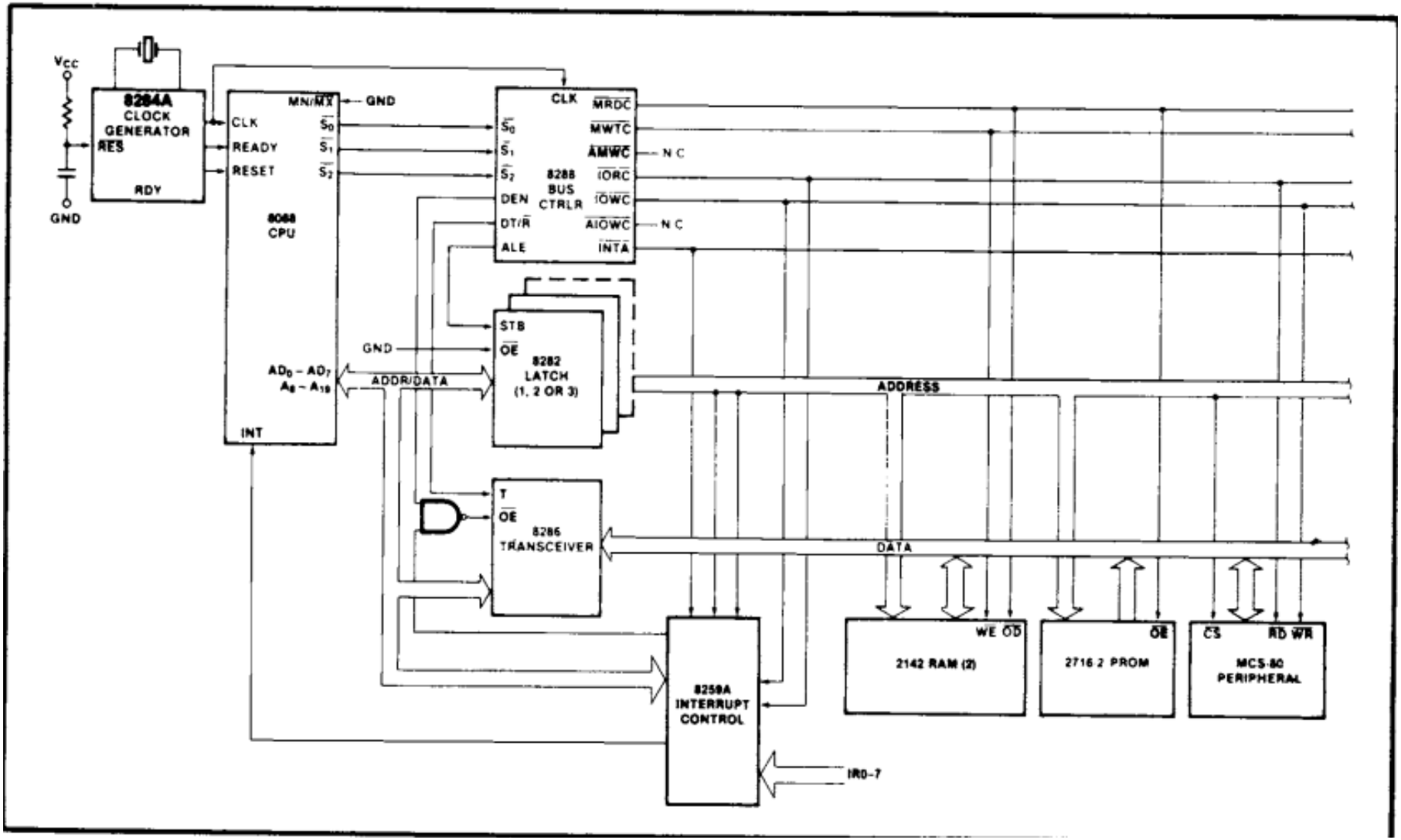
Features of Minimum & Maximum Mode

Feature	Minimum Mode	Maximum Mode
Bus width	8-bit	Multiplexed bus
Address bus width	20-bit	20-bit
Control signal	Single bus control signal	Multiple bus control signals
Additional support chips	Fewer support chips required	Additional support chips required
Coprocessor support	Not supported	Supported
Max no. of coprocessors	0	Up to 3
Bus controller	Not required	Required
Clock generator	Required	Required
Data buffer	Not required	Required
Interrupt controller	Built-in	External

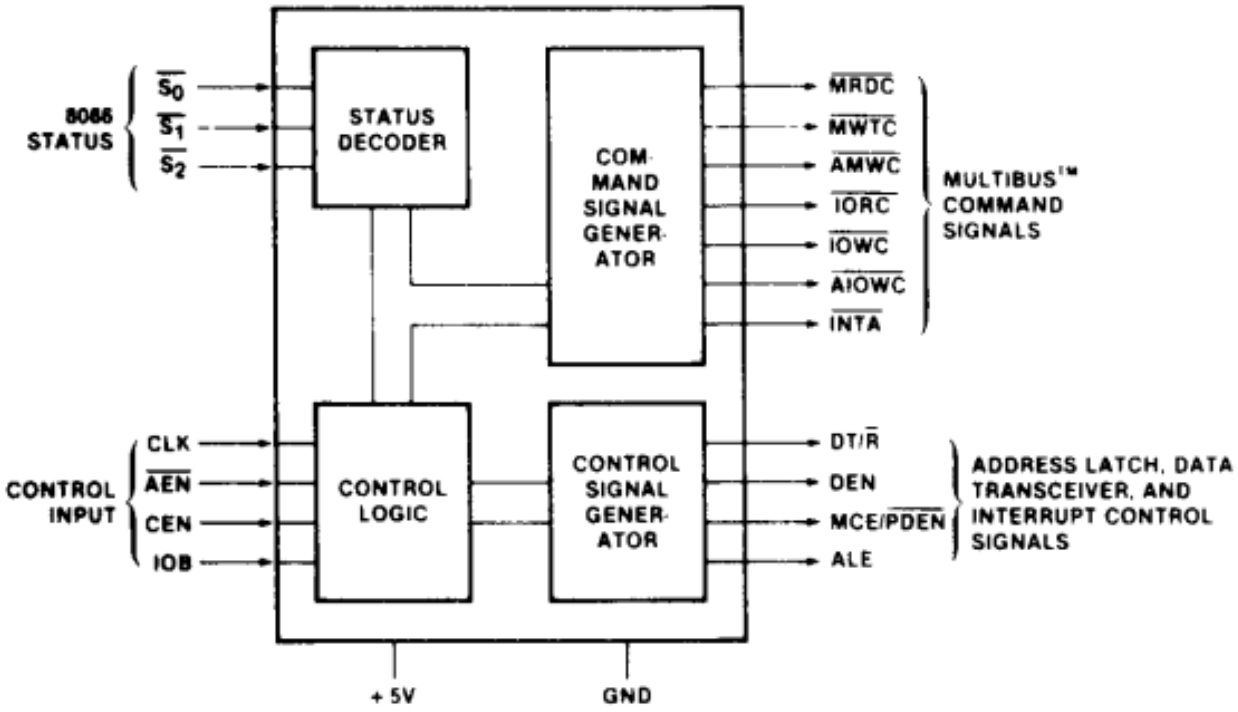
Minimum Mode Operation

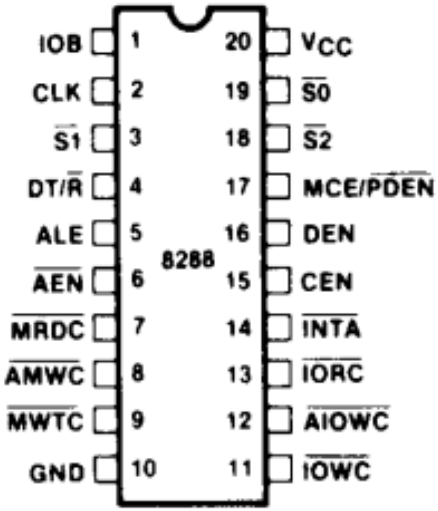


Maximum Mode Operation



8288 Bus Controller





The 8288 bus controller; (a) block diagram and (b) pin-out.

Pin Functions

S_2, S_1, and S_0	**Status inputs** are connected to the status output pins on the 8086/8088 microprocessor. These three signals are decoded to generate the timing signals for the system.
CLK	The **clock** input provides internal timing and must be connected to the CLK output pin of the 8284A clock generator.
ALE	The **address latch enable** output is used to demultiplex the address/data bus.
DEN	The **data bus enable** pin controls the bidirectional data bus buffers in the system. Note that this is an active high output pin that is the opposite polarity from the $\overline{\text{DEN}}$ signal found on the microprocessor when operated in the minimum mode.
DT/$\overline{\text{R}}$	The **data transmit/receive** signal is output by the 8288 to control the direction of the bidirectional data bus buffers.
$\overline{\text{AEN}}$	The **address enable** input causes the 8288 to enable the memory control signals.
CEN	The **control enable** input enables the command output pins on the 8288.
IOB	The **I/O bus mode** input selects either the I/O bus mode or system bus mode operation.

Pin Functions

$\overline{\text{AIOWC}}$	The **advanced I/O write** is a command output used to provide I/O with an advanced I/O write control signal.
$\overline{\text{IORC}}$	The **I/O read command** output provides I/O with its read control signal.
$\overline{\text{IOWC}}$	The **I/O write command** output provides I/O with its main write signal.
$\overline{\text{AMWT}}$	The **advanced memory write** control pin provides memory with an early or advanced write signal.
$\overline{\text{MWTC}}$	The **memory write** control pin provides memory with its normal write control signal.
$\overline{\text{MRDC}}$	The **memory read** control pin provides memory with a read control signal.
$\overline{\text{INTA}}$	The **interrupt acknowledge** output acknowledges an interrupt request input applied to the INTR pin.
MCE/$\overline{\text{PDEN}}$	The **master cascade/peripheral data** output selects cascade operation for an interrupt controller if IOB is grounded, and enables the I/O bus transceivers if IOB is tied high.

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Thank You