BITS Pilani

Microprocessors & Interfacing

Memory Interface

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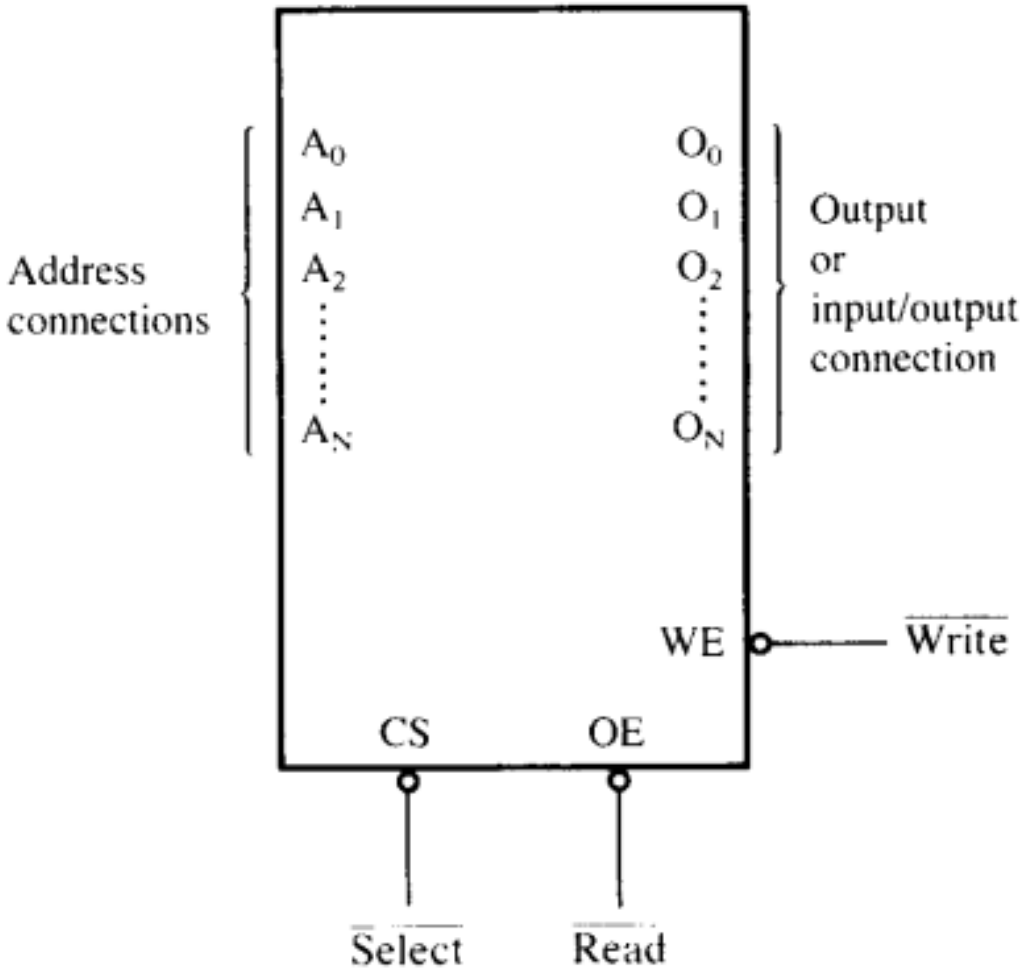
Common types of memory

- Read-only memory (ROM)
- Flash memory (EEPROM)
- Static random access memory (SRAM)
- Dynamic random access memory (DRAM)

Memory Device

Pin connections common to all memory devices are:

- Address inputs
- Data outputs or input/ outputs
- Some type of selection input
- At least one control input used to select a read or write operation



Address Connections

- A 1K memory device has 10 address pins (A0–A9)
- 10 address inputs are required to select any of its 1024 memory locations
- It takes a 10-bit binary number (1024 different combinations) to select any single location on a 1024-location device

Data Connections

- All memory devices have a set of data outputs or input/outputs.
- The data connections are the points at which data are entered for storage or extracted for reading.
- Data pins on memory devices are labeled D0 through D7 for an 8-bit-wide memory
- An 8-bit-wide memory device is often called a byte-wide memory

Selection Connections

- Each memory device has an input—sometimes more than one—that selects or enables the memory device.
- This type of input is most often called a chip select (CS’), chip enable (CE’), or simply select (S’) input.
- RAM memory generally has at least one CS’ or S’ input, and ROM has at least one CE’ .
- If the CS’,S’,CE’ or input is active (a logic 0), the memory device performs a read or write operation; if it is inactive (a logic 1), the memory device cannot do a read or a write because it is turned off or disabled.
- If more than one connection is present, all must be activated to read or write data

Control Connections

- All memory devices have some form of control input or inputs.
- A ROM usually has only one control input, while a RAM often has one or two control inputs.

ROM - output enable (OE') or gate (G')

- OE' and CE' are both active, output is enabled

RAM – R/W' along with CS' – can read and write

- WE' and OE'(or G') – can read and write

ROM

- Read-only memory (ROM) permanently stores programs and data that are resident to the system and must not change when power supply is disconnected.
- Known as nonvolatile memory
- ROM is often used to store firmware, BIOS, and other critical system software that needs to be permanently stored and not modified during normal operation

EPROM

- EPROM (erasable programmable read-only memory), a type of ROM, is more commonly used when software must be changed often

- EPROM is erasable if exposed to high-intensity ultraviolet light for about 20 minutes or so, depending on the type of EPROM

- EPROMs are used in applications where occasional updates or changes to the stored data are necessary but not frequent enough to warrant the use of EEPROM or flash memory.

2716, 2K*8 EPROM

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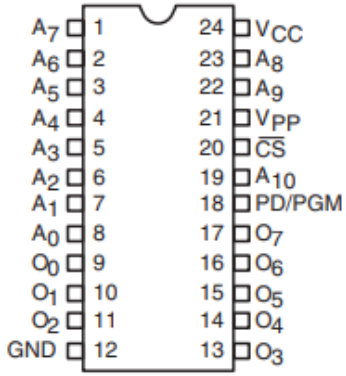
PIN CONFIGURATION



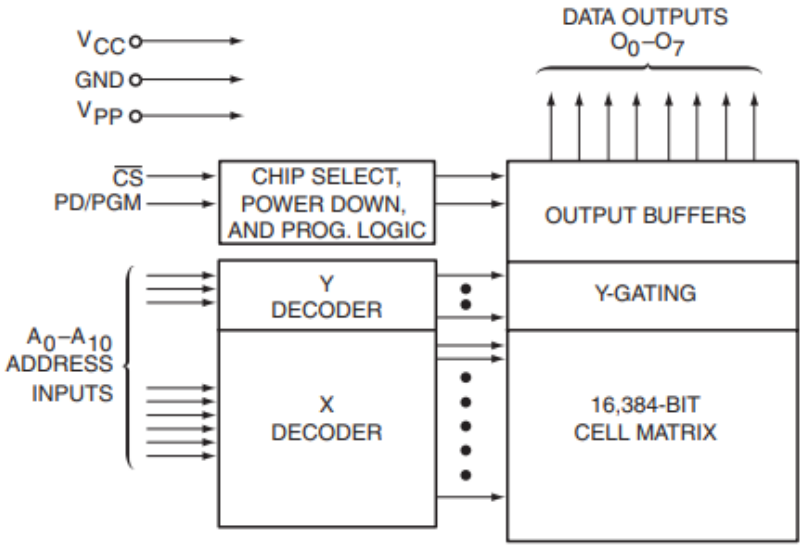
PIN NAMES

A_0–A_{10}	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O_0–O_7	OUTPUTS

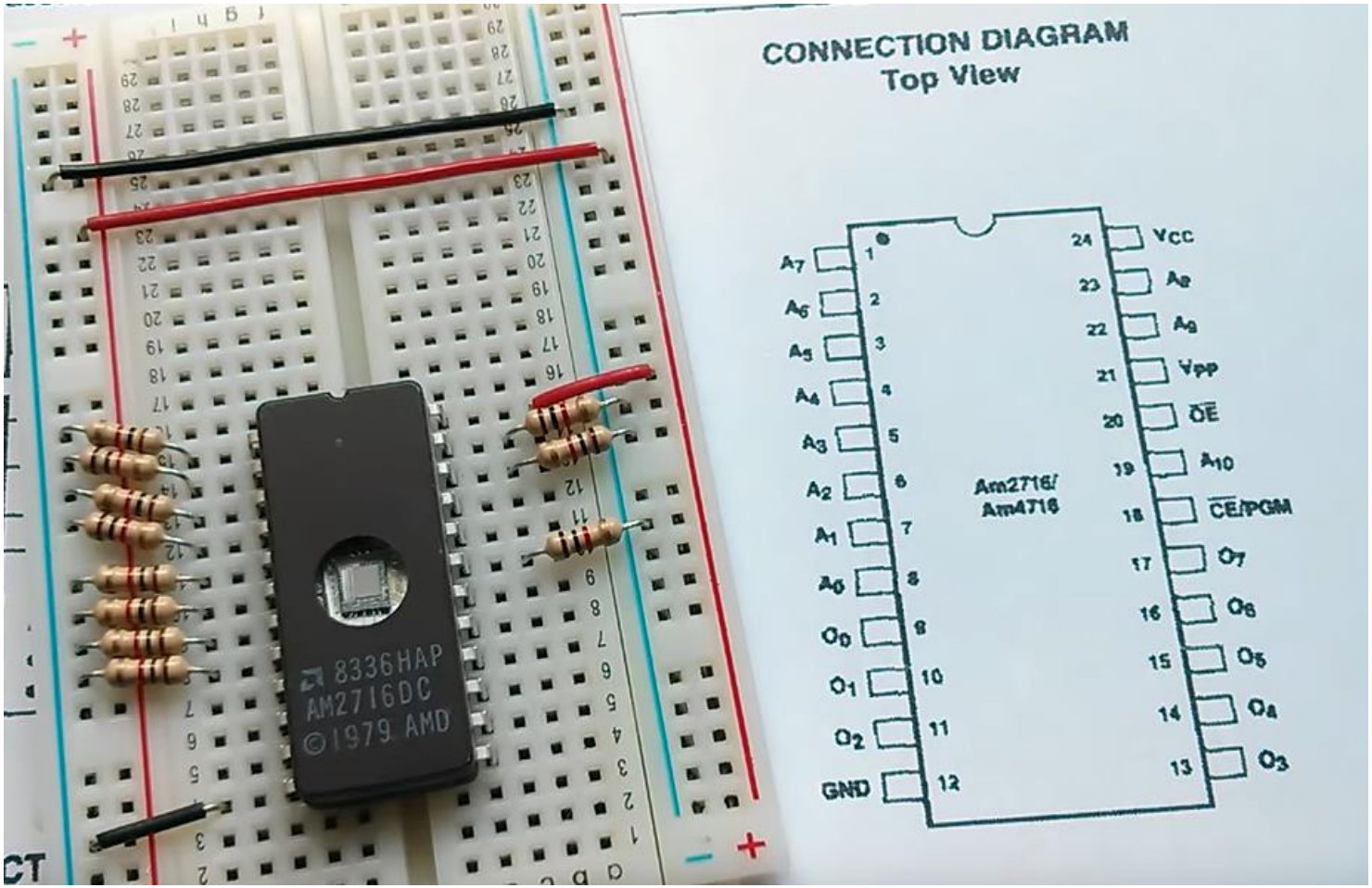
MODE SELECTION

MODE \ PINS	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

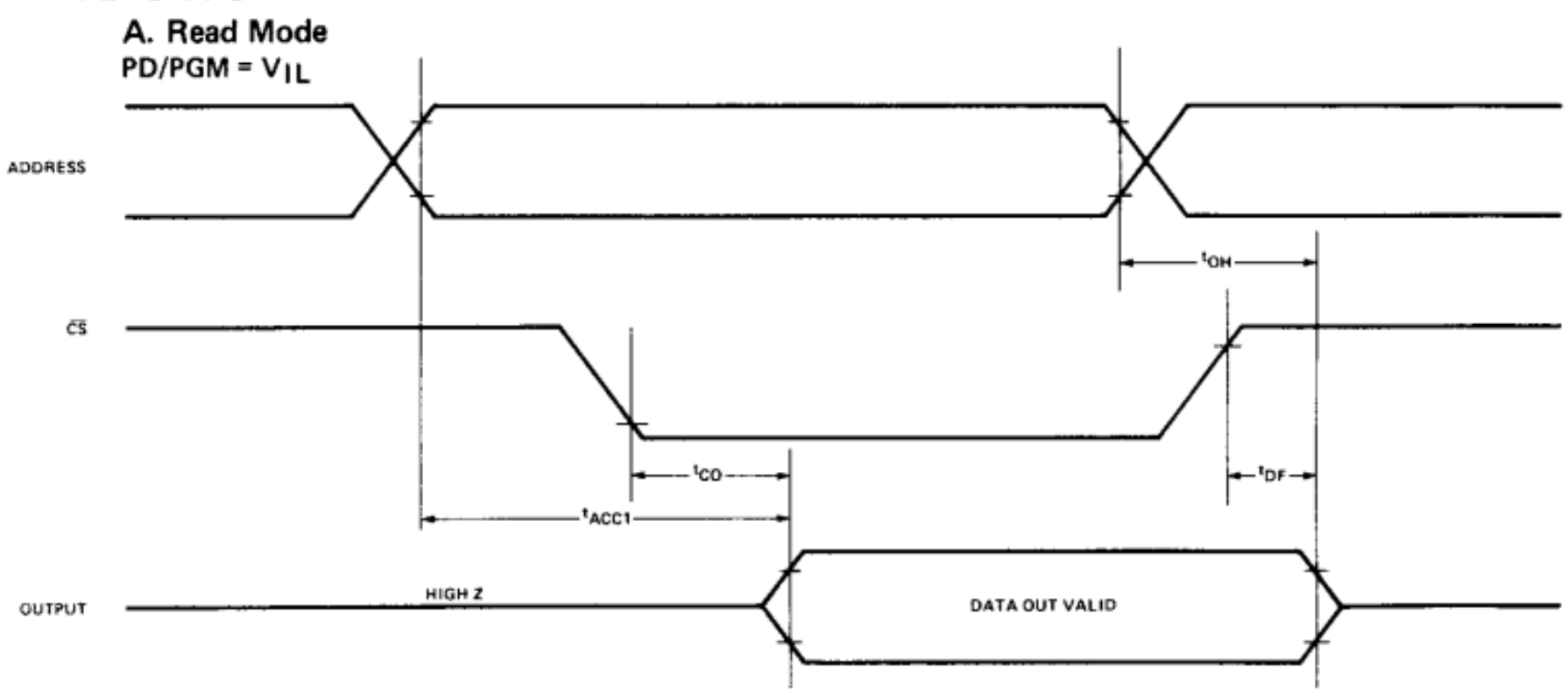
BLOCK DIAGRAM



How chip is connected



The timing diagram of 2716 EPROM



Memory Access Time

- T_{ACC} is measured from the appearance of the address at the address inputs until the appearance of the address at the address output

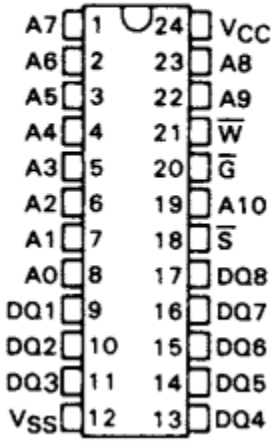
- Basic speed of EPROM is 450 ns

- Wait states are required to ensure smooth operations.

Static RAM

- Static RAM memory devices retain data for as long as DC power is applied.
- Because no special action (except power) is required to retain stored data, these devices are called static memory.
- Also called volatile memory because they will not retain data without power.

TMS4016 . . . NL PACKAGE
(TOP VIEW)



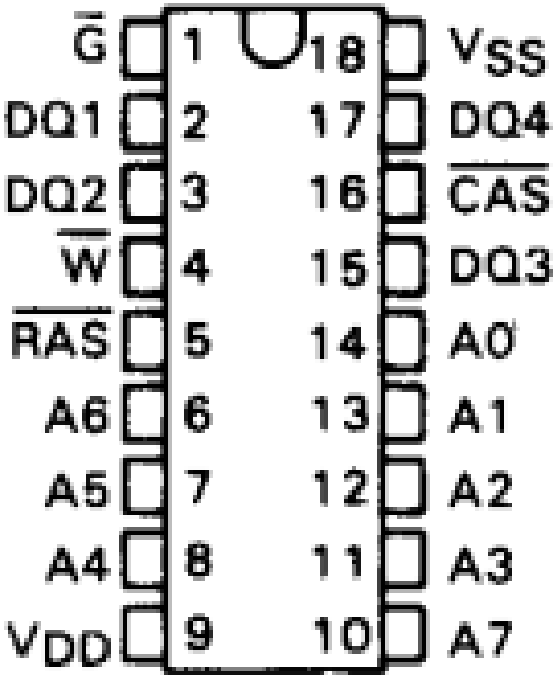
PIN NOMENCLATURE	
A0 – A10	Addresses
DQ1 – DQ8	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{S}$	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

Dynamic RAM (DRAM) Memory

- DRAM is essentially the same as SRAM, except that it retains data for only 2 or 4 ms on an integrated capacitor
- In DRAM, the entire contents of the memory are refreshed with 256 reads in a 2- or 4-ms interval
- Refreshing also occurs during a write, a read, or during a special refresh cycle
- DRAM is widely used as the main memory in computers and other digital devices due to its cost-effectiveness and high storage capacity.
- Another disadvantage of DRAM memory is that it requires so many address pins that the manufacturers have decided to multiplex the address inputs.

TMS4464, 64K × 4 dynamic RAM

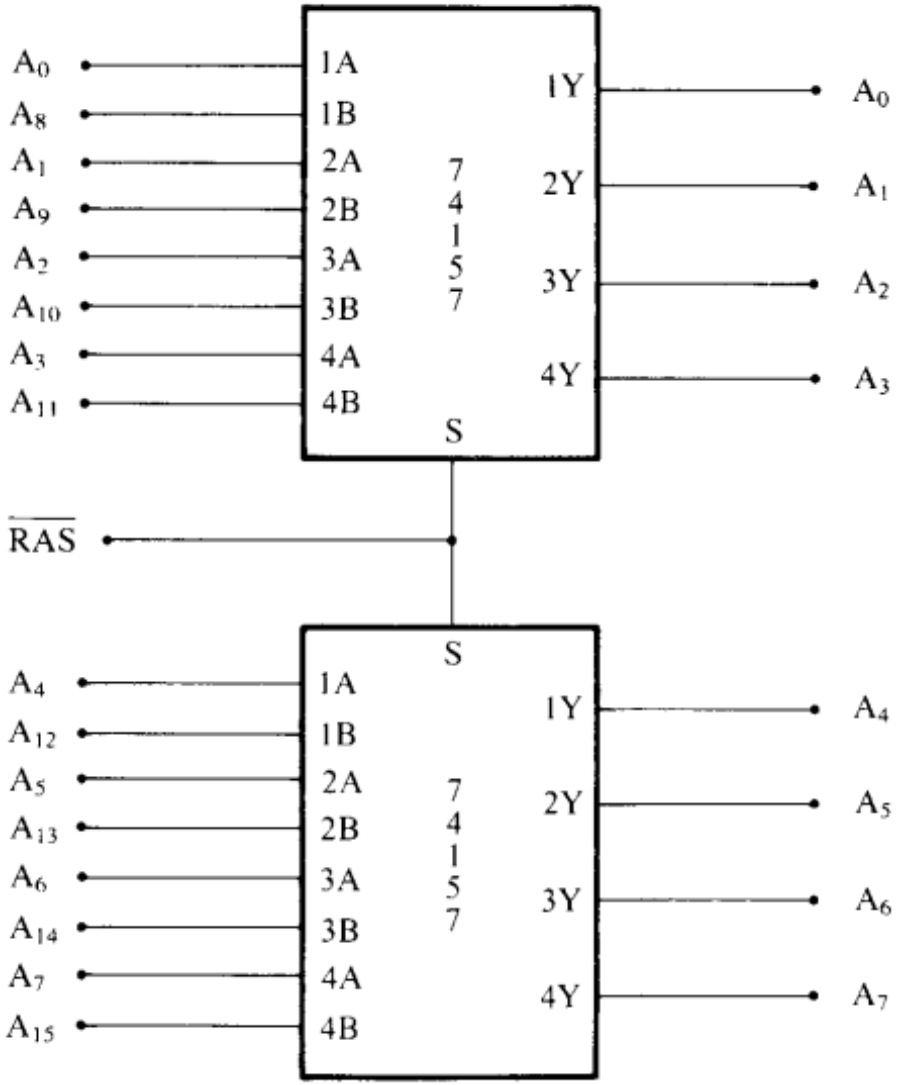
TMS4464 . . . JL OR NL PACKAGE
(TOP VIEW)



(a)

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1-DQ4	Data-In/Data-Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

Address multiplexer for the TMS4464 DRAM



References

- https://www.youtube.com/watch?v=P0oJPvwca6I

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Thank You