BITS Pilani

Microprocessors & Interfacing

8254 Programmable Interrupt Timer

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8254 Timer

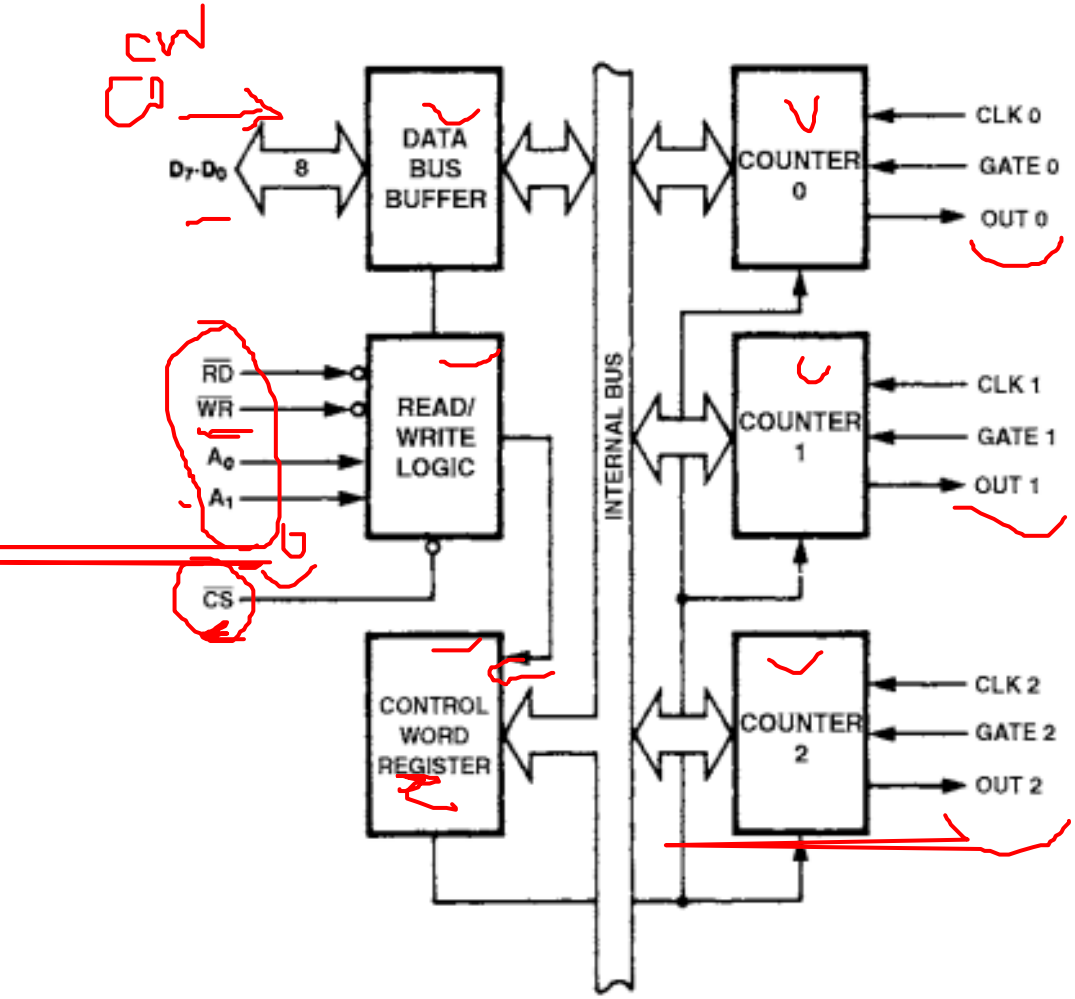
- The 8254 programmable interval timer consists of three independent 16-bit programmable counters (timers).
- Each counter is capable of counting in binary or binary-coded decimal (BCD).
- The maximum allowable input frequency to any counter is 10 MHz.
- This device is useful wherever the microprocessor must control real-time events. Some examples of usage include real-time clock and an events counter, and for motor speed and direction control.

8254 Timer

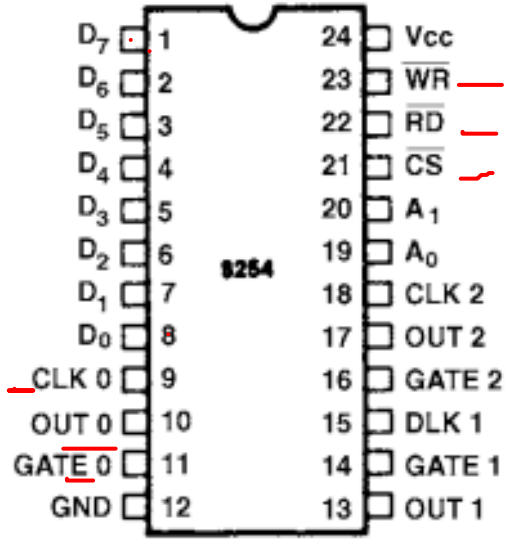
This timer also appears in the personal computer decoded at ports 40H–43H to do the following:

1. Generate a basic timer interrupt that occurs at approximately 18.2 Hz.
2. Cause the DRAM memory system to be refreshed.
3. Provide a timing source to the internal speaker and other devices. The timer in the personal computer is an 8253 instead of an 8254.

Functional Description



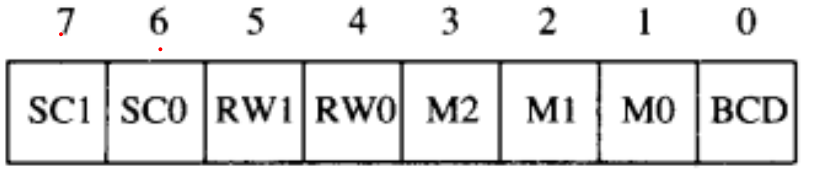
A_1	A_0	Function
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control word



Pin Definitions

A_0, A_1	The **address inputs** select one of four internal registers within the 8254. See Table 11–4 for the function of the A_1 and A_0 address bits.
CLK	The **clock** input is the timing source for each of the internal counters. This input is often connected to the PCLK signal from the microprocessor system bus controller.
$\overline{\text{CS}}$	**Chip select** enables the 8254 for programming and reading or writing a counter.
G	The **gate input** controls the operation of the counter in some modes of operation.
GND	**Ground** connects to the system ground bus.
OUT	A **counter output** is where the waveform generated by the timer is available.
$\overline{\text{RD}}$	**Read** causes data to be read from the 8254 and often connects to the $\overline{\text{IORC}}$ signal.
Vcc	**Power** connects to the +5.0 V power supply.
$\overline{\text{WR}}$	**Write** causes data to be written to the 8254 and often connects to the write strobe ($\overline{\text{IOWC}}$).

Programming the 8254



Selects a BCD when a logic 1

Selects the mode (mode 0 - mode 5)

Read/write control
- 00 = counter latch command
- 01 = read/write least-significant byte only
- 10 = read/write most-significant byte only
- 11 = read/write least-significant byte first, followed by the most-significant byte

Selects counter
- 00 = counter 0
- 01 = counter 1
- 10 = counter 2
- 11 = read-back command

Programming the 8254

Control Word Format

$A_1,A_0 = 11$ $\overline{CS} = 0$ $\overline{RD} = 1$ $\overline{WR} = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

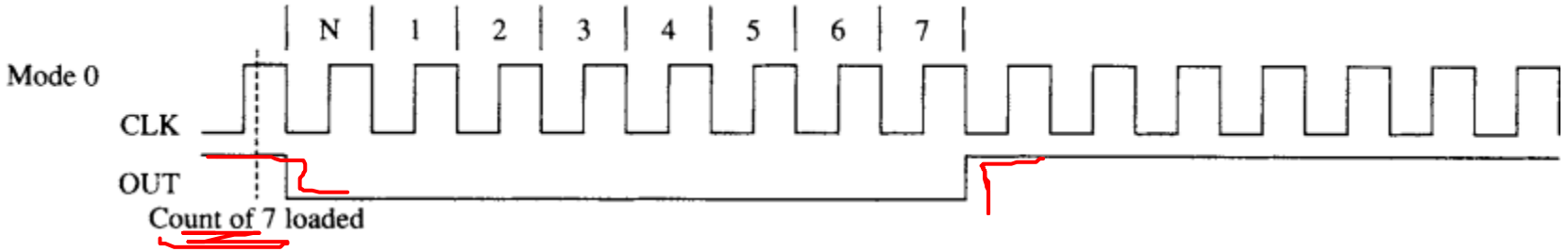
Read Write Operation Summary

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Figure 14. Read/Write Operations Summary

Mode 0 (Interrupt on Terminal Count)

- Allows the 8254 counter to be used as an events counter.
- In this mode, the output becomes a logic 0 when the control word is written and remains there until N plus the number of programmed counts. For example, if a count of 5 is programmed, the output will remain a logic 0 for 6 counts beginning with N. Note that the gate (G) input must be a logic 1 to allow the counter to count. If G becomes a logic 0 in the middle of the count, the counter will stop until G again becomes a logic 1.



Mode 0

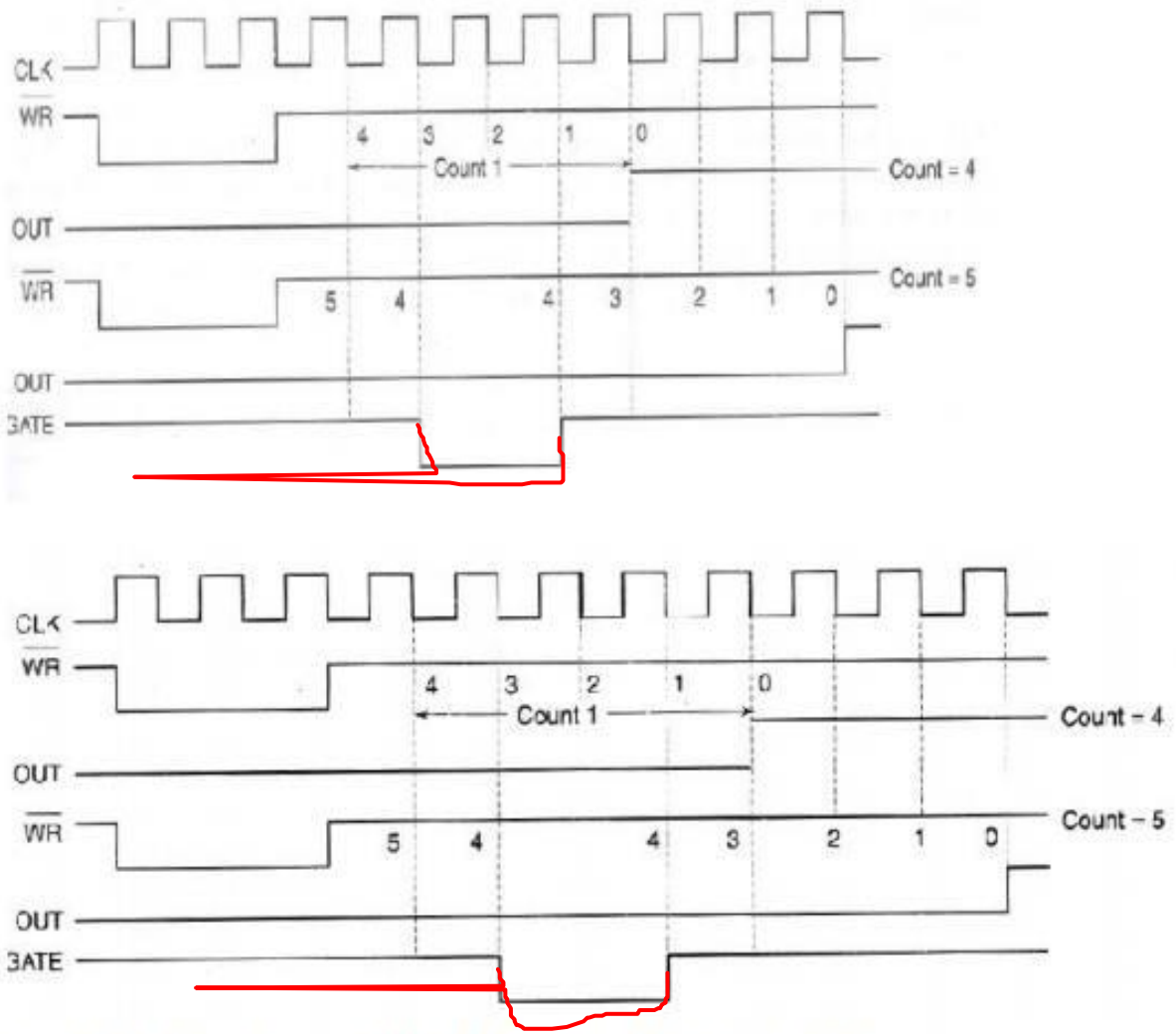
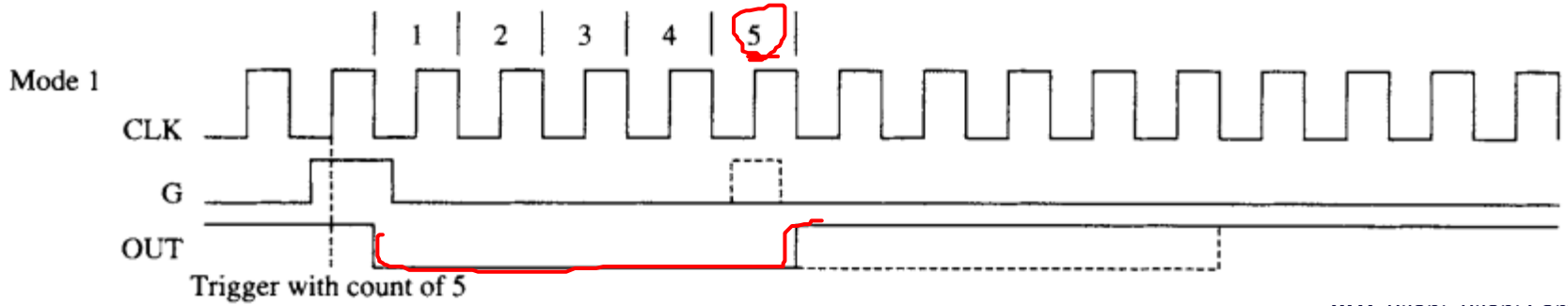


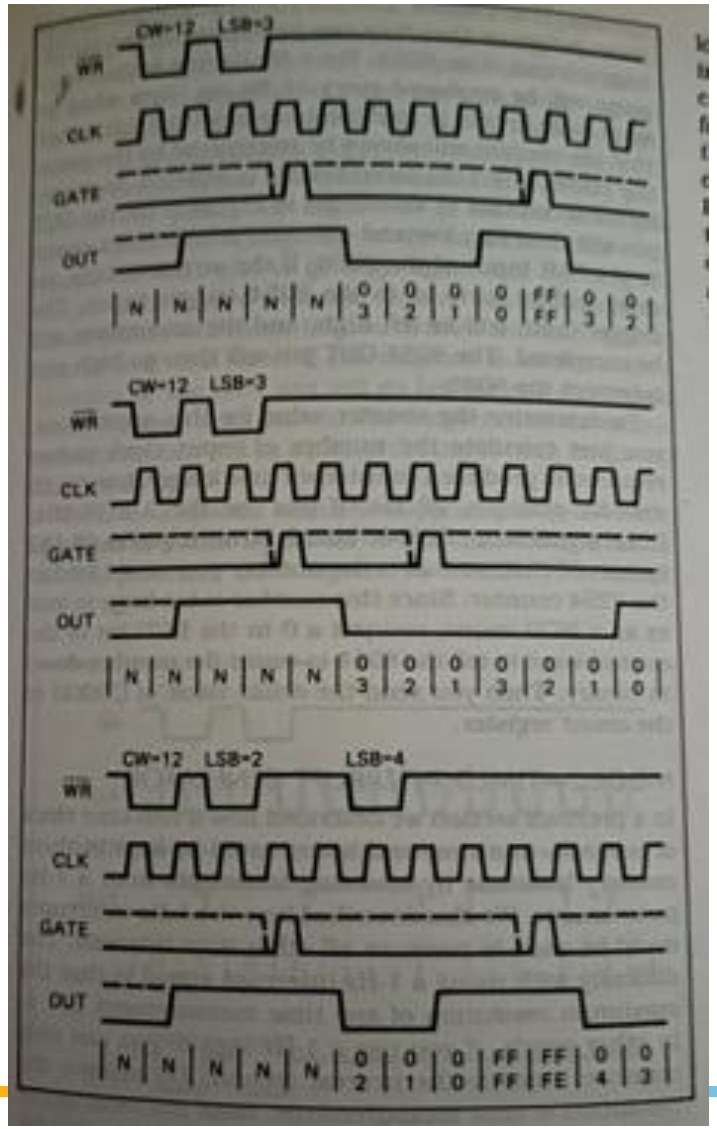
Fig. 3. 27 Waveforms WR, OUT and GATE in Mode 0

Mode 1 Programmable One Shot

- Causes the counter to function as a retriggerable, monostable multivibrator (one-shot).
- In this mode the G input triggers the counter so that it develops a pulse at the OUT connection that becomes a logic 0 for the duration of the count.
- If the count is 10, then the OUT connection goes low for 10 clocking periods when triggered. If the G input occurs within the duration of the output pulse, the counter is again reloaded with the count and the OUT connection continues for the total length of the count.

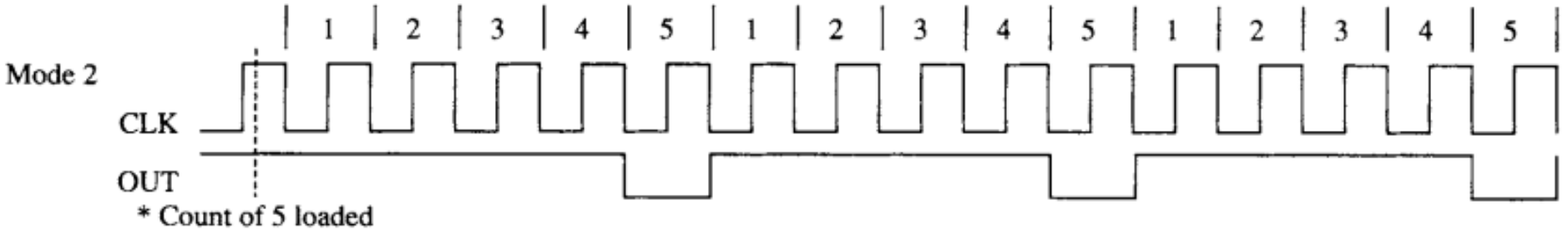


Mode 1


CW=12 LSB=3
WR
CLK
GATE
OUT
N N N N N 03 02 01 00 FFFF 03 02
CW=12 LSB=3
WR
CLK
GATE
OUT
N N N N N 03 02 01 03 02 01 00
CW=12 LSB=2 LSB=4
WR
CLK
GATE
OUT
N N N N N 02 01 00 FFFF FFFE 04 03

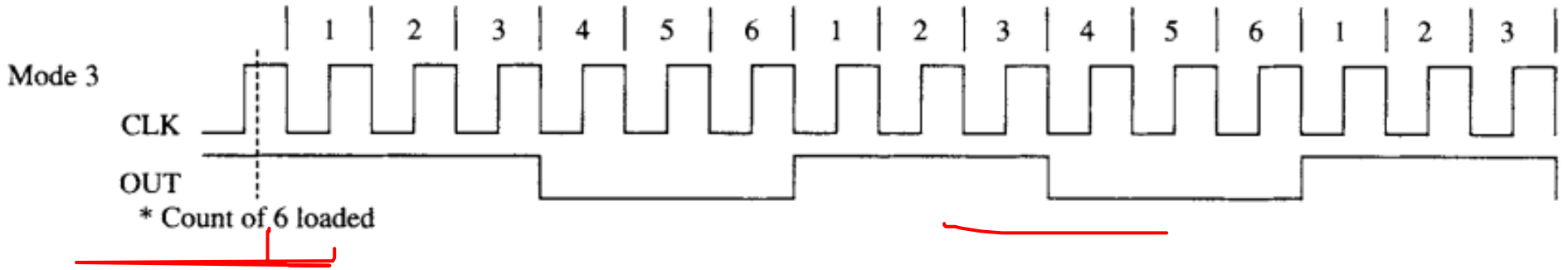
Mode 2 Rate Generator

- Allows the counter to generate a series of continuous pulses that are one clock pulse wide.
- The separation between pulses is determined by the count. For example, for a count of 10, the output is a logic 1 for nine clock periods and low for one clock period.
- This cycle is repeated until the counter is programmed with a new count or until the G pin is placed at a logic 0 level.
- The G input must be a logic 1 for this mode to generate a continuous series of pulses



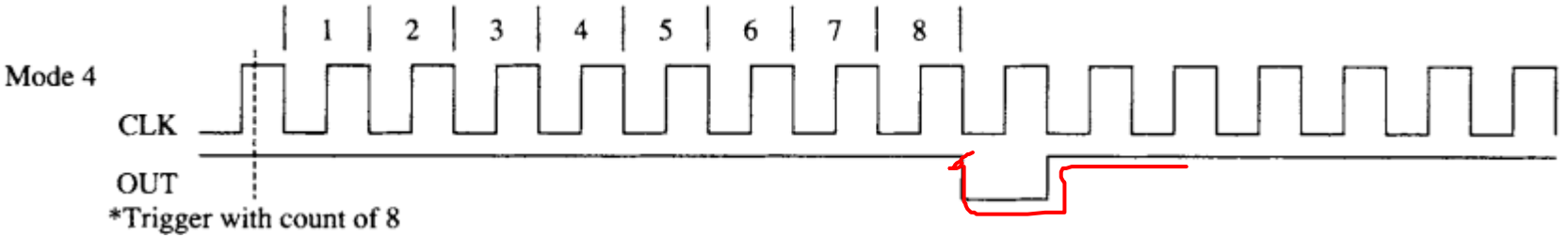
Mode 3 Square Wave Generator

- Generates a continuous square wave at the OUT connection, provided that the G pin is a logic 1.
- If the count is even, the output is high for one half of the count and low for one half of the count. If the count is odd, the output is high for one clocking period longer than it is low.
- For example, if the counter is programmed for a count of 5, the output is high for three clocks and low for two clocks.



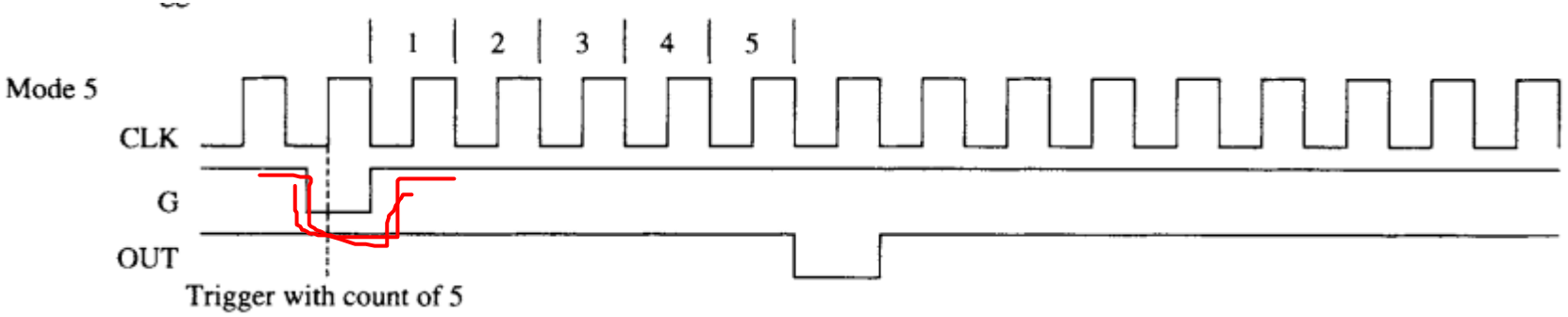
Mode 4 S/W Trigger Strobe

- Allows the counter to produce a single pulse at the output.
- If the count is programmed as a 10, the output is high for 10 clocking periods and low for one clocking period.
- The cycle does not begin until the counter is loaded with its complete count.
- This mode operates as a software triggered oneshot.
- As with modes 2 and 3, this mode also uses the G input to enable the counter. The G input must be a logic 1 for the counter to operate for these three modes.

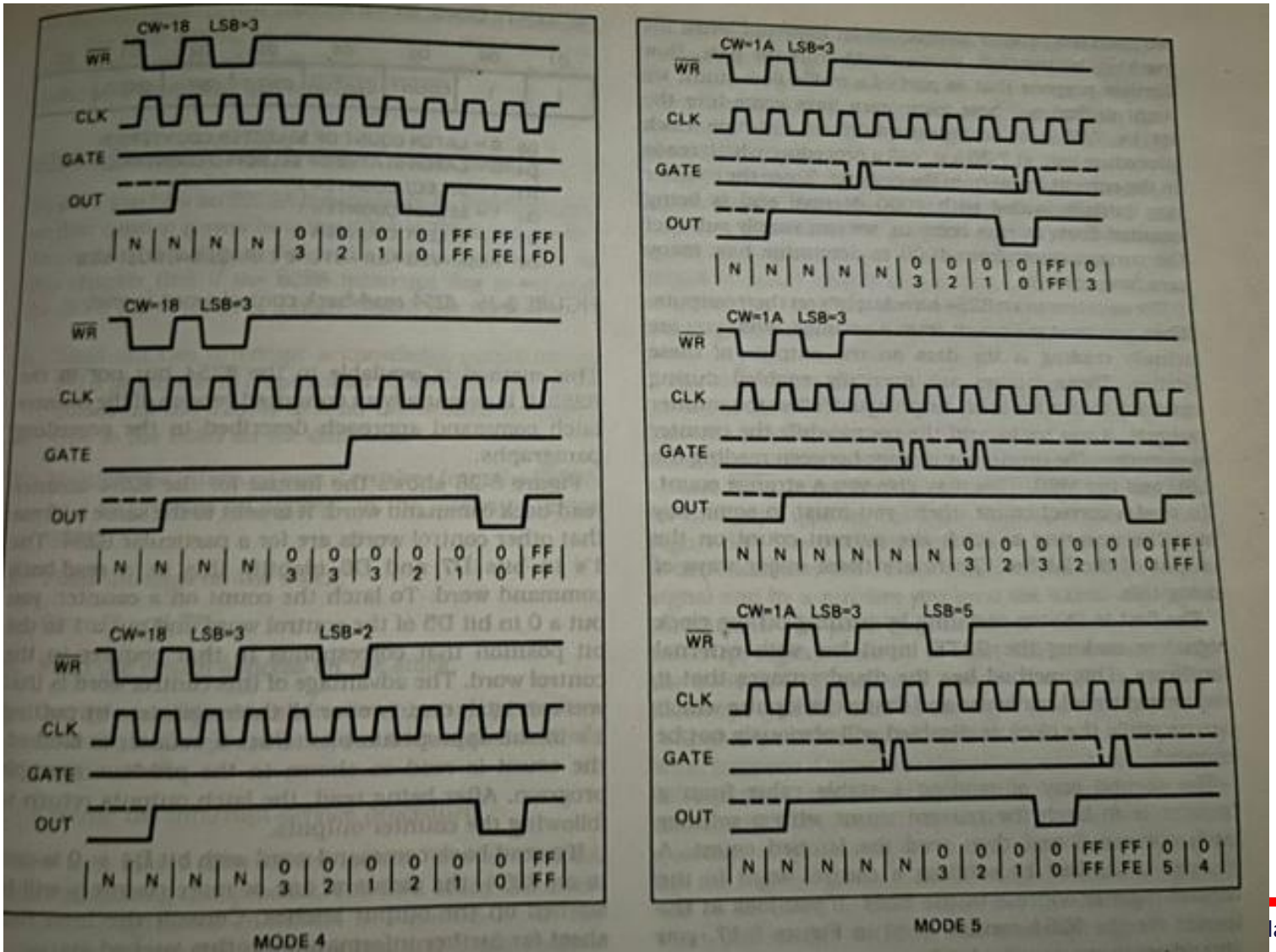


Mode 5 H/W Trigger Strobe

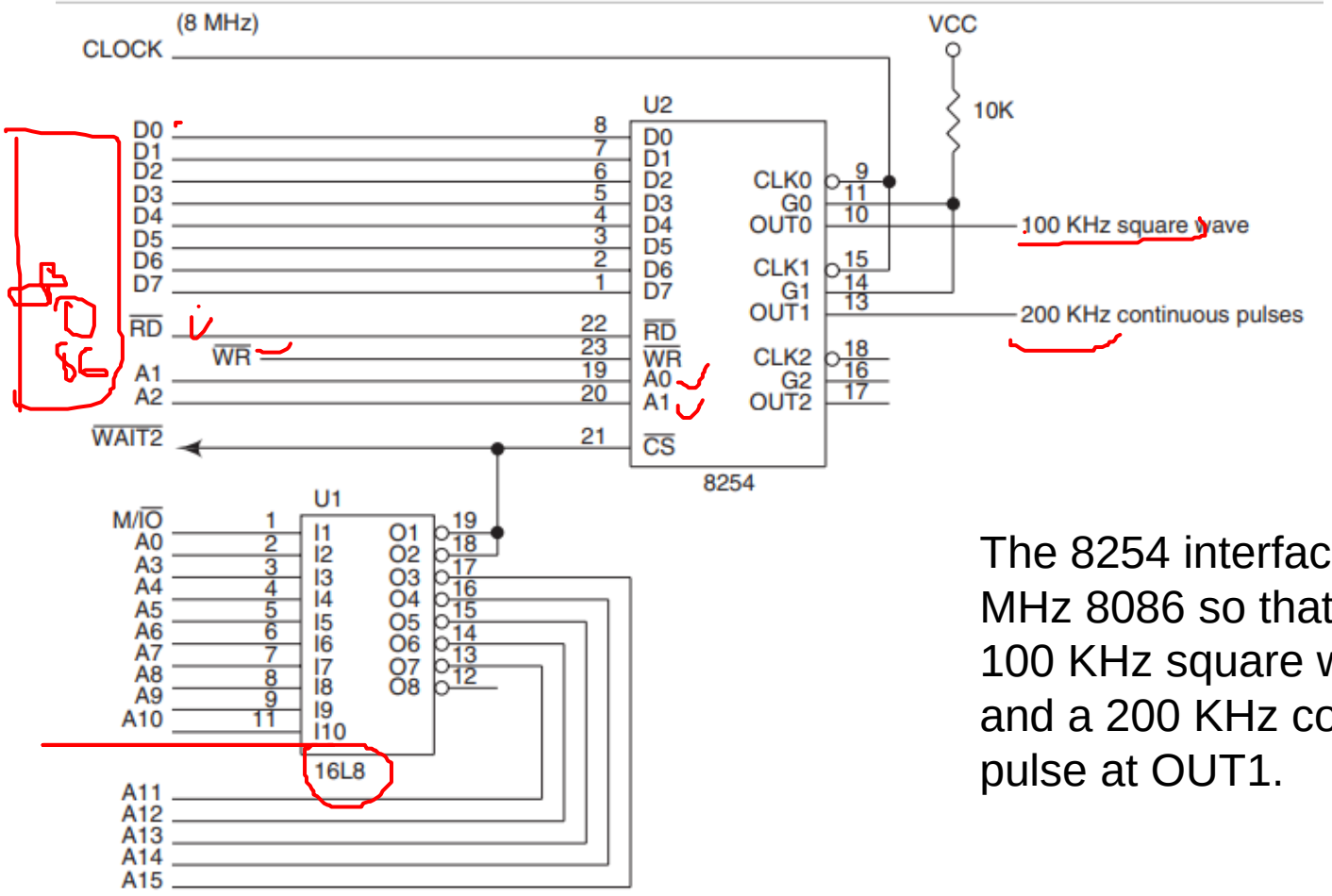
- A hardware triggered one-shot that functions as mode 4, except that it is started by a trigger pulse on the G pin instead of by software.
- This mode is also similar to mode 1 because it is retriggerable.



Mode 4 Vs Mode 5



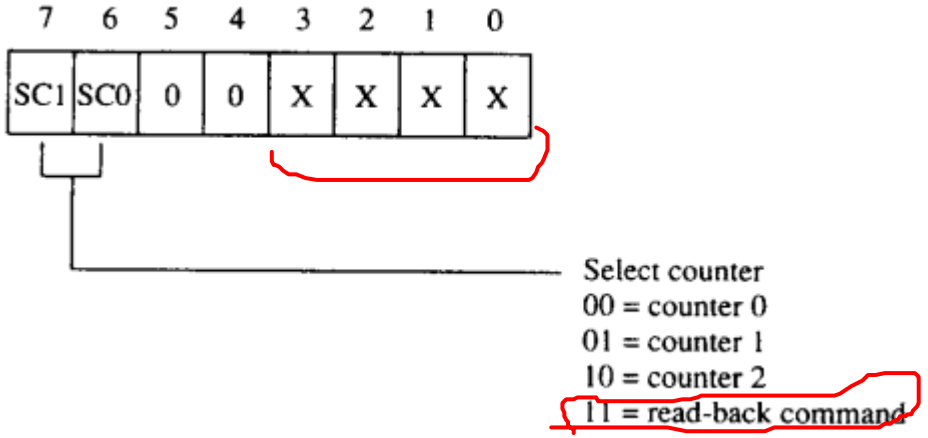
Generating a Waveform with the 8254



The 8254 interfaced to an 8 MHz 8086 so that it generates a 100 KHz square wave at OUT0 and a 200 KHz continuous pulse at OUT1.

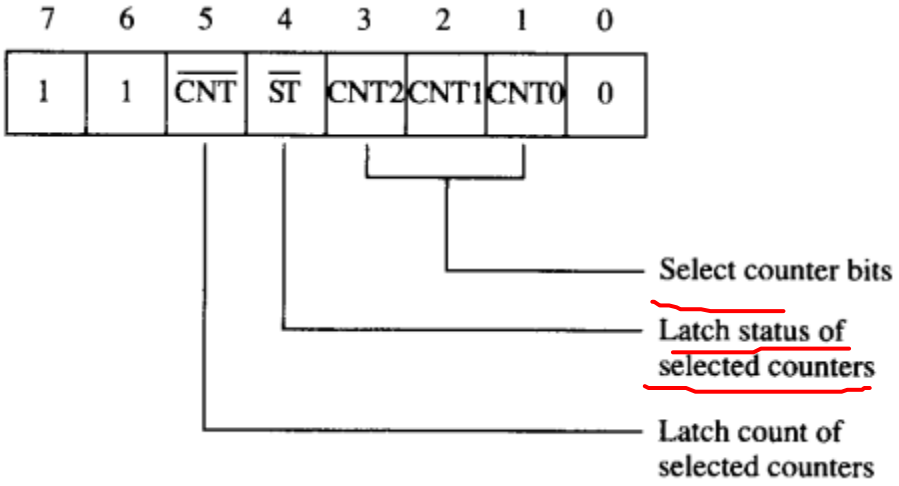
Reading a Counter

- Each counter has an internal latch that is read with the read counter port operation. These latches will normally follow the count.
- If the contents of the counter are needed, then the latch can remember the count by programming the counter latch control word which causes the contents of the counter to be held in a latch until they is read. Whenever a read from the latch or the counter is programmed, the latch tracks the contents of the counter



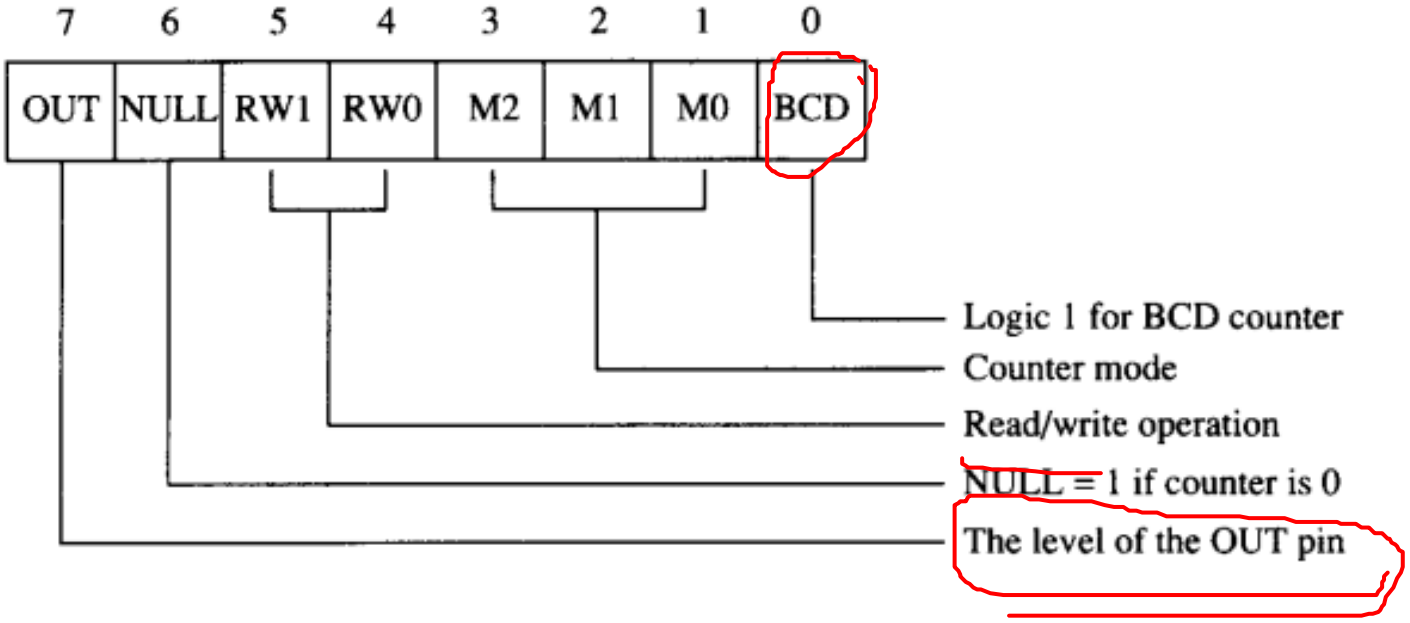
The 8254-2 read-back control word

- When it is necessary for the contents of more than one counter to be read at the same time, we use the read-back control word.
- With the read-back control word, the CNT' bit is a logic 0 to cause the counters selected by CNT0, CNT1, and CNT2 to be latched. If the status register is to be latched, then the bit is placed at a logic 0.



The 8254-2 status register

- Status register, which shows the state of the output pin, whether the counter is at its null state (0), and how the counter is programmed.



Programming 8254

```
;A procedure that programs the 8254 timer
TIME    PROC    NEAR USES AX DX
        MOV  DX, 703H          ; Control register
        MOV  AL, 00010110B     ; Program counter 0: Mode 3, LSB only
        OUT  DX, AL
        MOV  AL, 01010100B     ; Program counter 1: Mode 2, LSB only
        OUT  DX, AL

        MOV  DX, 700H          ; Counter 0
        MOV  AL, 80            ; Load initial count 80d into counter 0
                               ; LS byte of initial count
        OUT  DX, AL
        MOV  DX, 701H          ; Counter 1
        MOV  AL, 40            ; Load initial count 40d into counter 1
        OUT  DX, AL
        MOV  AL, 0             ;Then MS byte of initial count
        OUT  DX, AL
        RET
TIME    ENDP
```

Applications of 8254

- Real time clock
- Event-counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

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