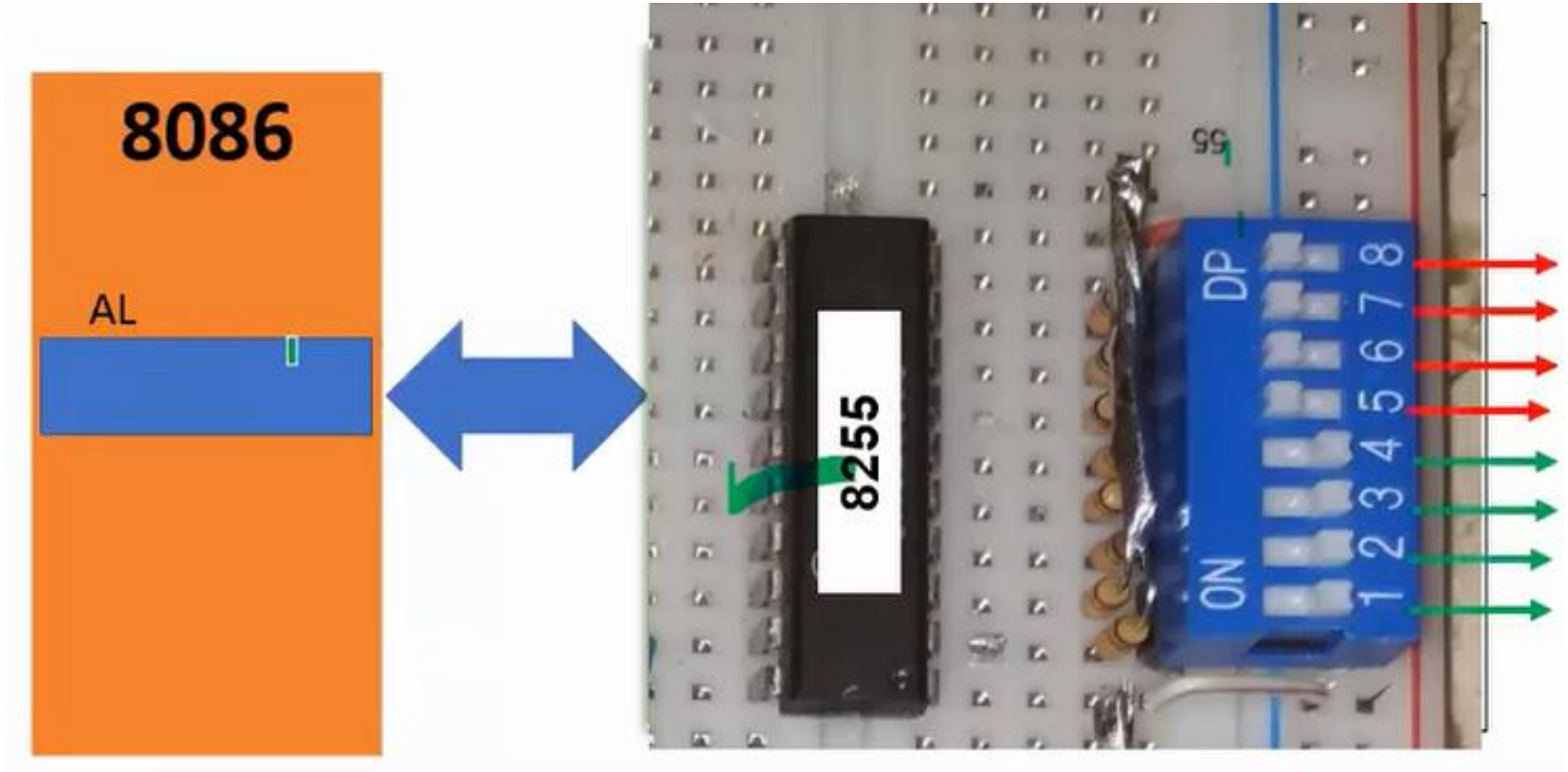
Microprocessors & Interfacing

8255 IO Interfacing

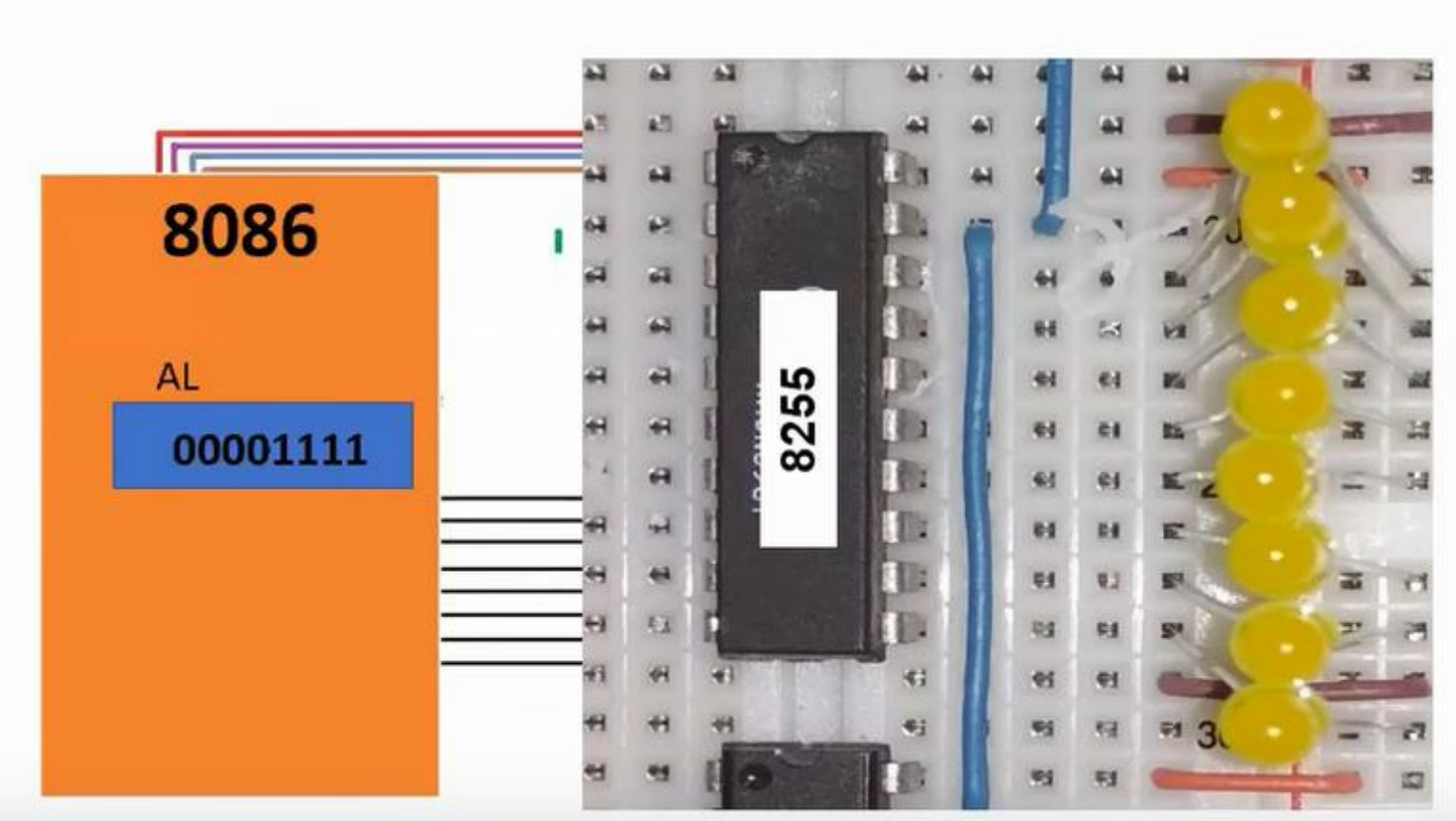
BITS Pilani

Dr. Gargi Prabhu
Department of CS & IS

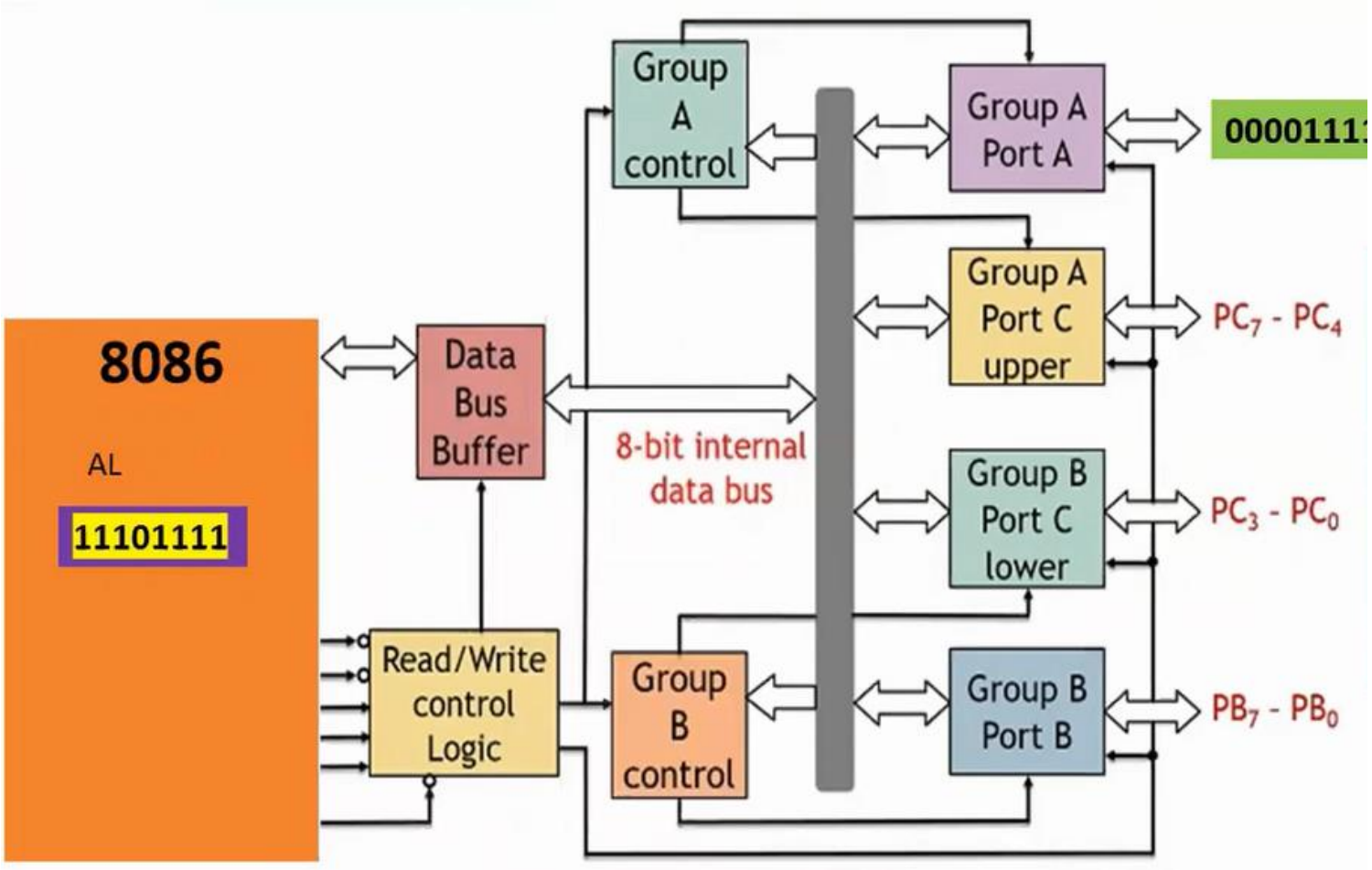
82C55 Interfacing : IN AL, 15



OUT 15, AL



Interfacing



Bidirectional Mode

- In bidirectional mode, each of the three I/O ports (Port A, Port B, and Port C) can function as both input and output.
- This means that each bit of the port can be individually configured as either an input or an output.
- This flexibility is useful when interfacing with external devices that both send and receive data through the same port.

Handshaking Mode

- Handshaking refers to a method of communication between two devices where control signals are exchanged to coordinate the transfer of data.
- In the context of the 8255, handshaking mode is often used in conjunction with bidirectional mode to ensure reliable data transfer between the microprocessor and external devices. Handshaking involves signals such as Strobe (STB), Acknowledge (ACK), and Busy (BSY) that indicate the readiness of devices to send or receive data.

Mode 0

1. Two 8-bit ports (port A and port B) and two 4-bit ports (port C upper and lower) are available. The two 4-bit

ports can be combined used as a third 8-bit port.

2. Any port can be used as an input or output port.

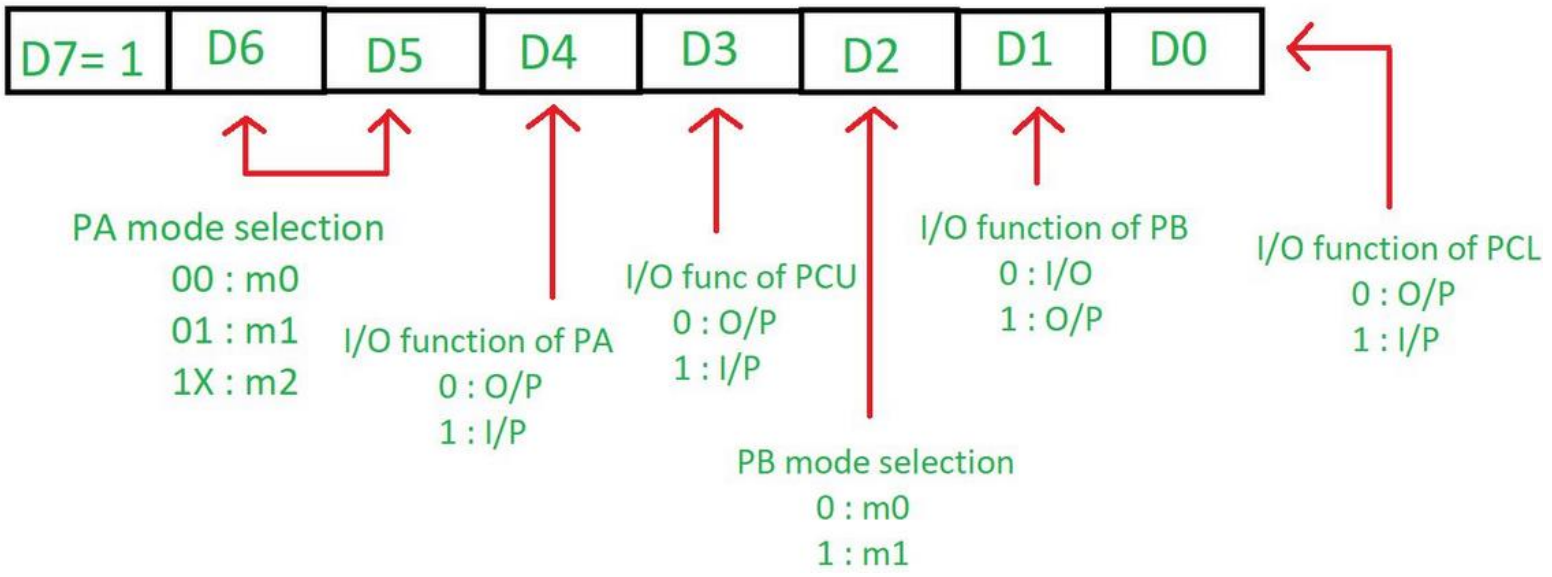
3. Output ports are latched. Input ports are not latched.

4. A maximum of four ports are available

Mode 0 Example

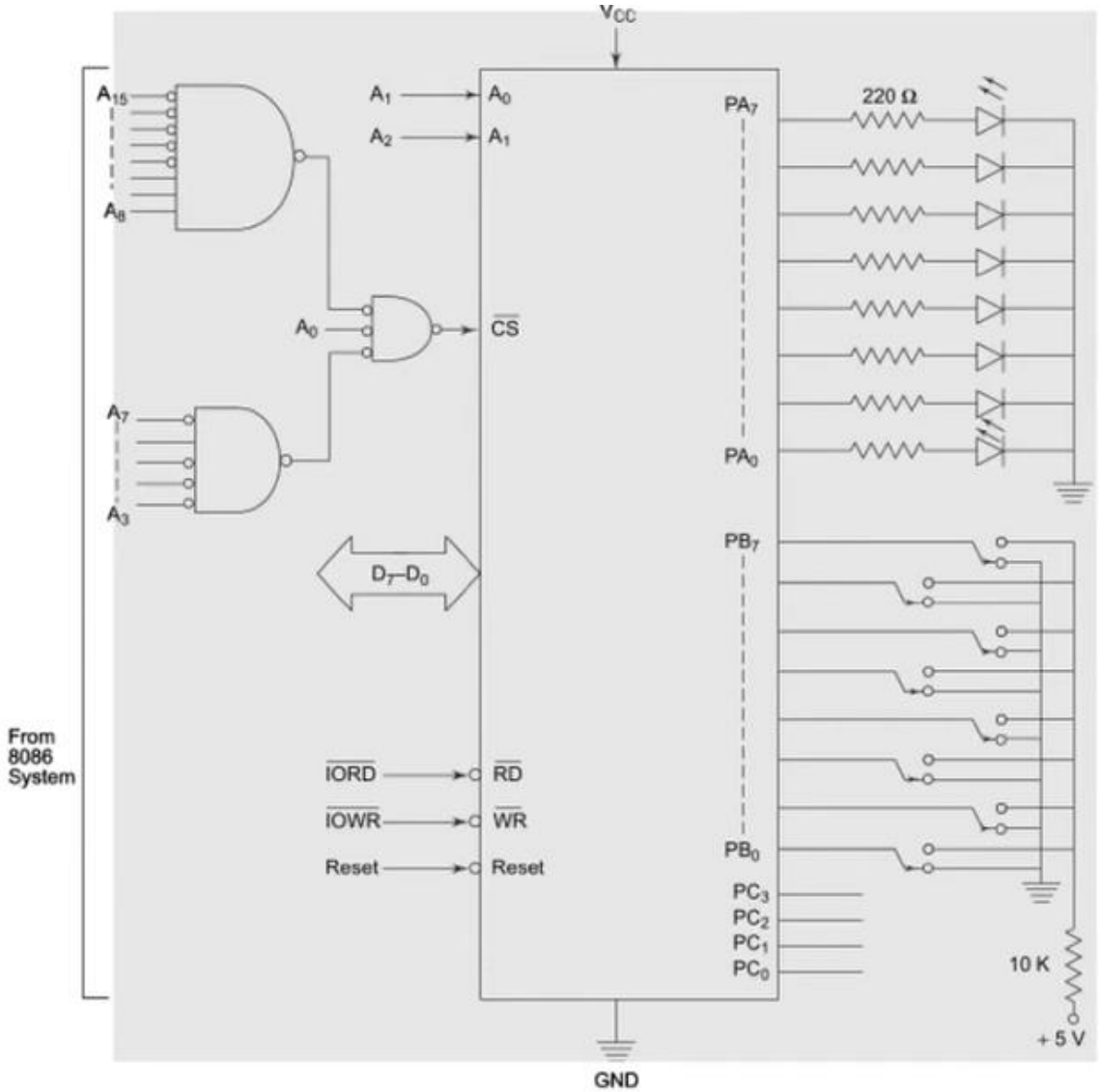
Interface an 8255 chip with 8086 to work as an I/O port. Initialize port A as output port, Port B as I/P port and Port C as O/p port. Port A address should be 0740H. Write an ALP to sense switch positions SW0-SW7 connected to port B. The sensed pattern to be displayed on port A, to which 8 LED's are connected, while port C displays number of on switches out ot eight switches.

Control Word



B7	B6	B5	B4	B3	B2	B1	B0	Control word
1	0	0	0	0	0	1	0	= 82 H
I/O mode	Port A in mode 0		Port A, O/P	Port C, O/P	Port B, mode 0	Port B, I/P	Port C, O/P	

Circuit


Vcc
A15
A8
A1
A2
A0
A1
A0
CS
A7
A3
D7–D0
From 8086 System
IORD
IOWR
Reset
RD
WR
Reset
PA7
PA0
PB7
PB0
PC3
PC2
PC1
PC0
220 Ω
10 K
+5 V
GND

Port Register Addressing

8255	I/O Address lines																Hex. Port Addresses
Ports	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_{09}	A_{08}	A_{07}	A_{06}	A_{05}	A_{04}	A_{03}	A_{02}	A_{01}	A_{00}	
PortA	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0740H
Port B	0	0	0	0	0	1	1	1	0	1	0	0	0	0	1	0	0742H
Port C	0	0	0	0	0	1	1	1	0	1	0	0	0	1	0	0	0744H
CWR	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	0746H

Program

```
     MOV DX, 0746 H          ; Initialise CWR with
     MOV AL, 82 H            ; control word 82H
     OUT DX, AL              ;
     SUB DX,04               ; Get address of port B in DX
     IN AL, DX               ; Read port B for switch
     SUB DX,02               ; positions in to AL and get port A address
                             ; in DX.
     OUT DX, AL              ; Display switch positions on port A
     MOV BL, 00 H            ; Initialise BL for switch count
     MOV CH, 08H             ; Initialise CH for total switch number
YY:  ROL AL                  ; Rotate AL through carry to check,
     JNC XX                  ; whether the switches are on or
     INC BL                  ; off, i.e. either 1 or 0
XX :DEC CH                   ; Check for next switch. If
     JNZ YY                  ; all switch are checked, the
     MOV AL, BL              ; number of on switches are
     ADD DX, 04              ; in BL.Display it on port C
     OUT DX,AL               ; lower.
     HLT                     ; Stop
```

Mode 1 (Strobed Input)

- Mode 1 operation causes port A and/or port B to function as latching input devices.
- This allows external data to be stored into the port until the microprocessor is ready to retrieve it.
- Port C is also used in mode 1 operation—not for data, but for control or handshaking signals that help operate either or both port A and port B as strobed input ports.
- The strobed input port captures data from the port pins when the strobe (STB') is activated.

Input control signal definitions

- STB’ (Strobe input) – If this lines falls to low, the data available at 8-bit input port is loaded into input latches.
- IBF (Input buffer full) – If this signal rises to logic 1, it indicates that data has been loaded into latches, i.e. it works as an acknowledgement.
- INTR (Interrupt request) – This active high output signal can be used to interrupt the CPU whenever an input device requests the service.

  The INTR becomes a logic 1 when the STB’ input returns to logic 1, and is cleared when the data are input from the port by the microprocessor

Input control signal definitions

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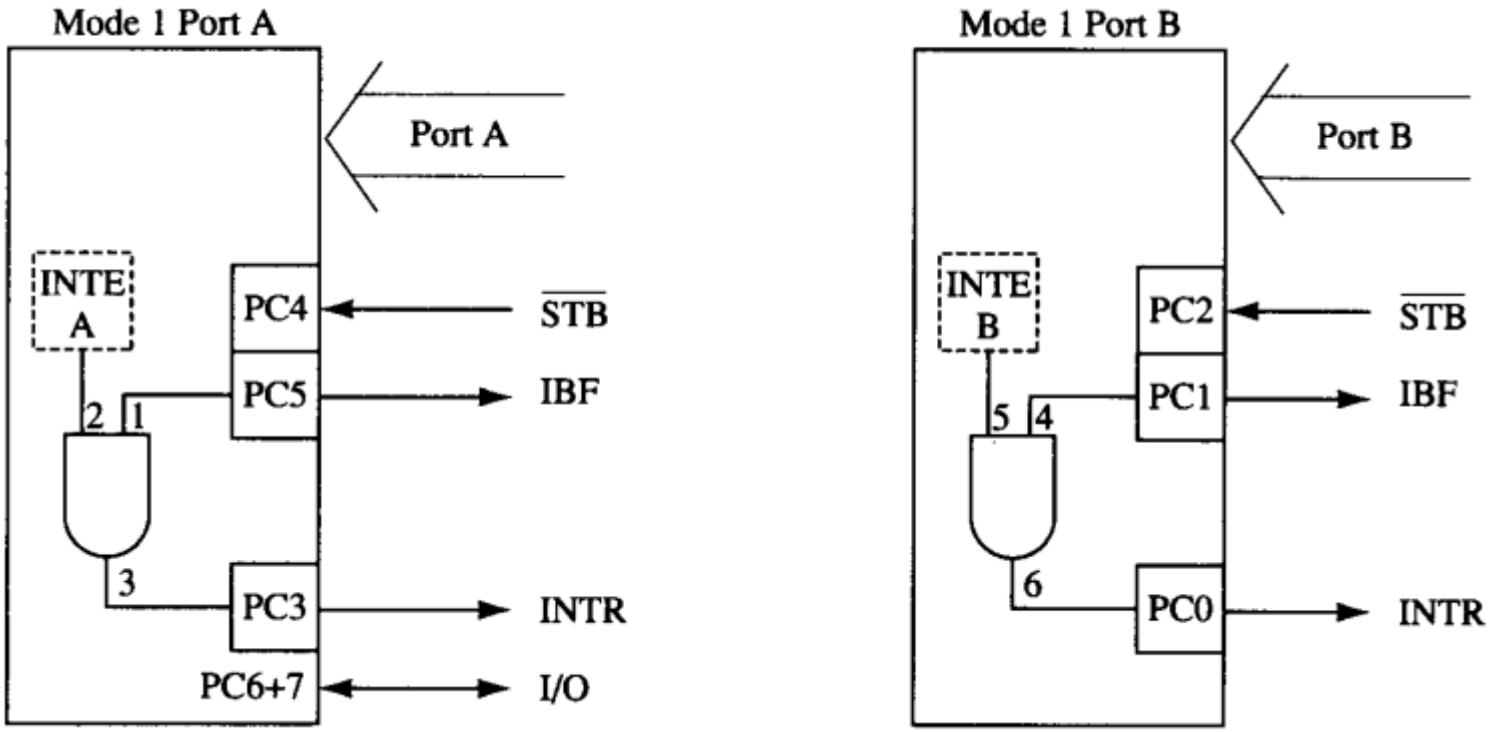
- **INTE** - The interrupt enable signal is neither an input nor an output; it is an internal bit programmed via the port PC4 (port A) or PC2 (port B) bit position.
- **PC7, PC6** - The port C pins 7 and 6 are general-purpose I/O pins that are available for any purpose.

Internal structure : Strobed input operation (mode 1) of the 82C55



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Thank You