Microprocessors & Interfacing

Macros & Hardware Specification

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Macros

- A macro is a group of instructions that perform one task, just as a procedure performs one task.
- Creating a macro is very similar to creating a new opcode
- Assembler inserts macro instructions into the program

Example

```
                        MOVE    MACRO A,B
                                PUSH  AX
                                MOV   AX,B
                                MOV   A,AX
                                POP   AX
                                ENDM

                                MOVE VAR1,VAR2      ;;move VAR2 into VAR1

0000  50                1       PUSH  AX
0001  A1 0002 R         1       MOV   AX,VAR2
0004  A3 0000 R         1       MOV   VAR1,AX
0007  58                1       POP   AX

                                MOVE  VAR3,VAR4     ;;move VAR4 into VAR3
0008  50                1       PUSH  AX
0009  A1 0006 R         1       MOV   AX,VAR4
000C  A3 0004 R         1       MOV   VAR3,AX
000F  58                1       POP   AX
```

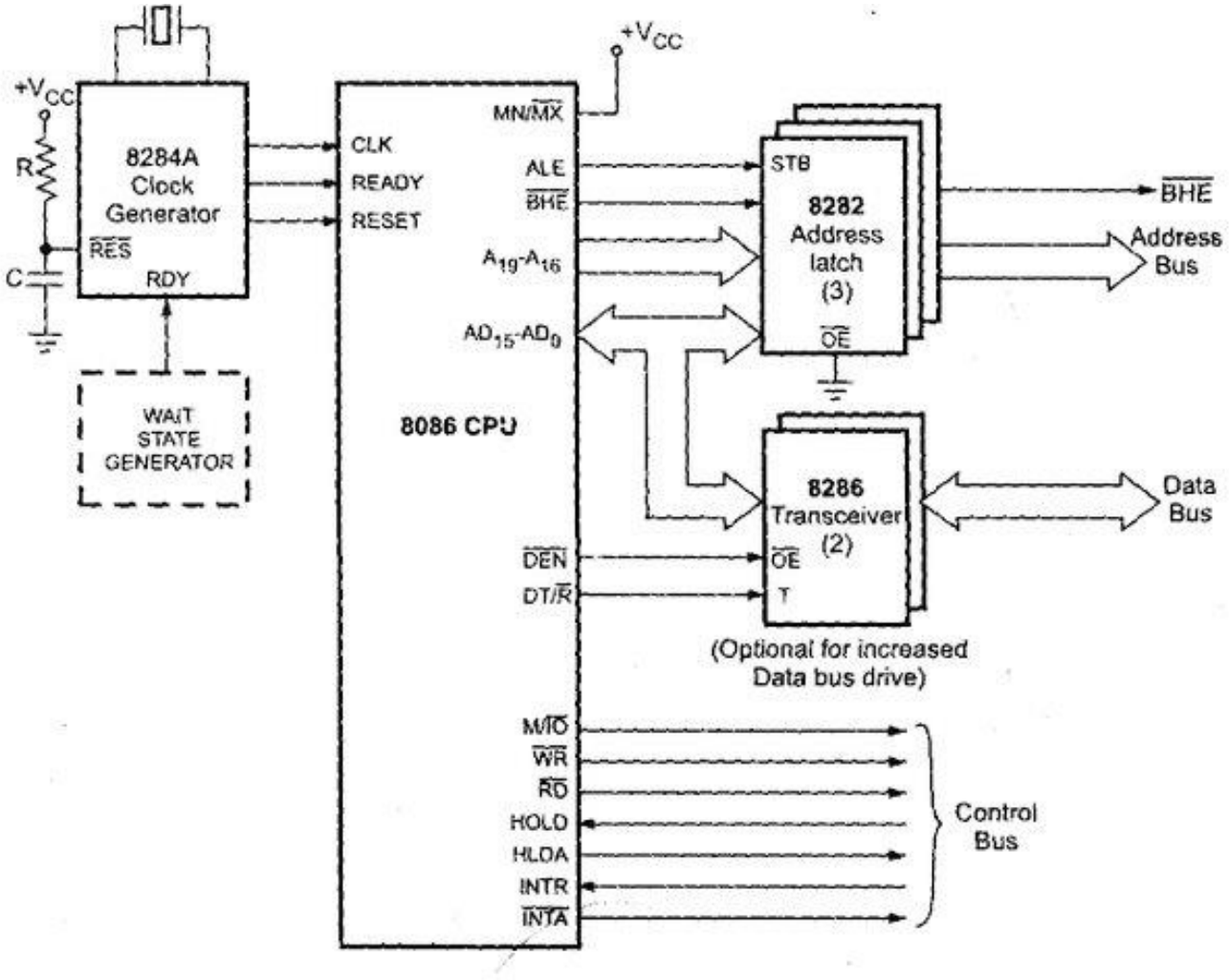
Local Variables in Macro

```
                                FILL    MACRO WHERE, HOW_MANY    ;;fill memory
                                        LOCAL FILL1
                                        PUSH  SI
                                        PUSH  CX
                                        MOV   SI,OFFSET WHERE
                                        MOV   CX,HOW_MANY
                                        MOV   AL,0
                                FILL1:  MOV   [SI],AL
                                        INC   SI
                                        LOOP  FILL1
                                        POP   CX
                                        POP   SI
                                        ENDM

                                        FILL  MES1,5

                        1               LOCAL FILL1
0014  56                 1              PUSH  SI
0015  51                 1              PUSH  CX
0016  BE 0000 R          1              MOV   SI,OFFSET MES1
0019  B9 0005            1              MOV   CX,5
001C  B0 00              1              MOV   AL,0
0029  88 04              1      ??0000:MOV   [SI],AL
```

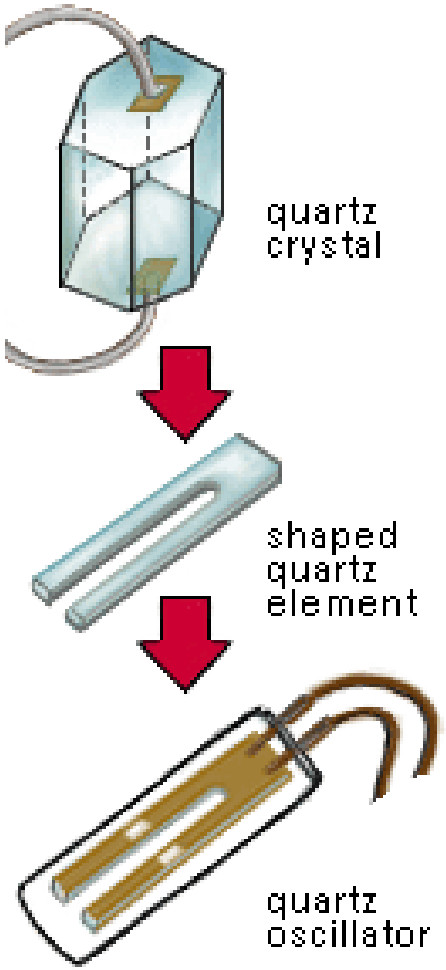
Hardware Specifications



Clock

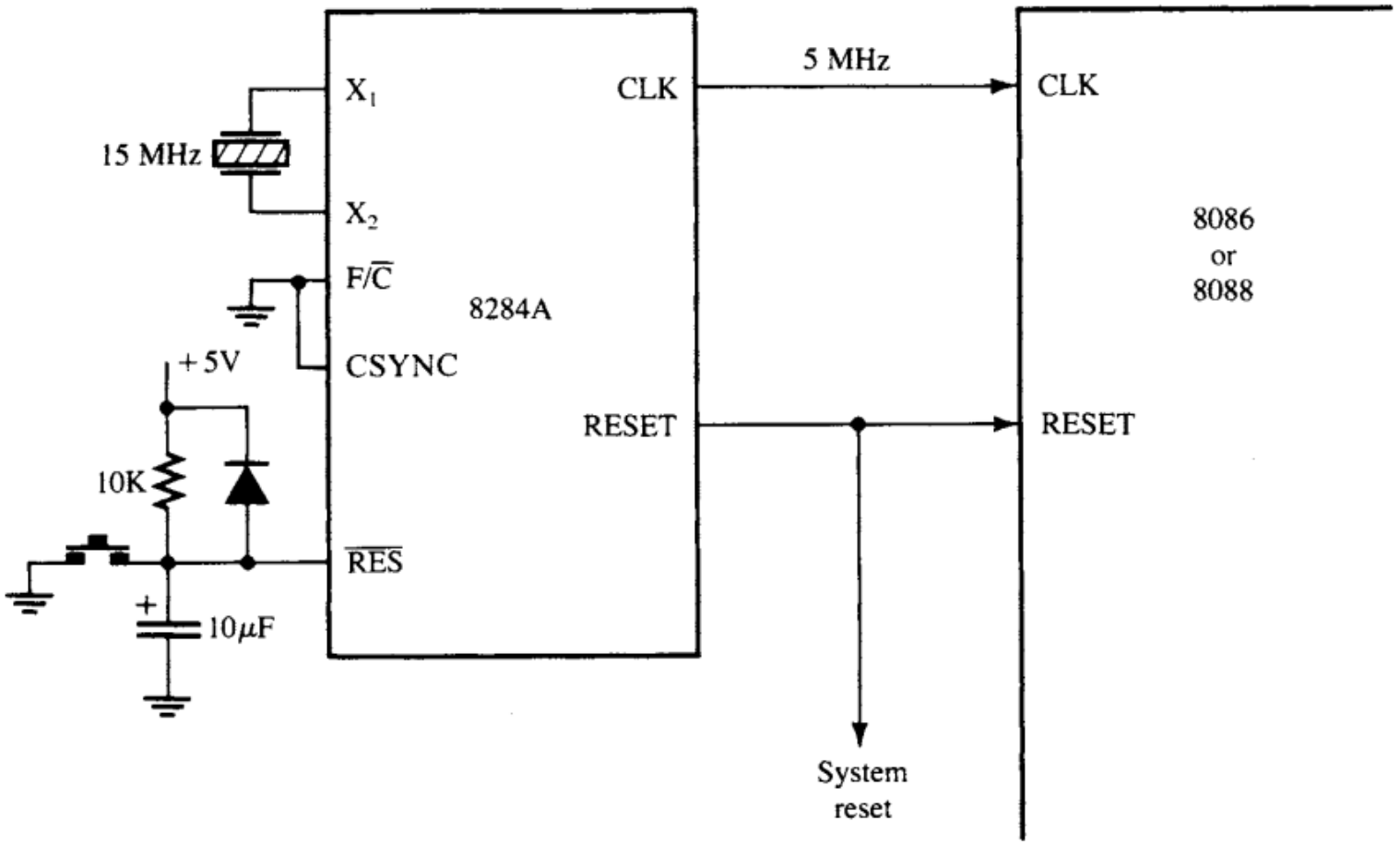
- CLK is crystal controlled clock sent to 8086 from an external clock generator device such as 8284
- One cycle of this clock is called a state
- A state is measured as falling edge of one clock pulse to falling edge of next clock pulse
- Different versions of 8086 have maximum clock frequencies of between 5MHz and 10MHz
- The minimum time of one state will be between 100nS to 200nS
- A basic operation such as reading a byte from memory /port or writing a byte to a memory/port is called a machine cycle

Clock

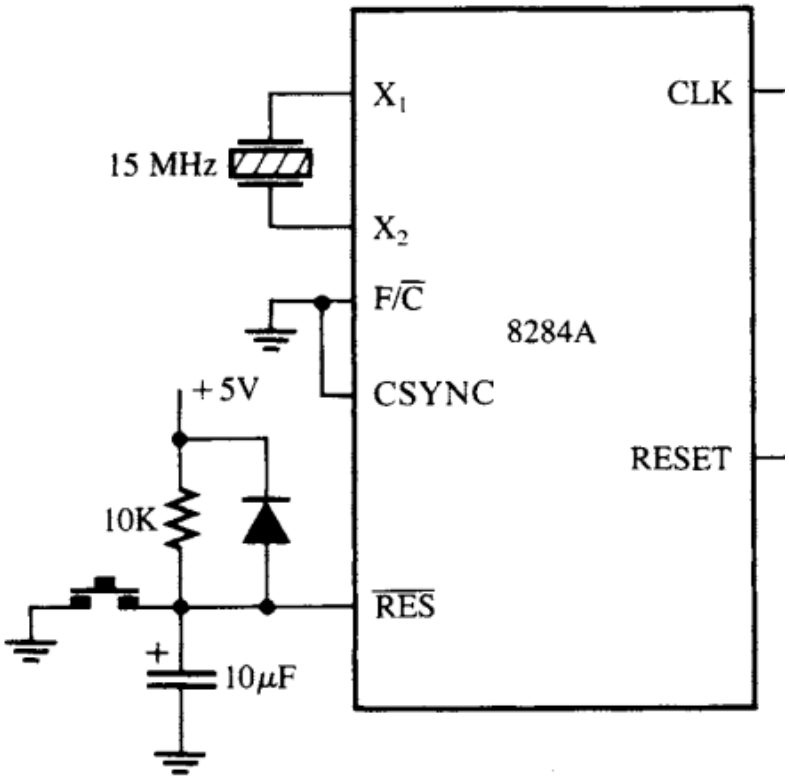


When a voltage source is applied to a small thin piece of quartz crystal, it begins to change shape producing a characteristic known as the **Piezo-electric effect**.

Clock


15 MHz
X_1
X_2
F/$\overline{C}$
CSYNC
+5V
10K
$\overline{RES}$
+
10μF
8284A
CLK
RESET
5 MHz
CLK
RESET
8086
or
8088
System
reset

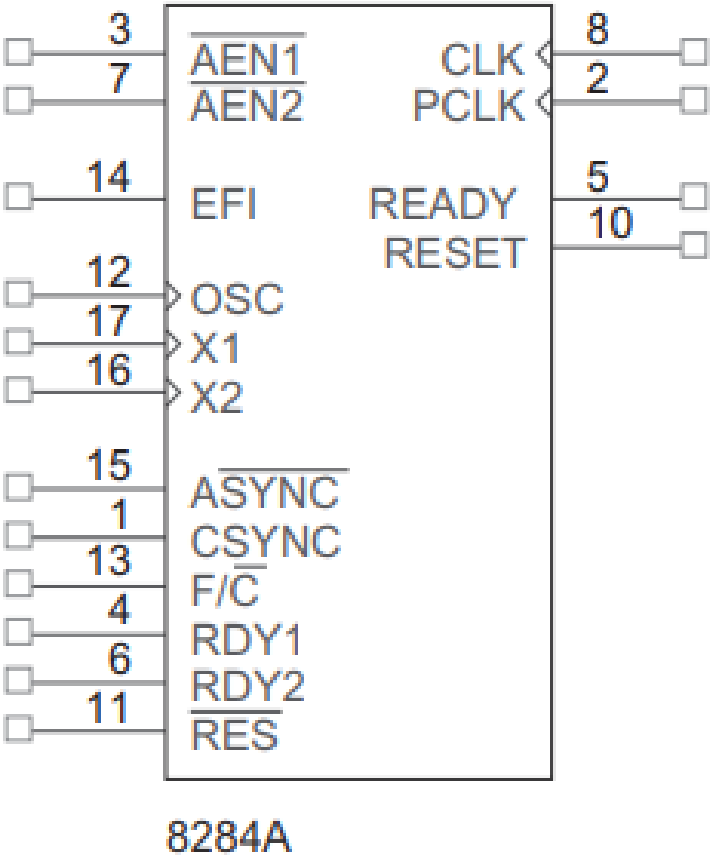
Clock Generator 8284A



The 8284A provides the following basic functions or signals:

- Clock generation
- RESET synchronization
- READY synchronization
- TTL-level peripheral clock signal

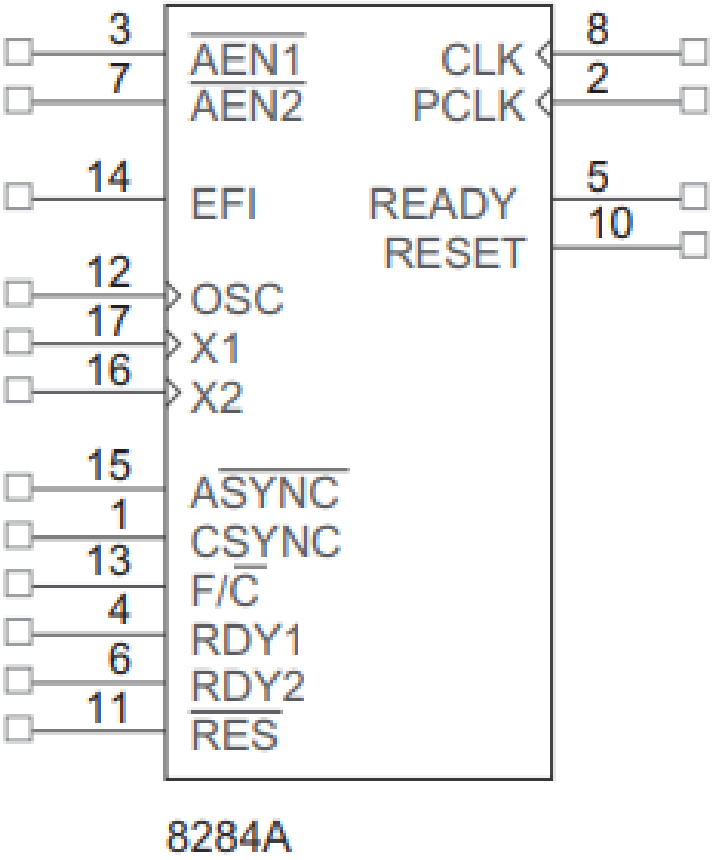
8284A Pin-out



X1 & X2

- These two are the input pins of 8284 and is required while connecting quartz crystal.
- When External Frequency Input(EFI) is provided then X1 is connected with V_{CC} or GND.
- The crystal oscillator pins connect to an external crystal used as the timing source for the clock generator and all its functions.

8284A Pin-out

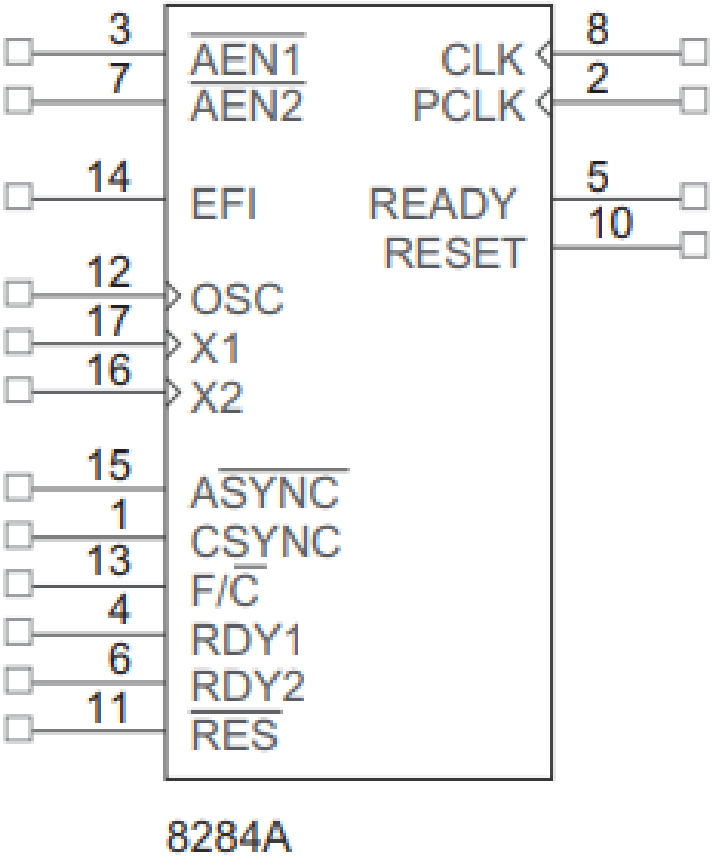


8284A

$\overline{\text{AEN1}}$ & $\overline{\text{AEN2}}$

- The address enable pins are provided to qualify the bus ready signals, RDY1 and RDY2
- Used to cause wait states, along with the RDY1 and RDY2 inputs.
- Wait states are generated by the READY pin of the 8086/8088 microprocessors, which is controlled by these two inputs

8284A Pin-out



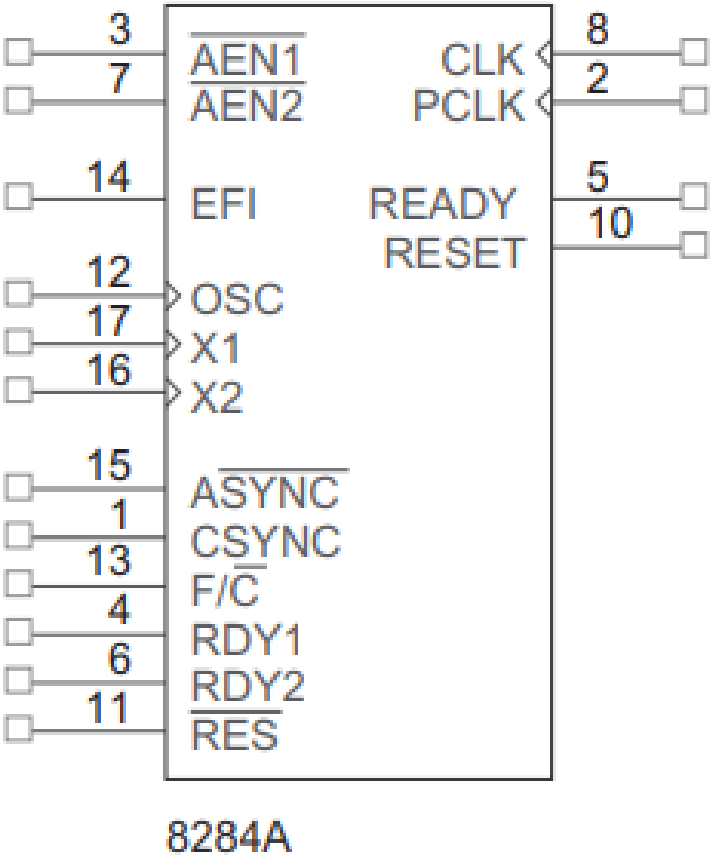
RDY1 and RDY2

- **T**he bus ready inputs are provided, in conjunction with the AEN pins, to cause wait states in an 8086/8088-based system

$\overline{\text{ASYNC}}$

he ready synchronization selection input selects either one or two stages of synchronization for the RDY1 and RDY2 inputs.

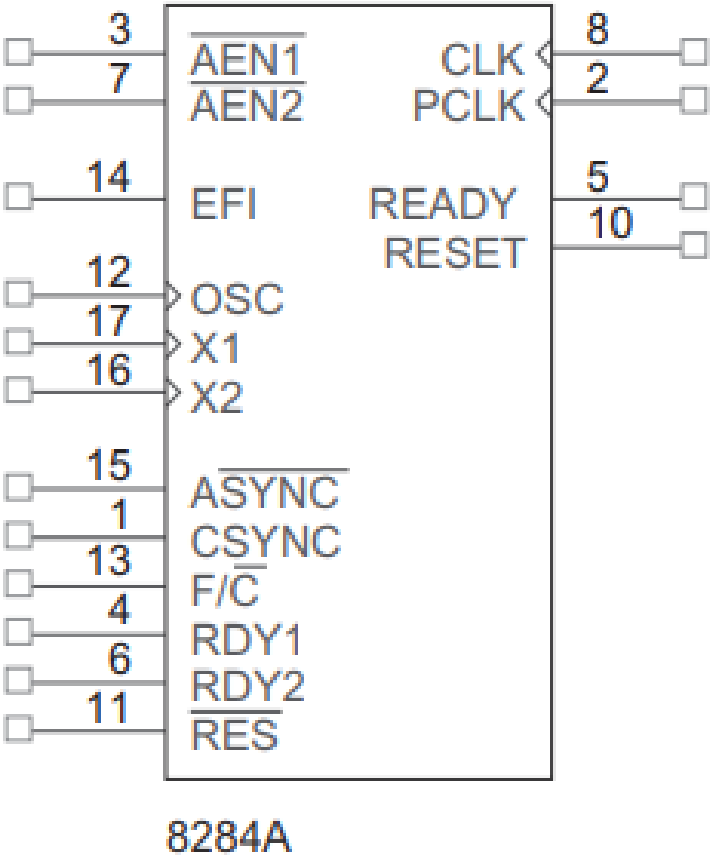
8284A Pin-out



READY

- Ready is an output pin that connects to the 8086/8088 READY input.
- This signal is synchronized with the RDY1 and RDY2 inputs.

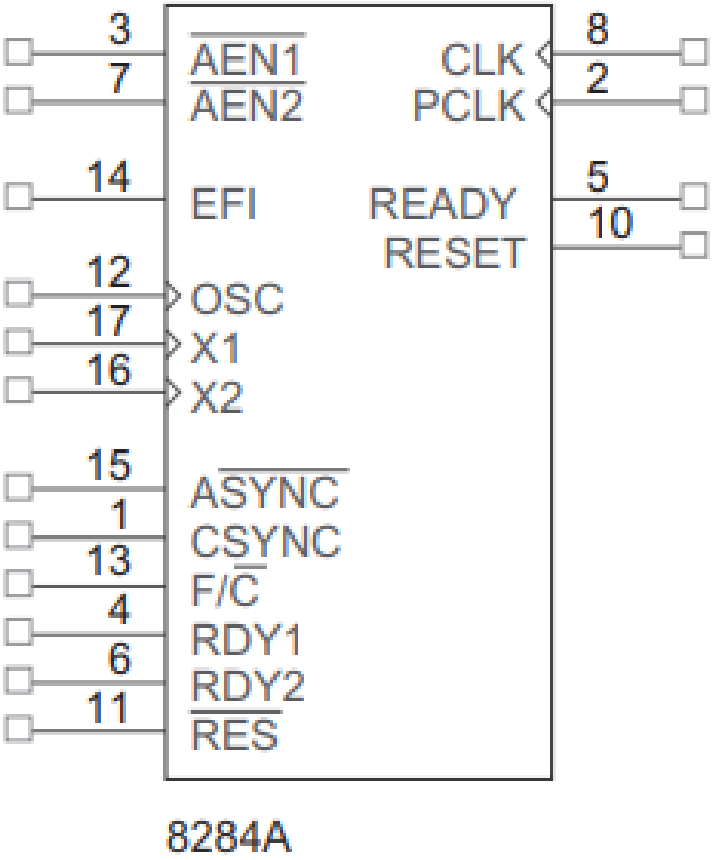
8284A Pin-out



GND
The ground pin connects to ground.

VCC
This power supply pin connects to +5.0 V with a tolerance of ±10%.

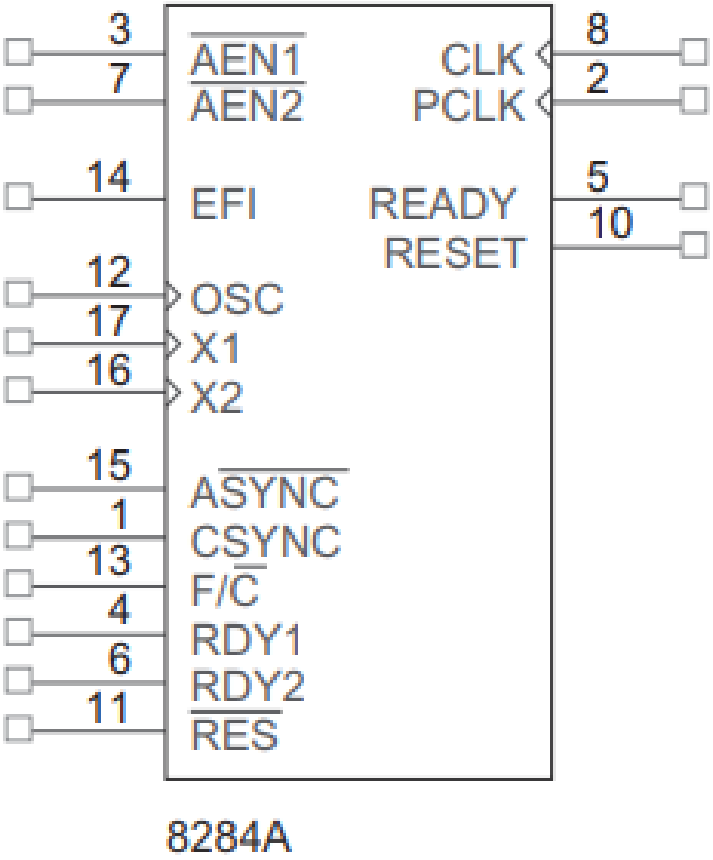
8284A Pin-out



PCLK

- The peripheral clock signal is one sixth the crystal or EFI input frequency, and has a 50% duty cycle.
- The PCLK output provides a clock signal to the peripheral equipment in the system.

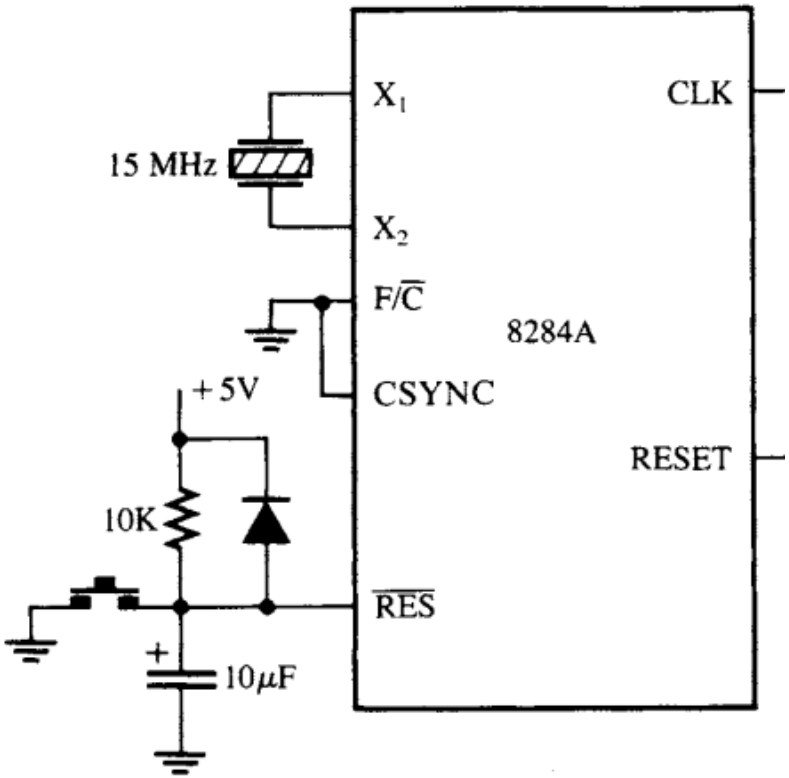
8284A Pin-out



OSC

- The oscillator output is a TTL-level signal that is at the same frequency as the crystal or EFI input.
- The OSC output provides an EFI input to other 8284A clock generators in some multiple-processor systems

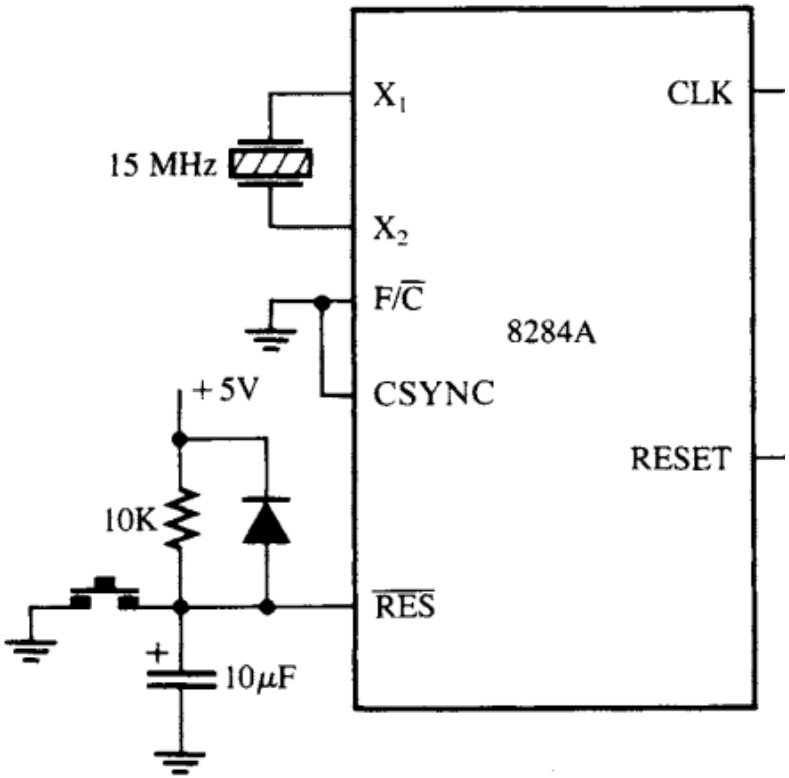
Clock



F/C’

- The frequency/crystal select input chooses the clocking source for the 8284A.
- If this pin is held high, an external clock is provided to the EFI input pin; if it is held low, the internal crystal oscillator provides the timing signal.
- The external frequency input is used when the F/C’ pin is pulled high.
- EFI supplies the timing whenever the F/C’ pin is high

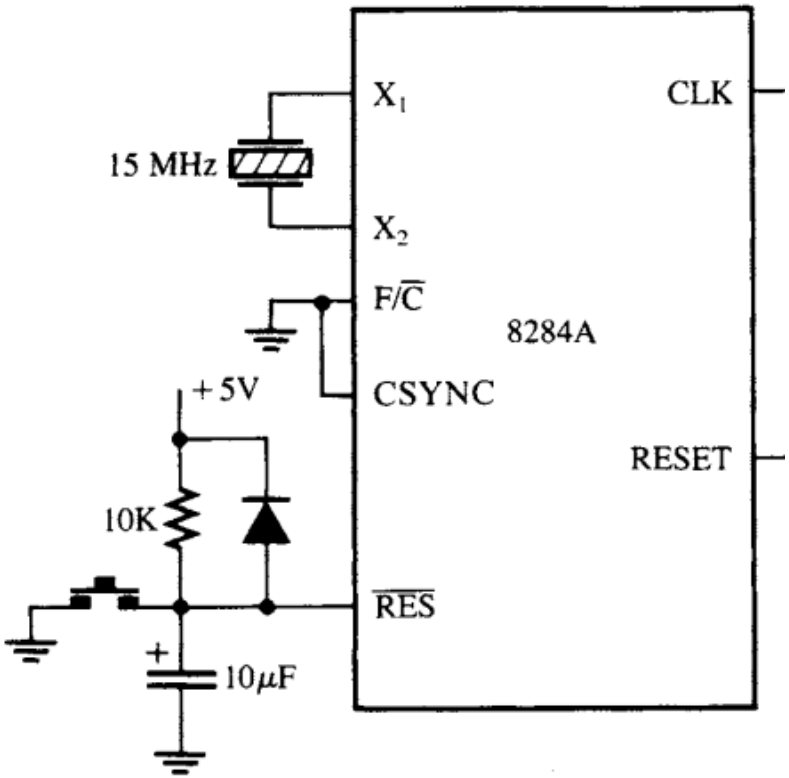
Clock



CSYNC

- Stands for clock synchronization. It is an active high signal that synchronizes the clock signal of various 8284 chips present in a single system.
- As this pin shows the significance of EFI based operation, thus it is grounded when the crystal is present between the inputs X_1 and X_2.

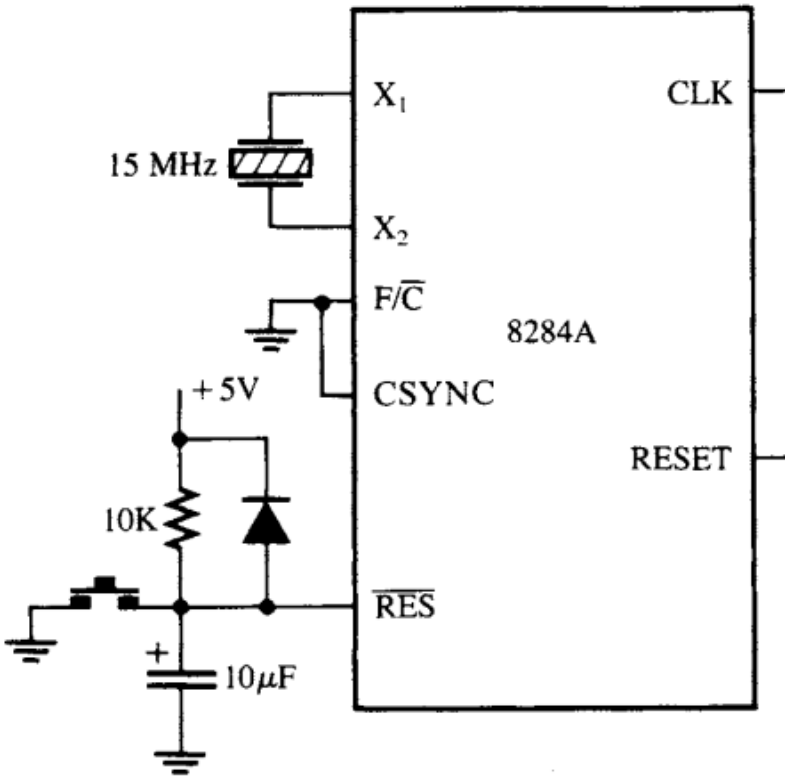
Clock



RES'

- It is an active low pin that produces a reset signal for 8284.
- The pin is connected to the RC network for providing power on reset.

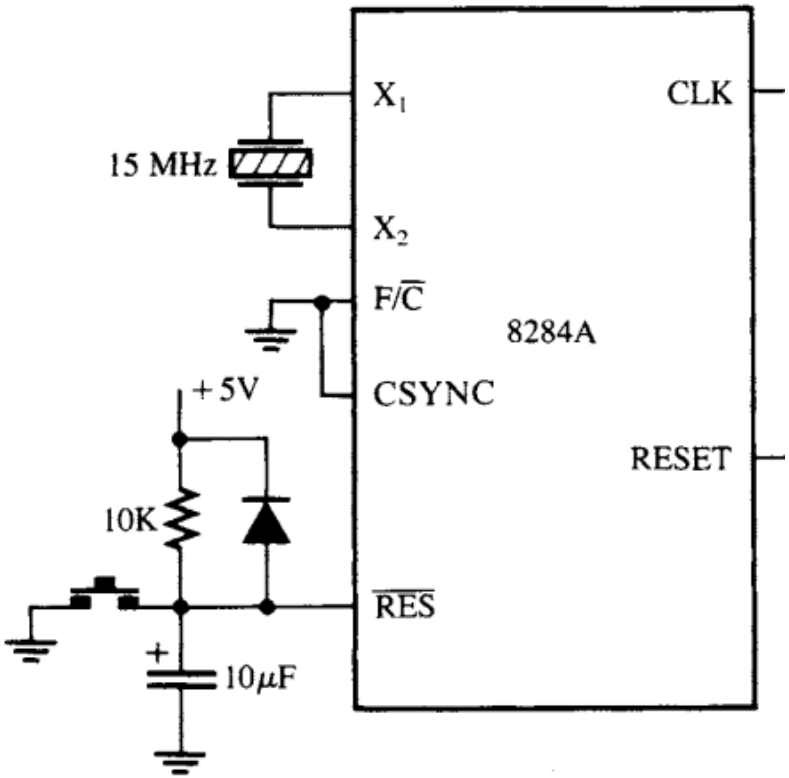
Clock



CLK

- Stands for clock.
- The signal frequency at this pin will be one-third to the EFI/crystal frequency having a duty cycle of 33%.
- It is connected to the clock input of the processor.

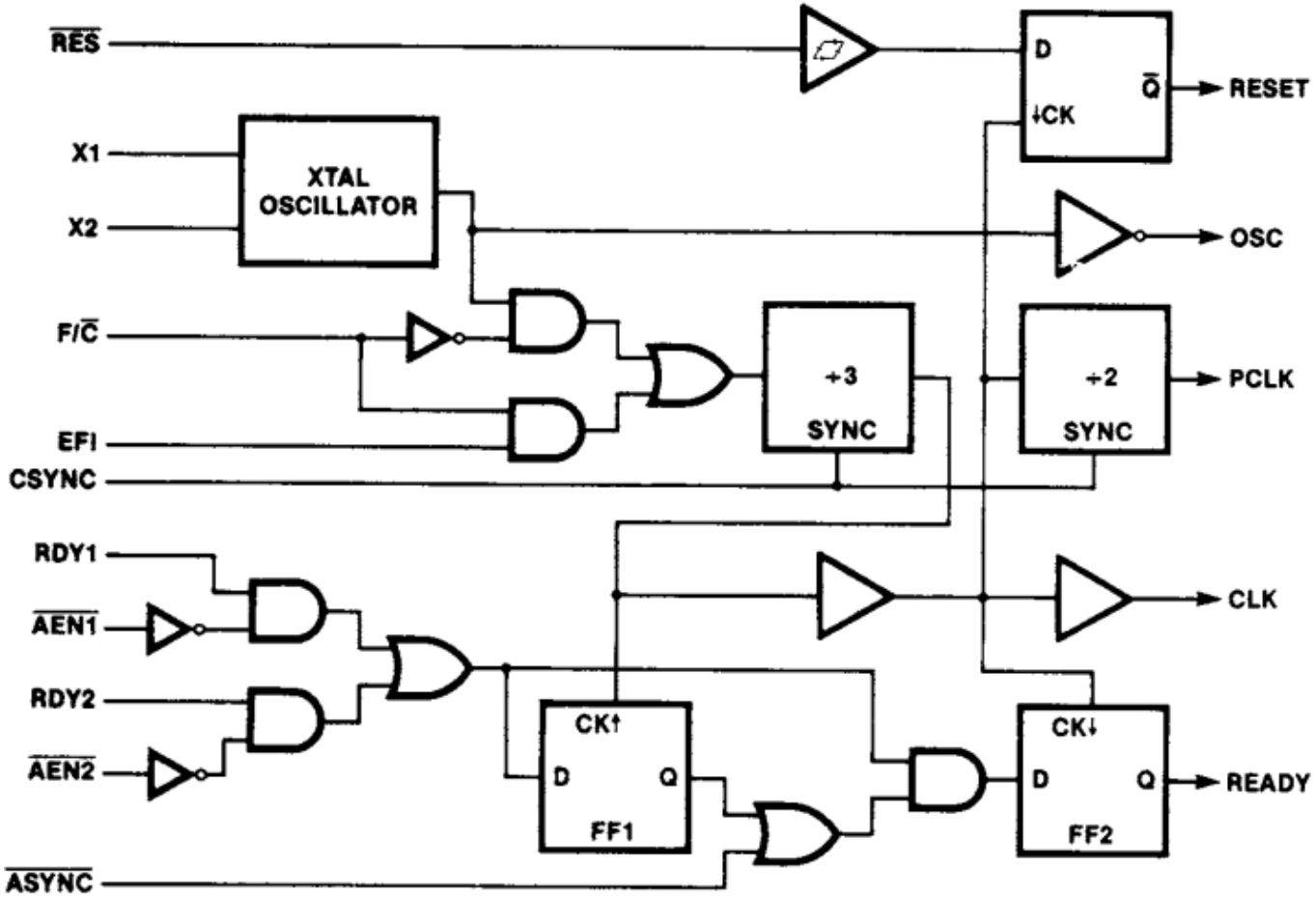
Clock



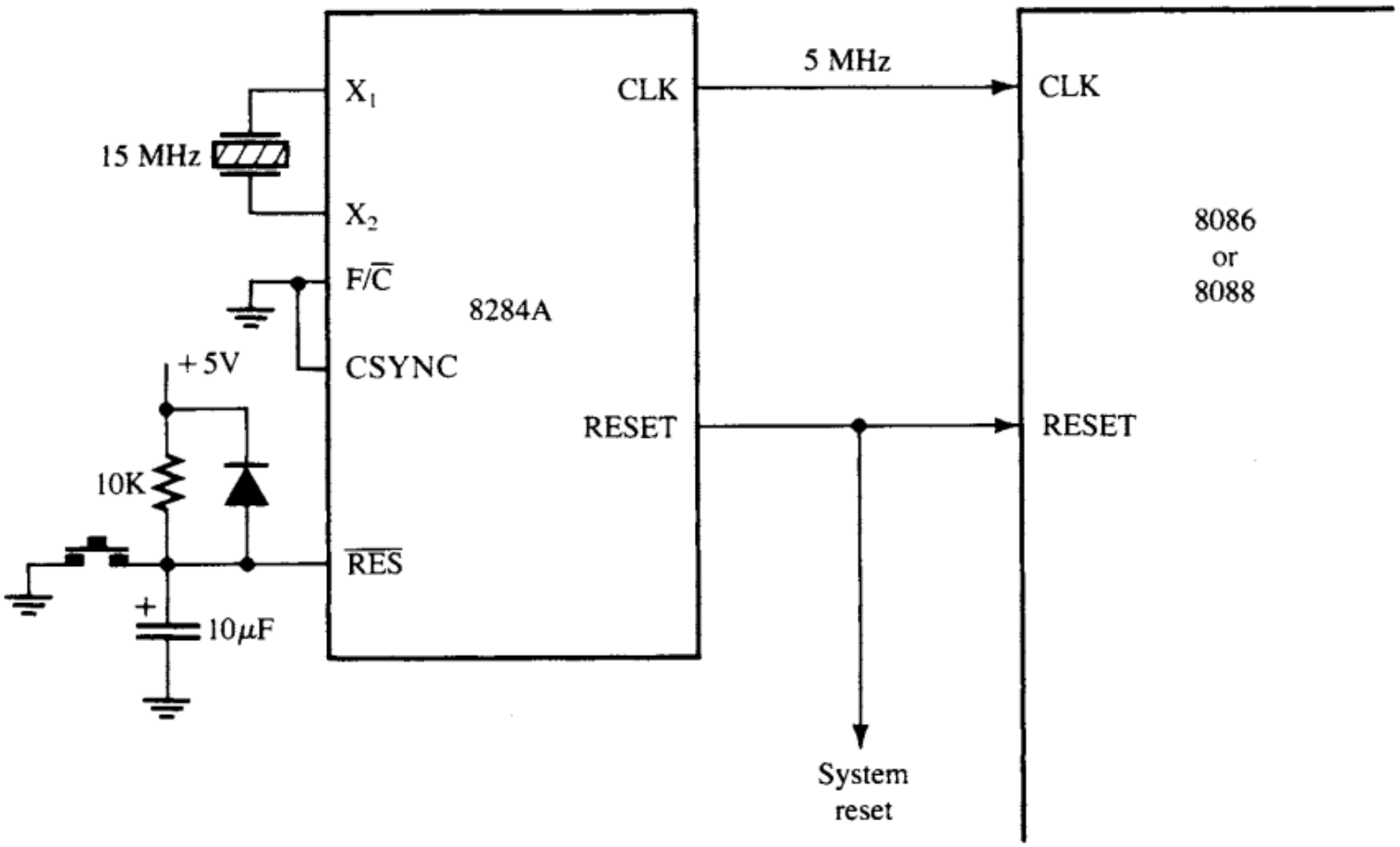
RESET

- This pin provides the reset signal to the processor and peripheral devices,
- it is an active-high pin.

Internal Diagram – 8284A



Clock


15 MHz
X1
X2
F/C
CSYNC
+5V
10K
RES
10μF
8284A
CLK
RESET
5 MHz
System
reset
CLK
RESET
8086
or
8088

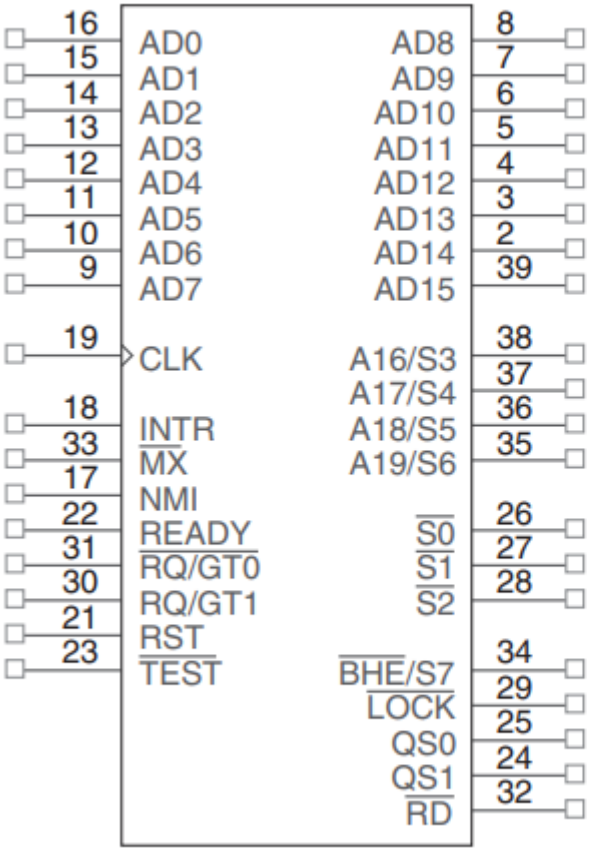
Minimum & Maximum Mode

innovate achieve lead

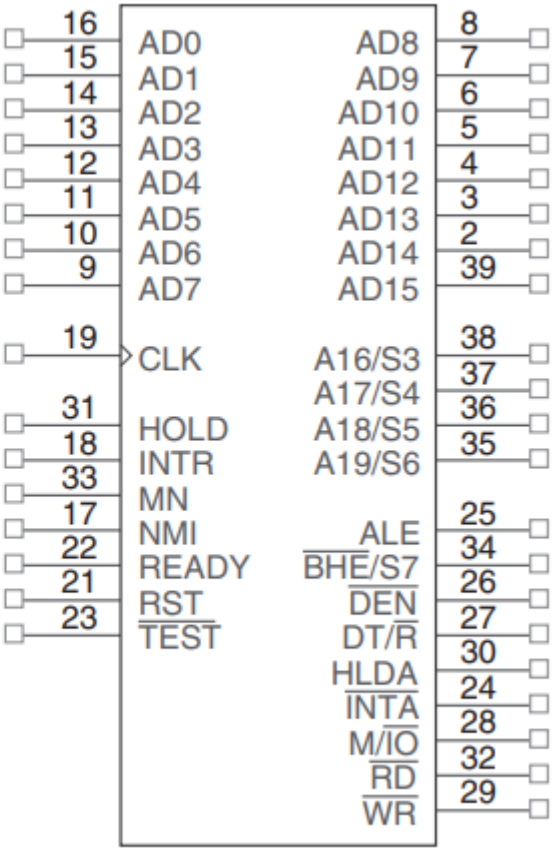
- 8088/8086 can be configured to work in any of the two modes
- Minimum Mode
  - MN/MX' –logic 1
  - Single processor in system
  - Smaller systems/ Cheaper

- Maximum Mode
  - MN/MX' – logic 0
  - Larger systems – more than one processor
  - e.g. – Numeric Data processor (8087) –co-processor

Pin Diagram

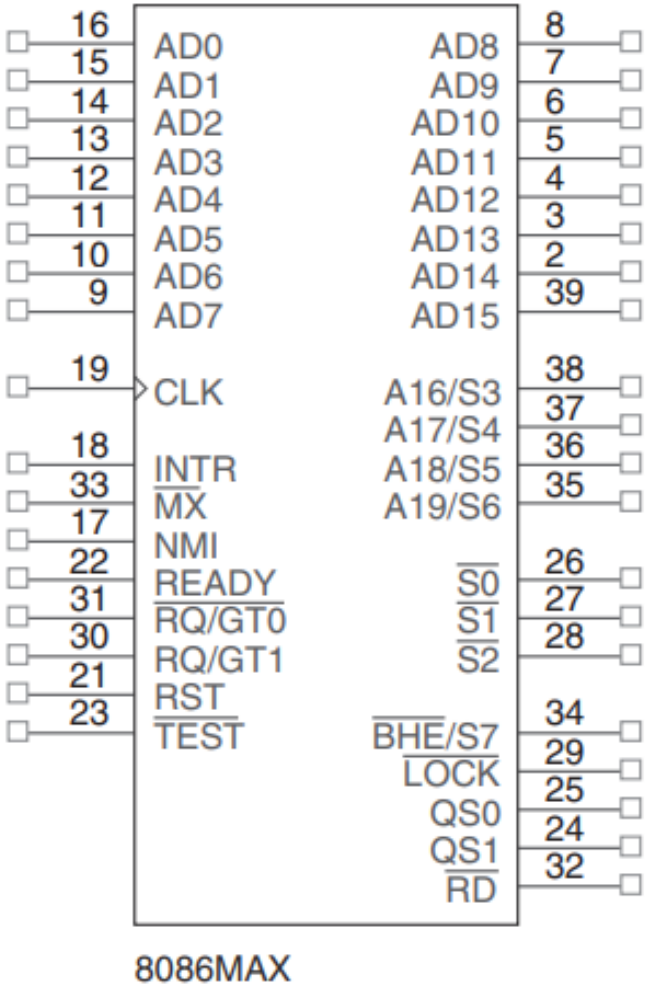


8086MAX



8086MIN

Input/output Characteristics



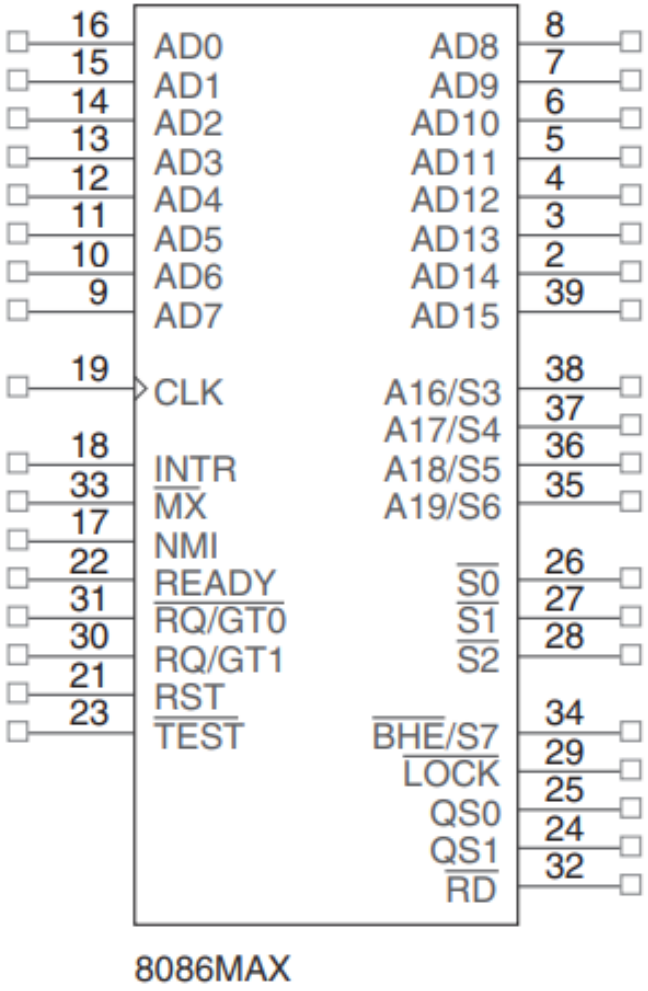
Input Characteristics

Logic Level	*Voltage*	*Current*
0	0.8 V maximum	±10 μA maximum
1	2.0 V minimum	±10 μA maximum

Output Characteristics

Logic Level	*Voltage*	*Current*
0	0.45V maximum	2.0 mA maximum
1	2.4 V minimum	–400 μA maximum

Pin Diagram



8086MAX

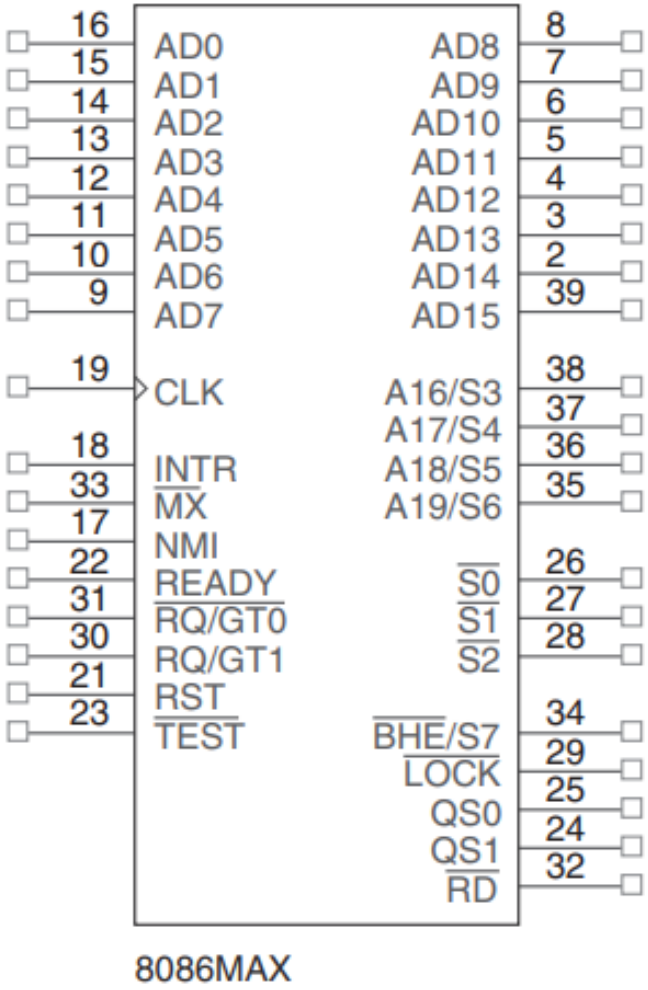
AD0-AD15: Address/Data bus.

- These are low order address bus.
- They are multiplexed with data.
- When AD lines are used to transmit memory address the symbol A is used instead of AD, for example A0-A15. When data are transmitted over AD lines the symbol D is used in place of AD, for example D0-D7, D8-D15 or D0-D15.

A16-A19: High order address bus.

- These are multiplexed with status signals.
- ALE=1 -> Address
- ALE=0 -> Data

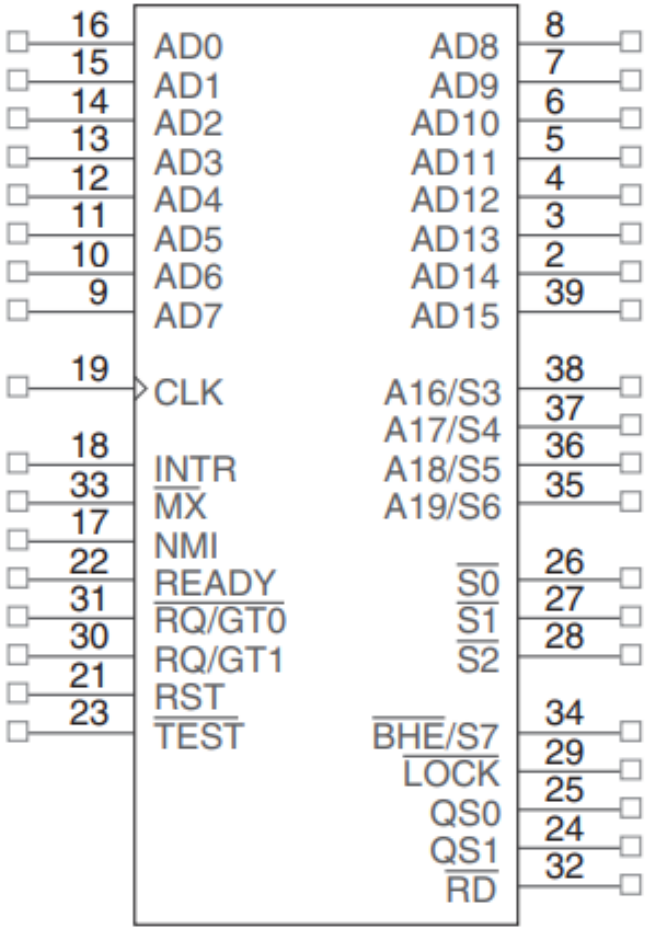
Pin Diagram



S2, S1, S0: Status pins.

- These pins are active during T4, T1 and T2 states and is returned to passive state (1,1,1 during T3 or Tw (when ready is inactive).
- These are used by the 8288 bus controller for generating all the memory and I/O operation) access control signals.
- Any change in S2, S1, S0 during T4 indicates the beginning of a bus cycle.

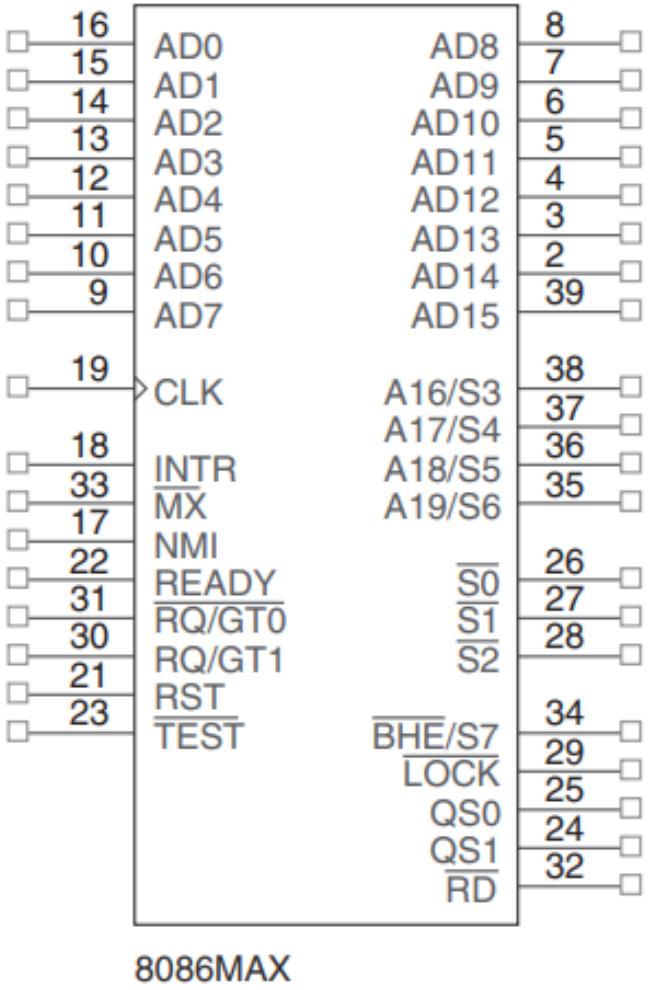
Pin Diagram



8086MAX

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	*Function*
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

Pin Diagram

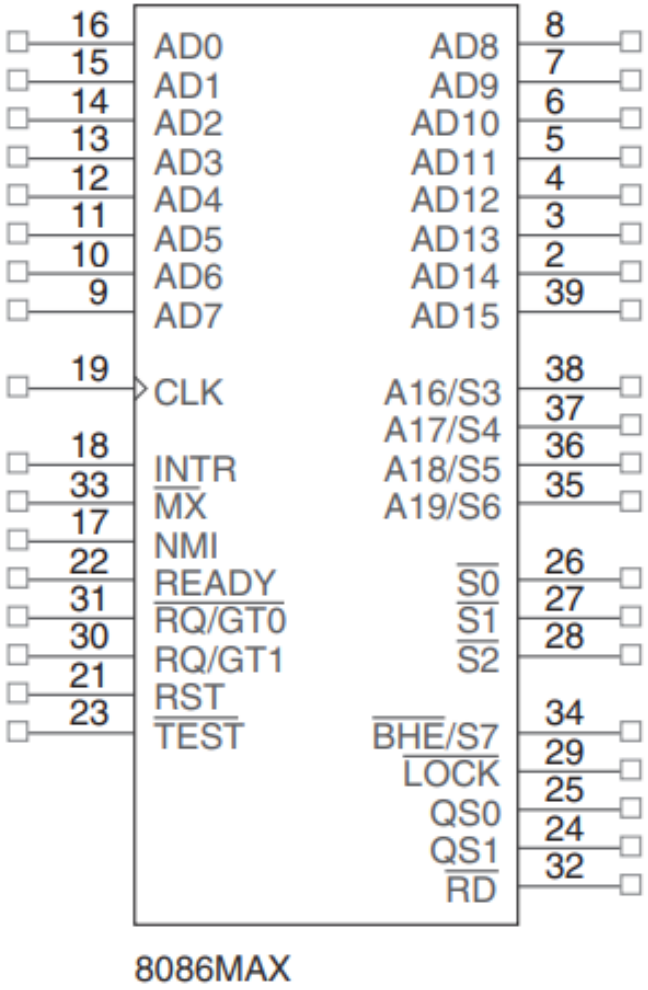


8086MAX

A16/S3, A17/S4, A18/S5, A19/S6 : The specified address lines are multiplexed with corresponding status signals.

S_4	S_3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment

Pin Diagram

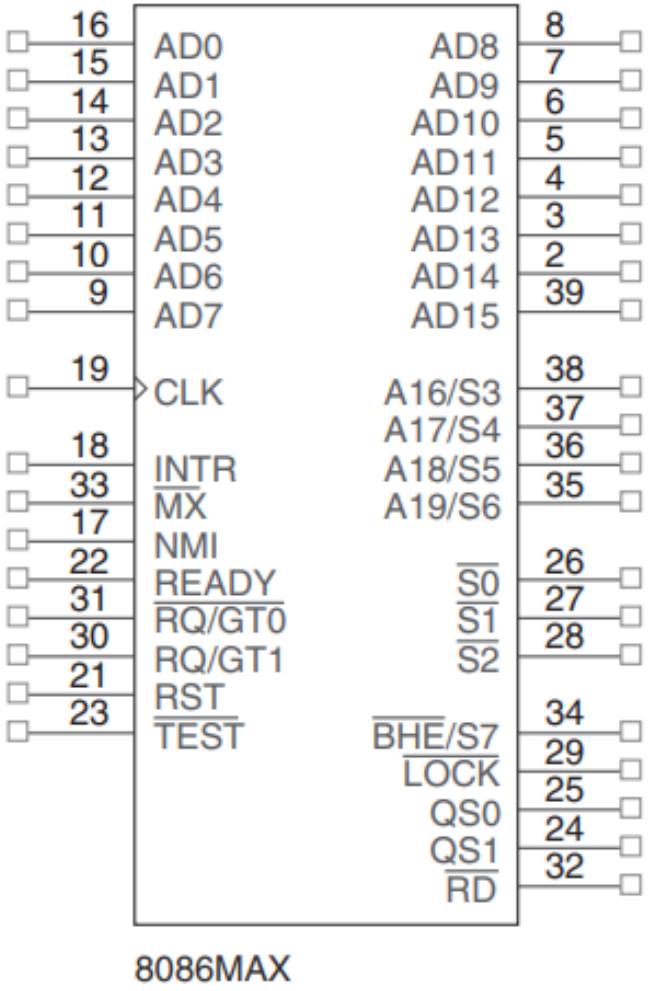


8086MAX

$\overline{RD}$

- Whenever the read signal is a logic 0, the data bus is receptive to data from the memory or I/O devices connected to the system.
- This pin floats to its high-impedance state during a hold acknowledge.

Pin Diagram

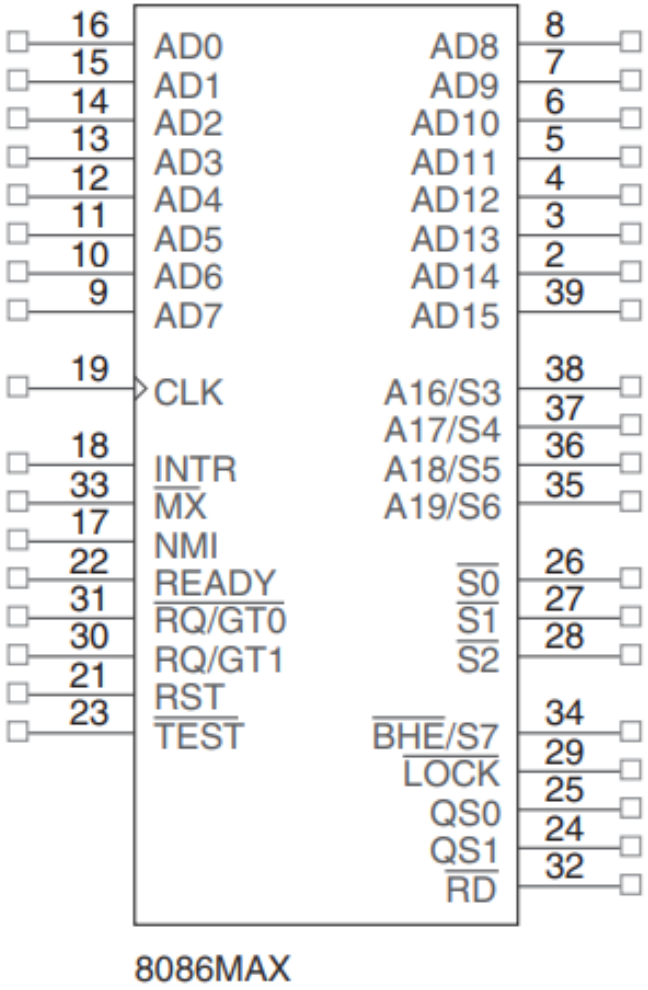


8086MAX

READY

- The READY input is controlled to insert wait states into the timing of the microprocessor.
- If the READY pin is placed at a logic 0 level, the microprocessor enters into wait states and remains idle.
- If the READY pin is placed at a logic 1 level, it has no effect on the operation of the microprocessor

Pin Diagram



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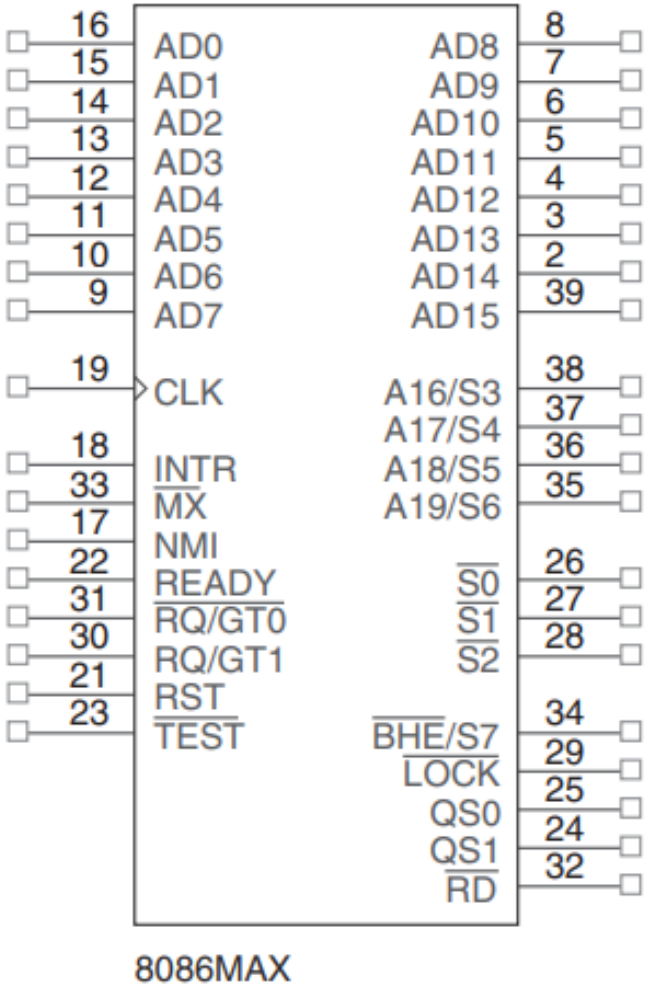
Pin Diagram

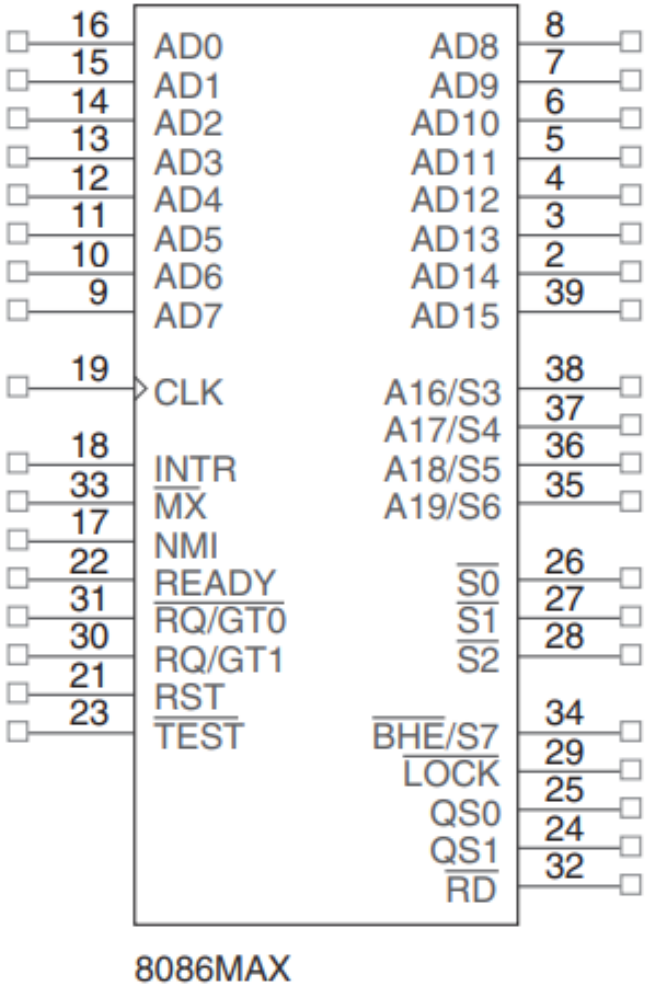


8086MAX

INTR

- Interrupt request is used to request a hardware interrupt.
- If INTR is held high when IF = 1, the 8086/8088 enters an interrupt acknowledge cycle (becomes active) after the current instruction has completed execution.

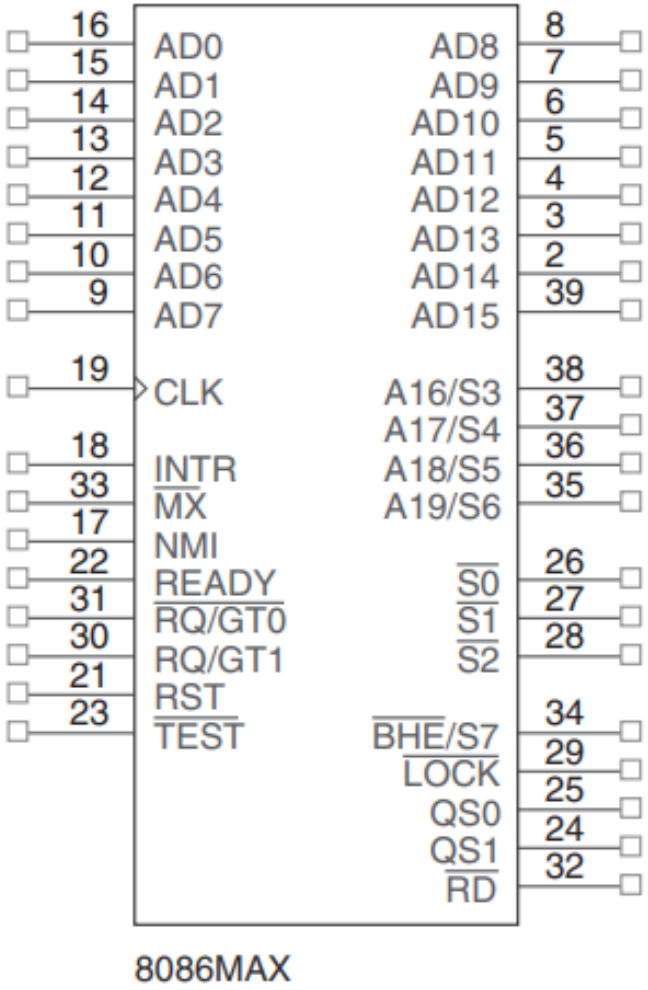
Pin Diagram



TEST

- The Test pin is an input that is tested by the WAIT instruction.
- If is a logic 0, the WAIT instruction functions as an NOP and if is a logic 1, the WAIT instruction waits for to become a logic 0.
- The pin is most often connected to the 8087 numeric coprocessor

Pin Diagram

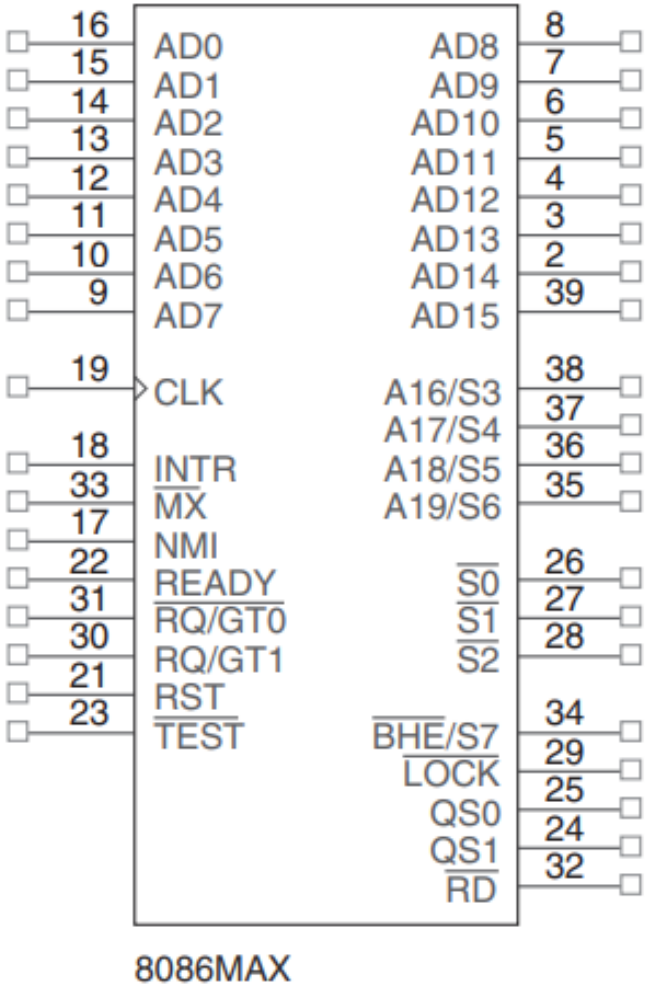


8086MAX

NMI

- The non-maskable interrupt input is similar to INTR except that the NMI interrupt does not check to see whether the IF flag bit is a logic 1.
- If NMI is activated, this interrupt input uses interrupt vector 2

Pin Diagram

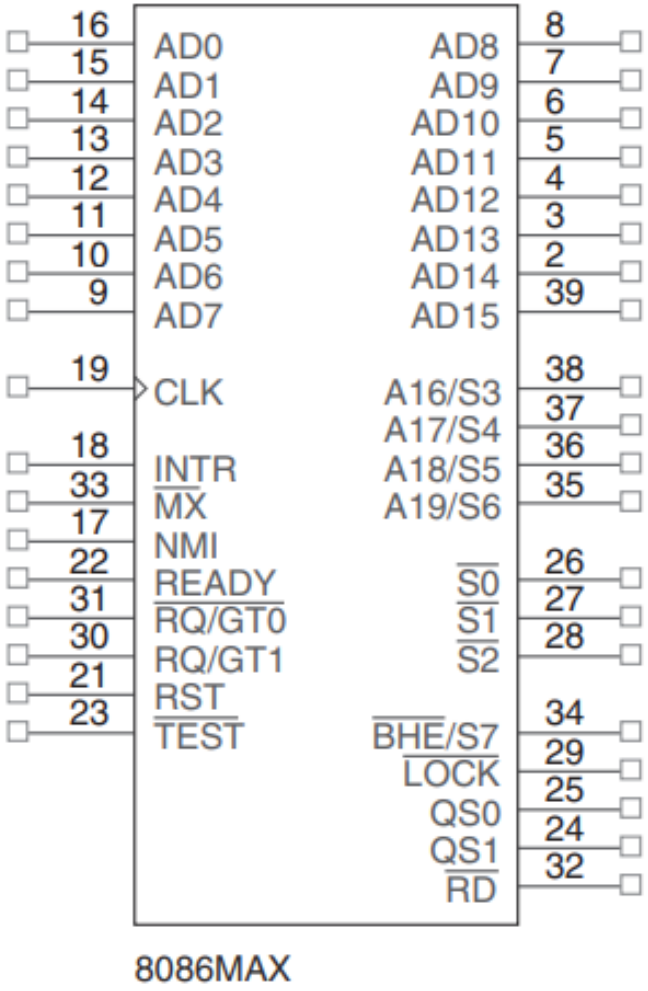


8086MAX

RESET

- The reset input causes the microprocessor to reset itself if this pin is held high for a minimum of four clocking periods.
- Whenever the 8086 or 8088 is reset, it begins executing instructions at memory location FFFFOH and disables future interrupts by clearing the IF flag bit.

Pin Diagram

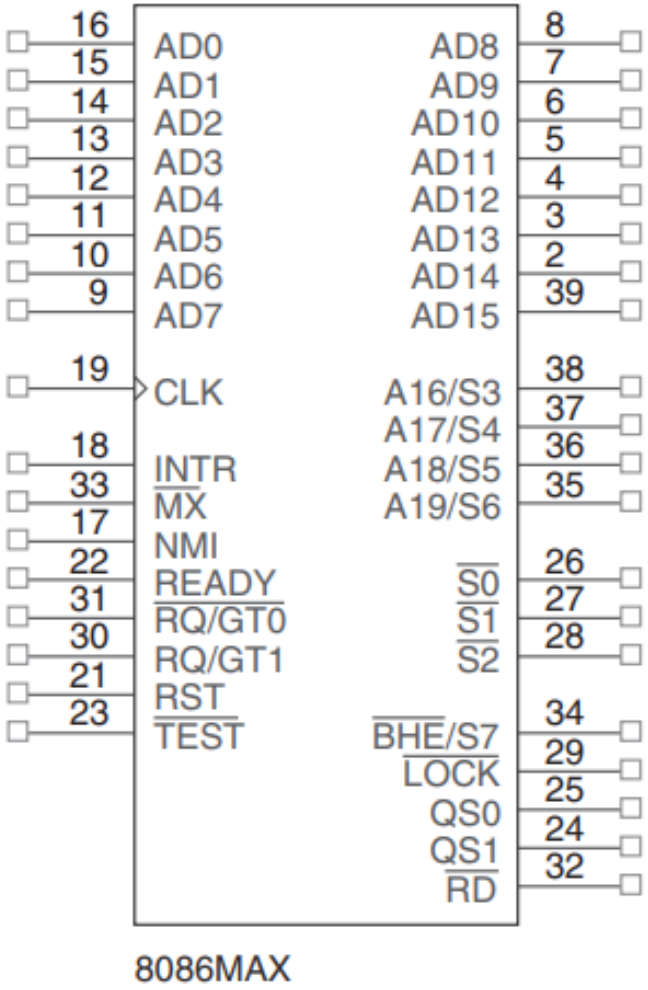


8086MAX

CLK

- The clock pin provides the basic timing signal to the microprocessor.
- The clock signal must have a duty cycle of 33 % (high for one third of the clocking period and low for two thirds) to provide proper internal timing for the 8086/8088.

Pin Diagram

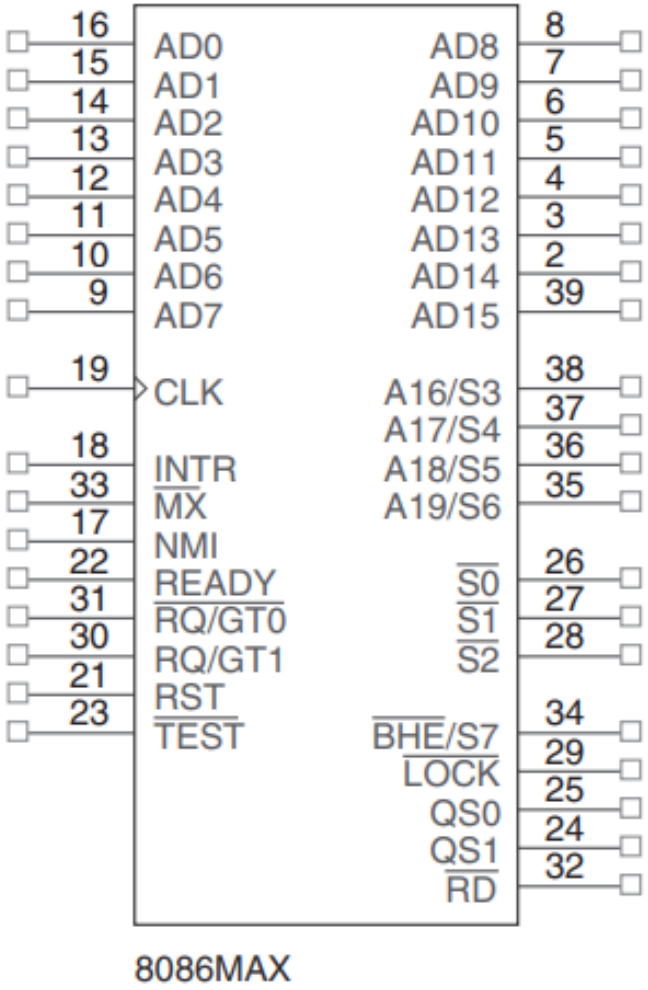


8086MAX

VCC

- This power supply input provides a +5.0 V, ±10 % signal to the microprocessor.

Pin Diagram

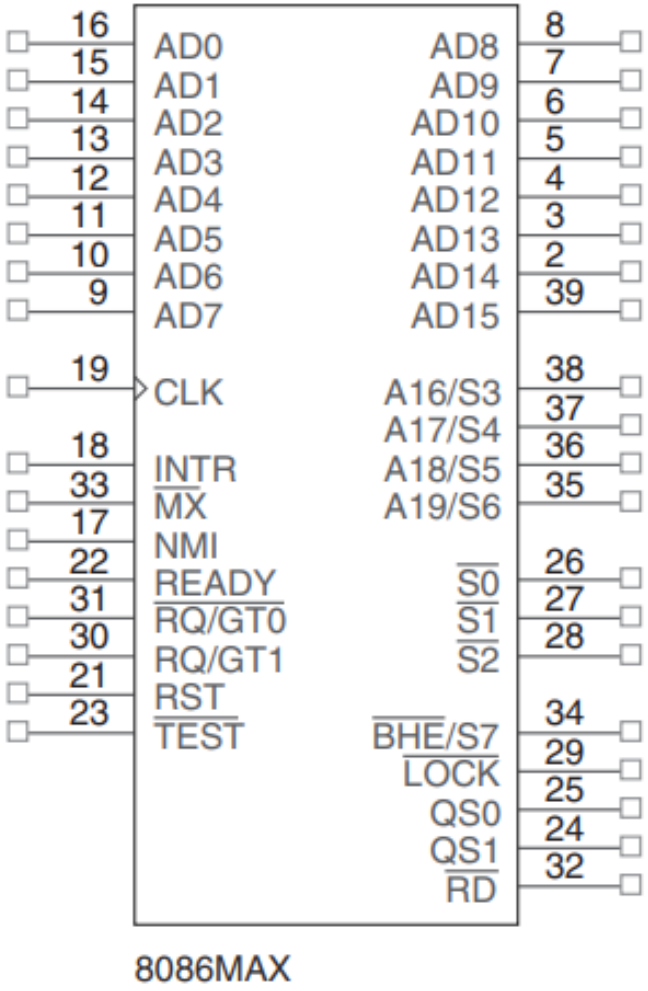


8086MAX

GND

- The ground connection is the return for the power supply.
- Note that the 8086/8088 microprocessors have two pins labeled GND—both must be connected to ground for proper operation

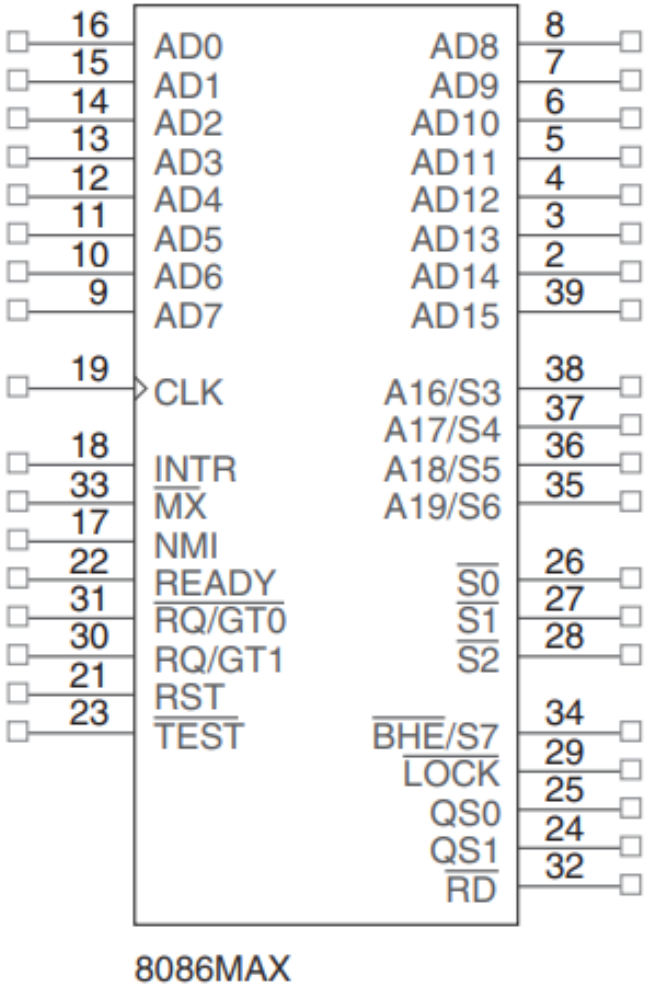
Pin Diagram



MN/$\overline{MX}$

- The minimum/maximum mode pin selects either minimum mode or maximum mode operation for the microprocessor.
- If minimum mode is selected, the MN/ pin must be connected directly to +5.0 V

Pin Diagram

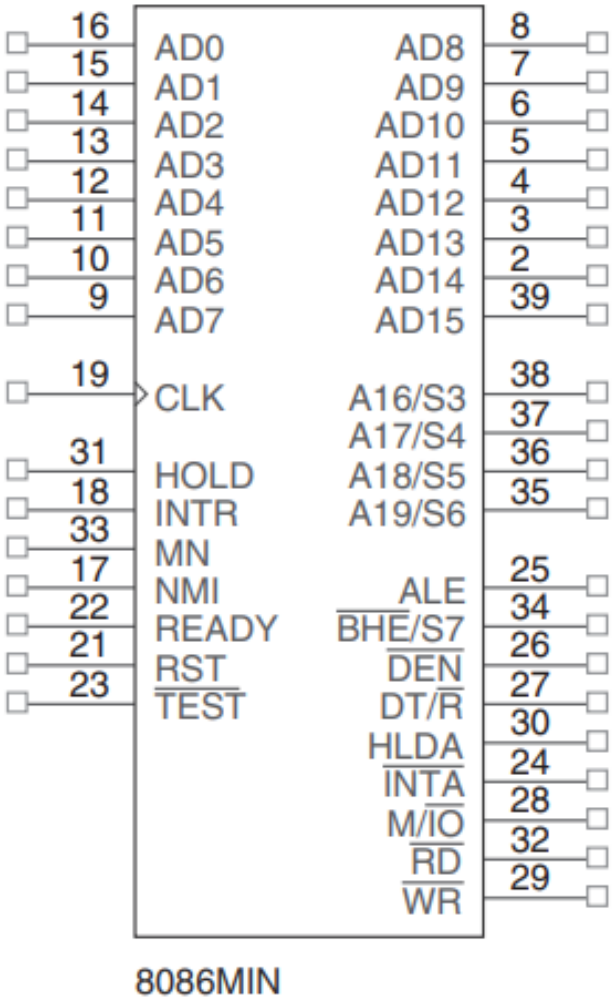


8086MAX

$\overline{\text{BHE}}$ S7

- The bus high enable pin is used in the 8086 to enable the most-significant data bus bits (D15–D8) during a read or a write operation.
- The state of S7 is always a logic 1.

Pin Diagram: Minimum Mode



- Minimum mode operation of the 8086/8088 is obtained by connecting the MN/ pin directly to +5.0 V.

M/IO

- M/IO pin selects memory or I/O.

- This pin indicates that the microprocessor address bus contains either a memory address or an I/O port address.

- This pin is at its high-impedance state during a hold acknowledge.

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Thank You