Microprocessors & Interfacing

8259A

BITS Pilani

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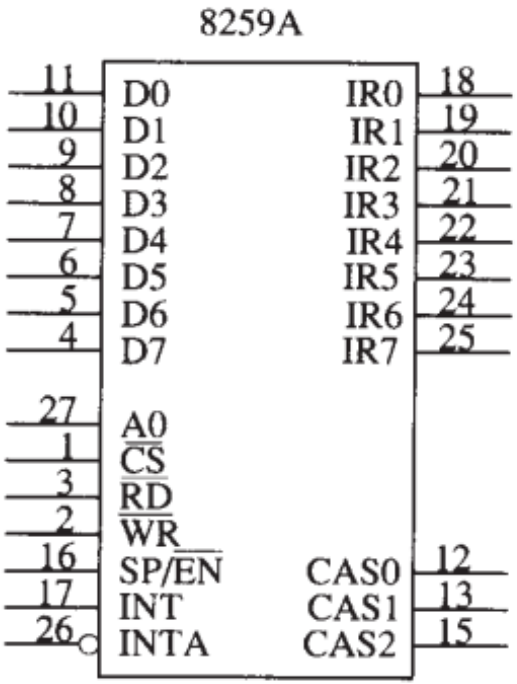
8259A

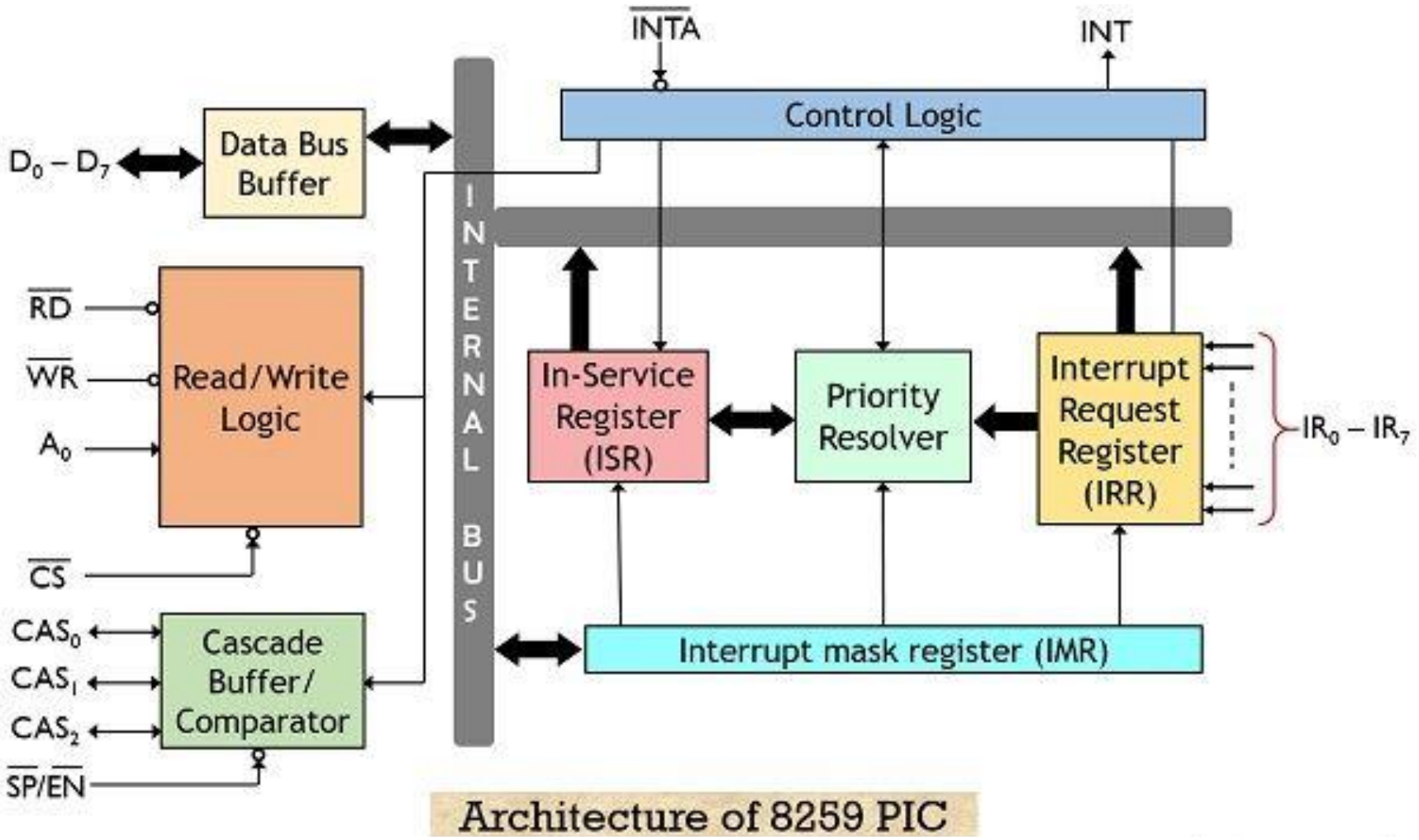
- The 8259A programmable interrupt controller (PIC) adds eight vectored priority encoded interrupts to the microprocessor.
- This controller can be expanded, without additional hardware, to accept up to 64 interrupt requests.
- This expansion requires a master 8259A and eight 8259A slaves.

8259A Chip



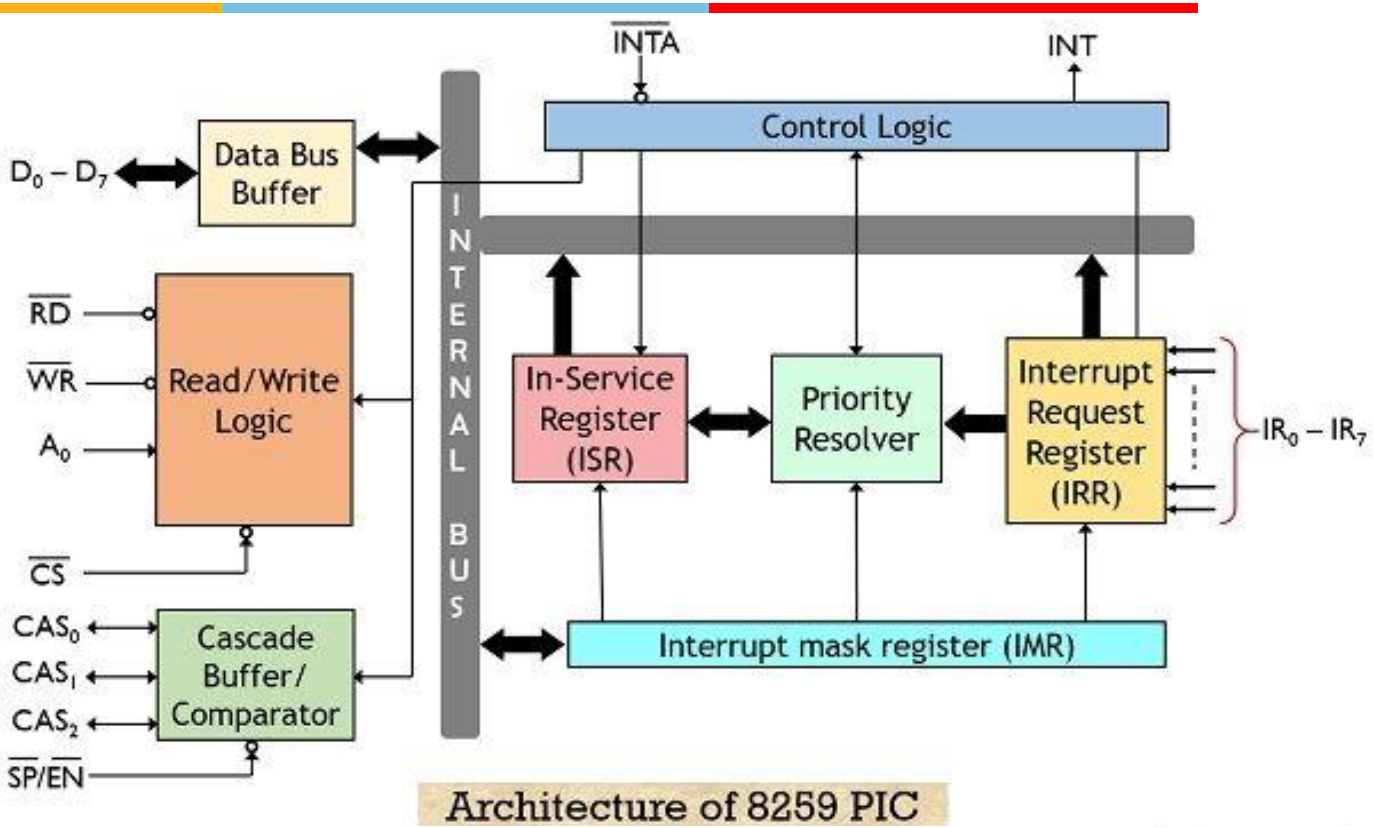
D_0–D_7	The bidirectional **data connections** are normally connected to the data bus on the microprocessor.
IR_0–IR_7	**Interrupt request inputs** are used to request an interrupt and to connect to a slave in a system with multiple 8259As.
$\overline{WR}$	The **write input** connects to write strobe signal ($\overline{IOWC}$) on the microprocessor.
$\overline{RD}$	The **read input** connects to the $\overline{IORC}$ signal.
INT	The **interrupt output** connects to the INTR pin on the microprocessor from the master and is connected to a master IR pin on a slave.
$\overline{INTA}$	**Interrupt acknowledge** is an input that connects to the $\overline{INTA}$ signal on the system. In a system with a master and slaves, only the master $\overline{INTA}$ signal is connected.
A_0	The A_0 **address input** selects different command words within the 8259A.
$\overline{CS}$	**Chip select** enables the 8259A for programming and control.
SP/$\overline{EN}$	**Slave program/enable buffer** is a dual-function pin. When the 8259A is in buffered mode, this is an output that controls the data bus transceivers in a large microprocessor-based system. When the 8259A is not in the buffered mode, this pin programs the device as a master (1) or a slave (0).
CAS_0–C	The **cascade lines** are used as outputs from the master to the slaves for cascading multiple 8259As in a system.

Block Diagram



Architecture of 8259 PIC

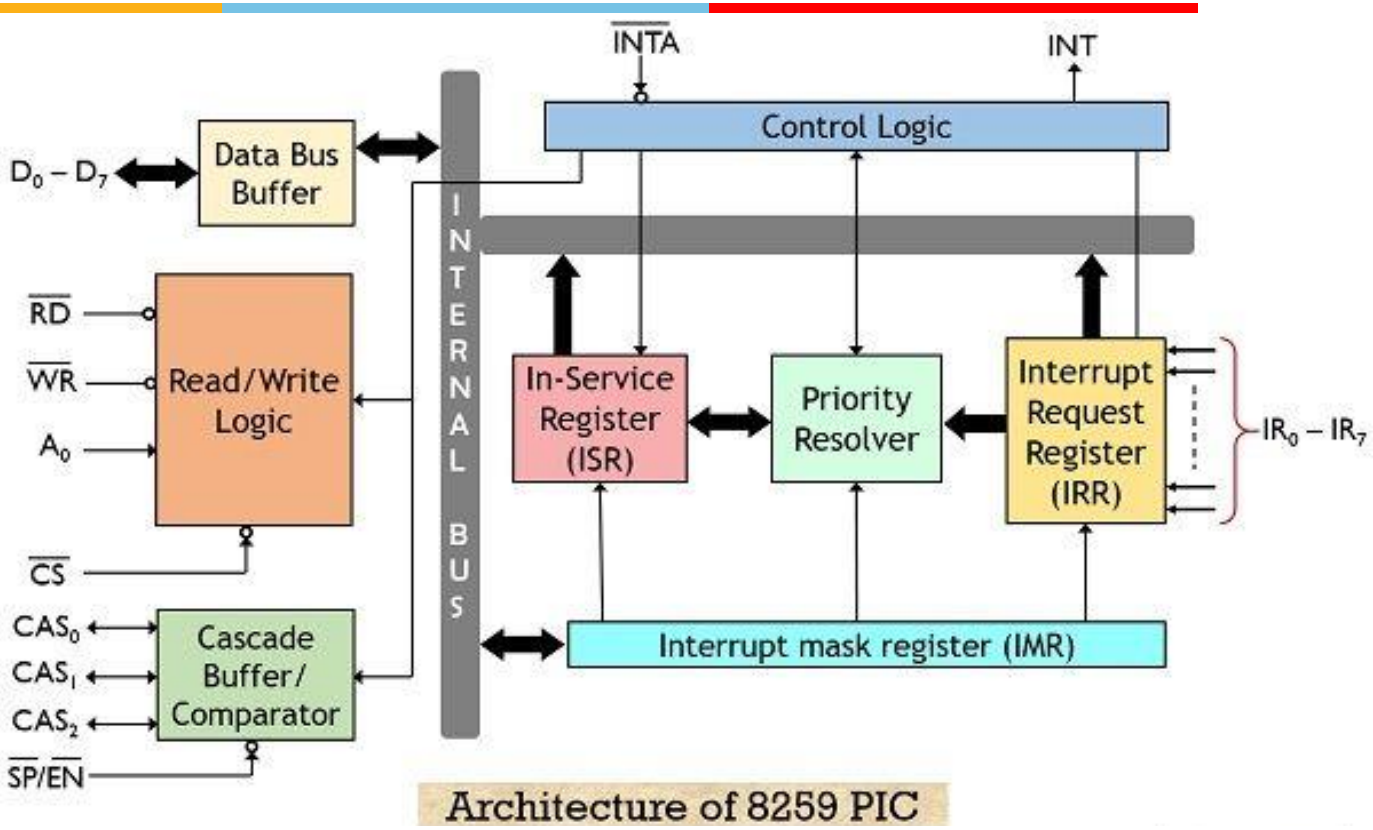
Block Diagram



Architecture of 8259 PIC

Data Bus Buffer: 8259 has tri-stated bidirectional 8-bit data bus buffer (i.e., D_0 to D_7) that interfaces with the internal bus of the processor. The 8085 microprocessor sends/ receives, control or status words to/ from the 8259 using data bus buffer.

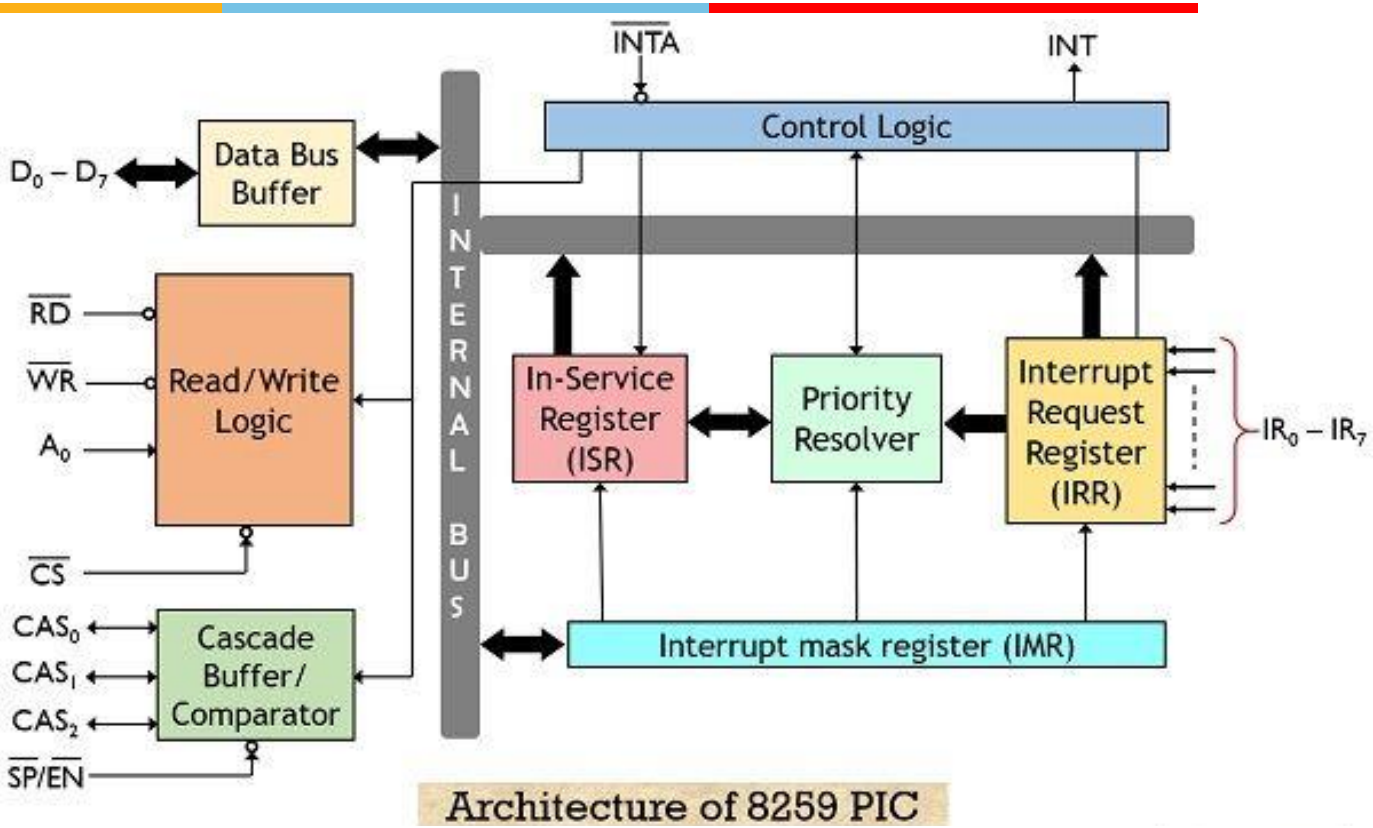
Block Diagram



Architecture of 8259 PIC

Read/ Write Logic: This unit is responsible for controlling the internal read-write operations of the system. It holds initialization command word register and operation command word register inside which various control formats exist that are needed for the device operation.

Block Diagram



Architecture of 8259 PIC

Control Logic: This unit is the heart of the architecture of 8259. It controls the overall operation of the system by sending the INTR signal to the processor whenever an interrupt request is generated.

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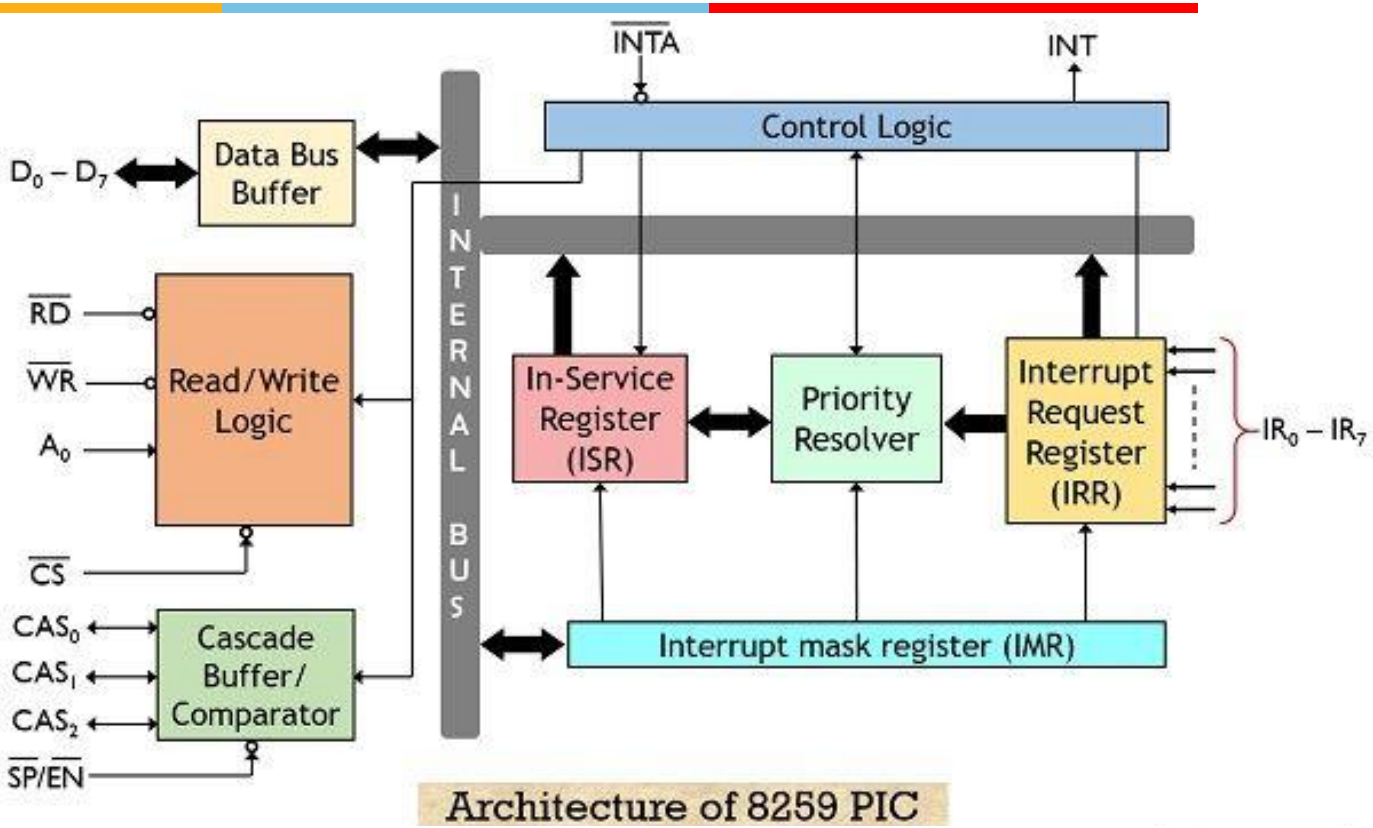

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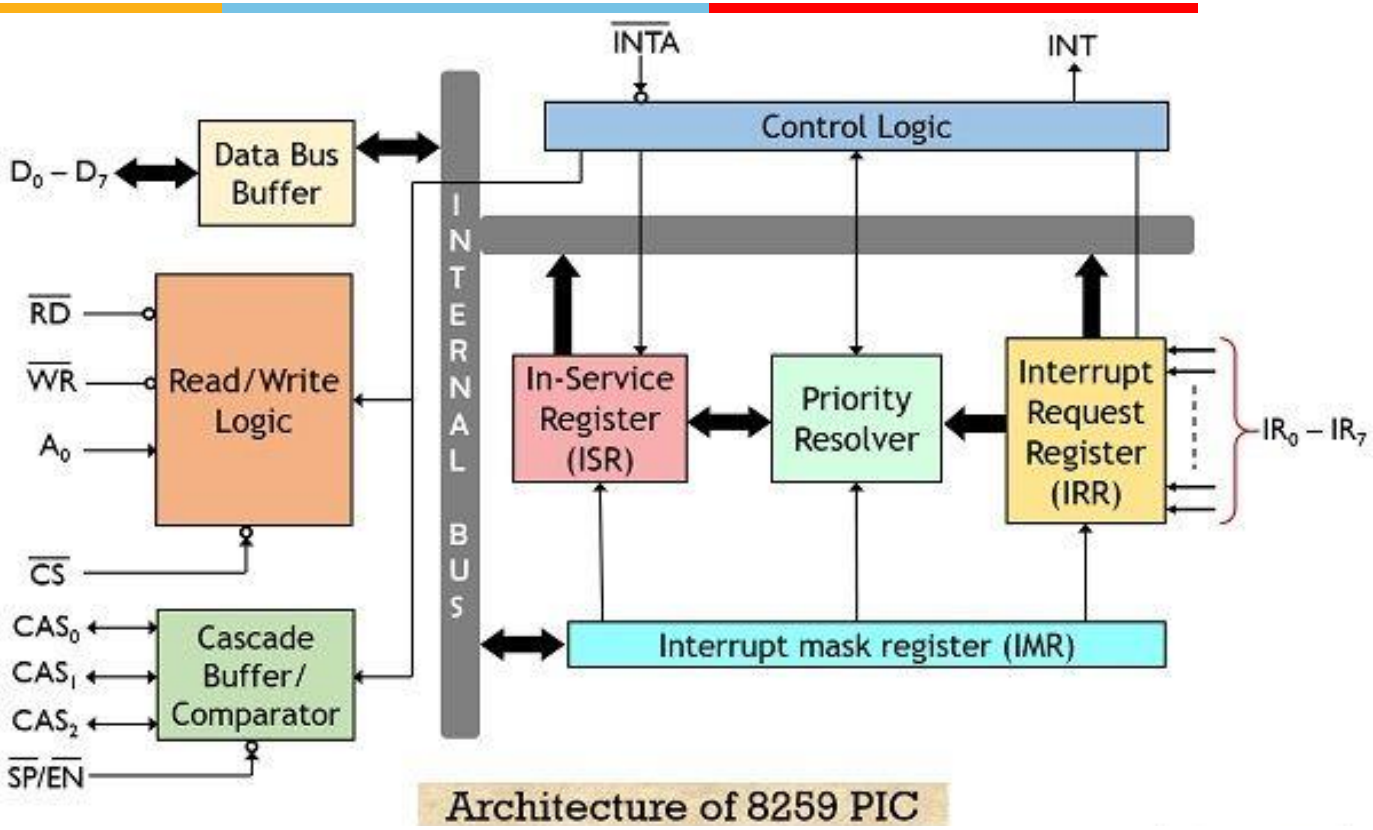

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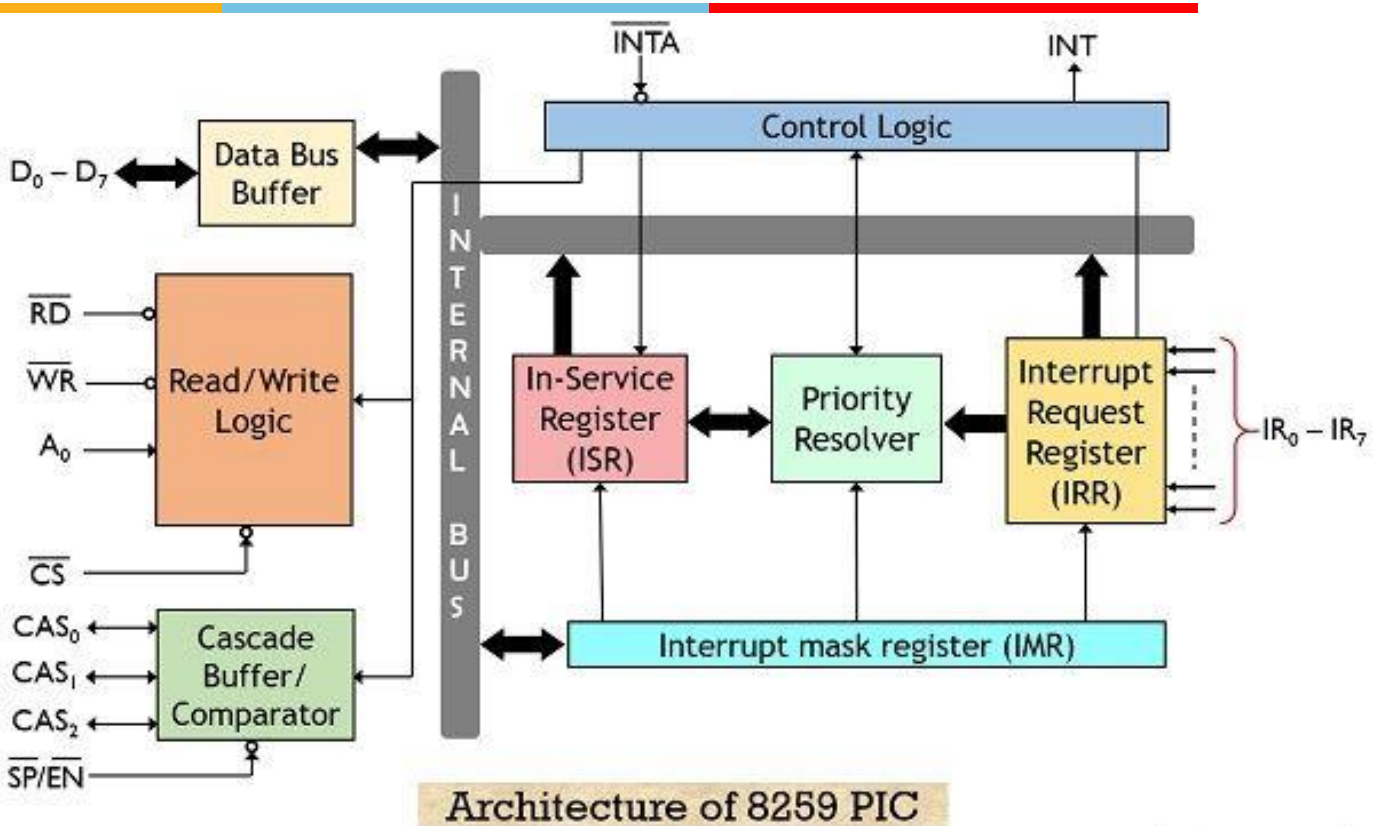
Interrupt request register (IRR): This unit stores the interrupt requests generated by the peripheral devices. We know that 8259 has 8 interrupt request pins (i.e., IR_0 to IR_7). So, the unit can store 8 interrupt requests that are requesting the service from the processor.

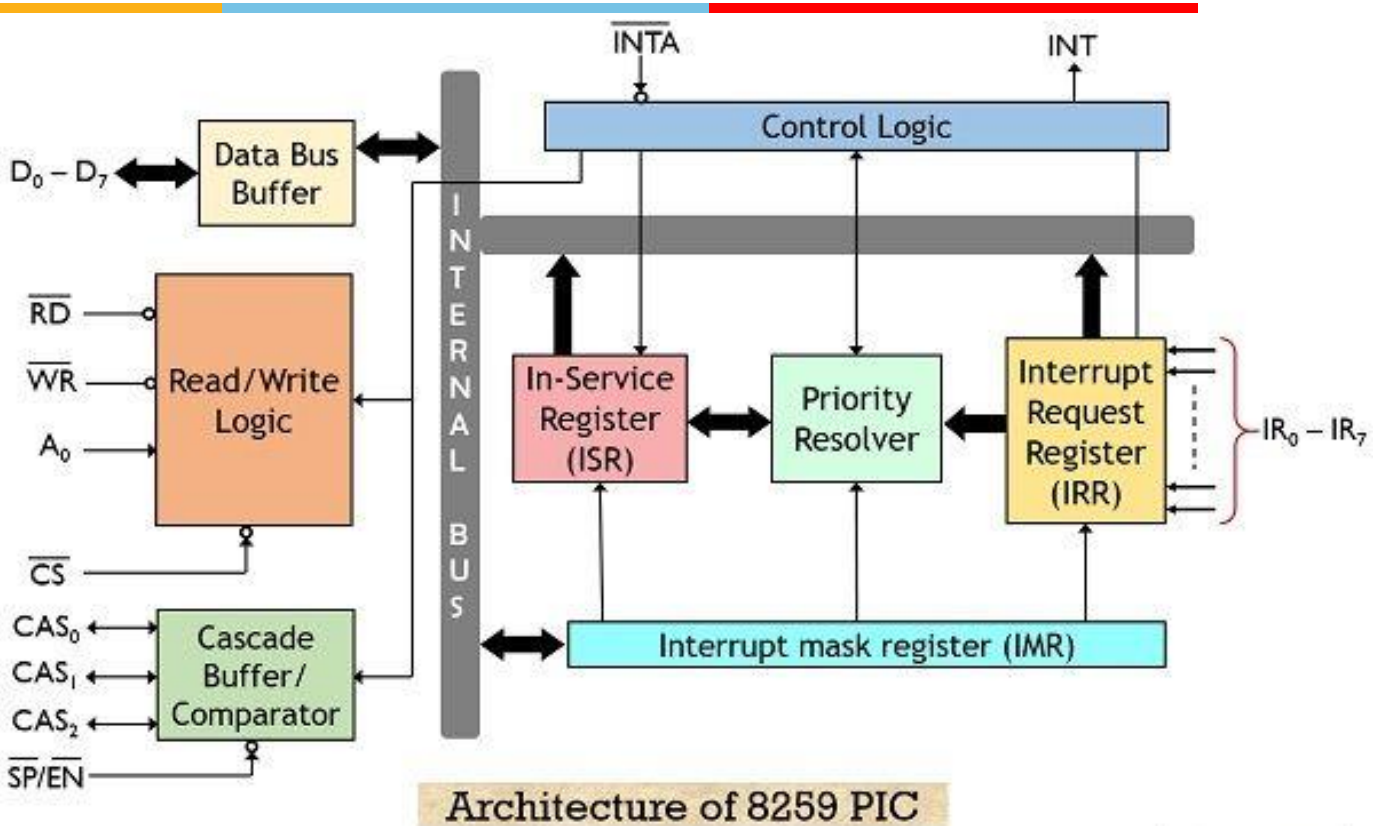
Block Diagram



Architecture of 8259 PIC

Priority Resolver: This logic unit decides that among all the interrupt request present in the IRR which holds the highest priority and needs to be executed first.

Block Diagram



Architecture of 8259 PIC

In-service register: Here the name of the unit is itself indicating the operation performed by it. This register unit stores the interrupts which are currently being executed by the processor.

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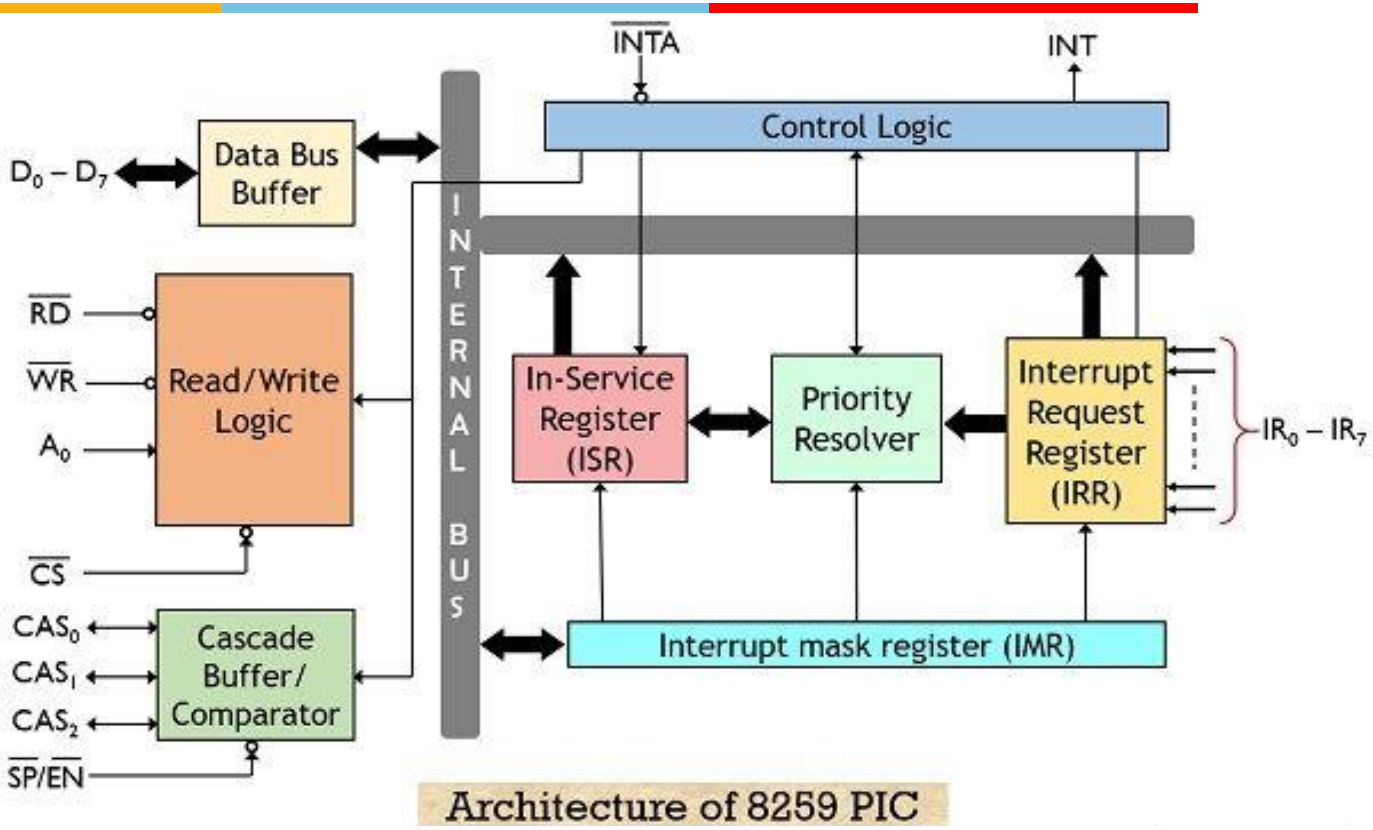

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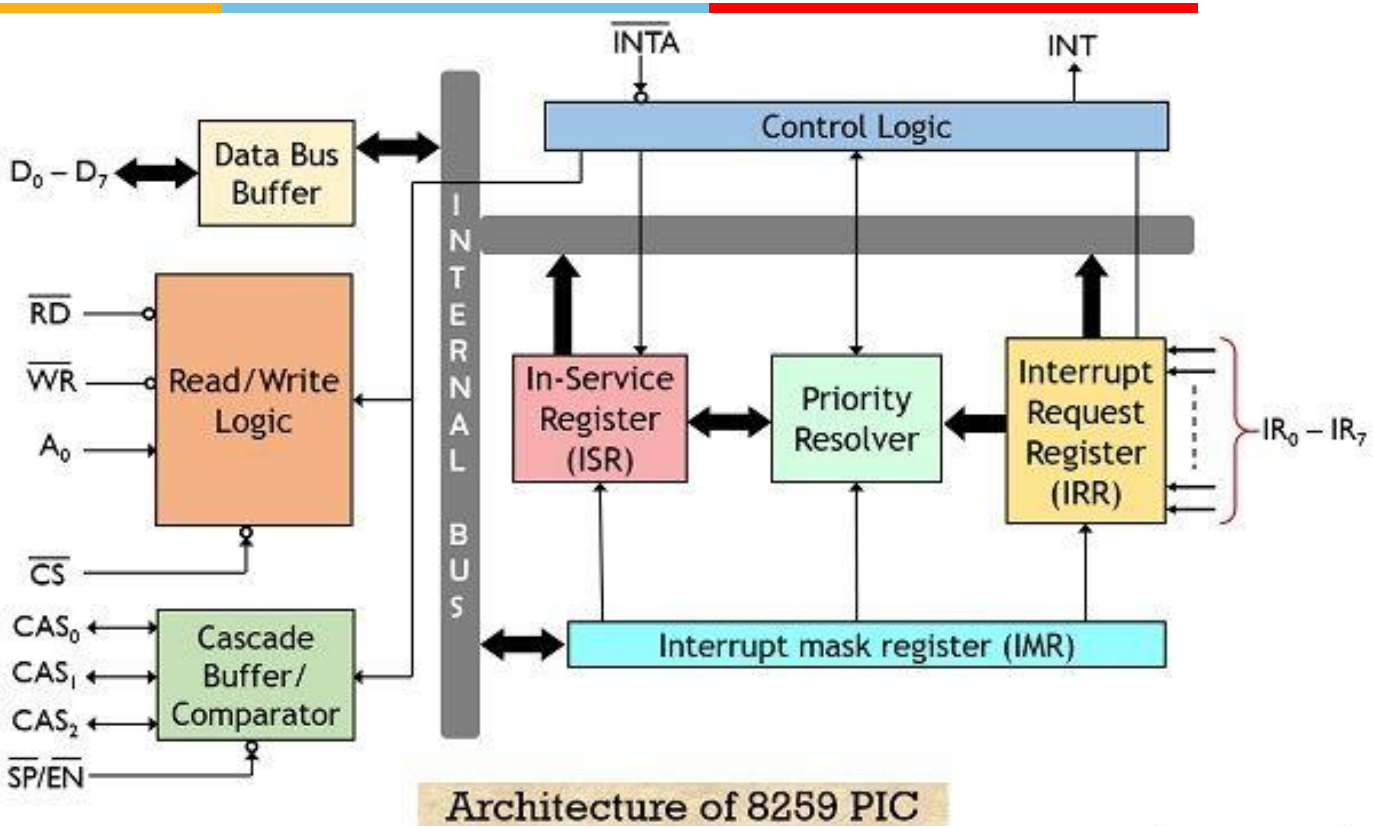
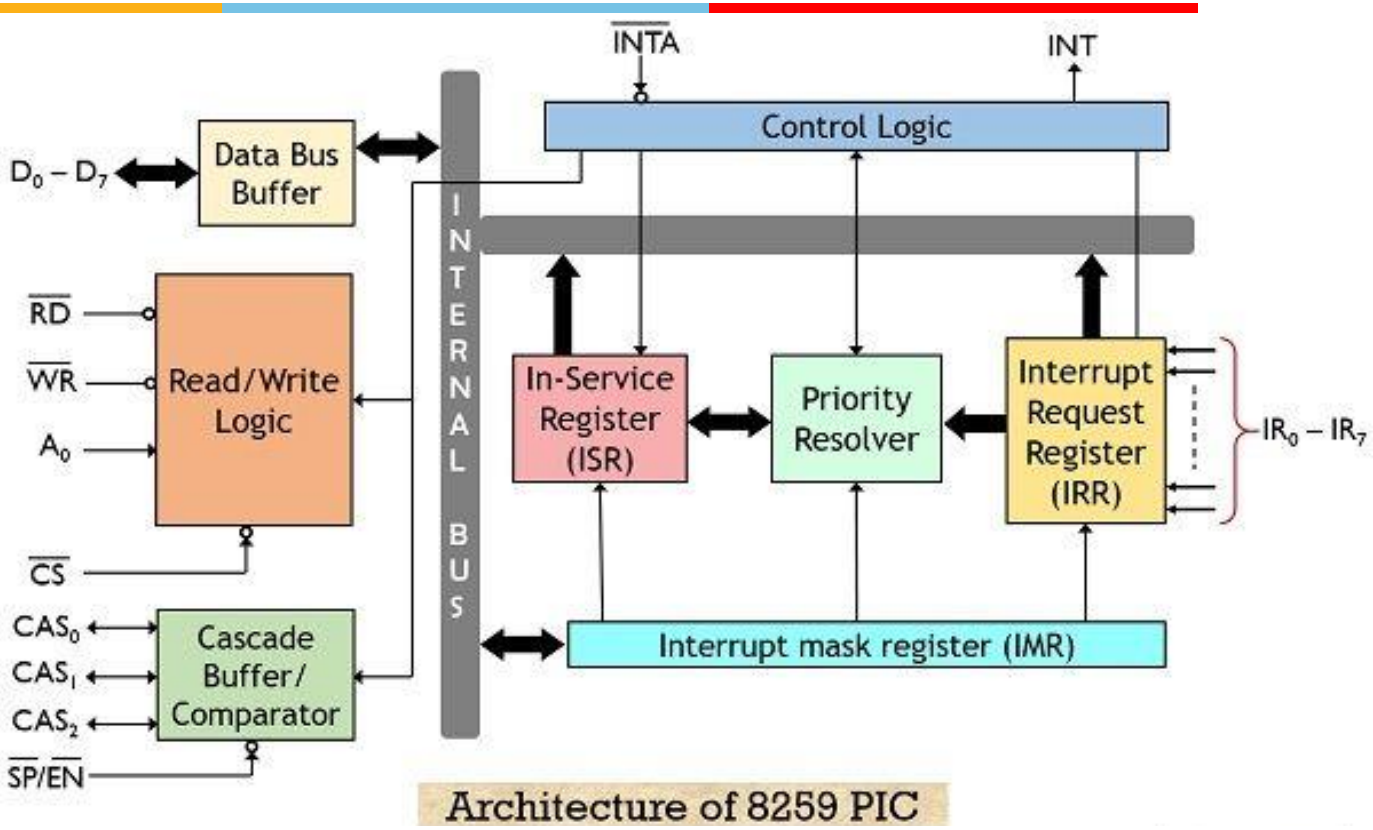


Architecture of 8259 PIC

Interrupt mask register: This register unit holds the masking bit of those interrupts which are to be masked. Through operation command word (OCW) the processor sends the required information and programs the interrupt mask register.

Block Diagram



Architecture of 8259 PIC

Cascade buffer/comparator: As we have already discussed that by cascading multiple 8259, the number of interrupts handled by 8259 can be expanded up to 64. The unit allows the comparison of IDs of different 8259s cascaded together..

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Thank You