Microprocessors & Interfacing

Hardware Design

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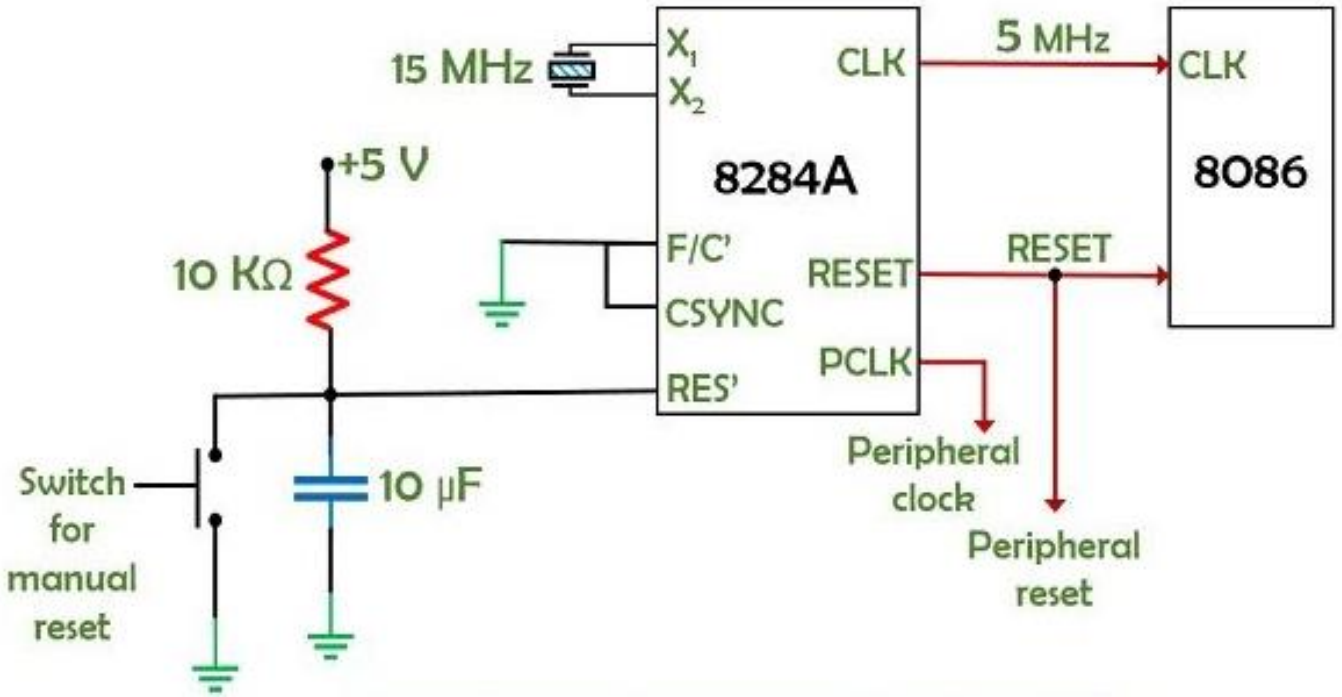
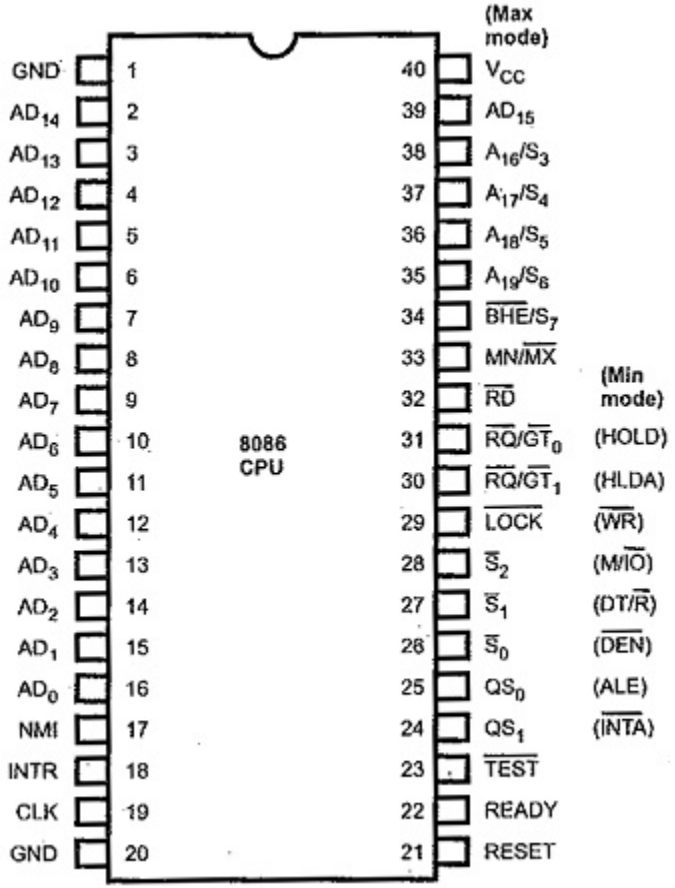
Interfacing 8284 with 8086



Min Max Mode


(Max mode)
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
8086 CPU
40 VCC
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE/S7
33 MN/MX
32 RD
31 RQ/GT0 (HOLD)
30 RQ/GT1 (HLDA)
29 LOCK (WR)
28 S2 (M/IO)
27 S1 (DT/R)
26 S0 (DEN)
25 QS0 (ALE)
24 QS1 (INTA)
23 TEST
22 READY
21 RESET
(Min mode)

Difference between Minimum & Maximum Mode

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Minimum mode	Maximum mode
There can be only one processor.	There can be multiple processors.
Performance is slower.	Performance is faster.
The circuit is simple.	The circuit is complex.
Multiprocessing cannot be performed.	Multiprocessing can be performed.
MN/MX is 1 to indicate the minimum mode.	MN/MX is 0 to indicate the maximum mode
The 8086 generates INTA for interrupt acknowledgment.	The 8288 Bus Controller generates the interrupt acknowledgment signal (INTA).
The 8086 itself provides an ALE for the latch.	Because there are several processors, the 8288 bus controller provides ALE for the latch.
The system is more affordable.	The system costs more money.
It is used for small systems.	It is used for large systems.
The multiprocessor setup is not supported.	The multiprocessor configuration is accepted.

Demultiplexing the Buses

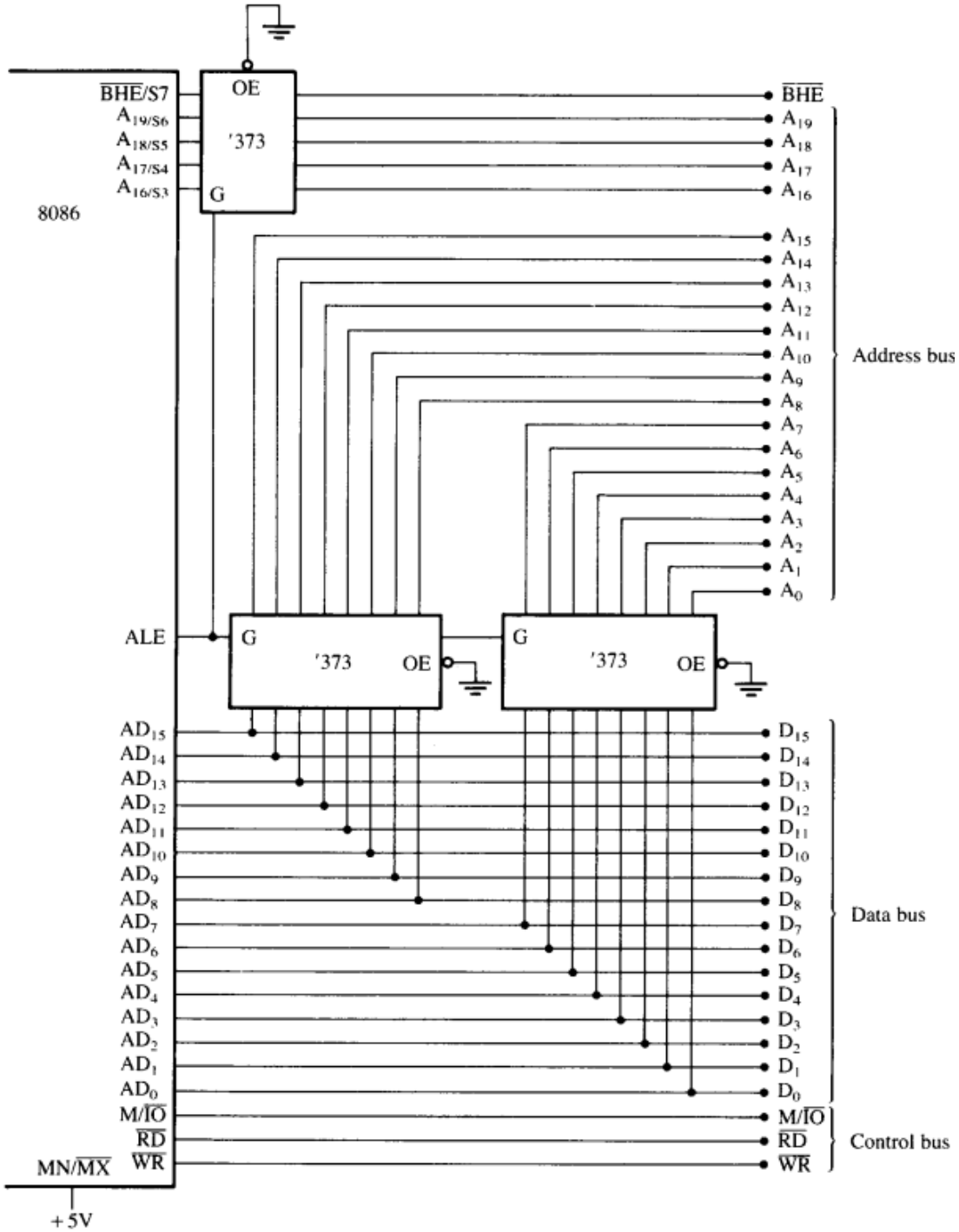
All computer systems have three buses:

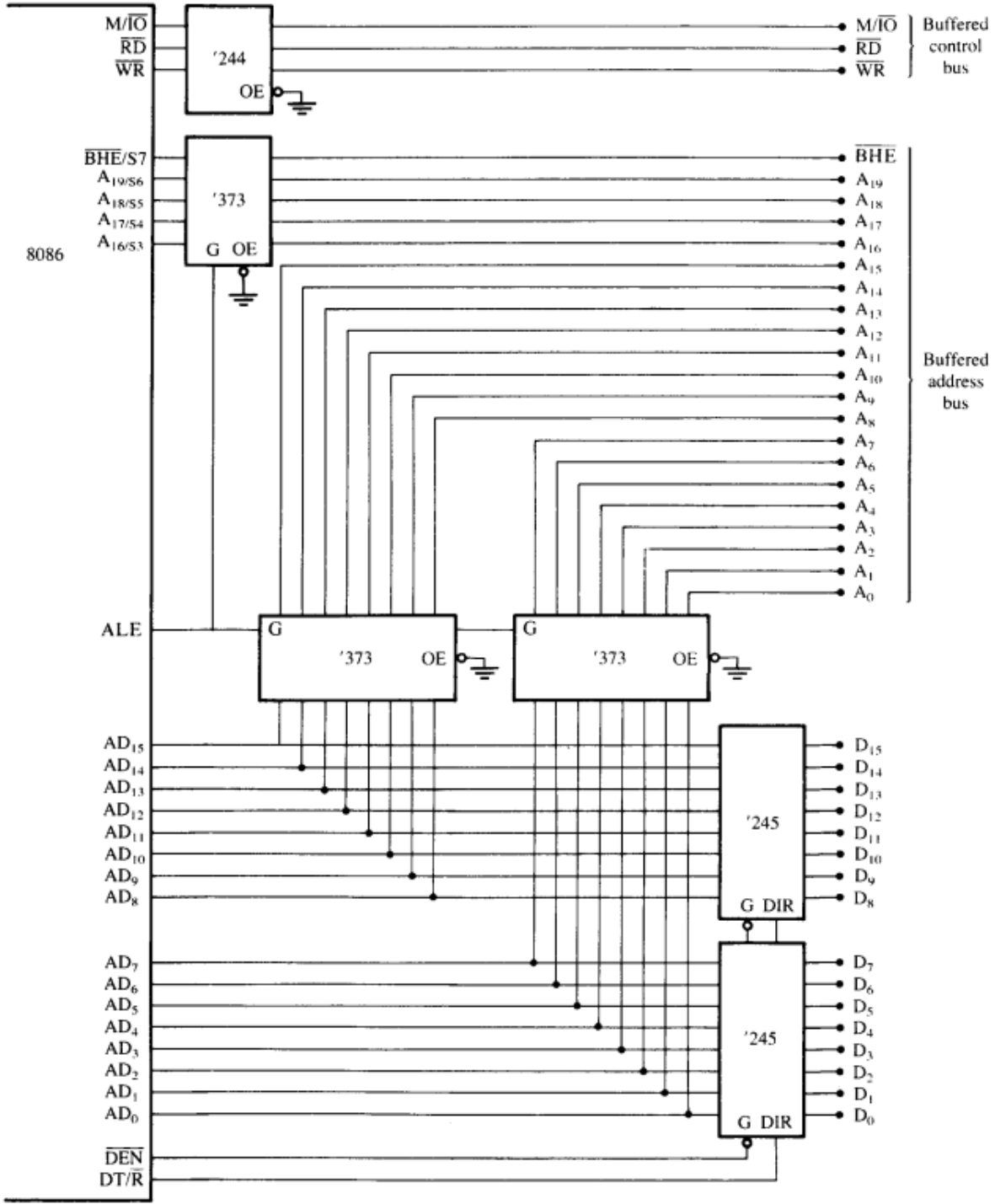
(1) an address bus that provides the memory and I/O with the memory address or the I/O port number

(2) a data bus that transfers data between the micro processor and the memory and I/O in the system

(3) a control bus that provides control signals to the memory and I/O.

- Two 74LS373 or 74LS573 transparent latches are used to demultiplex the address/data lunes


8086
BHE/S7
A19/S6
A18/S5
A17/S4
A16/S3
OE
'373
G
BHE
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
Address bus
ALE
G
'373
OE
G
'373
OE
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
Data bus
M/IO
RD
WR
M/IO
RD
WR
Control bus
MN/MX
+5V


8086
M/IO
RD
WR
'244
OE
M/IO
RD
WR
Buffered control bus
BHE/S7
A19/S6
A18/S5
A17/S4
A16/S3
'373
G OE
BHE
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
Buffered address bus
ALE
G
'373
OE
G
'373
OE
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
'245
G DIR
D15
D14
D13
D12
D11
D10
D9
D8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
'245
G DIR
D7
D6
D5
D4
D3
D2
D1
D0
DEN
DT/R

Bus Timing

- The 8086/8088 microprocessors use the memory and I/O in periods called bus cycles.
- Each bus cycle equals four system-clocking periods (T states)
- If the clock is operated at 5 MHz , one 8086 bus cycle is complete in ……ns
- This means that the microprocessor reads or writes data between itself and memory or I/O at a maximum rate of…… million times a second.

Generation of control signal

M/IO’	RD’	WR’	Bus cycle
1	0	1	MEMR’
1	1	0	MEMW’
0	0	1	IOR’
0	1	0	IOW’

Bus Timing

During T1

- The address of the memory or I/O location is sent out via the address bus and the address/data bus connections.
- Control signals are also sent out

During T2,

- The 8086/8088 microprocessors issue the RD' or WR' signal, DEN' , and in the case of a write, the data to be written appear on the data bus.
- The DEN' signal turns on the data bus buffers, if they are present in the system, so the memory or I/O can receive data to be written, or so the microprocessor can accept the data read from the memory or I/O for a read operation

Bus Timing

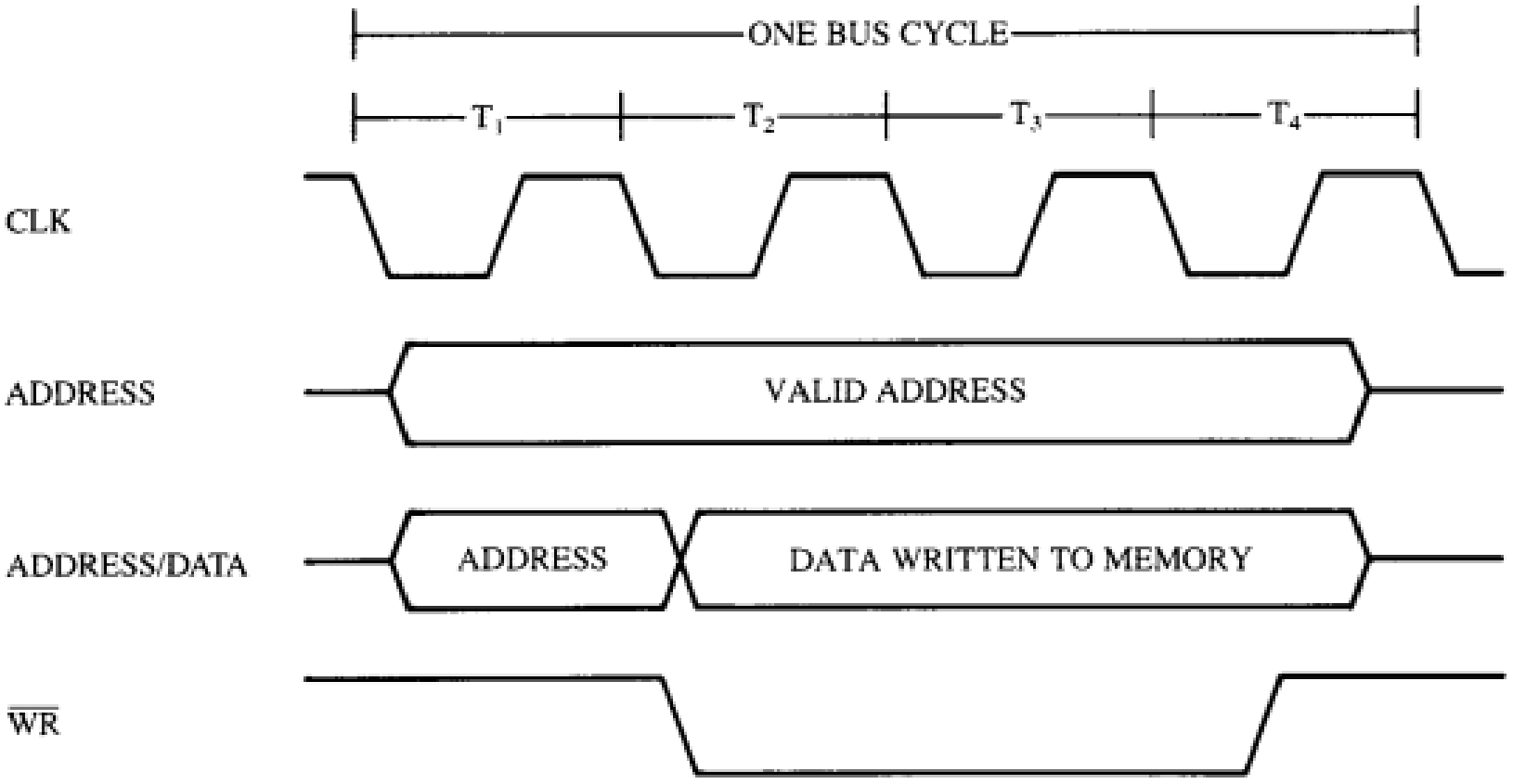
During T3

- If the bus cycle happens to be a read bus cycle, the data bus is sampled at the end of T3

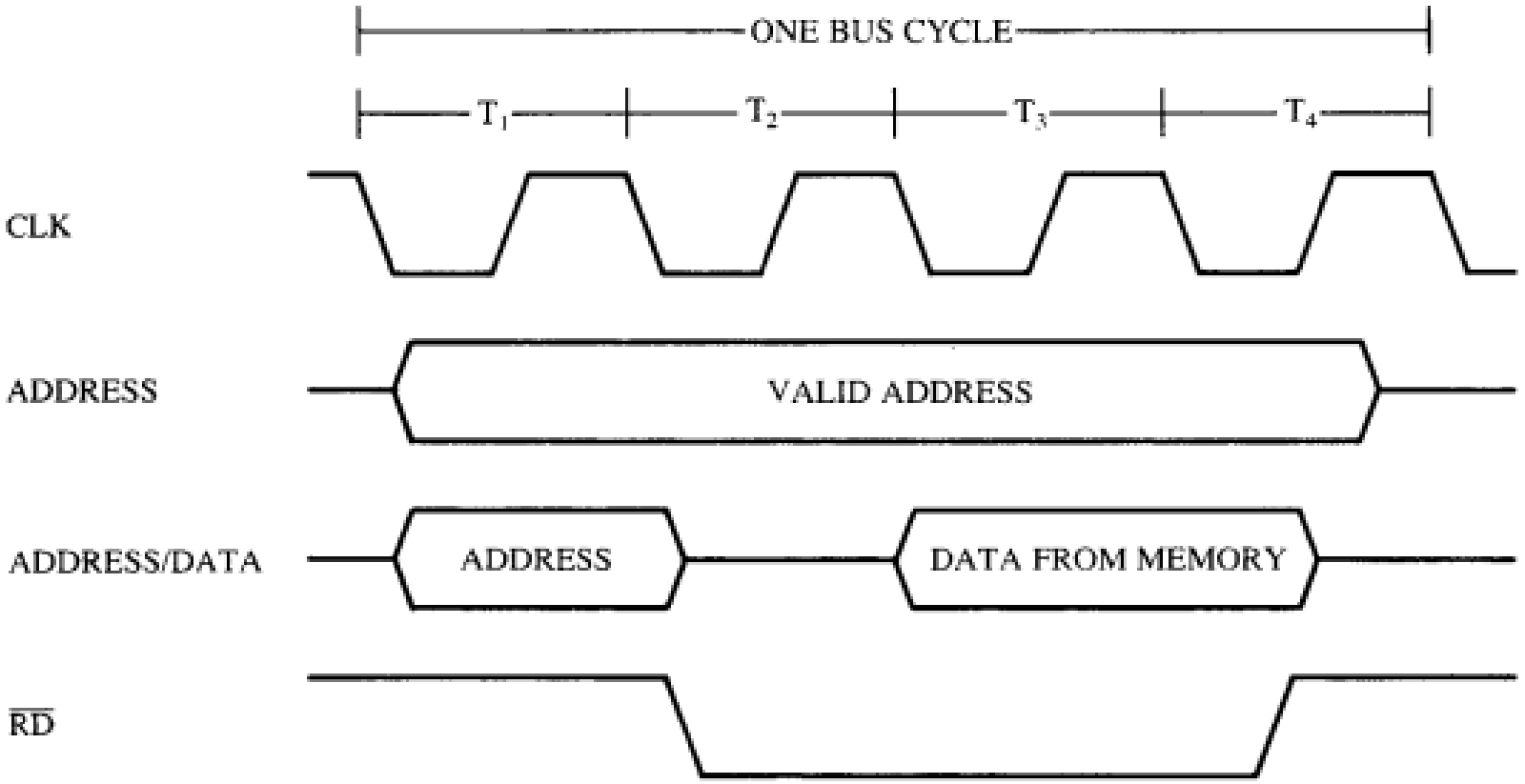
During T4

- All bus signals are deactivated in preparation for the next bus cycle.
- 8086/8088 samples the data bus connections for data that are read from memory or I/O.
- At the trailing edge of the WR' signal transfers data to the memory or I/O, which activates and writes when the WR' signal returns to a logic 1 level

Bus Timing


ONE BUS CYCLE
T1
T2
T3
T4
CLK
ADDRESS
VALID ADDRESS
ADDRESS/DATA
ADDRESS
DATA WRITTEN TO MEMORY
WR

Read Timing


ONE BUS CYCLE
T1
T2
T3
T4
CLK
ADDRESS
VALID ADDRESS
ADDRESS/DATA
ADDRESS
DATA FROM MEMORY
RD

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Thank You