Microprocessors & Interfacing

Programming Model

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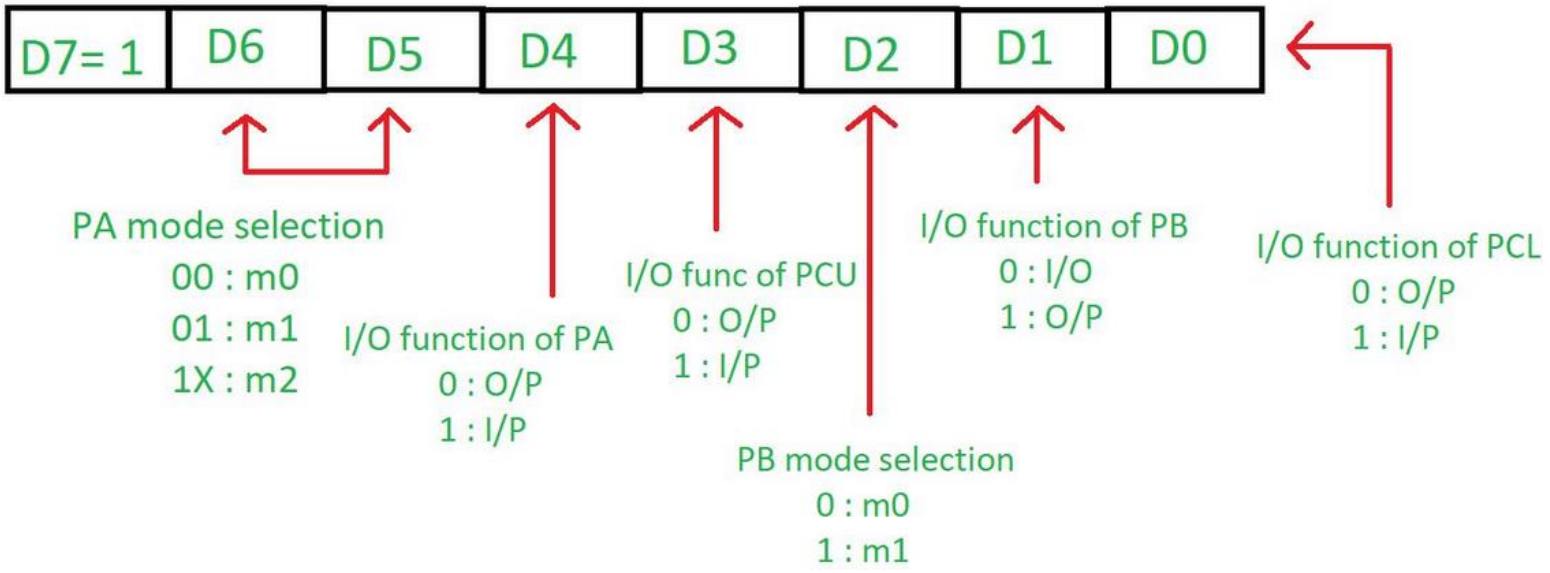
Control Word



Mode 1 (Strobed Input)

- Mode 1 operation causes port A and/or port B to function as latching input devices.
- This allows external data to be stored into the port until the microprocessor is ready to retrieve it.
- Port C is also used in mode 1 operation—not for data, but for control or handshaking signals that help operate either or both port A and port B as strobed input ports.
- The strobed input port captures data from the port pins when the strobe (STB') is activated.

Input control signal definitions

- **STB' (Strobe input)** – If this lines falls to low, the data available at 8-bit input port is loaded into input latches.
- **IBF (Input buffer full)** – If this signal rises to logic 1, it indicates that data has been loaded into latches, i.e. it works as an acknowledgement.
- **INTR (Interrupt request)** – This active high output signal can be used to interrupt the CPU whenever an input device requests the service.

  The INTR becomes a logic 1 when the STB' input returns to logic 1, and is cleared when the data are input from the port by the microprocessor

Input control signal definitions

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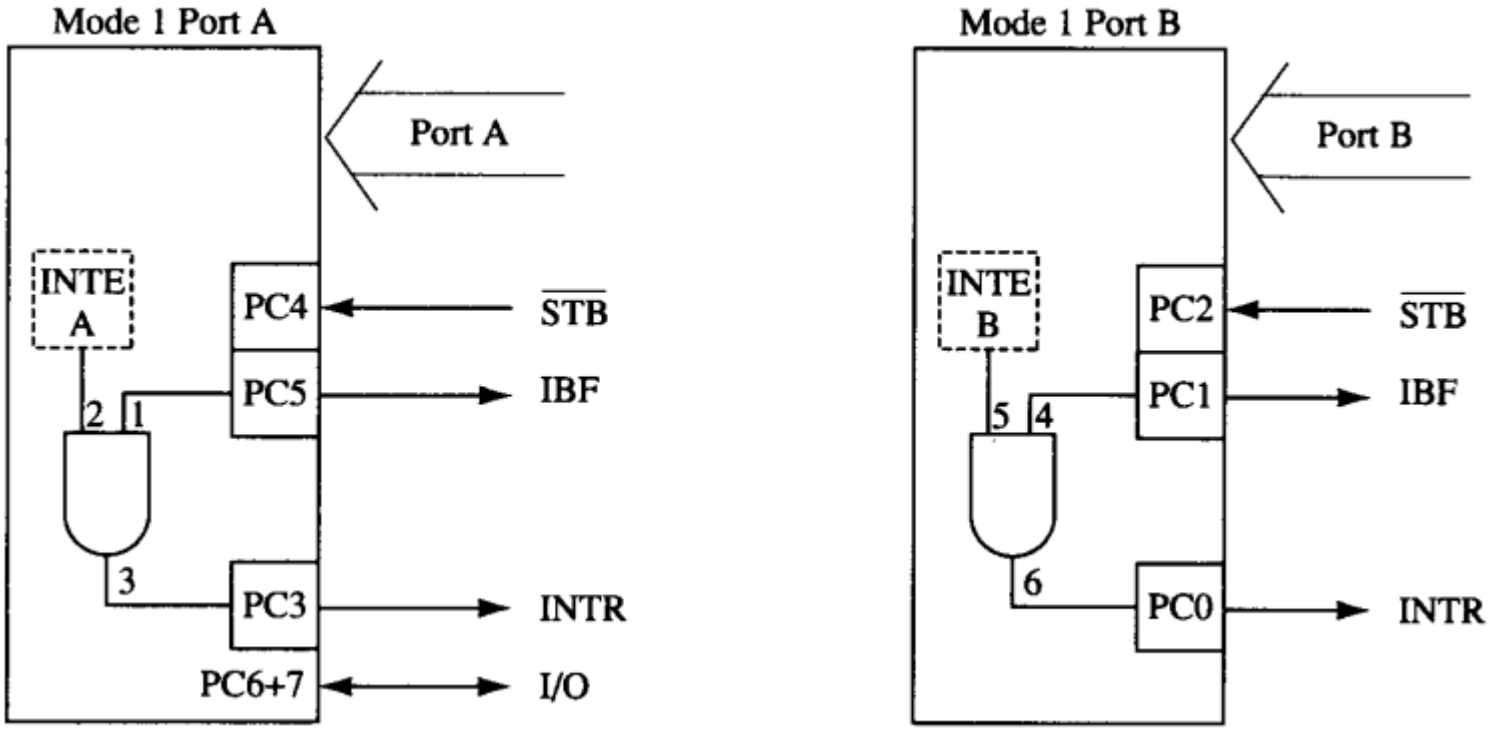
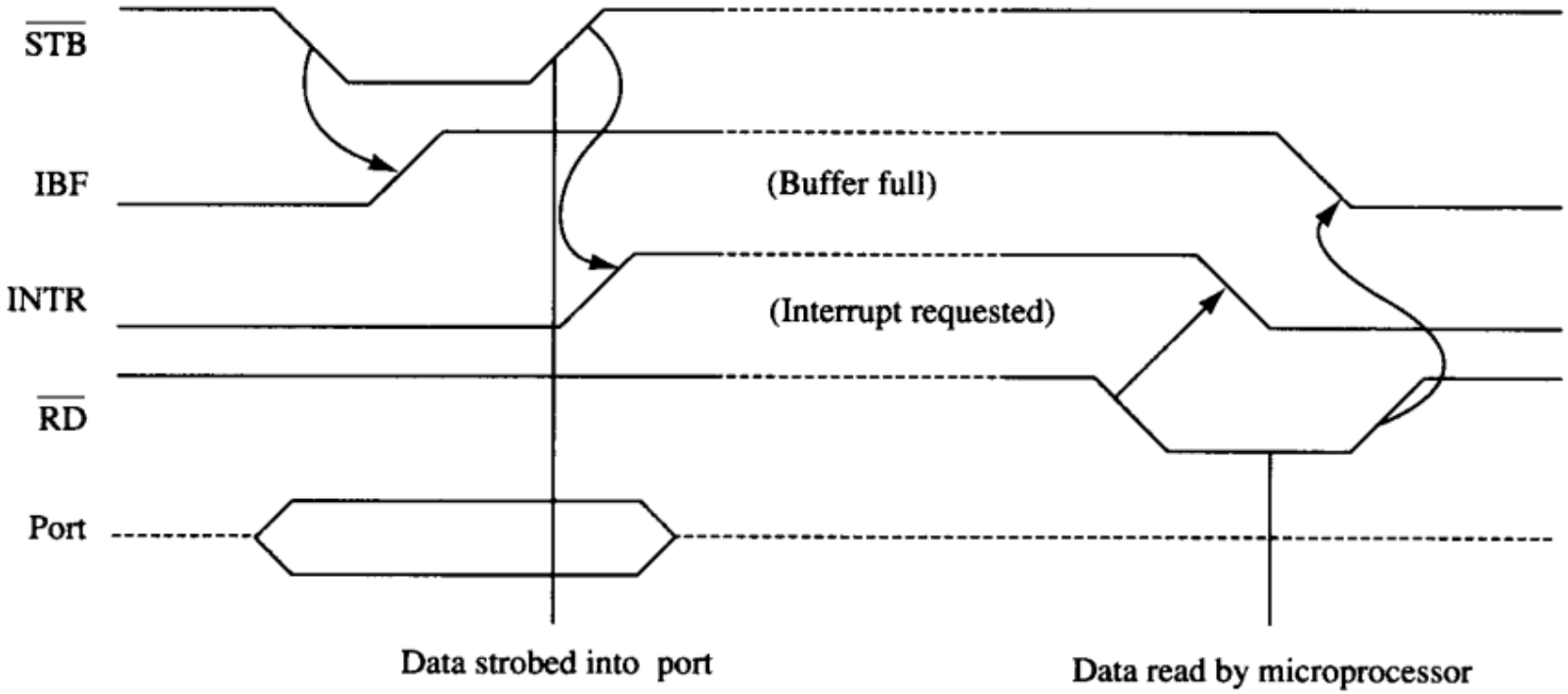
- **INTE** - The interrupt enable signal is neither an input nor an output; it is an internal bit programmed via the port PC4 (port A) or PC2 (port B) bit position.
- **PC7, PC6** - The port C pins 7 and 6 are general-purpose I/O pins that are available for any purpose.

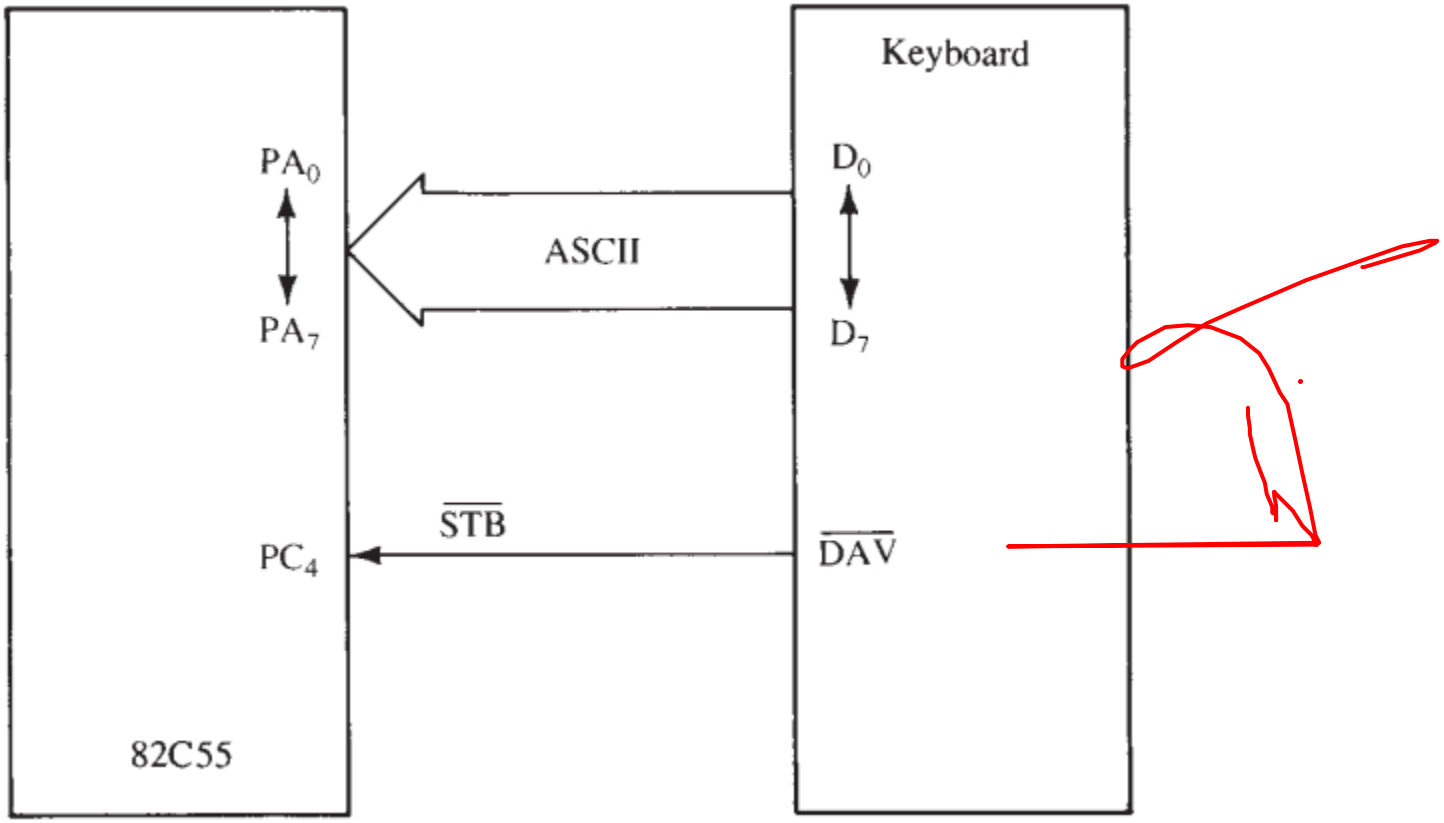
Internal structure : Strobed input o peration (mode 1) of the 82C55



Strobed input operation (mode 1) of the 82C55



Keyboard Interfacing Mode 1



Reading from Keyboard

```
;A procedure that reads the keyboard encoder and
;returns the ASCII key code in AL

      BIT5   EQU   20H
      PORTC  EQU   22H
      PORTA  EQU   20H

      READ   PROC  NEAR

             .REPEAT                    ;poll IBF bit
                    IN    AL,PORTC
                    TEST  AL,BIT5
             .UNTIL !ZERO?
             IN    AL.PORTA             ;get ASCII data
             RET

      READ   ENDP
```

Mode 1 Strobbed Output

- Whenever data are written to a port programmed as a strobed output port, the OBF’ (output buffer full) signal becomes a logic 0 to indicate that data are present in the port latch.
- This signal indicates that data are available to an external I/O device that removes the data by strobing the ACK’ (acknowledge) input to the port.
- The ACK’ signal returns the OBF’ signal to a logic 1, indicating that the buffer is not full.

Signal Definitions for Mode 1 Strobed Output

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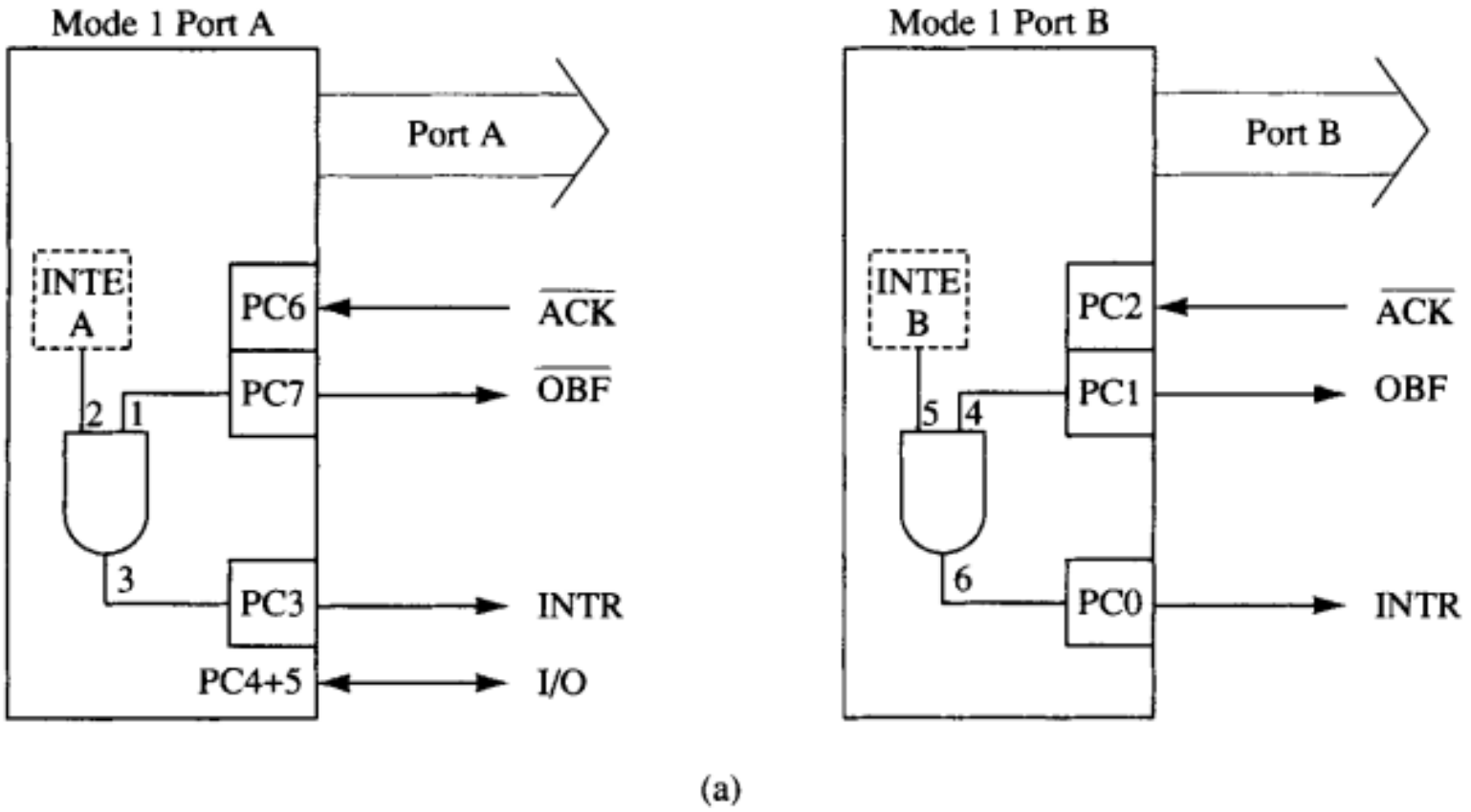
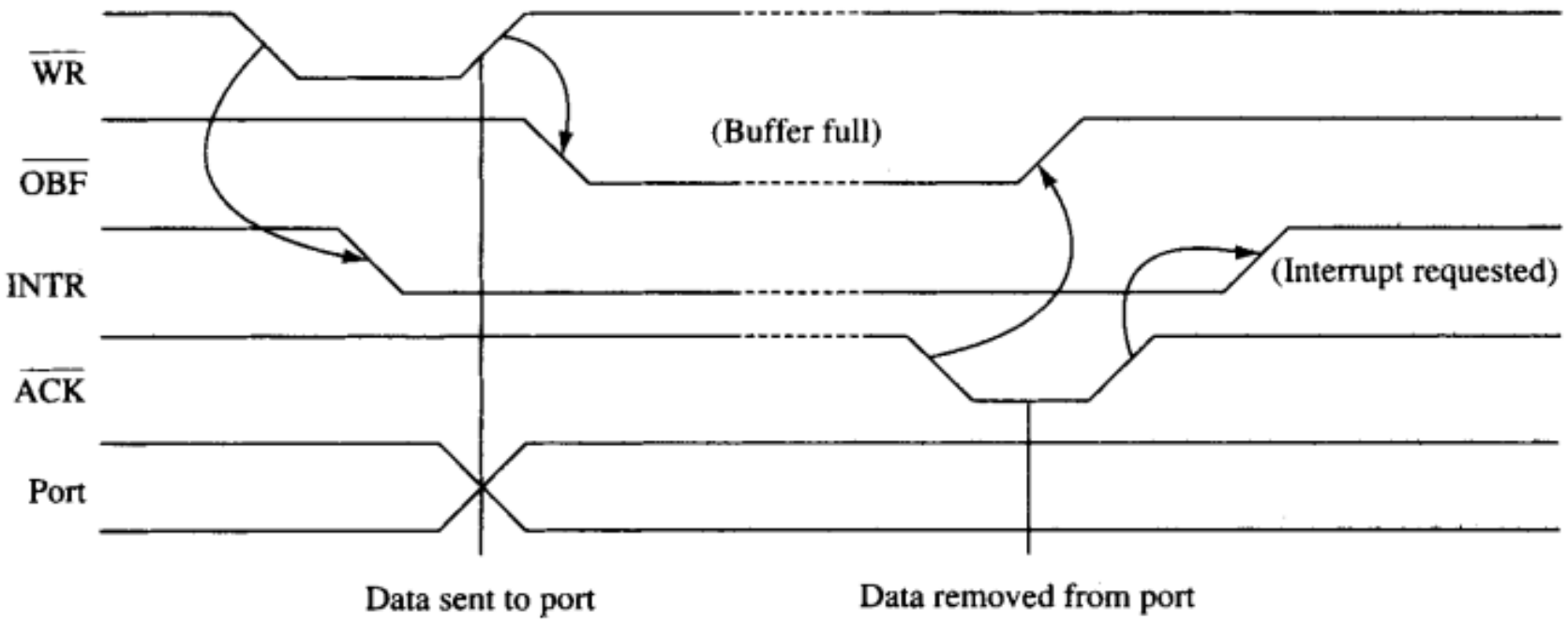
$\overline{\text{OBF}}$	**Output buffer full** is an output that goes low whenever data are output (OUT) to the port A or port B latch. This signal is set to a logic 1 whenever the $\overline{\text{ACK}}$ pulse returns from the external device.
$\overline{\text{ACK}}$	The **acknowledge signal** causes the $\overline{\text{OBF}}$ pin to return to a logic 1 level. The $\overline{\text{ACK}}$ signal is a response from an external device, indicating that it has received the data from the 82C55 port.
INTR	**Interrupt request** is a signal that often interrupts the microprocessor when the external device receives the data via the $\overline{\text{ACK}}$ signal. This pin is qualified by the internal INTE (**interrupt enable**) bit.
INTE	**Interrupt enable** is neither an input nor an output; it is an internal bit programmed to enable or disable the INTR pin. The INTE A bit is programmed using the PC_6 bit and INTE B is programmed using the PC_2 bit.
PC_4, PC_5	Port C pins PC_4 and PC_5 are general-purpose I/O pins. The bit set and reset command is used to set or reset these two pins.

Internal Structure

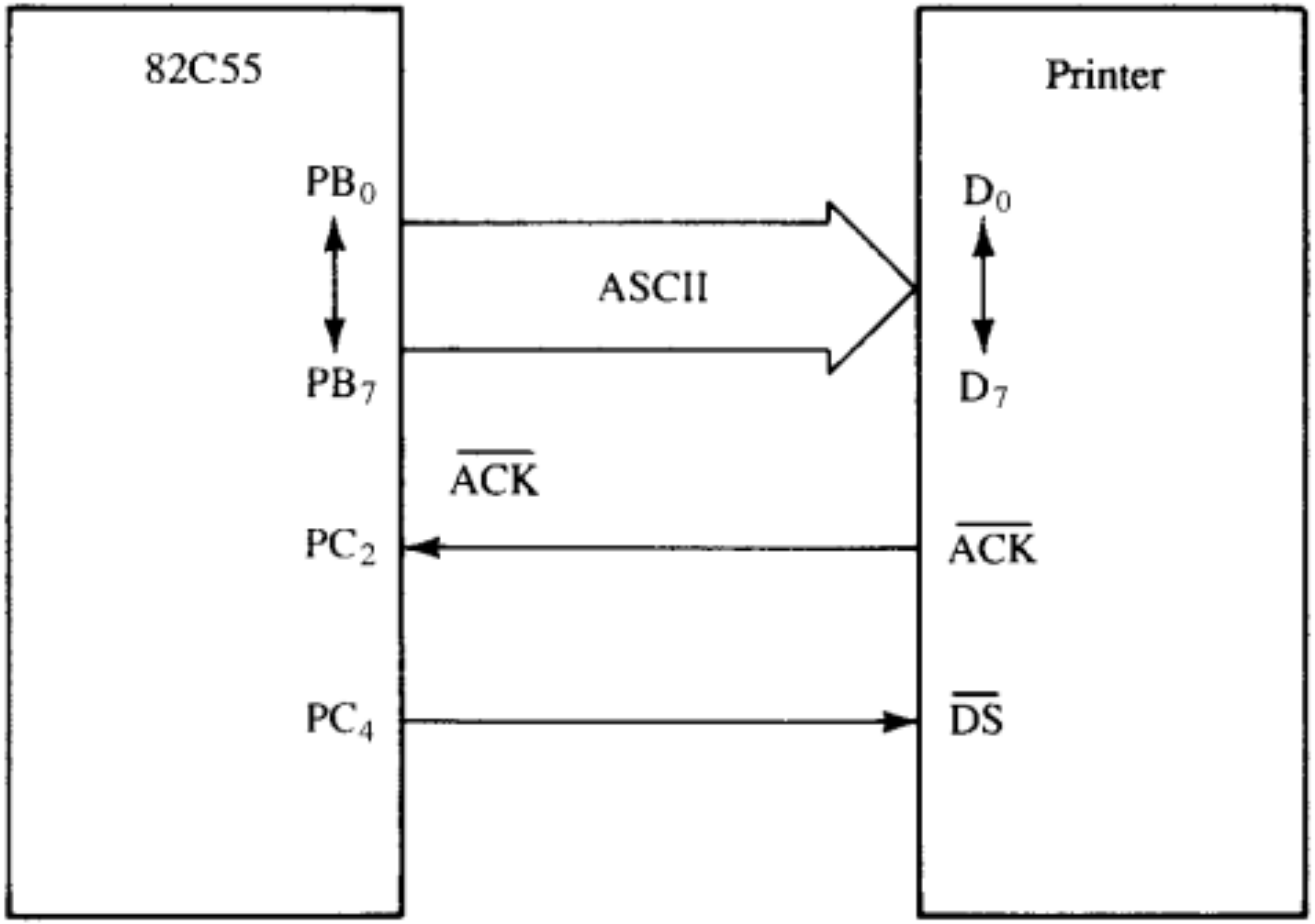


(a)

Timing Diagram



Example



Code

```
;A procedure that transfers an ASCII character from AH to the printer
;connected to port B

BIT1   EQU    2
PORTC  EQU    63H
PORTB  EQU    61H
CMD    EQU    63H

PRINT  PROC   NEAR

       .REPEAT                      ;wait for printer ready
              IN    AL,PORTC
              TEST  AL,BIT1
       .UNTIL !ZERO?
       MOV   AL,AH                  ;send ASCII
       OUT   PORTB,AL
       MOV   AL,8                   ;pulse data strobe
       OUT   CMD,AL
       MOV   AL,9
       OUT   CMD,AL
       RET

PRINT  ENDP
```

Mode 2 Bidirectional Operation

- In mode 2, which is allowed with group A only, port A becomes bidirectional, allowing data to be transmitted and received over the same eight wires.
- Bidirectional bused data are useful when interfacing two computers.
- This mode is commonly employed in various applications such as interfacing with parallel communication devices, controlling input/output devices, and implementing communication protocols where bidirectional data transfer is required.

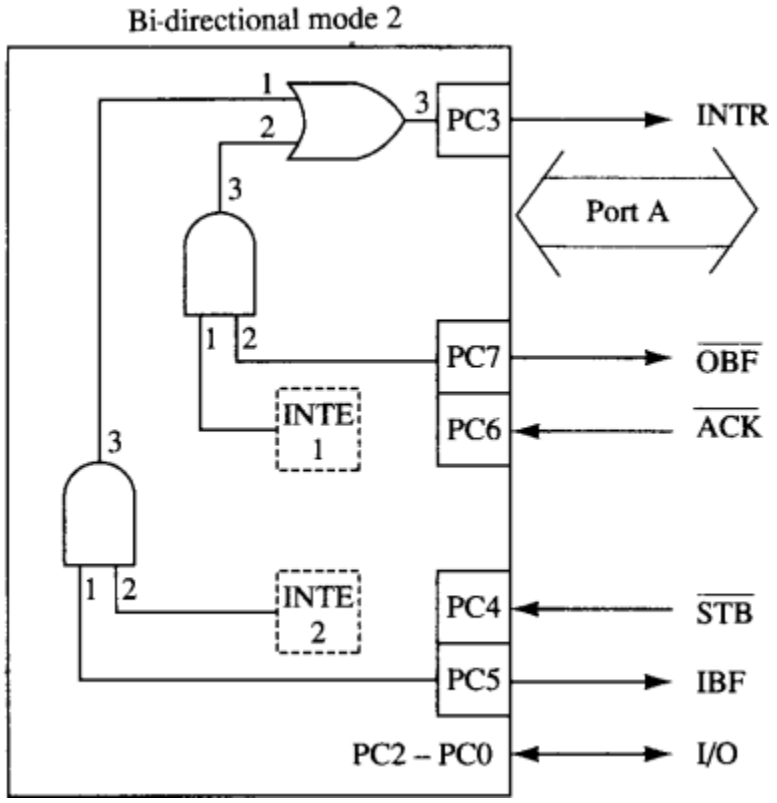
Signal Definition – Mode 2

INTR	**Interrupt request** is an output used to interrupt the microprocessor for both input and output conditions.
$\overline{\text{OBF}}$	**Output buffer full** is an output indicating that the output buffer contains data for the bidirectional bus.
$\overline{\text{ACK}}$	**Acknowledge** is an input that enables the three-state buffers so that data can appear on port A. If $\overline{\text{ACK}}$ is a logic 1, the output buffers of port A are at their high-impedance state.
$\overline{\text{STB}}$	The **strobe** input loads the port A input latch with external data from the bidirectional port A bus.
IBF	**Input buffer full** is an output used to signal that the input buffer contains data for the external bidirectional bus.
INTE	**Interrupt enable** are internal bits (INTE1 and INTE2) that enable the INTR pin. The state of the INTR pin is controlled through port C bits PC_6 (INTE1) and PC_4 (INTE2).
PC_0, PC_1, and PC_2	These pins are general-purpose I/O pins in mode 2 controlled by the bit set and reset command.

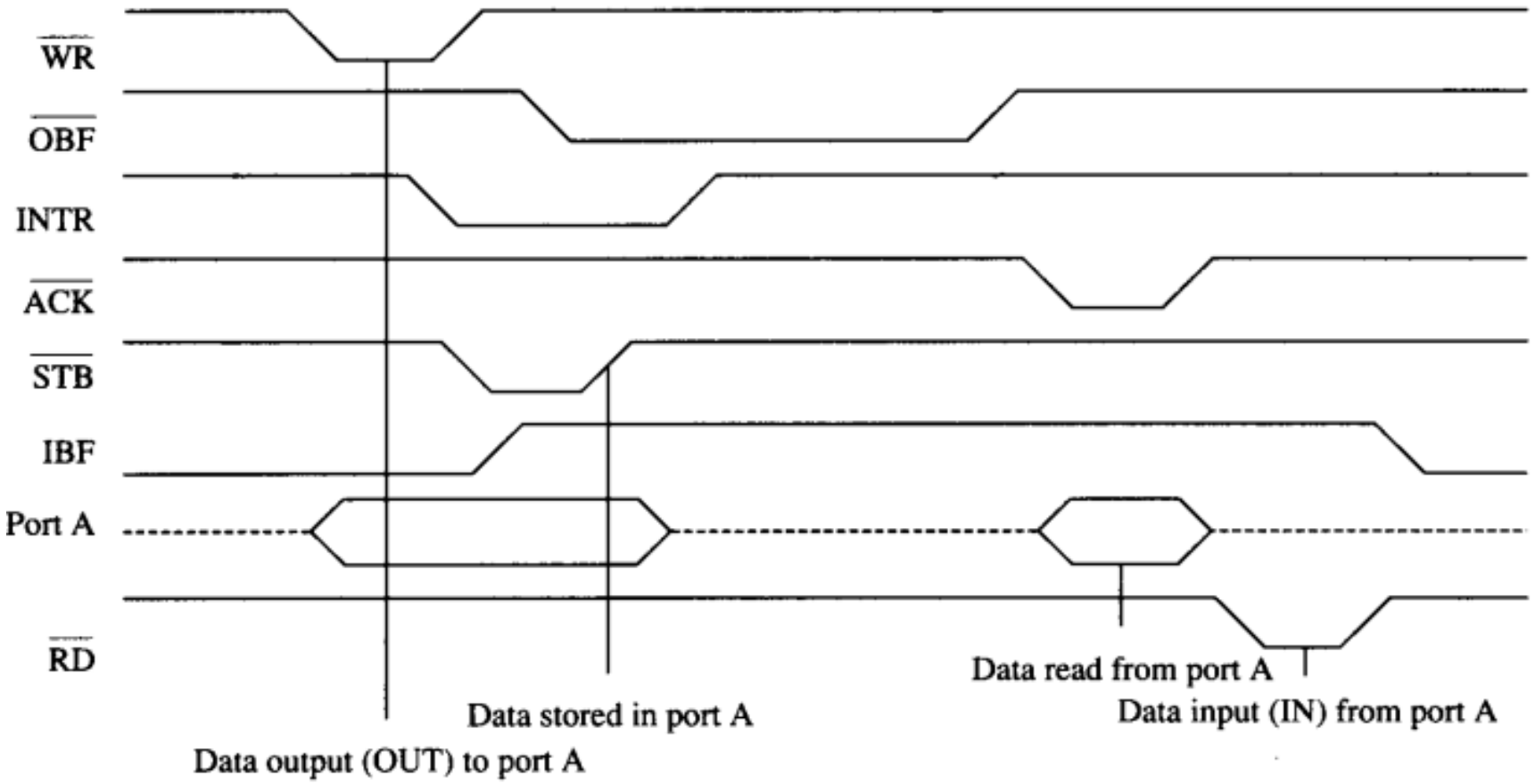
The Bidirectional Bus

- The bidirectional bus is used by referencing port A with the IN and OUT instructions.
- To transmit data through the bidirectional bus, the program first tests the OBF' signal to determine whether the output buffer is empty.
- If it is, then data are sent to the output buffer via the OUT instruction.
- The external circuitry also monitors the signal to decide whether the microprocessor has sent data to the bus. As soon as the output circuitry sees a logic 0 on , it sends back the signal to remove it from the output buffer. The signal sets the bit and enables the three-state output buffers so that data may be read.

Internal Structure



Timing


WR
OBF
INTR
ACK
STB
IBF
Port A
RD
Data output (OUT) to port A
Data stored in port A
Data read from port A
Data input (IN) from port A

Example

```
;A procedure transmits AH through the bidirectional bus

BIT7   EQU   80H
PORTC  EQU   62H
PORTA  EQU   60H

TRANS  PROC NEAR

       .REPEAT                          ;test OBF
             IN    AL,PORTC
             TEST  AL,BIT7
       .UNTIL !ZERO?
       MOV   AL,AH                      ;send data
       OUT   PORTA,AL
       RET

TRANS ENDP
```

Example

```
;A procedure that reads data from the bidirectional bus into AL

BIT5   EQU  20H
PORTC  EQU  62H
PORTA  EQU  60H

READ   PROC NEAR

       .REPEAT                      ;test IBF
              IN    AL,PORTC
              TEST  AL,BIT5
       .UNTIL !ZERO?
       IN   AL,PORTA
       RET

READ   ENDP
```

Mode Summary

		Mode 0		Mode 1		Mode 2
Port A		IN	OUT	IN	OUT	I/O
Port B		IN	OUT	IN	OUT	Not used
Port C	0	IN	OUT	$INTR_B$	$INTR_B$	I/O
	1			IBF_B	$\overline{OBF}_B$	I/O
	2			$\overline{STB}_B$	$\overline{ACK}_B$	I/O
	3			$INTR_A$	$INTR_A$	INTR
	4			$\overline{STB}_A$	I/O	$\overline{STB}$
	5			IBF_A	I/O	IBF
	6			I/O	$\overline{ACK}_A$	$\overline{ACK}$
	7			I/O	$\overline{OBF}_A$	$\overline{OBF}$

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Thank You