Microprocessors & Interfacing

Programming Model

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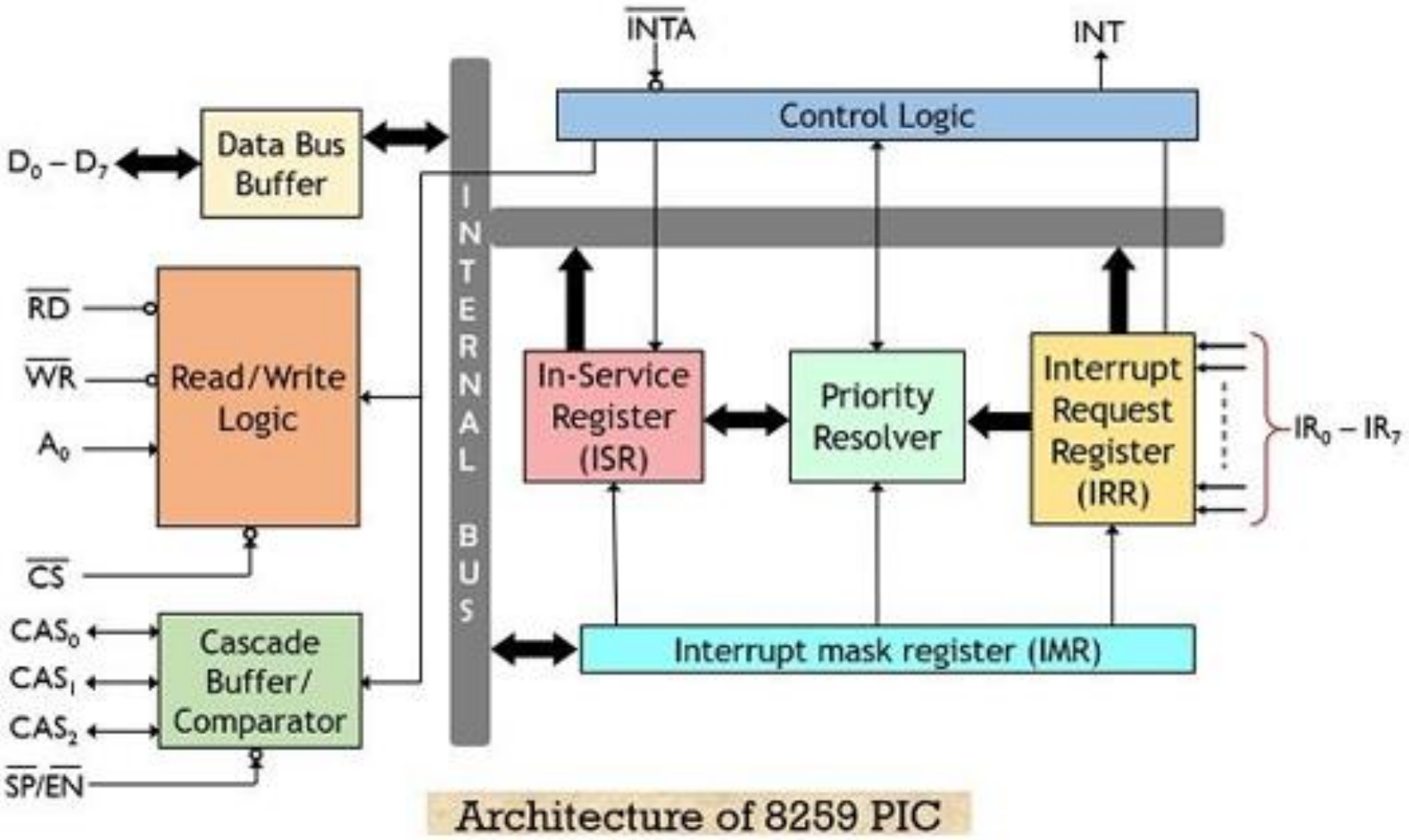
8259A

- The 8259A programmable interrupt controller (PIC) adds eight vectored priority encoded interrupts to the microprocessor.
- This controller can be expanded, without additional hardware, to accept up to 64 interrupt requests.
- This expansion requires a master 8259A and eight 8259A slaves.

Block Diagram



Architecture of 8259 PIC

8259A Command Word

Command word of 8259 is divided into two parts :

Initialization command words(ICW): These are used during the initialization phase to configure the 8259 for its operation. There are four ICWs, ICW1, ICW2, ICW3, and ICW4, each serving a specific purpose in setting up the PIC.

Operating command words(OCW): Once the PIC is initialized, these command words are used to control its operation during normal operation. OCWs include commands for enabling, masking, and prioritizing interrupts, among other functions.

Initialization command words(ICW)

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- ICW is given during the initialization of 8259 i.e. before its start functioning.
- ICW_1 and ICW_2 commands are compulsory for initialization.
- ICW_3 command is given during a cascaded configuration.
- If ICW_4 is needed, then it is specified in ICW_1.
- The sequence order of giving ICW commands is fixed i.e. ICW_1 is given first and then ICW_2 and then ICW_3.
- Any of the ICW commands can not be repeated, but the entire initialization process can be repeated if required.

Operating command words(OCW)

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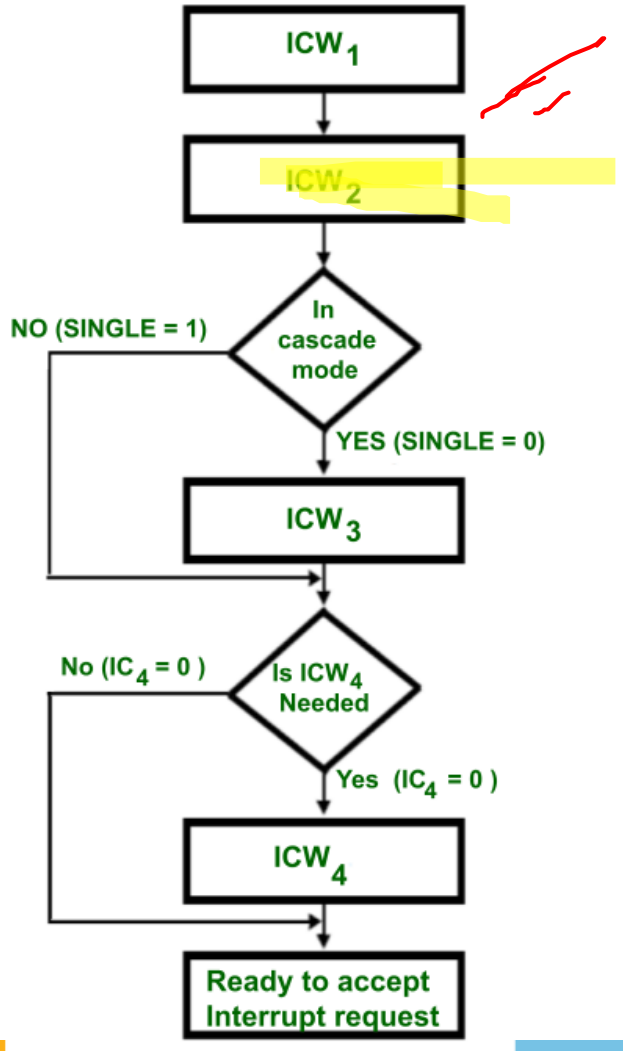
- OCW is given during the operation of 8259 i.e. microprocessor starts using 8259.
- OCW commands are not compulsory for 8259.
- The sequence order of giving OCW commands is not fixed.
- The OCW commands can be repeated.

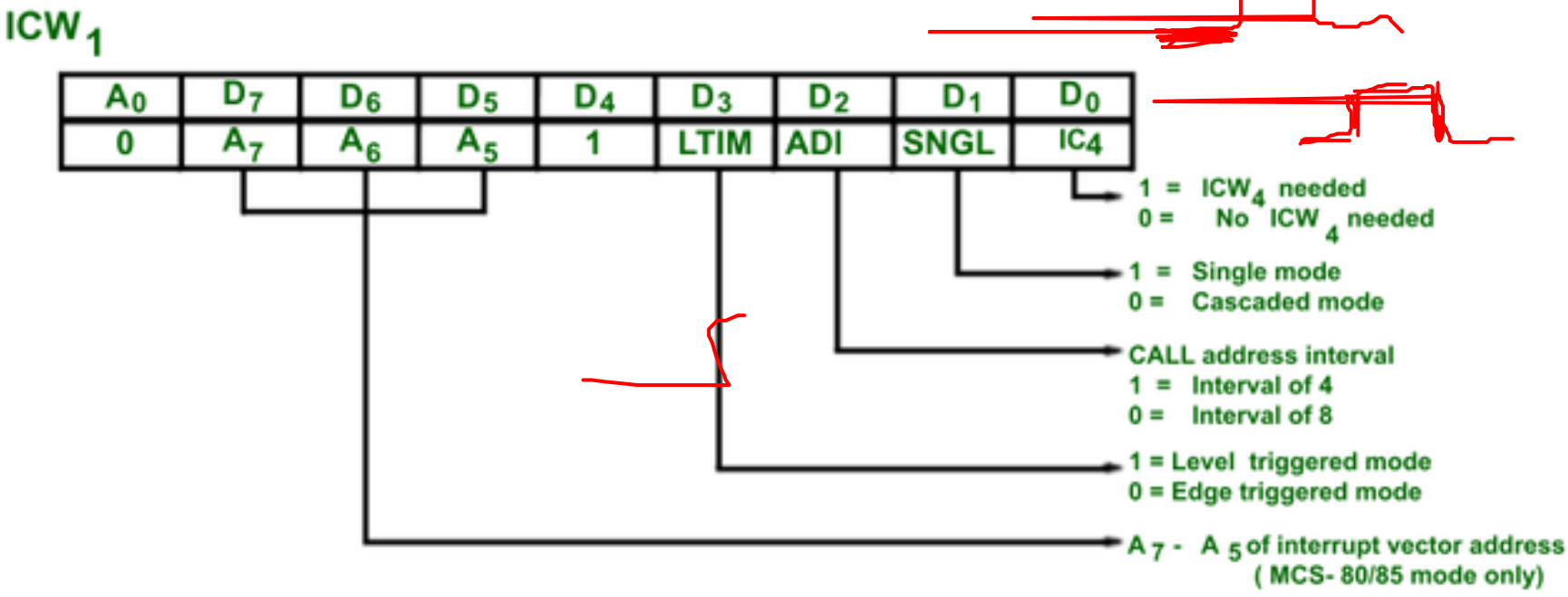
Initialization sequence of 8259



ICW_1 command

- The control word is recognized as ICW_1 when $A_0 = 0$ and $D_4 = 1$.
- It has the control bits for Edge and level triggering mode, single/cascaded mode, call address interval and whether ICW4 is required or not.
- Address lines A_7 to A_5 are used for interrupt vector addresses.

ICW_1 command



ICW_1 command

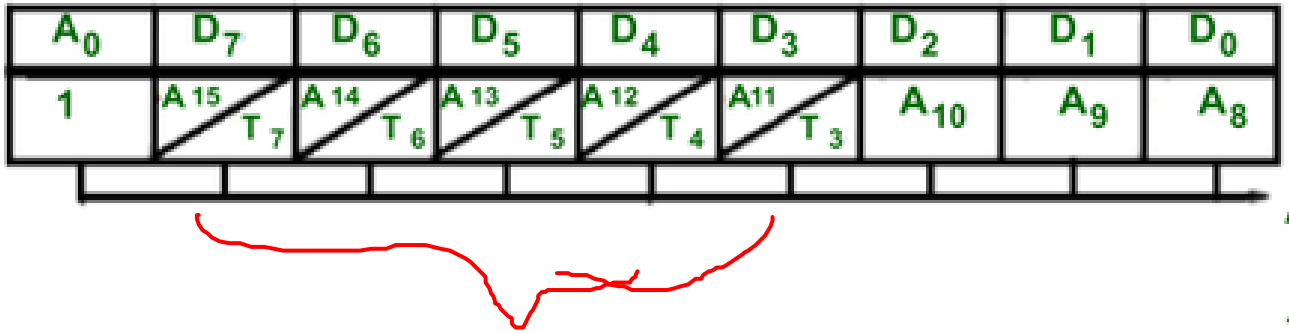
When the ICW_1 is loaded, then the initializations performed are:

- The edge sense circuit is reset because, by default, 8259 interrupt is edge triggered.
- The interrupt mask register is cleared.
- IR7 is assigned to priority 7.
- Slave mode address is assigned as 7.
- When $D_0 = 0$, this means IC_4 command is not required. Therefore, functions used in IC4 are reset.
- Special mask mode is reset and status read is assigned to IRR.

ICW_2 command

- The control word is recognized as ICW_2 when A_0= 1.
- It stores the information regarding the interrupt vector address.
- In the 8085 based system, the A15 to A_8 bits of control word is used for interrupt vector addresses.
- In the 8086 based system, T_6 to T_3 bits are inserted instead of A_{15} to A_8 and A_{10} to A_8 are used for selecting interrupt level, i.e. 000 for IR_0 and 111 for IR_7

ICW_2 command



A_{15} - A_8 of interrupt vector address
(MCS- 80/85 mode only)

T_7 - T_3 of interrupt vector address
(8086/8088 mode only)

ICW_3

ICW_3 (Master device)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

1 = IR input has a slave
0 = IR input does not have a slave

ICW_3 (Slave device)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	ID_2	ID_1	ID_0

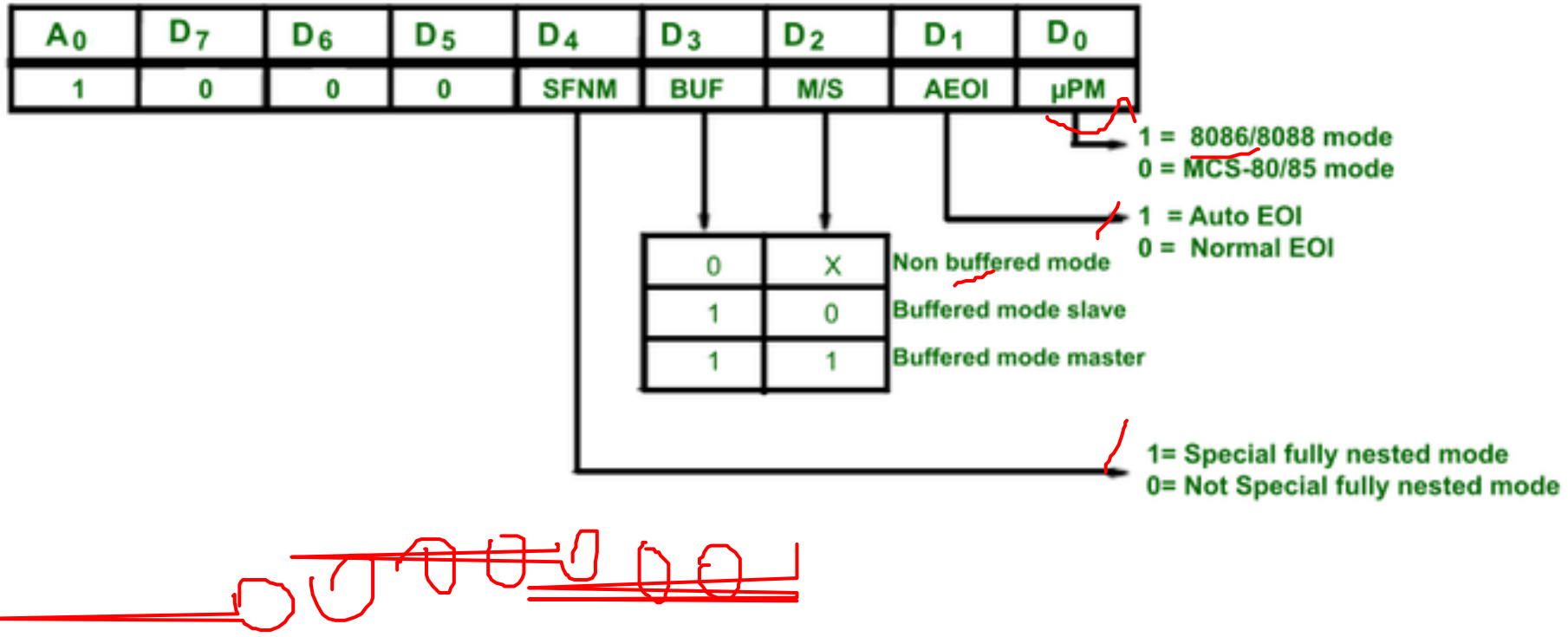
Slave Id

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

ICW_4

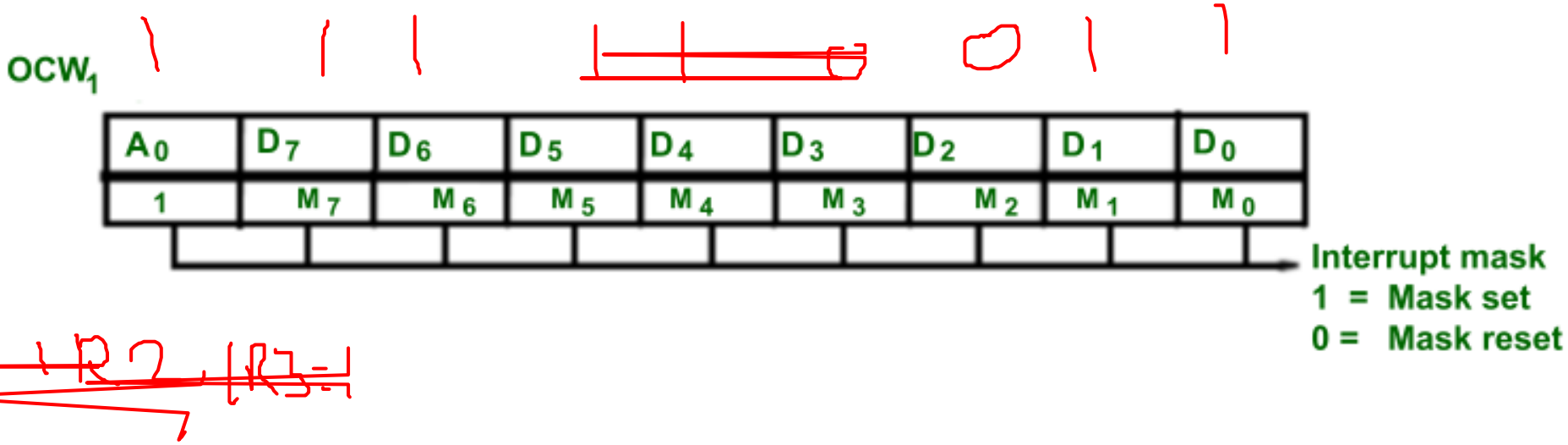
- When AEOI = 1, then Automatic end of interrupt mode is selected.
- When SFMN = 1, then a special fully nested mode is selected. when BUF = 0 , then Non buffered mode is used (i.e. M/S is don't care) and when M/S = 1, then 8259 is master, otherwise it is a slave.
- When µPM = 1, then 8086 operations are performed, otherwise 8085 operations are performed

ICW_4


A0 D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 SFNM BUF M/S AEOI µPM
1 = 8086/8088 mode
0 = MCS-80/85 mode
1 = Auto EOI
0 = Normal EOI
0 X Non buffered mode
1 0 Buffered mode slave
1 1 Buffered mode master
1= Special fully nested mode
0= Not Special fully nested mode

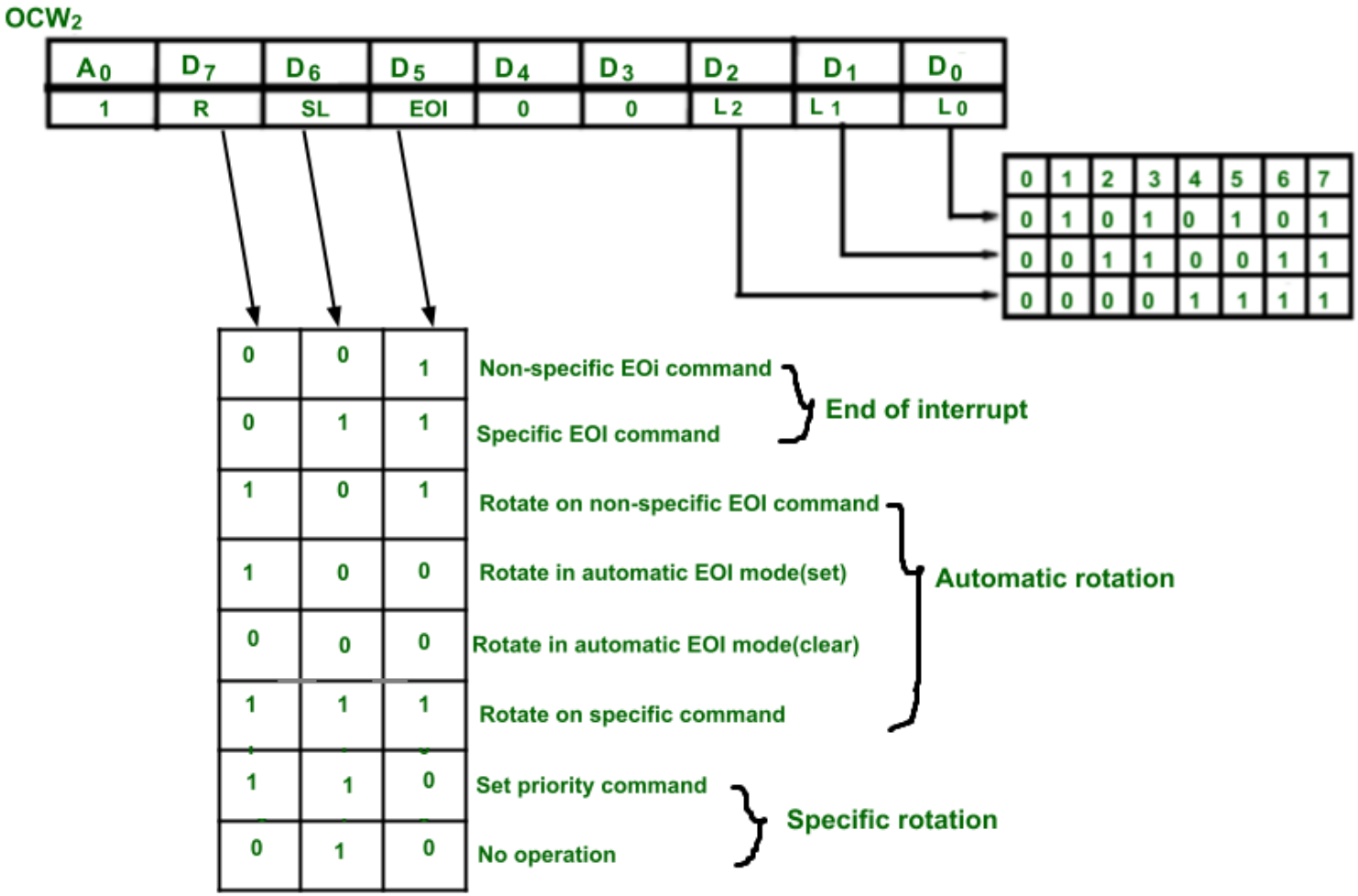
OCW_1

- It is used to set and reset the mask bits in IMR(interrupt mask register). $M_7 – M_0$ describes 8 mask bits



OCW_2

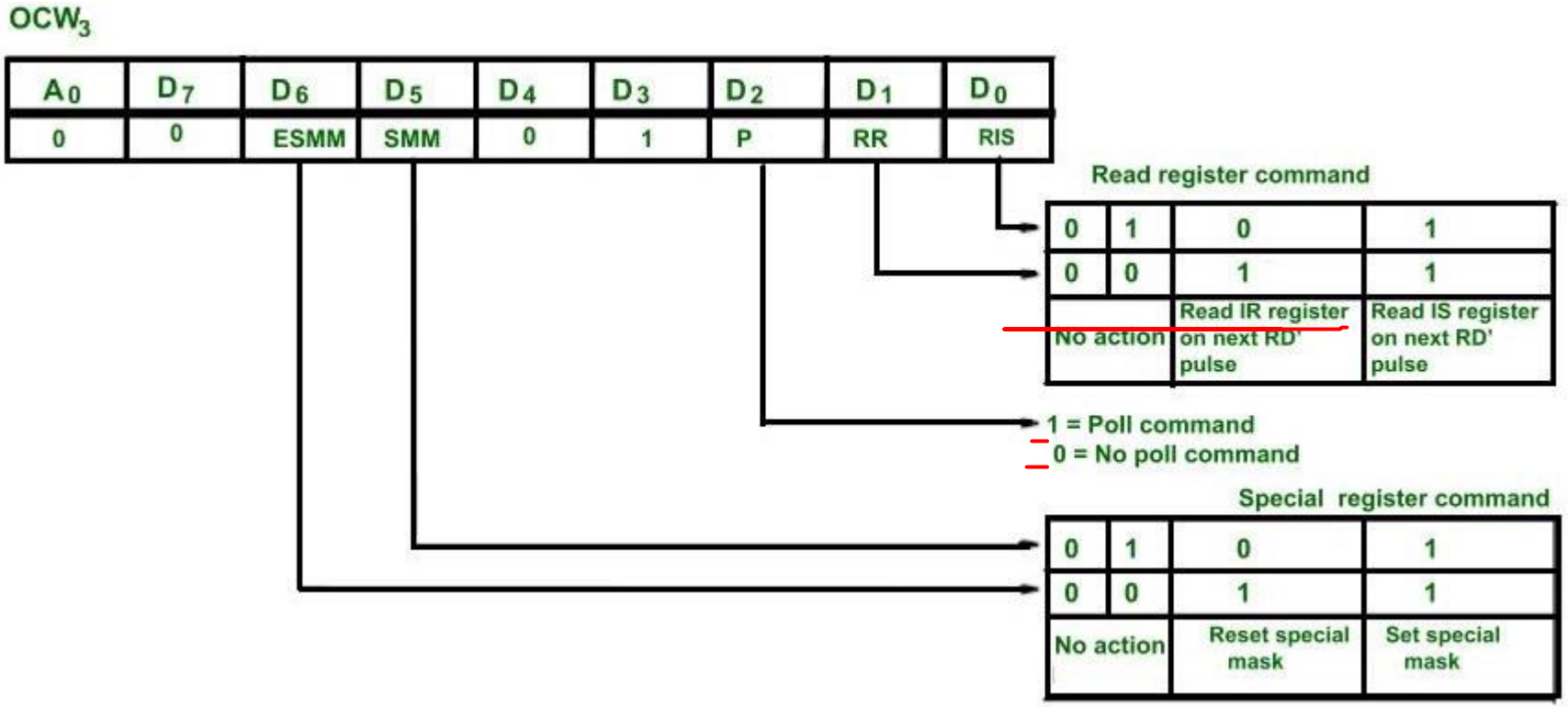
It is used for selecting the mode of operation of 8259. Here L_2 to L_0 are used to describe interrupt level on which action need to be performed.



OCW_3

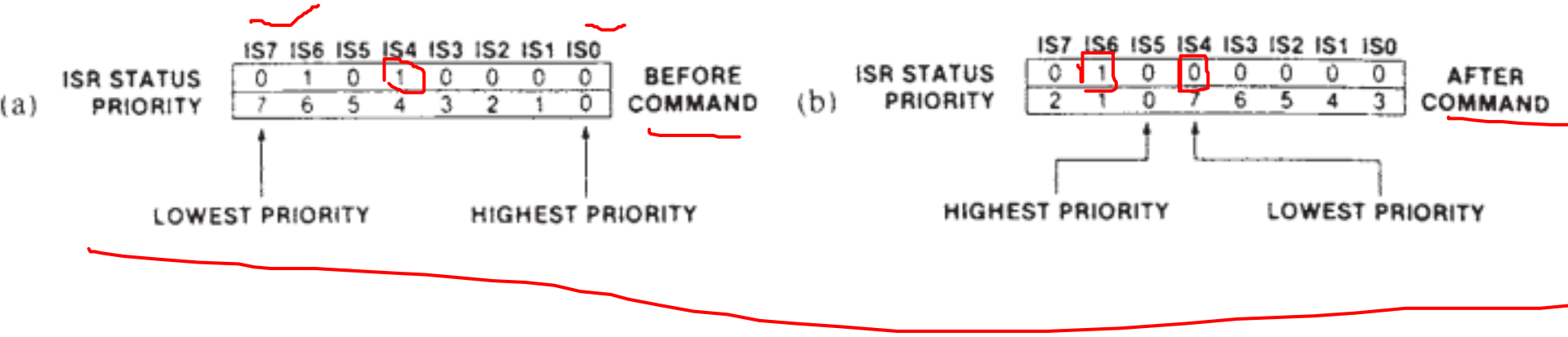
- When the ESMM (Enable special mask mode) bit is set, then the SMM bit is don't care. If SMM = 1 and ESMM = 1, then 8259 will enter in Special mask mode.
- If ESMM = 1 and SMM = 0, then 8259 will return into normal mask mode.
- RR and RIS are used to give the read register command.
- P = 1 is used for poll command.

OCW_3


OCW3
A0 D7 D6 D5 D4 D3 D2 D1 D0
0 0 ESMM SMM 0 1 P RR RIS
Read register command
0 1 0 1
0 0 1 1
No action
Read IR register on next RD' pulse
Read IS register on next RD' pulse
1 = Poll command
0 = No poll command
Special register command
0 1 0 1
0 0 1 1
No action
Reset special mask
Set special mask

Status Register

- Three status registers are readable in the 8259A: interrupt request register (IRR), in-service register (ISR), and interrupt mask register (IMR).



Programming 8259A

```
PIC1      EQU   48H          ;8259A control A0 = 0
PIC2      EQU   49H          ;8259A control A0 = 1
ICW1      EQU   1BH          ;8259A ICW1
ICW2      EQU   80H          ;8259A ICW2
ICW4      EQU   3            ;8259A ICW4
OCW1      EQU   0FEH         ;8259A OCW1

;
;program 8259A
;
          MOV   AL,ICW1      ;program ICW1
          OUT   PIC1,AL
          MOV   AL,ICW2      ;program ICW2
          OUT   PIC2,AL
          MOV   AL,ICW4      ;program ICW4
          OUT   PIC2,AL
          MOV   AL,OCW1      ;program OCW1
          OUT   PIC2,AL
          STI                ;enable INTR pin
;
```

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Thank You