EE4-17
EE9-AO4

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2014

MSc and EEE PART IV: MEng and ACGI

Corrected Copy

HIGH PERFORMANCE ANALOGUE ELECTRONICS

Friday, 2 May 10:00 am

Time allowed: 3:00 hours

There are FOUR questions on this paper.

Answer ALL questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : E. Rodriguez-Villegas
Second Marker(s) : P. Georgiou

THE QUESTIONS

1. a) Figure 1.1 shows an LC ladder circuit that implements a low pass filter function.

   i) Write down the ladder state equations and use these to draw the scaled signal flow graph. [4]

   ii) Show how the scaled signal flow graph can be realized using the circuit shown in Figure 1.2. Identify which blocks are amplifiers and which blocks are integrators. [2]

   iii) State one advantage and one disadvantage of MOSFET-C integrators compared to transconductor-C integrators for realising this filter. [2]

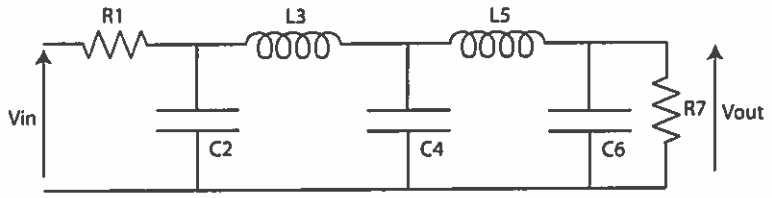

Figure 1.1

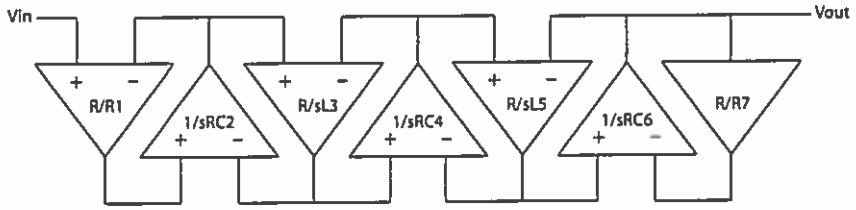

Figure 1.2

b) Figure 1.3 shows a differential MOSFET-C integrator which requires the two inputs ($V1$ and $V2$) to be balanced.

   i) Calculate the voltage (Vc) required to give a unity gain frequency of 1×10^9 rad/s. Assume that $\beta = 5$ mA/V, $V_{th} = 0.7$ V, $C = 20$ pF. All transistors are matched and the virtual earth is at 0 V. [4]

   ii) Draw a MOSEFT-C integrator circuit which operates like the one in Figure 1.3 but does not require the two inputs to be balanced. Give an expression for the differential output of your circuit. [4]

   iii) Which circuit (the one in Figure 1.3 or yours from (ii)) is preferable when there is an on-chip variation in the threshold voltage V_{th}? Explain your answer. [1]

   iv) For both circuits, explain how you would compensate for a change in the threshold voltage. Using your value for Vc from (i), what is the maximum change in V_{th} that could be tolerated if the chip supply voltage is 3 V? [3]

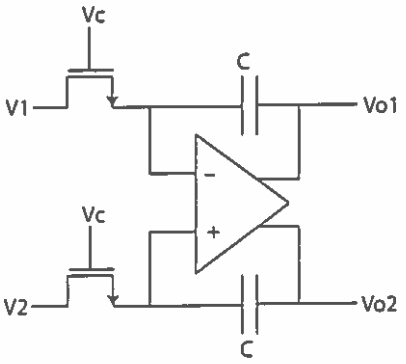

Figure 1.3

2. a) In the circuit of Figure 2.1 all capacitors are the same size: $0.25C_T$ where C_T is the total capacitance.

i) Re-draw the circuit with all of the noise sources referred to the gate of the transistor. [2]

ii) If $V2$, $V3$, and $V4$ are constant find an expression for the noise referred to the input (Vin). All parasitic capacitances can be ignored. [5]

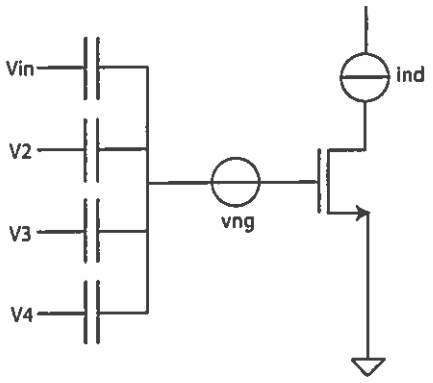

Figure 2.1

b) Define noise factor and noise figure. [2]

c) Figure 2.2 shows two cascaded stages. G1 and G2 are the power gains of the two stages, vns is noise present at the input due to the source, and vnt is the total noise present at the output.

i) Show that the noise factor of the cascaded pair is

$$F = F1 + \frac{F2 - 1}{G1} \tag{2.1}$$

[3]

ii) For a given system: G1 = 100, F1 = 2, G2 = 20, and F2 = 3. Calculate the signal to noise ratio at the input if the signal to noise ratio at the output is 50 dB. Give your answer in dB. [3]

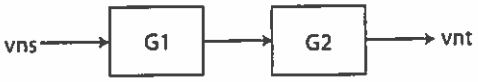

Figure 2.2

d) For the chain of three cascaded stages in Figure 2.3 calculate the total noise figure. For each block the number on the left is the noise factor and the number on the right is the power gain. [5]

Figure 2.3

3. a) Briefly explain the role of the mixer in a superhetrodyne receiver system. [2]

b) A superhetrodyne receiver system is receiving a signal at 900 MHz and has an intermediate frequency of 100 MHz. Explain how an RF signal at 1900 MHz could interfere with the reception of the wanted signal. [3]

c) For the multiplier in Figure 3.1, derive an expression for the output current ($Iout = Ic1 - Ic2$) if the input Va is small. State the range of Va your expression is valid for. [6]

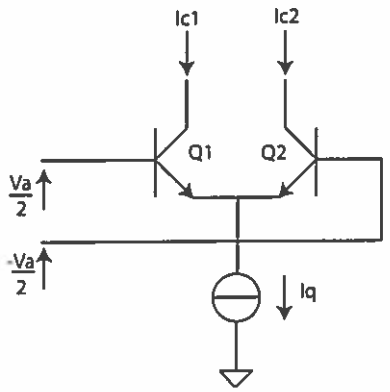

Figure 3.1

d) Figure 3.2 shows a Gilbert multiplier.

i) Explain how emitter degeneration resistors can be used to increase the linear range of the multiplier in Figure 3.2. Draw a diagram to show where you would place them. If all of the transistors have $g_m = 1$ mS state suitable values for the resistors. [5]

ii) Explain how pre-distortion can be used to increase the linear range of the multiplier in Figure 3.2. Draw a circuit that can be used to realise suitable pre-distortion. [4]

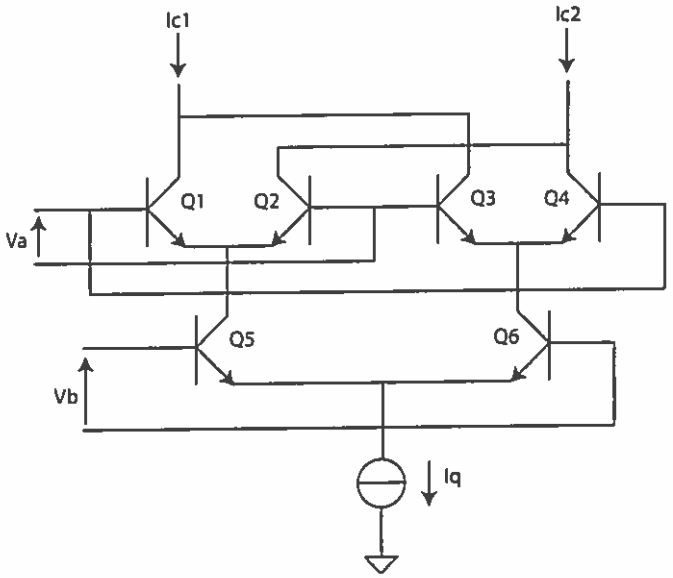

Figure 3.2

4. a) Draw the input-output relationship of an ideal transconductor and the input-output relationship of a typical non-ideal transconductor. [2]

b) The transistors in the differential pair of Figure 4.1 are operating in the saturation region. Show that

$$\begin{aligned} Iout &= Id1 - Id2 \\ &= Vd\sqrt{2\beta Is - \beta^2 Vd^2}. \end{aligned} \tag{4.1}$$

Hint: First solve for $Id1$ and $Id2$ using the quadratic formula. [7]

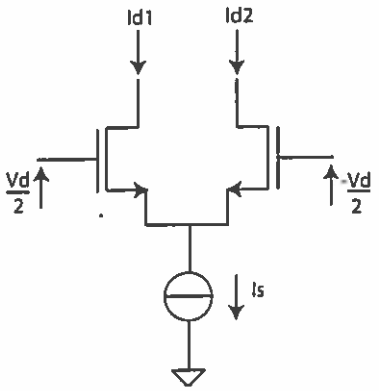

Figure 4.1

c) Explain how a quadratic bias current could be used to linearise this transconductor. Give an expression for the resulting transconductance. [3]

d) Draw a circuit that can be used to generate a suitable quadratic bias current. State how to bias your circuit so that the transconductor in Figure 4.1 will be linearised. [4]

e) The maximum input range of the circuit is found to be 100 mVpp.

i) Calculate the maximum possible input referred noise if the circuit must have a signal-to-noise ratio of 60 dB. [2]

ii) If most of the actual noise present is flicker noise, explain briefly techniques you could use for decreasing the noise without changing the circuit topology. [2]