E3.05
ISE3.19

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2008

EEE/ISE PART III/IV: MEng, BEng and ACGI

Corrected Copy

DIGITAL SYSTEM DESIGN

Q1

Friday, 9 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : T.J.W. Clarke

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X[7:0] is an eight bit bus with X7 being the MSB and X0 the LSB.

Hexadecimal numbers are prefixed with '$'. For example the decimal number 10 is written as $A.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

1. Figure 1.1 depicts the state diagram of a 5-state finite state machine (FSM) with inputs *in_A* and *in_B*, and an output *FSM_out*. One-hot state encoding is used. The output is *FSM_out* set high in state S4 and low in all other states. All input signals change shortly before the rising edge of the clock signal *clk*.

   a) Draw the state transition table for this FSM. Hence, or otherwise, design the FSM in the form of Boolean equations. State any assumptions used.

   [10 Marks]

   b) Explain briefly why one-hot state encoding is particularly suitable for FPGA implementation. Estimate the resource utilization if your design is implemented using an Altera Cyclone-II FPGA.

   [5 Marks]

   c) Assuming that the FSM is initially at state S0, draw a timing diagram showing the output *FSM_out* and the state variable S4:S0 for inputs *in_A* and *in_B* shown in Figure 1.2. You may use the timing diagram template provided at the end of this paper.

   [5 Marks]

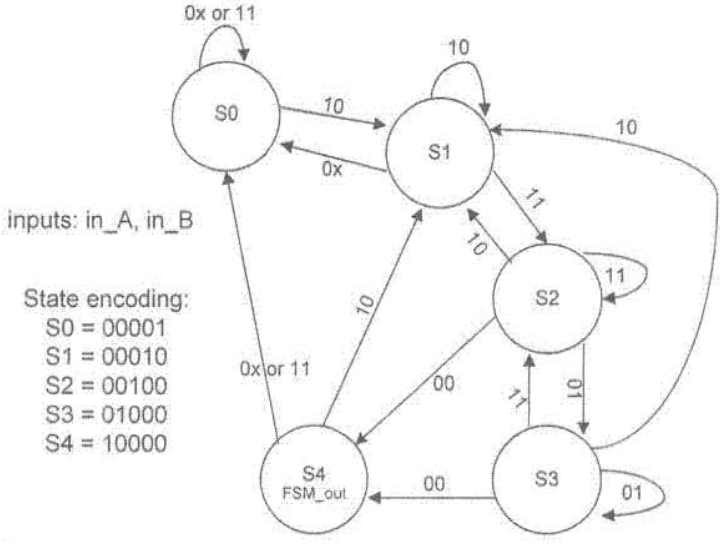


Figure 1.1

use timing diagram template not fig 1.2

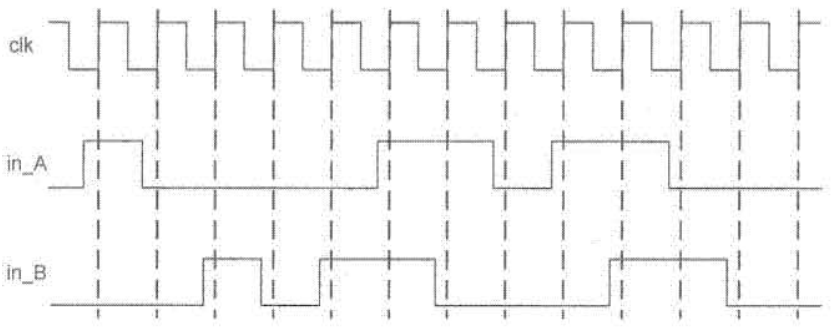


Figure 1.2

2. The rotation mode of the CORDIC algorithm is described by the following iterative equations where the vector (x_i, y_i) is rotated through the angle α_i to obtain the scaled vector (x_{i+1}, y_{i+1}). z_i and z_{i+1} are angular variables for the i[th] iteration.

$$x_{i+1} = x_i - y_i \tan\alpha_i$$
$$y_{i+1} = y_i + x_i \tan\alpha_i$$
$$z_{i+1} = z_i - \alpha_i$$

Figure 2.1 shows a table of arctan values relevant to the CORDIC algorithm

a) Explain how the CORDIC algorithm may be employed to evaluate sin α and cos α where α = 47.163°. Illustrate your answer by considering the angle of rotation over 10 iterations.

[12 Marks]

b) Design in the form of block diagram a CORDIC module to evaluate sin α and cos α.

[8 Marks]

k	$\tan^{-1}(k)$ (degrees)
1	45.000
0.5	26.565
0.25	14.036
0.125	7.125
0.0625	3.576
0.03125	1.790
0.015625	0.895
0.007813	0.448
0.003906	0.224
0.001953	0.112

Figure 2.1

3. a) What is the meaning and function of a 'parity bit' in connection with storage of digital information in memory?

[2 marks]

b) Show how to correct single bit errors in data storage by adding a number of parity check bits to the data being stored. If N check bits are added, how many data bits is it possible to protect against single-bit errors? Illustrate your answer using 4-bit data as an example.

[3 marks]

c) Figure 3.1 shows an error-correcting memory module that can correct single bit error in the data `D7:0`. The signal *ERROR* at the output is high when an error is detected and low otherwise.

i) Design the parity bit generator circuit in the form of Boolean equations.

[5 marks]

ii) Design the parity checking circuit and the error correction circuit. Demonstrate that your design works properly with the example `D7:0` = 10100011 where an error has occurred in D2 within the memory module. Gate level design is not required.

[10 marks]

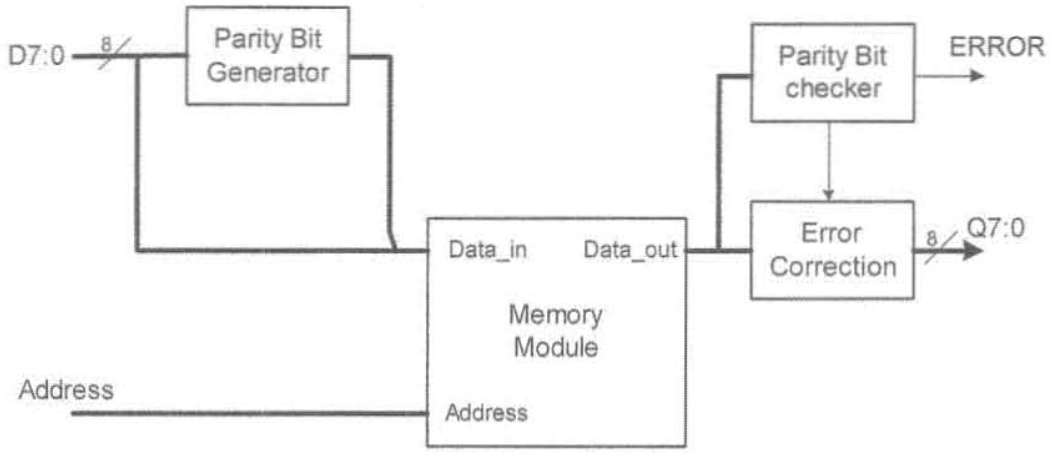


Figure 3.1

4. *Figure 4.1* shows a microprocessor connected to a 16M x 32 bit SDRAM module through an address decoder and an interface circuit. The timing of the microprocessor and the SDRAM for reading a burst of four memory words is shown in *Figure 4.2*. The address bus `A31:0` becomes valid and the address strobe signal $\overline{AS}$ is asserted at time `B` after the rising edge of the clock signal `CLK` during the clock cycle T0. The period of the clock is `A`. At time `C` after $\overline{AS}$ is asserted, the address decoder circuit produces a chip select signal $\overline{CS}$, which is asserted low for addresses in the range \$00000000 to \$00FFFFFF provided that $\overline{AS}$ is also low. The row address strobe signal $\overline{RAS}$ and the column address strobe signal $\overline{CAS}$ are asserted by the SDRAM interface circuit for one clock cycle on the falling edge of the clock during T1 and T4 respectively. The data from the SDRAM becomes valid just before the third clock cycle after $\overline{CAS}$ is asserted.

The microprocessor reads four consecutive words from SDRAM on the rising edge of the clock if the $\overline{DTACK}$ signal is sampled low.

Design the address decoder and the SDRAM interface circuit to generate $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{DTACK}$ and the memory address bus signals `AD11:0` where the output timing is as specified in Figure 4.2. State the relationship between the time periods `A`, `B` and `C`, and any other constraints or assumptions under which your design is valid.

[20 marks]

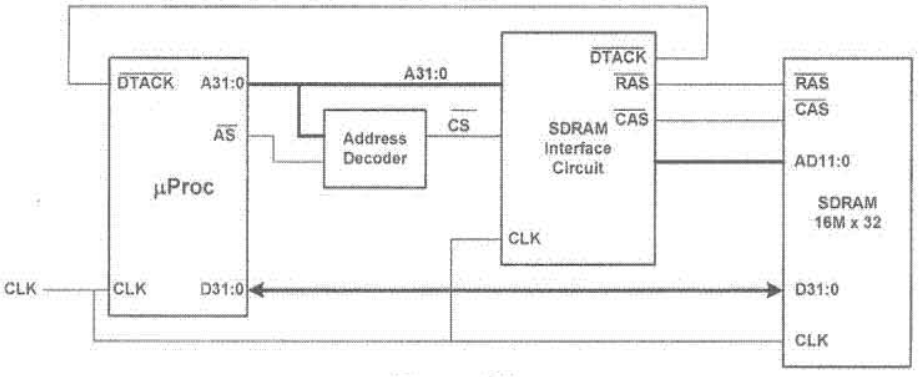


Figure 4.1

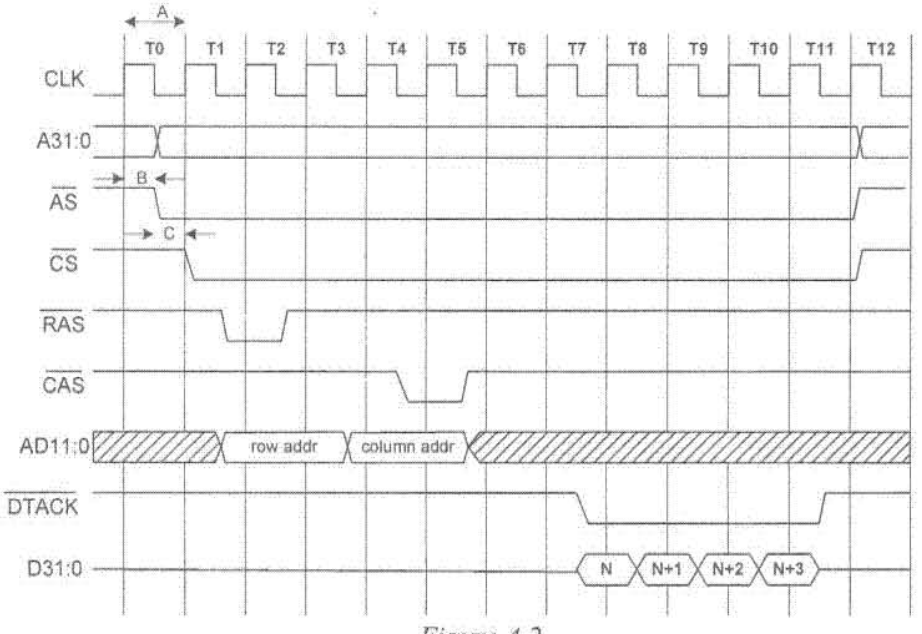


Figure 4.2

5. *Figure 5.1* shows an averaging circuit that computes the average of every four consecutive samples of an eight bit data stream *data_in* according to the equation:

$$y(n) = \frac{x(4n) + x(4n+1) + x(4n+2) + x(4n+3)}{4}$$

where fractional values are rounded down to the nearest integer.

The input samples are clocked into the circuit at an input sample rate of 40 MHz. The averaged output is produced on *data_out* at 10 MHz as shown in *Figure 5.2* shortly after the rising edge of the output clock signal *clk_out* which is derived from the system clock *clk*.

Using adders, counters, registers and any other logic gates, design the averaging circuit. You may assume that the input-to-output delay of the adder is 10 ns. The *data_in* signals are valid 3 ns before the rising edge of the clock. The propagation delays of all other gates, the clock-to-Q delay and the set-up times of flip-flops are all 2 ns. The hold-times of flip-flops are 0 ns. Verify that your circuit would work at 40MHz.

[20 marks]

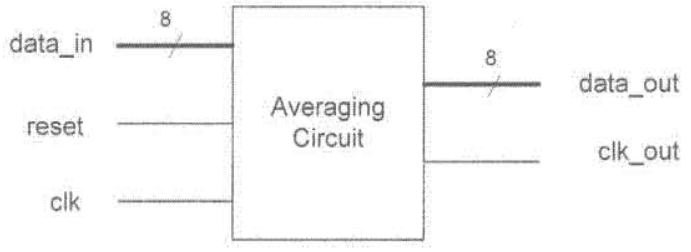


Figure 5.1

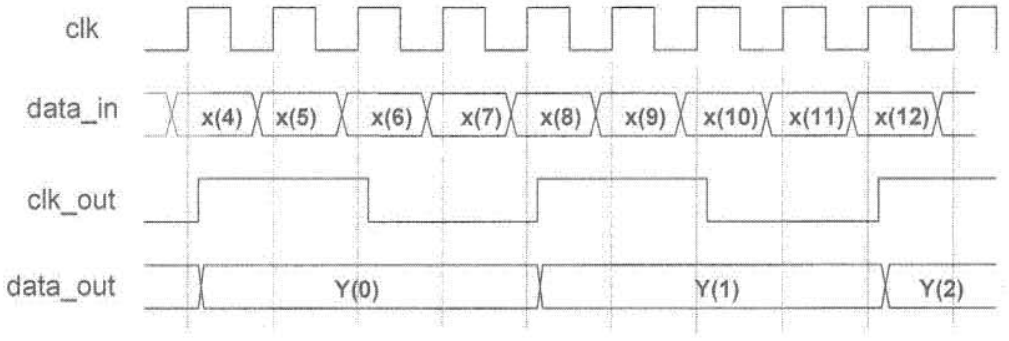


Figure 5.2

6. Given that x is an N-bit signed 2's complement number, the following equation applies:

$$x = \sum_{j=0}^{N/2-1} 2^{2j}(-2x_{2j+1} + x_{2j} + x_{2j-1}) \qquad \text{where } x_{-1} = 0, \text{ and for } i \geq 0,\ x_i \text{ is bit } i \text{ of } x.$$

Using an 8-bit binary adder, a 13-bit register, a 6-input multiplexer, and any additional gates required, design a circuit that multiplies two 6-bit 2's complement signed numbers in three clock cycles to give a 12-bit 2's complement answer. Draw a timing diagram showing the control signals required for your circuit.

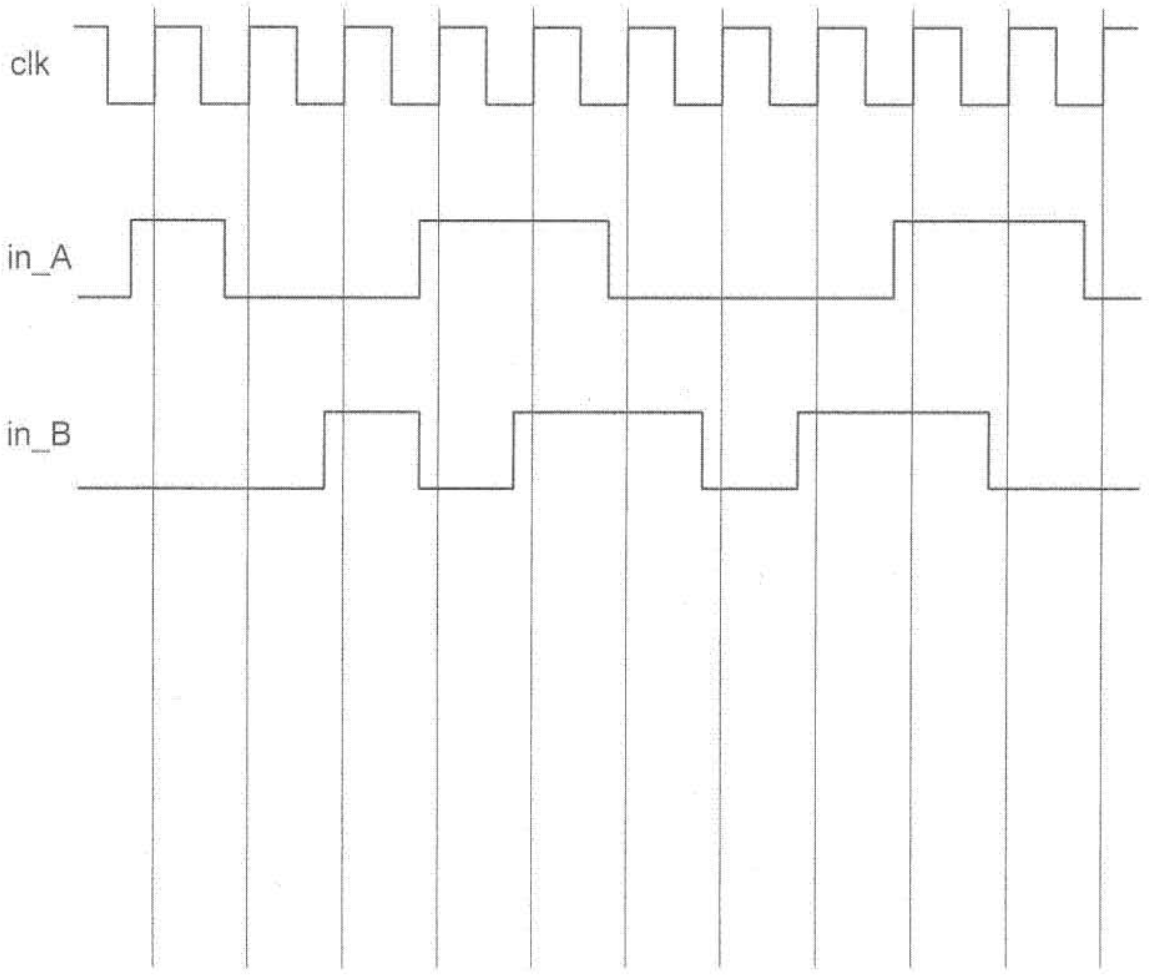
[15 marks]

Given that the propagation delays of the various components are as follows: MUX – 1ns; adder – 1ns per bit; register – 1ns; XOR/XNOR gate – 2ns; any other gates – 1ns; and that the data set-up time for the register is 1.5ns, derive the maximum possible clock frequency for your circuit. State any further assumptions you make.

[5 marks]

[END]

Timing Diagram Template for Question 1



(If you use this template, please make sure that you attach it with your answer book.)

Candidate Number: _____