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IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2008

MSc and EEE PART IV: MEng and ACGI

HIGH PERFORMANCE ANALOGUE ELECTRONICS

Thursday, 15 May 10:00 am

Time allowed: 3:00 hours

Corrected Copy
None

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : E. Rodriguez-Villegas
Second Marker(s) : D.G. Haigh

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The Questions

1.

(a) Two sine waves of frequencies w_0 and w_1 are connected to two inputs of a mixer. Using the relevant mathematics, show exactly what signal will be produced at the output. Describe how the output would change if one of the sine waves were replaced with a bandlimited signal

[4]

(b) Explain the need for "mixing" between carrier and modulating signal

[4]

(c) Which block would you normally tune to select different RF channels?

[4]

(d) What are the advantages and disadvantages of a double super heterodyne receiver versus a simple heterodyne receiver?

[4]

(e) What is a direct conversion receiver? What are its main advantage and disadvantage?

[4]

2. (a) Figure 2.1 represents the block diagram of what type of system?

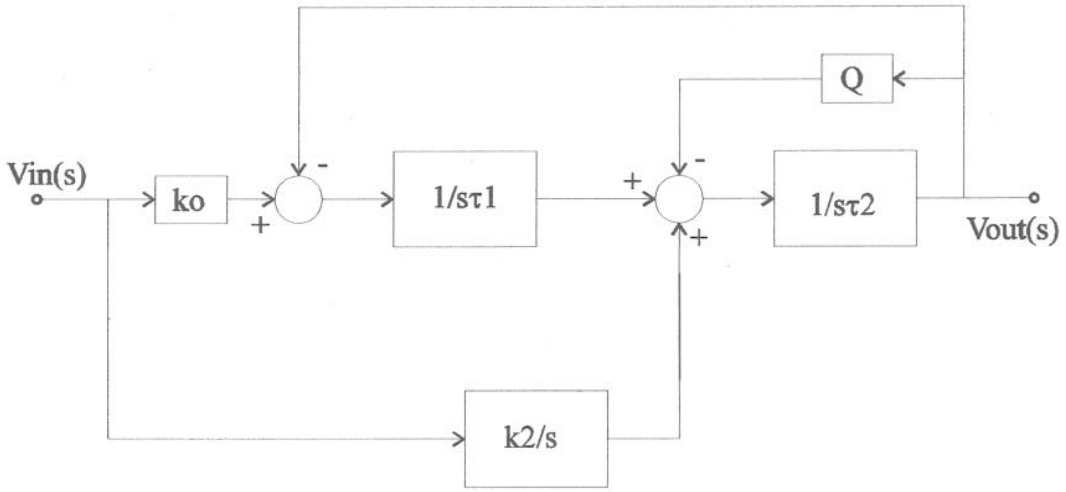

Figure 2.1

[6]

(b) Give the names of the building blocks that are required to implement the system in Figure 2.1.

[2]

(c) Draw a possible implementation for the integrator in Figure 2.1.

[3]

(d) In not more than 5 lines, what are the advantages and disadvantages of the block implementation that you chose?

[5]

(e) How would you modify the previous block diagram to implement a bandpass filter? Draw a block diagram for this filter.

[4]

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3. (a) Figure 3.1 shows the schematic and equivalent symbol of a FGMOS transistor. Ignoring parasitic effects and assuming that the capacitors connected to the floating gate have value C_i (for $i=[1,N]$), the voltage at the floating gate is given by:

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i$$

where C_T is the total capacitance seen by the floating gate.

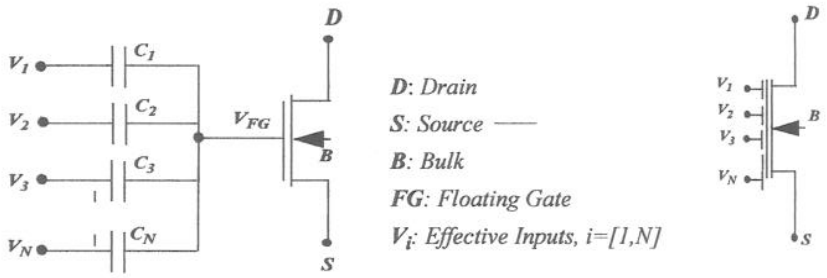


Figure 3.1

Neglecting second order effects, the current in a FGMOS transistor in strong inversion saturation region is given by:

$$I \approx \beta \left(\sum_{i=1}^{N} \frac{C_i}{C_T} V_i - V_T \right)^2$$

where all the parameters have their usual meaning. Based on this find the output current, I_{out} for the circuit in Figure 3.2 as a function of β, $(V_{i+}-V_{i-})$ and I_{bias}, knowing that:

- All the input capacitances have the same value: $0.5C_T$, except for those connected to V_{i+} and V_{i-} in M3, which are $0.25C_T$.
- All the transistors are assumed to be identical, with equal values of β and V_T.

(**Note**: It is useful to express the input voltages as the sum of a common mode component ($V_{CM}=(V_{i+}+V_{i-})/2$) and a differential mode component ($V_{in}=(V_{i+}-V_{i-})$)

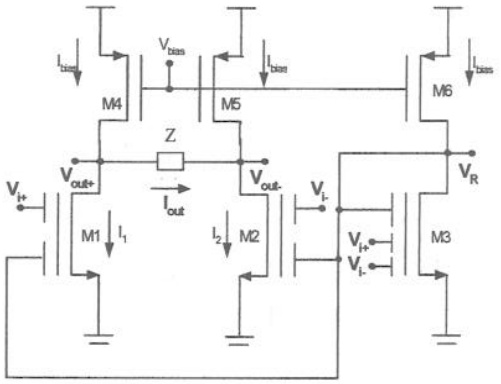


Figure 3.2

[10]

(b) If the gate to drain parasitic capacitance, $C_{GD,}$ is taken into account, the expression for the voltage at the floating gate is:

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{GD}}{C_T} V_D .$$

Knowing that the output resistance of the previous circuit is dominated by the output resistance of the FGMOS transistor, i.e.,

$$R_{out} \approx \frac{1}{g_{ds(M1)}} \approx \left(\frac{\partial I_1}{\partial V_{out+}} \right)^{-1}$$

find an expression for the output resistance of the circuit in Figure 3.2, as a function of C_{GD}, C_T, β and I_{bias}, assuming that the transistors are in the strong inversion saturation region.

[5]

(c) How would you improve the output resistance of the circuit in Figure 3.2?

[5]

4. Figure 4.1 represents a MOS differential pair. Using the following simplified expressions for the currents in strong and weak inversion:

$$I_D = \beta(V_{GS} - V_T)^2$$

$$I_D = I_o exp\left(\frac{V_{GS}}{nU_T}\right)$$

(a) Find an expression for the output current (I_{out}=I_{d1}-I_{d2}) when the transistors are operating in: a) strong inversion. b) weak inversion.

[10]

(b) Using the differential pair as the basic building block, draw the circuit diagram for a mixer.

[5]

(c) Explain what could you do to improve the dynamic range of the mixer.

[5]

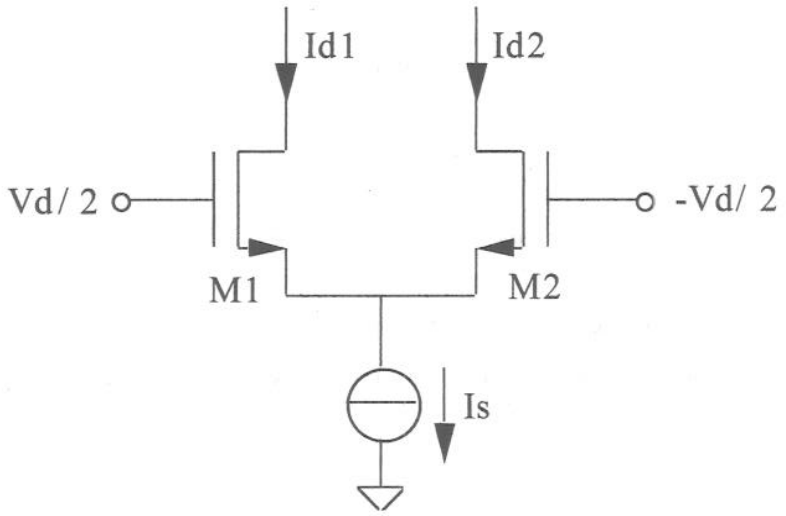


Figure 4.1

5. (a) Explain very briefly the causes of different noise sources in a MOS transistor and give expressions for them.

[5]

(b) Draw a small signal model for a MOS transistor including all the noise sources. Find an expression for the equivalent noise at the input.

[5]

(c) Find an expression for the equivalent noise at the input (V_{in}) of the circuit in Figure 5.1, where V_i (for $i=[2,N]$) are constant voltages. You can neglect shot noise.

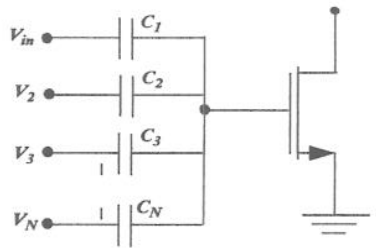
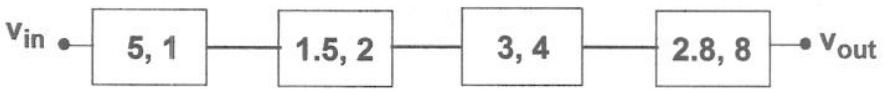


Figure 5.1

[5]

(d) Find the noise figure for the system in Figure 5.2. For each block the number on the left represents its gain and the number on the right its noise figure.



[5]

6. Figure 6.1 shows the schematic and equivalent symbol of a FGMOS transistor. Ignoring parasitic effects and assuming that the capacitors connected to the floating gate have a value C_i (for $i=[1,N]$), the voltage at the floating gate is given by:

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i$$

where C_T is the total capacitance seen by the floating gate.

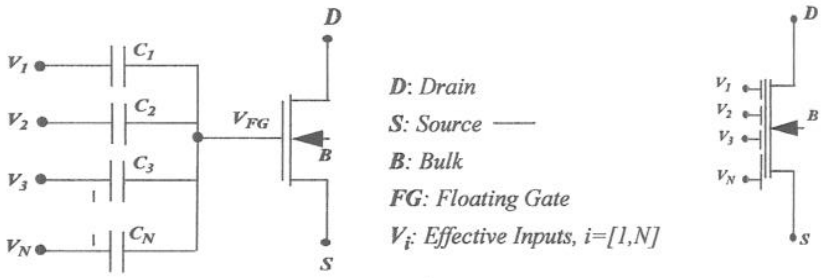


Figure 6.1

Neglecting second order effects, the current in a FGMOS transistor in weak inversion saturation region is given by:

$$I \approx Is\exp(V_{FG}/(nU_T))$$

where all the parameters have their usual meaning. Based on this:

(a) Find an expression for the current of a FGMOS transistor operating in the weak inversion saturation region as a function of I_S, C_i (for $i=[1,N]$), C_T, n, U_T and V_i (for $i=[1,N]$).

[4]

(b) Find the output current, I_{out} for the circuit in Figure 6.2 as a function of n, U_T, $V_{in}=(V_{i+}-V_{i-})$ and I_{bias}, knowing that:

- All the input capacitances have the same value: $0.5C_T$, except for those connected to V_{i+} and V_{i-} in M3, which are $0.25C_T$.
- All the transistors are assumed to be identical, this is equal n, U_T and I_S.

(**Note**: It is useful to express the inputs as the sum of a common mode component ($V_{CM}=(V_{i+}+V_{i-})/2$) and a differential mode component ($V_{in}=(V_{i+}-V_{i-})$)

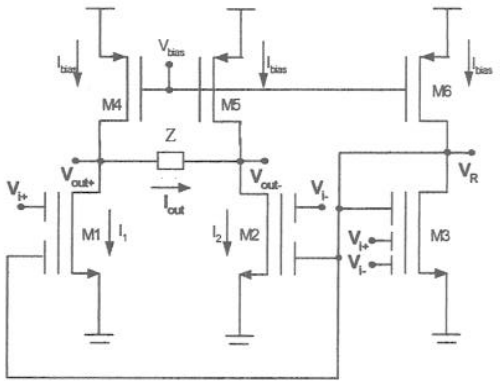


Figure 6.2

[4]

(c) What would be the output current of the circuit in Figure 6.2 if MOS transistors were used instead?

[4]

(d) The output current of the circuit in Figure 6.2 is a non-linear function of V_{in}. Find the third order term in a Taylor expansion of the output current equation. Based on your result: how does using FGMOS devices (instead of MOS) improve the linearity of the circuit?

[4]

(e) How would you modify the FGMOS transistors in the transconductor of Figure 6.2 to have an extra input terminal.

[4]