E3.11
E4.42
AO8

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2009

MSc and EEE PART III/IV: MEng, BEng.and ACGI

Corrected Copy · Page 2

ADVANCED ELECTRONIC DEVICES

Friday, 8 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer Question One and FOUR other questions.

All questions carry equal marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	K. Fobelets, K. Fobelets
	Second Marker(s) :	W.T. Pike, W.T. Pike

Special instructions for invigilators

Q1 is Compulsory

Special instructions for students

Q1 is Compulsory

Constants and Formulae

permittivity of free space:	$\varepsilon_o = 8.85 \times 10^{-12}$ F/m
permeability of free space:	$\mu_o = 4\pi \times 10^{-7}$ H/m
intrinsic carrier concentration in Si:	$n_{i\,Si} = 1.45 \times 10^{10}$ cm^{-3} at $T = 300$K
intrinsic carrier concentration in GaAs:	$n_{i\,GaAs} = 2.1 \times 10^{6}$ cm^{-3} at $T = 300$K
intrinsic carrier concentration in $Al_{0.3}Ga_{0.7}As$:	$n_{i\,AlGaAs} = 2.1 \times 10^{3}$ cm^{-3} at $T = 300$K
dielectric constant of Si:	$\varepsilon_{Si} = 11.8$
dielectric constant of SiO_2:	$\varepsilon_{ox} = 4$
dielectric constant of GaAs:	$\varepsilon_{GaAs} = 12.9$
dielectric constant of AlAs:	$\varepsilon_{AlAs} = 10.1$
electron affinity of GaAs	$\chi_{GaAs} = 4.07$ eV
electron affinity of AlAs	$\chi_{AlAs} = 3.03$ eV
effective density of states of GaAs	$N_{C\,GaAs} = 4.7 \times 10^{17}$ cm^{-3}
	$N_{V\,GaAs} = 9.0 \times 10^{18}$ cm^{-3}
effective density of states of $Al_{0.3}Ga_{0.7}As$	$N_{C\,AlGaAs} = 6.5 \times 10^{17}$ cm^{-3}
	$N_{V\,AlGaAs} = 1.1 \times 10^{19}$ cm^{-3}
bandgap GaAs	$E_{g\,GaAs} = 1.42$ eV
bandgap AlAs	$E_{g\,AlAs} = 2.67$ eV
thermal voltage:	$kT/e = 0.026$V at $T = 300$K
charge of an electron:	$e = 1.6 \times 10^{-19}$ C

$$I_{DS} = \frac{\mu C_{ox} W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

MOSFET current

$$V_{th} = \phi_m - \phi_s + 2\left[\frac{\sqrt{eN_A \varepsilon kT \ln\left(\frac{N_A}{n_i}\right)}}{C_{ox}} + \frac{kT}{e}\ln\left(\frac{N_A}{n_i}\right)\right]$$

Threshold voltage

$$J = \frac{eD_n n_p}{L_n}\left(e^{\frac{eV}{kT}} - 1\right) + \frac{eD_p p_n}{L_p}\left(e^{\frac{eV}{kT}} - 1\right)$$

Diode diffusion current density

$$V_0 = \frac{kT}{e}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Built-in voltage

$$W_{depl}(V) = \left[\frac{2\varepsilon(V_0 - V)}{e}\frac{N_A + N_D}{N_A N_D}\right]^{1/2}$$

Depletion width in pn diode

$$\phi_F = \frac{kT}{e}\ln\left(\frac{N_A}{n_i}\right)$$

Difference between intrinsic level E_i and Fermi level E_F.

$$p = N_v e^{(E_v - E_F)/kT} \text{ and } p_i = N_v e^{(E_v - E_i)/kT}$$

$$n = N_c e^{(E_F - E_c)/kT} \text{ and } n_i = N_c e^{(E_i - E_c)/kT}$$

Carrier density

1. This question is compulsory.

   a. Give three different methods to gate a field effect transistor. [3]

   b. Is the mobility of the electrons in the channel of an AlGaAs/GaAs HEMT higher or lower than in a GaAs MESFET. Give a brief explanation. [3]

   c. What happens (↑increases, ↓decreases or = remains the same) to the following performance parameters when the gate length of the MOSFET is reduced from 1mm to 100nm while all the other geometrical and material parameters remain the same? [4]
   Threshold voltage, V_{th}
   Sub-threshold slope, S
   Drain induced barrier lowering, $DIBL$
   Off current, I_{off}

   d. Why is the current below the threshold voltage of a MOSFET non-zero? [4]

   e. What is the influence of the interface state density on the gating action of a MESFET? [3]

   f. Give three reasons why CMOS on SOI is faster and has lower power consumption that CMOS on bulk Si. [3]

   g. For what type of surface channel Si MOSFET is the introduction of tensile strain increasing the carrier mobility in the channel (n or p)? Give two reasons for the mobility increase. [3]

   h. Why do the sub-threshold slope, S and drain induced barrier lowering, DIBL improve in finFETs? [4]
   Give a brief explanation for each.

   i. Give three methods to fabricate Si nanowires. [3]

2.

a. Explain how a SOI (silicon on insulator) substrate is prepared using the smart cut technique. Use sketches to illustrate your explanation. [5]

b. In an n-type MOSFET on partially depleted (PD) SOI, with source and bulk connected to ground, a neutral region exists.
   i) Is this neutral region n-doped, p-doped or depleted? [2]
   ii) Does the top gate control all charges in this neutral region? [2]
   iii) What effect does this neutral region have on the output characteristics (I_{DS}-V_{DS}) of the MOSFET at high drain voltages? Give a sketch of I_{DS}-V_{DS} to illustrate your explanation. [4]
   iv) Suggest a method to improve the performance in the given device. [2]

c. Sketch the energy band diagram (E_c, E_v, E_F) from gate to bottom of the substrate of a PD nMOS on SOI. The biasing conditions are: top gate voltage $V_{GS} > V_{th} > 0V$ (threshold voltage) and the substrate is grounded. Assume that the gate metal workfunction is smaller than that of p-Si and that the substrate is p-type. [5]

d. Under the assumption that the energy bands are flat band when no voltages are applied, calculate the minimum thickness of the SOI Si body for partially depleted operation. The doping density in the Si body is $N_A = 10^{16}\ cm^{-3}$, the substrate voltage remains connected to ground during operation and the temperature is $T=300K$. [10]

3. Figure 3.1 gives the variation of the value of the bandgap as a function of the lattice constant of different semiconductor alloys.

a.

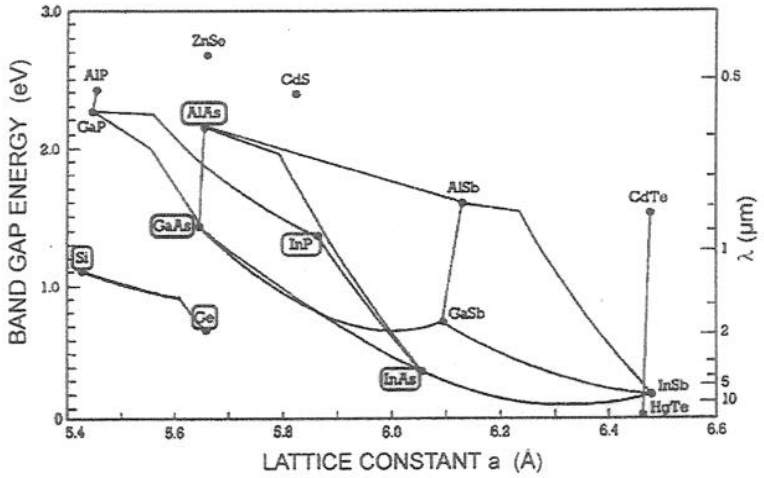


Figure 3.1: The energy band gap as a function of the lattice spacing of different semiconductors and semiconductor alloys.

i) Give the value of the bandgap of GaAs and AlAs. [1]
ii) Give the general expression for the band gap of $Al_xGa_{1-x}As$ and calculate the value of the bandgap of $Al_{0.3}Ga_{0.7}As$. [3]
iii) Estimate the bandgap of $AlSb_{0.5}As_{0.5}$. [2]
iv) Estimate the value of the stress in AlSb when grown on AlAs. [2]
v) Why might Ge be grown successfully on GaAs? [2]

b. Figure 3.2 gives a sketch of the energy band diagram for two semiconductors that are in contact and without external bias.

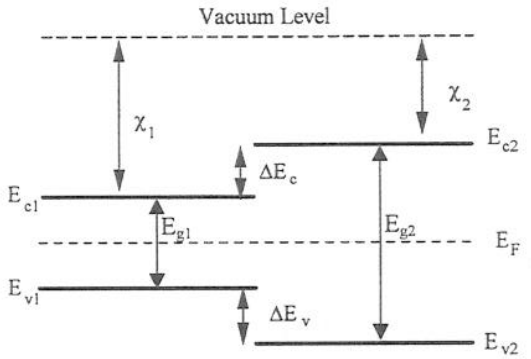


Figure 3.2: Schematic energy band diagram relative to the vacuum level of a small and large bandgap material at contact.

i) Give the type of doping in both materials [2]
ii) Give the expression for the conduction band offset ΔE_c by applying the electron affinity rule. [2]
iii) Give the expression for the valence band offset ΔE_v. [2]

c. Draw the energy band diagram of a heterojunction composed of p-type GaAs and n-type $Al_{0.3}Ga_{0.7}As$. The material parameters are given in the formulae list. The doping density is $N_A = 5\ 10^{17}\ cm^{-3}$ and $N_D = 10^{18}\ cm^{-3}$. Calculate all the values of the difference in energy between the different energy levels E_G, E_C, E_V, ΔE_C, ΔE_V and the Fermi level E_F in both materials and at the junction. [10]

d. Why is an undoped set-back layer used between the AlGaAs doping layer and the GaAs layer in a HEMT? [4]

4. A Medici input file is given in fig. 4.1. The questions on this input file are given on the next page 7.

```
TITLE   INTERESTING DEVICE

MESH

X.MESH x.min=0.00   x.max=0.04   h1=0.010
X.MESH x.min=0.04   x.max=0.20   h1=0.001
X.MESH x.min=0.20   x.max=0.24   h1=0.010

Y.MESH y.min=0.00   y.max=0.054   h1=0.001

REGION  num=1 x.min=0.00 x.max=0.240  y.min=0.002 y.max=0.052 silicon
REGION  num=2 x.min=0.00 x.max=0.240  y.min=0.000 y.max=0.002 s.oxide
REGION  num=3 x.min=0.00 x.max=0.240  y.min=0.052 y.max=0.054 s.oxide

ELECTR  name=source x.min=0.00 x.max=0.00 y.min=0.00 y.max=0.054
ELECTR  name=drain  x.min=0.24 x.max=0.24 y.min=0.00 y.max=0.054

ELECTR  name=gate x.min=0.05  x.max=0.10 y.min=0.000 y.max=0.000
ELECTR  name=gate x.min=0.05  x.max=0.10 y.min=0.054 y.max=0.054

ELECTR  name=gate x.min=0.140  x.max=0.190 y.min=0.000 y.max=0.000
ELECTR  name=gate x.min=0.140  x.max=0.190 y.min=0.054 y.max=0.054

PROFILE  x.min=0.00 x.max=0.05 Y.MIN=0.00 Y.MAX=0.054
+       N-TYPE  N.PEAK=1.e19  UNIFORM

PROFILE  x.min=0.190 x.max=0.240 Y.MIN=0.00 Y.MAX=0.054
+       N-TYPE  N.PEAK=1.e19  UNIFORM

PROFILE  x.min=0.050 x.max=0.190 Y.MIN=0.00 Y.MAX=0.054
+       P-TYPE  N.PEAK=5.e15  UNIFORM

CONTACT  name=gate PRINT ALUMINUM

MODELS  CONMOB E.EFFECT TEMPERAT=300. PRINT

SYMBOLIC GUMMEL CARRIERS=2  ELECTRON   HOLES
METHOD  ITLIMIT=20
SOLVE   V(drain)=0.000  V(gate)=0.00

SYMBOLIC NEWTON  CARRIERS=2  ELECTRON   HOLES
MODELS ANALYTIC E.EFFECT  TEMPERAT=300. PRINT
SOLVE   V(drain)=0.0   V(gate)=0.00

SOLVE  ELEC=drain   VSTEP=0.02 NSTEP=5 PROJECT
SOLVE  ELEC=gate    VSTEP=0.02 NSTEP=50 PROJECT

LOG IVFILE=outputfile

LOOP STEPS=90
SOLVE  ELEC=gate  VSTEP=-0.02  NSTEP=1  PROJECT
L.END
```

Figure 4.1: A MEDICI input file.

Question continues on next page!

a. Draw the geometrical structure of the device defined in the MEDICI input file given in fig. 4.1. Include all semiconductor regions (material type and doping type) and contact regions, add dimensions for each region. [20]

b. What type of device does this file represent? [4]

c. What type of data is saved in "outputfile" in the command line:
LOG IVFILE=outputfile? [3]

d. Which command line do you need to use to change the temperature of the calculations? [3]

5. Fig. 5.1 shows a schematic diagram of a double gated MOSFET. The source is at the left and the drain at the right of the structure. The gates are independently gated with gate voltages V_{G1} and V_{G2}. The gate oxide thickness is the same for both gates. The gate metal is the same for both gates and the workfunction of the metal is equal to the workfunction of the p-Si. The p-type Si body is not depleted when $V_{GS1} = V_{GS2} = 0$ V. V_S is grounded.

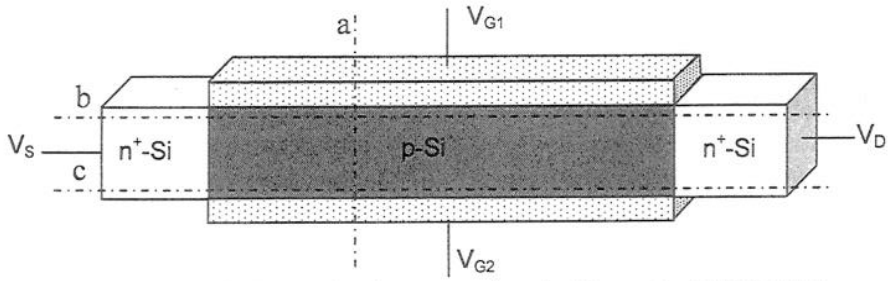


Figure 5.1: Schematic diagram of a double gated MOSFET.

a. Sketch the energy band diagram through the gates along the line "a". All bias voltages are zero. [5]

b. Sketch the energy band diagram through the gates along the line "a". Now the bias condition is: $V_S = V_D = 0$ V. $V_{GS1} > 0$ V and $V_{GS2} < 0$ V. [5]

c. Sketch the energy band diagram from source to drain along the line "b". The bias is as in 5b: $V_S = V_D = 0$ V. $V_{GS1} > 0$ V and $V_{GS2} < 0$ V. [5]

d. Sketch the energy band diagram from source to drain along the line "c". The bias is as in 5b: $V_S = V_D = 0$ V. $V_{GS1} > 0$ V and $V_{GS2} < 0$ V. [5]

e. How many possible electron channels does this device have under the given bias conditions? [5]

f. Will there be electron flow from source to drain and hole flow from drain to source when the gate bias is as in 5b and a positive voltage is applied on the drain $V_D > 0$ V, $V_S = 0$ V? Explain briefly. [5]

6. Figure 6.1 gives the extracts of the Medici input files you were given for your coursework.

```
1... TITLE Synopsys MEDICI Example 1 - 1.5 Micron N-Channel MOSFET
2... MESH SMOOTH=1
3... X.MESH WIDTH=3.0 H1=0.125
4... Y.MESH N=1 L=-0.025
5... Y.MESH N=3 L=0.
6... Y.MESH DEPTH=1.0 H1=0.125
7... Y.MESH DEPTH=1.0 H1=0.250
8... ELIMIN COLUMNS Y.MIN=1.1
9... SPREAD LEFT WIDTH=.625 UP=1 LO=3 THICK=.1 ENC=2
10... SPREAD RIGHT WIDTH=.625 UP=1 LO=3 THICK=.1 ENC=2
11... SPREAD LEFT WIDTH=100 UP=3 LO=4 Y.LO=0.125
12... REGION SILICON
13... REGION OXIDE IY.MAX=3
14... ELECTR NAME=Gate X.MIN=0.625 X.MAX=2.375 TOP
15... ELECTR NAME=Substrate BOTTOM
16... ELECTR NAME=Source X.MAX=0.5 IY.MAX=3
17... ELECTR NAME=Drain X.MIN=2.5 IY.MAX=3
18... PROFILE P-TYPE N.PEAK=3E15 UNIFORM OUT.FILE=MDEX1DS
19... PROFILE P-TYPE N.PEAK=2E16 Y.CHAR=.25
20... PROFILE N-TYPE N.PEAK=2E20 Y.JUNC=.34 X.MIN=0.0 WIDTH=.5 XY.RAT=.75
21... PROFILE N-TYPE N.PEAK=2E20 Y.JUNC=.34 X.MIN=2.5 WIDTH=.5 XY.RAT=.75
22... CONTACT NAME=Gate N.POLY


23... TITLE Synopsys MEDICI Example 1G - 1.5 Micron N-Channel MOSFET
24... MESH IN.FILE=MDEX1MS
25... SYMB NEWTON CARRIERS=1 ELECTRONS
26... LOG OUT.FILE=MDEX1GI
27... SOLVE V(Drain)=.1
28... SOLVE V(Gate)=.2 ELEC=Gate VSTEP=.2 NSTEP=9

29... TITLE Synopsys MEDICI Example 1D - 1.5 Micron N-Channel MOSFET
30... MESH IN.FILE=MDEX1MS
31... SYMB CARRIERS=0
32... METHOD ICCG DAMPED
33... SOLVE V(Gate)=3.0
34... SYMB NEWTON CARRIERS=1 ELECTRON
35... LOG OUT.FILE=MDEX1DI
36... SOLVE V(Drain)=0.0 ELEC=Drain VSTEP=.2 NSTEP=15
```

Figure 6.1 Extract of the coursework input files

a. Give the thickness of the oxide in the MOSFET defined in the input file of fig. 6.1. [4]

b. What is the effect of the function SPREAD (see lines 9 – 11)? [4]

c. Which gate metal is used? [4]

d. What is the doping density in the ohmic contact regions? [4]

e. Which MOSFET characteristics are simulated when running the lines 23 – 28? [5]
Give the voltages or voltage ranges for V_{DS} and V_{GS} in this simulation.

f. Which MOSFET characteristics are simulated when running the lines 29 – 36? [5]
Give the voltages or voltage ranges for V_{DS} and V_{GS} in this simulation.

g. Are the current-voltage characteristics calculated for electrons, holes or both? [4]

Answers

1.

a. MOS gate
Shottky gate
p^+n junction gate [3]

b. Electron mobility is higher in the HEMT than the MESFET. Because HEMT is based on modulation doping. This means that the doping atoms are not in the channel region and therefore impurity scattering is reduced. Reduction of impurity scattering gives an increase in mobility: $\mu \propto \tau$ with τ average time between scattering events. [3]

c. Short channel effects: [4]

V_{th}	↓
S	↑
DIBL	↑
I_{off}	↑

d. Weak inversion region: the MOSFET behaves as a BJT and diffusion currents occur since the carrier concentration at the source side of the channel is higher than the carrier concentration at the drain side. [4]

e. The interface state density occurs between the Schottky contact and the semiconductor and is due to unfinished covalent bonds. These interface states create energy levels in the bandgap of the semiconductor that are partially filled. This imposes a new Fermi level at the surface and band bending occurs in order to equalise the Fermi levels. As a consequence the Schottky barrier height is determined by the interface states and not by the theoretical work function difference between gate metal and semiconductor. In general this causes a lowering of the Schottky barrier height (lower switch on voltage and higher leakage currents). [3]

f. BOX blocks substrate leakage currents.
Junction capacitances are reduced.
In FD SOI there is no neutral region and thus no minority carrier delay times. [3]

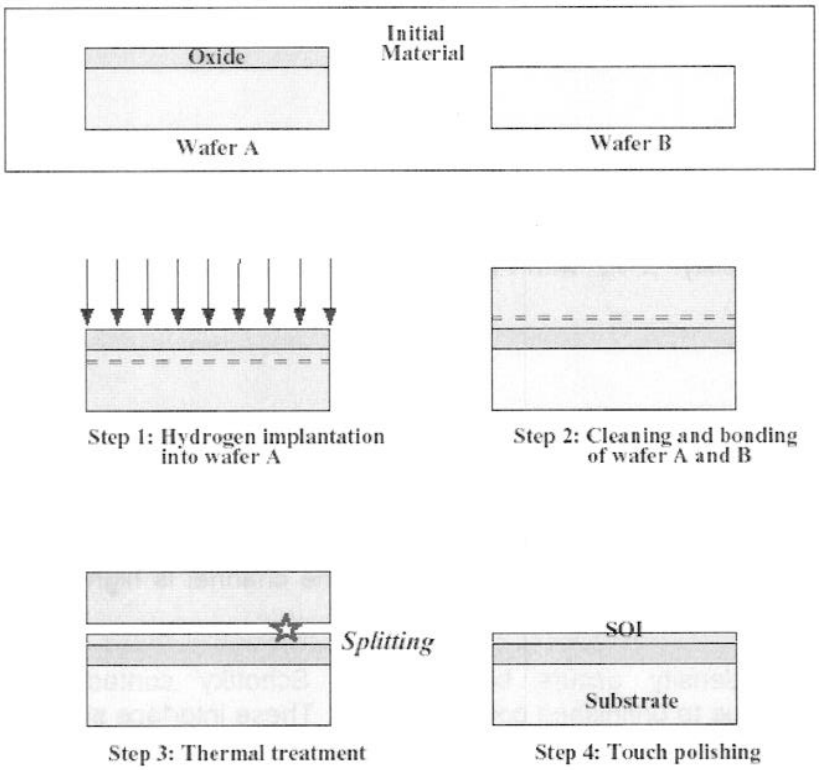
g. n-type
Electron mobility increases because phonon scattering and effective mass are reduced as a consequence of the splitting of the conduction band minima under tensile strain. [3]

h. DIBL decreases because the carriers in the channel are controlled by two gate capacitors in the finFET.
S decreases because the bulk capacitance decreases and the oxide capacitance effectively doubles. [4]

i. Epitaxial growth using Au particles as catalyst.
Wet chemical etching using Ag as catalyst.
Using anodised Al_2O_3 as templates. [3]

2.

a. [5]



Take two Si wafers. Oxidise the surface of one wafer.

Implant hydrogen into this wafer at the certain depth underneath the oxide. Clean the surfaces of the wafers and press them together. Van der Waals bonding between the surfaces will occur.

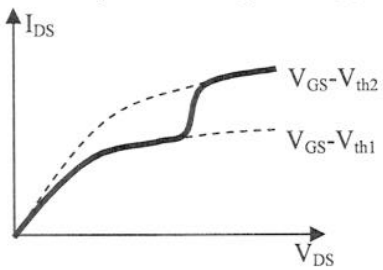
Anneal the bonded wafer and the wafer will split where the hydrogen implant has cause lattice damage. Polish the wafer with the BOX to smoothen the surface. Reuse the other wafer for a new process.

b. In an n-type MOSFET on partially depleted (PD) SOI, with source and bulk connected to ground, a neutral region exists.

i) p-doped [2]

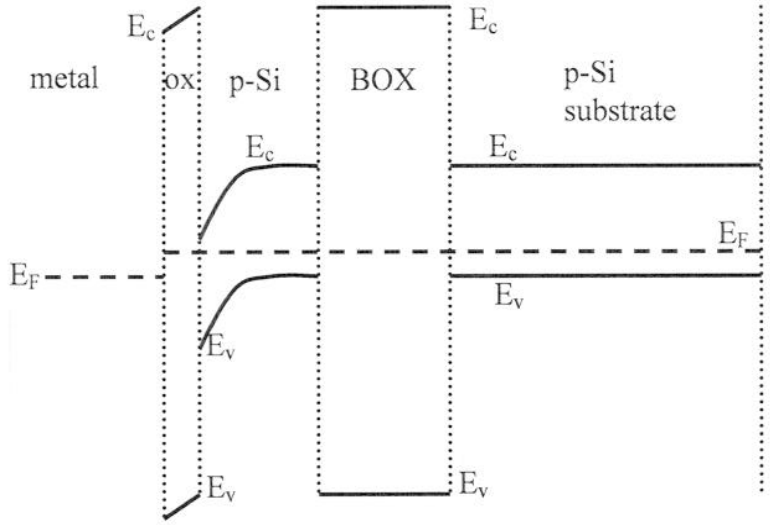
ii) No (floating region) [2]

iii) This will cause a kink effect in the I_{DS}-V_{DS} curves because of impact ionisation at high drain voltages. Holes will accumulate that the BOX surface and are trapped there, this will cause a threshold voltage shift thus the FET becomes more on than what expected for given V_{GS}. [4]



iv) Use substrate gating such that the remaining neutral (floating) region comes under the control of the BOX-Si substrate gate. Will require high voltages since the box is thick. [2]

c. [5]



d. Under the given assumptions. No band bending occurs at the BOX and no depletion is induced via a substrate voltage. Thus the minimum thickness must be larger than the maximum depletion width induced by the top gate such that a neutral region remains. See formulae list for depletion width W_{depl} and for ϕ_F: [10]

$$W_{depl}(V) = \left[\frac{2\varepsilon(V_0 - V)}{e} \frac{N_A + N_D}{N_A N_D} \right]^{1/2}$$

$$\phi_F = \frac{kT}{e} \ln\left(\frac{N_A}{n_i} \right)$$

In the given case, the built-in voltage is zero (no band bending at VGS=0V): V0=0V.
The voltage applied for creating the maximum depletion width is that needed for creating inversion. Thus $V=-2\phi_F$
Thus the expression for maximum depletion width becomes:

$$W_{depl}^{\max} = \left[\frac{4\varepsilon \frac{kT}{e} \ln\left(\frac{N_A}{n_i} \right)}{e} \frac{N_A + N_D}{N_A N_D} \right]^{1/2}$$

The situation of a MOS-gate can be approached by the one-sided junction where $N_D >> N_A$ thus the maximum depletion width becomes:

$$W_{depl}^{\max} = \left[\frac{4\varepsilon \frac{kT}{e} \ln\left(\frac{N_A}{n_i} \right)}{eN_A} \right]^{1/2} = \left[\frac{4 \times 11.8 \times 8.85\,10^{-14} \times 0.026 \times \ln\left(\frac{10^{16}}{1.45 \times 10^{10}} \right)}{1.6\,10^{-19} \times 10^{16}} \right] = 3.02\,10^{-5}\,cm = 302\,nm$$

Thus t_{Si} > 302 nm for PD S0I.

3.

a.

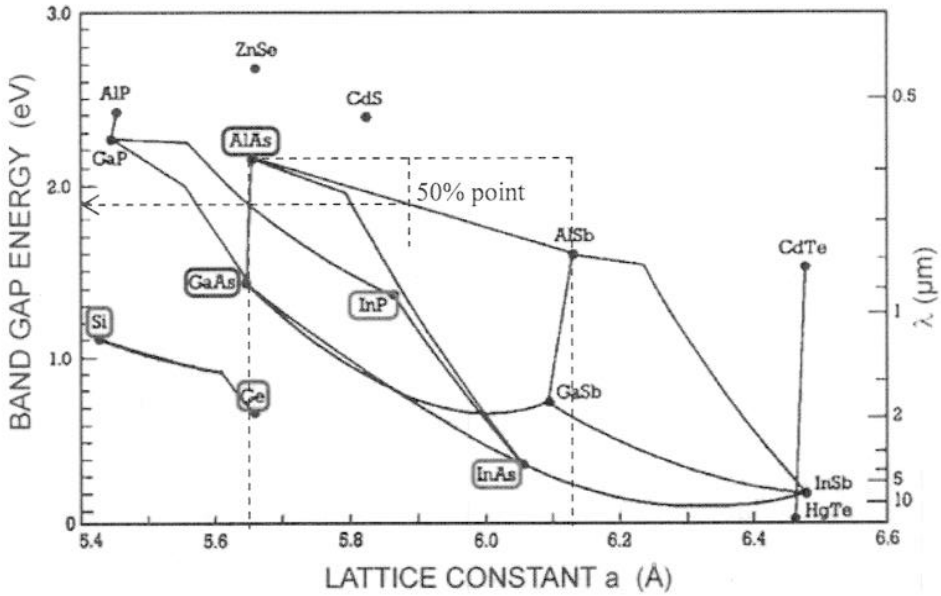


Figure 3.1: The energy band gap as a function of the lattice spacing of different semiconductors and semiconductor alloys.

i) $E_G^{GaAs} = 1.42\,eV$

$E_G^{AlAs} = 2.67\,eV$ [1]

ii) $E_G^{GaAlAs} = x \times E_G^{AlAs} + (1-x) \times E_G^{GaAs}$

$E_G^{GaAlAs}(x=0.3) = 0.4 \times 2.67\,eV + 0.7 \times 1.42\,eV = 2.06\,eV$ [3]

iii) This is halfway along the line between AlAs and AlSb given in fig. 3.1.

$E_G^{AlSbAs}(x=0.5) = 1.9\,eV$ [2]

iv) stress is given by $\varepsilon = \frac{a_2 - a_1}{a_1} = \frac{a_{AlSb} - a_{AlAs}}{a_{AlAs}} = \frac{6.12 - 5.66}{5.66} = 8.1 \times 10^{-2}$ [2]

v) yes because they have approximately the same lattice constant. [2]

b.

i) both are intrinsic, no doping, because E_F lies halfway bandgap. [2]

ii) $\chi_1 - \Delta E_c = \chi_2$ [2]

iii) $\Delta E_c + \Delta E_v = \Delta E_g = E_{g2} - E_{g1}$ or $\Delta E_v = E_{g2} - E_{g1} - \Delta E_c$ [2]

c. Distances between Fermi level and energy bands:
For GaAs.

$$p = N_A = N_v e^{(E_v - E_F)/kT}$$

$$E_F - E_v = kT \ln\left(\frac{N_v}{N_A}\right) = 0.026 \ln\left(\frac{9 \times 10^{18}}{5 \times 10^{17}}\right) = 7.5\,10^{-2}\,eV$$ [10]

$$n = N_D = N_c e^{(E_F - E_c)/kT}$$

$$E_c - E_F = kT \ln\left(\frac{N_c}{N_D}\right) = 0.026 \ln\left(\frac{5.6 \times 10^{17}}{10^{18}}\right) = -1.5\,10^{-2}\,eV$$

For AlGaAs with x=0.3

Note: negative sign means that the AlGaAs is degenerately doped.

Electron affinity:

For GaAs: χ_{GaAs}=4.07 eV

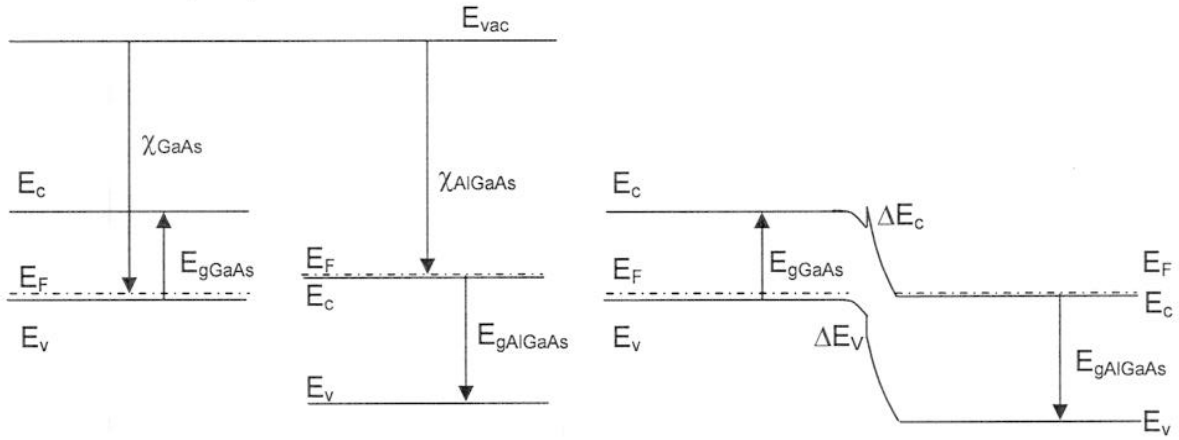
For AlGaAs, use linear interpolation:

$\chi_{AlGaAs}(x=0.3)=0.3\times\chi_{AlAs}+0.7\times\chi_{GaAs}=0.3\times3.03+0.7\times4.07=3.758\,eV$

Conduction band offset:

$\Delta E_C=\chi_{AlGaAs}-\chi_{GaAs}=3.8-4.1=-0.3$ eV

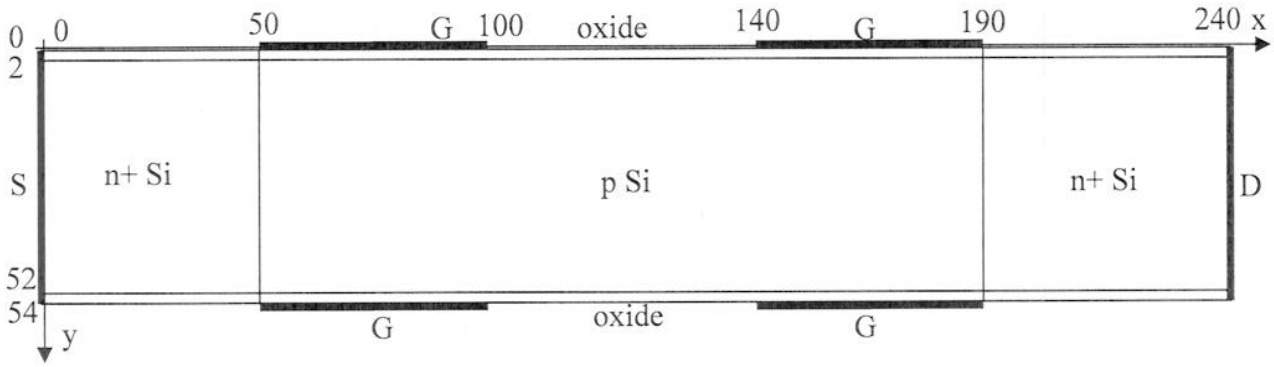
$\Delta E_v=\Delta E_G-|\Delta E_C|=2.06-1.42-0.3=0.34$ eV



d. To reduce coulomb scattering between the carriers in the channel and the ionised impurities of the doped supply layer. This increases mobility. [4]

4.

a. [20]



All dimensions are in nm. The oxide thickness is 2 nm, the gate lengths are 50 nm, the channel width is 50 nm and the channel length is 140 nm. n^+ doping is 10^{19} cm^{-3} and p doping is 10^{15} cm^{-3}.

b. It is a thin channel device with 4 gate contacts – a 4-gate thin fin MOS-gated FET. Could be the cross section of a finFET where the gate at each side is split in two. [4]

c. The data points of the transfer characteristics that are calculated in "LOOP". [3]

d. The command line on which "MODELS" are defined. [3]
MODELS CONMOB E.EFFECT **TEMPERAT=300.** PRINT

5.

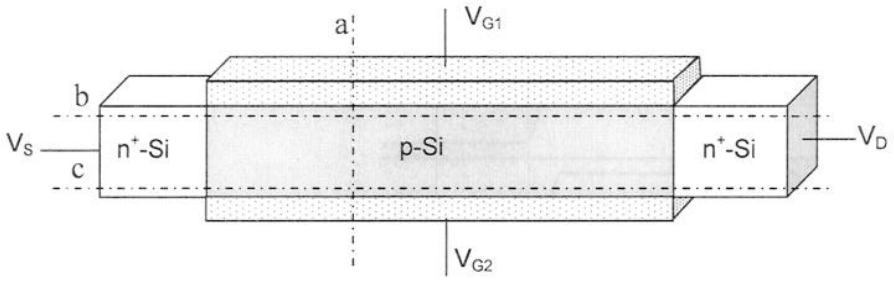
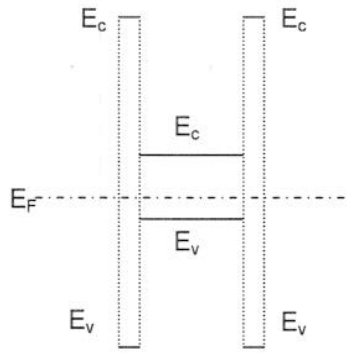
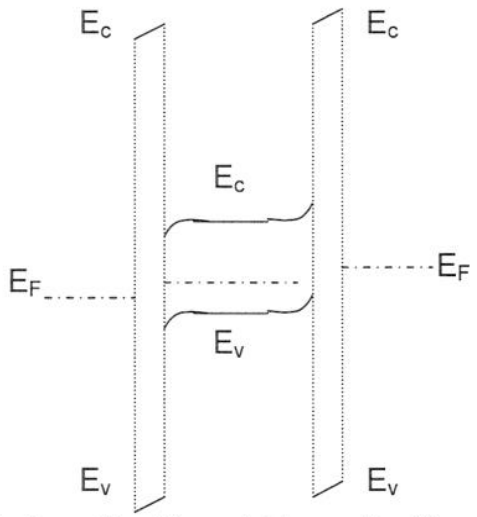


Figure 5.1: Cartoon of a double gated MOSFET. Left is the source, right the drain. Gate voltages V_{G1} and V_{G2} are applied independently. The gate oxide thickness is the same for both gates. The gate metal is the same for both gates and the workfunction of the metal is equal to the workfunction of the p-Si. The p-type Si body is not depleted when $V_{GS1}=V_{GS2}=0V$. V_S is grounded.

a. [5]

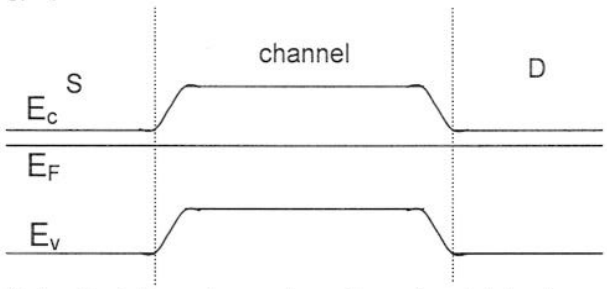


b. [5]



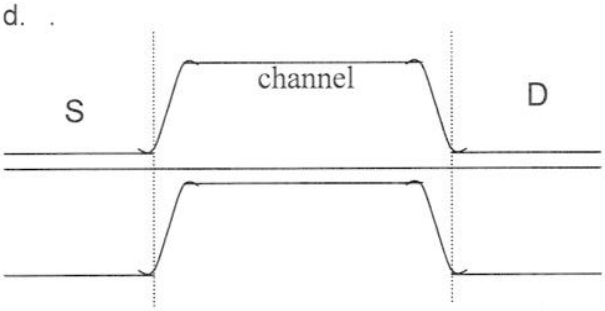
Left: positive V_{GS1}, right negative V_{GS2}.

c. . [5]



Note that the channel region should be less p-type and tending to n-type due to the applied gate voltage (hole depletion).

d. . [5]



Note that the channel region should be more p-type and tending to p^+-type due to the applied gate voltage (hole accumulation).

e. One. [5]

f. No. There will be an electron flow in the channel gated with $V_{GS1}>0$ as hole are depleted and an inverted channel made. Looking at the energy band diagram in c, we see that the source-channel potential barrier is lowered, thus allowing more electrons to cross when a drain voltage is applied.
For the other channel with $V_{GS2}<0$ there is hole accumulation and looking at the energy band diagram in d, we see that the source-channel and drain-channel potential barriers are increased, thus the holes flowing from drain into channel cannot be collected in the source and the electrons cannot cross the source-channel barrier[5]

6. Coursework Medici input files.

   a. 25 nm. [4]

   b. The SPREAD function increases separation between the grid lines to 100nm in the source and drain regions. Thus the oxide becomes thicker in those regions. [4]

   c. Aluminium [4]

   d. $N_D = 2\ 10^{20}\ cm^{-3}$ in both regions [4]

   e. The transfer characteristics (I_{DS} versus V_{GS}) for V_{DS}=0.1V and in a gate voltage range of $0.2\ V \leq V_{GS} \leq 2\ V$. [5]

   f. The output characteristics (I_{DS} versus V_{DS}) for V_{GS}=3V and in a drain voltage range of $0\ V \leq V_{GS} \leq 3\ V$.

   g. Electrons only [4]