EE3-01
EE9-AC1

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2014

MSc and EEE PART III/IV: MEng, Beng.and ACGI

Corrected Copy

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Monday, 13 January 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : P. Georgiou

1. Figure 1 below shows a single stage of a differential amplifier.

   (a) Draw a circuit schematic for the current source I_0 that ensures the differential gain is independent of temperature and power supply variation. Include any start up circuits that may be required. [6]

   (b) For your design, show that the gain bandwidth product is independent of temperature. [5]

   (c) Complete the circuit in Figure 1 to show the design of a two-stage amplifier. [6]

   (d) What is the significance of the Miller capacitance in a two stage op-amp ? [3]

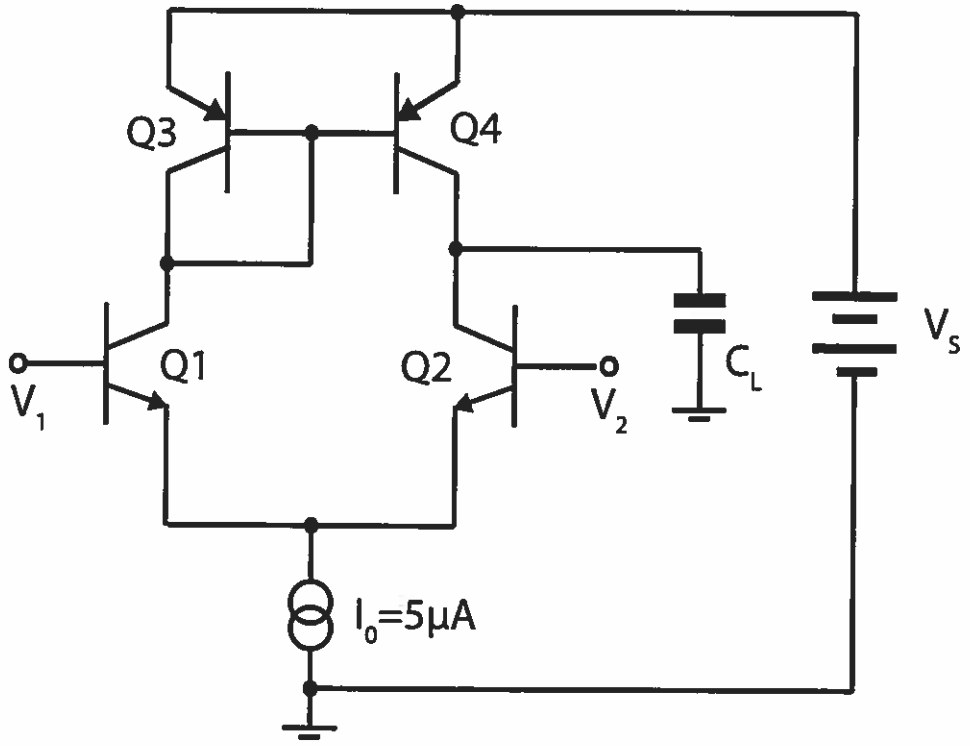

Figure 1.

2. Figure 2 (a, b and c) show three popular biasing schemes typically used in analogue integrated circuits.

   (a) Briefly explain the function of each of the circuits in Figure 2 (a, b and c) and derive expressions for the constant output parameter in each case, clearly indicating component design requirements and any approximations you have made. You may ignore bulk effects in the CMOS circuits.

   [12]

   (b) Sketch a suitable two-transistor and four-transistor potential divider voltage reference circuit and show that when VDD=+5V, VSS=-5V and ID=10uA, for an output voltage Vout=0, the four-transistor circuit consumes less area than the two transistor one. You may assume $K_P=8\mu A/V^2$, $K_N=17\mu A/V^2$, $V_{TN}=V_{TP}=1V$.

   [8]

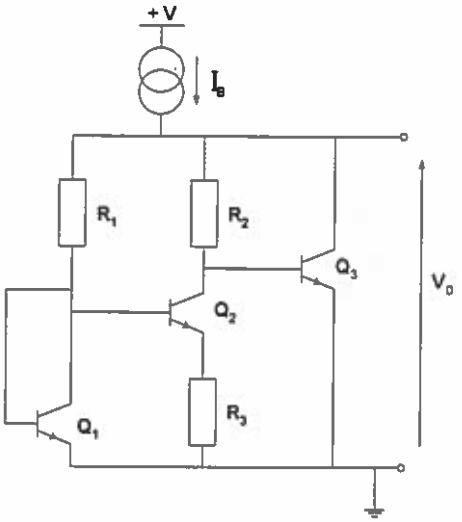

Figure 2(a)

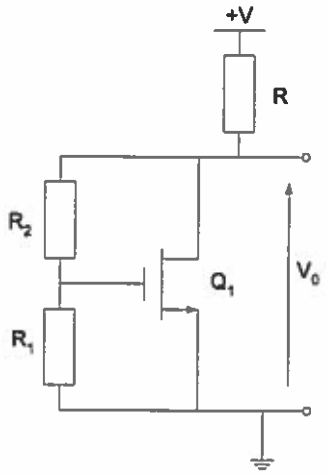

Figure 2(b)

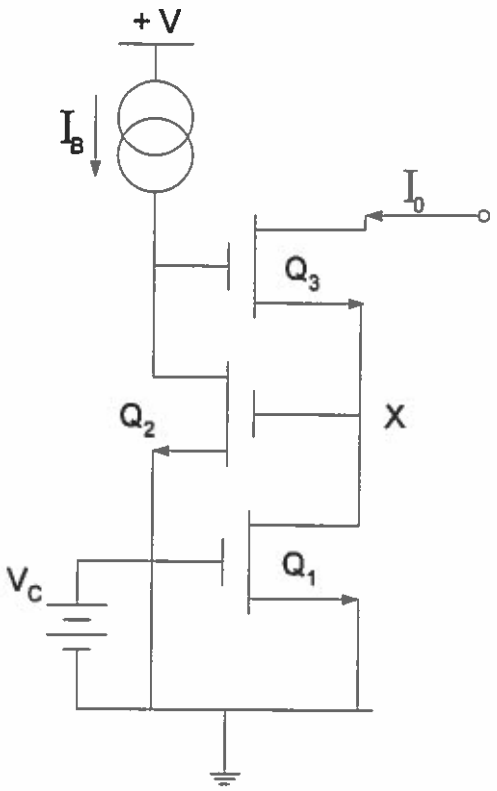

Figure 2(c)

3. (a) Two high-performance analogue-to-digital converters are the current-mode algorithmic converter and the sigma-delta converter. Sketch a typical architecture for ONE of these converter types and explain its principles of operation.

[10]

(b) Assume that the maximum resolution of any sampled-data converter is limited by switch noise (kT/C). Calculate the maximum resolution of a stereo-audio system running at a sample rate of 40 kHz. Assume a MOSFET switch aspect ratio $(W/L) = 1/8$, transconductance parameter $Kp = 20\ \mu A/V^2$ and a device threshold voltage $V_T = 1\ V$. The on voltage of the switch is a $5\ V$ reference (i.e. $V_{GS}on = V_{ref} = 5\ V$). You may also assume that the switch settles in $10\ \tau$ (where τ = time constant) over one period of the clock frequency.

Boltzmanns constant $k = 1.38 \times 10^{-23}\ J/K$ and the ambient temperature is $300\ K$.

[10]

4. Figure 4 shows a partially-designed two-stage CMOS op-amp required to give a voltage gain of approximately 80 dB, a slew-rate of 5 *V/μs* and a gain-bandwidth product of 3 MHz.

(a) Given that the technology is a fixed 5 μm double metal CMOS process, design the channel widths of transistors Q1, Q2 and Q6 for the op-amp to meet the above performance specifications. Aspect ratios of all other devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

[15]

(b) Describe the concept of 'common-centroid' and identify which transistors are critical for the layout of the CMOS op-amp.

[5]

CMOS TRANSISTOR MODEL PARAMETERS

MODEL PARAMETERS	Kp ($\mu A/V^2$)	λ (V^{-1})	V_{T0} (V)
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

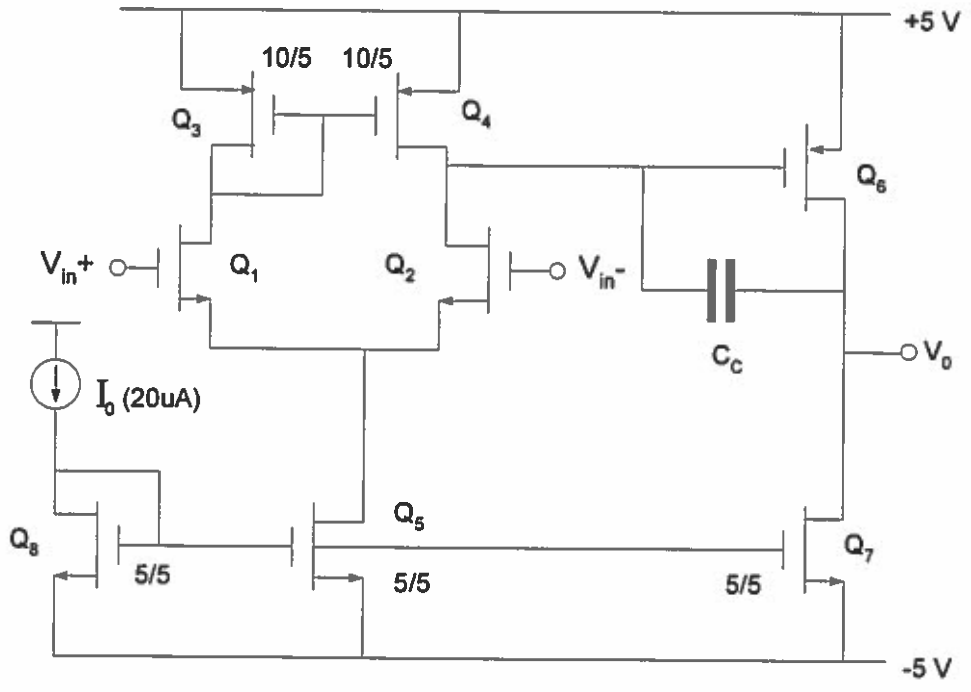

Figure 4

5. Figure 5 shows the basic design of an integrated circuit precision integrator.

(a) Derive an expression for the time constant of the integrator.

[7]

(b) Sketch suitable fully differential folded cascode op-amp architecture for Figure 5. Why is it important for the amplifier to have common-mode feedback?

[8]

(c) An alternative high speed Op-Amp is the current feedback amplifier. Please explain why the gain is independent of the bandwidth.

[5]

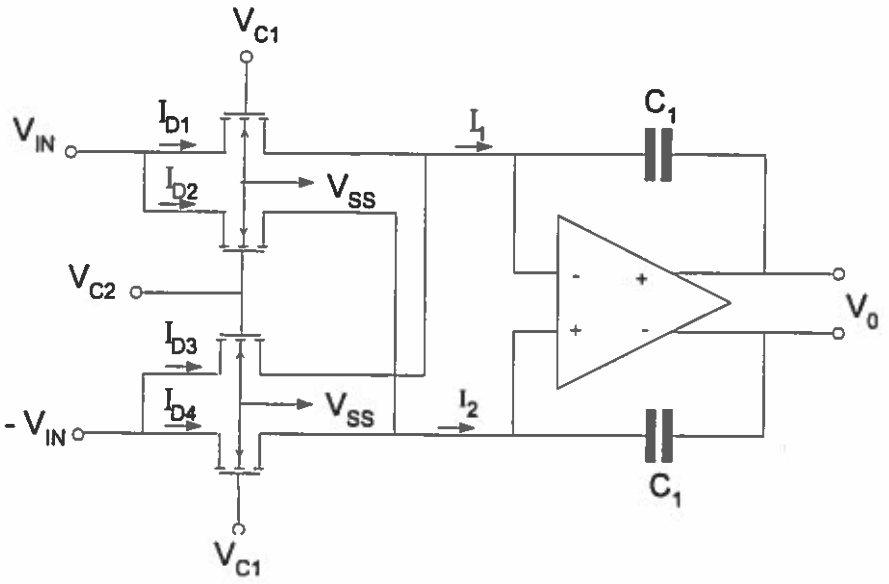

Figure 5

6.

(a) Sketch a 3rd-order Chebyshev low pass LC ladder filter and also sketch the switched capacitor ladder filter equivalent.

[10]

The filter is to have a cut-off frequency of 5kHz. The normalised inductance and capacitance of the ladder filter L2=1.096 and C1=C3=1.596. The values of capacitance in the switched-capacitor filter are 5.08pF for the capacitor based sections and 3.49pF for the inductive sections and all other switched capacitors are 1pF.

(b) Calculate the clock frequency required to achieve a cut-off frequency of 5KHz. Also derive and show that the selected values of capacitance for the switched-capacitor filter realise the normalised inductance and capacitance values of the original ladder filter.

[10]