IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2010/2011

EEE PART II: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 2

SAMPLE PAPER 1 (ISSUED DECEMBER 2010)

Time allowed: 2.00 hours

There are THREE questions on this paper.

ALL questions are compulsory.
Question 1 carries 40% of the marks and Questions 2 and 3 carry 30% each.

Any special instructions for invigilators and information for candidates are on page 1.

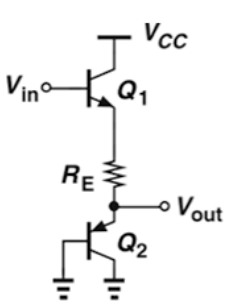
Basic expressions for voltage gain, input and output resistance for single stage amplifiers are given on the last page.

Examiners responsible First Marker(s): XXX
Second Marker(s) YYY

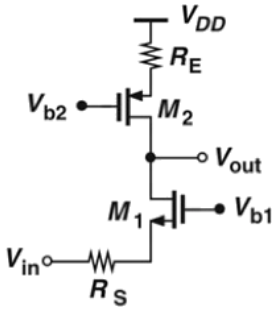
1. This question consists of 10 brief items. Each item can be answered in a few words or a short paragraph with use of a diagram and/or expression where helpful. Please answer all sub-questions, which carry equal marks.

a) Explain what is meant by *source degeneration* in MOSFET amplifiers (or emitter degeneration) in BJT amplifiers. What are the advantages/disadvantages of using this technique? [4]

b) Derive expressions (by inspection) for the voltage gain of the circuits shown below: [4]



(i)



(ii)

c) Explain the differences between *direct* and *capacitive coupling* and identify the related constraints when designing analogue integrated circuits. [4]

d) With the aid of a diagram derive the expression for *Millers Theorem* applied to a capacitance. [4]

e) State two benefits of using *negative feedback* in a system (over open-loop operation) and explain how the feedback achieves this. [4]

f) Given two amplifier types (voltage and transconductance), which should have the lower output impedance? Explain your answer. [4]

g) What is the *transit frequency* f_T of a transistor? Given the base-emitter capacitance of a BJT is 2.2pF, evaluate the transit frequency for a collector current of 5mA. [4]

h) A commercial op-amp (LM741) is quoted an open-loop gain of approximately 106dB. What would be the gain error if configured in closed-loop as an inverting amplifier for a voltage gain of 250? [4]

i) State two challenges in implementing voltage (or current) *bias generators* on-chip and briefly explain how each of these challenges may be overcome. [4]

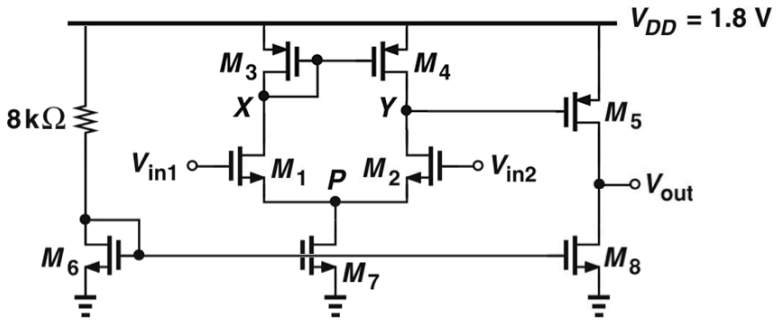
j) Explain how a *cascode stage* can be used to boost the voltage gain of an amplifier. What are the drawbacks of employing this technique? [4]

[Question 1 Total = 40]

2. A basic two stage operational amplifier is shown below:

This circuit consists of the differential pair (M_1 and M_2), an active current mirror (M_3 and M_4) to convert a differential to single-ended output, a second stage common source amplifier (M_5), and biasing circuit (8kΩ resistor and passive current mirror $M_{6\text{-}8}$).

Assume all devices are in saturation and $\lambda>0$ (i.e. $R_{out}<\infty$). Where required, use the following values: $\mu_nC_{ox}=200\mu A/V^2$, $\mu_pC_{ox}=100\mu A/V^2$, $V_{TH,n}=0.4V$, $V_{TH,p}=-0.5V$, $\lambda_n=0.1V^{-1}$, $\lambda_p=0.2V^{-1}$, $C_{GS}=(2/3)WLC_{ox}$, $C_{ox}=12fF/\mu m^2$, $C_{DB}\approx0$, $C_{SB}\approx0$ and $C_{GD}=C_0W$, where $C_0=0.2fF/\mu m$ denotes the gate-drain capacitance per unit width.



a) Derive an expression for the differential voltage gain of the first stage (V_y/V_{in1}-V_{in2}). [6]

b) Derive an expression for the voltage gain of the second stage (V_{out}/V_y) and therefore the total voltage gain ($Av=V_{out}/V_{in1}$-V_{in2}). [4]

c) Given that: $(W/L)_6=4/2$
$(W/L)_7=10/2$
$(W/L)_8=20/2$
Calculate the total power consumption of the circuit. [5]

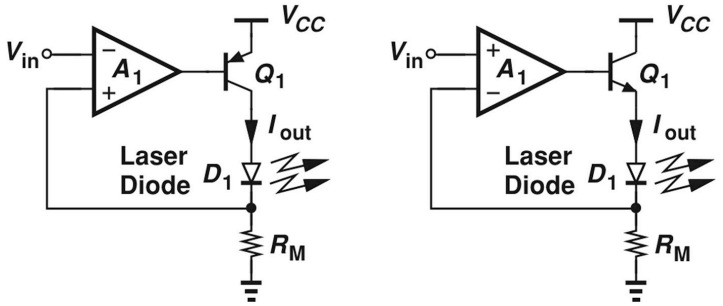
d) Given that: $(W/L)_1=(W/L)_2=250/1$
$(W/L)_3=(W/L)_4=4/4$
$(W/L)_5=40/4$
Calculate the voltage gain (in dB). [5]

e) Calculate the frequency of the pole associated with node Y ($f_{pY}=\omega_{pY}/2\pi$) using Millers Theorem. [5]

f) Calculate the frequency of the pole associated with the output node ($f_{pout}=\omega_{pout}/2\pi$). Which is the dominant pole? [5]

[Question 2 Total = 30]

3. A "laser diode" converts current to light (as in laser pointers). It is required to design a circuit that delivers a well-defined current to a laser diode. In order to achieve this, negative feedback is applied to regulate the output bias. Two circuits that can achieve this are shown below: (i) with a common emitter output stage and (ii) with a common source output stage. In both these configuration, the resistor R_M measures the current flowing through D_1 and amplifier A_1 subtracts the resulting voltage drop from V_{in}.



(i) (ii)

Assume R_M is very small and $V_A=\infty$.

a) Explain how both circuits apply negative feedback even though the operational amplifier inputs are connected differently. [3]

b) Considering the system as a whole (excluding only the laser diode), what type of amplifier is this? [2]

c) Which topology is preferable? Explain your selection. [3]

Answer the remaining questions considering only circuit topology with the common emitter output stage, i.e. (i).

d) Break the loop and determine the open-loop gain [5]

e) Determine the feedback factor and loop gain [5]

f) Derive an expression for the closed-loop gain [2]

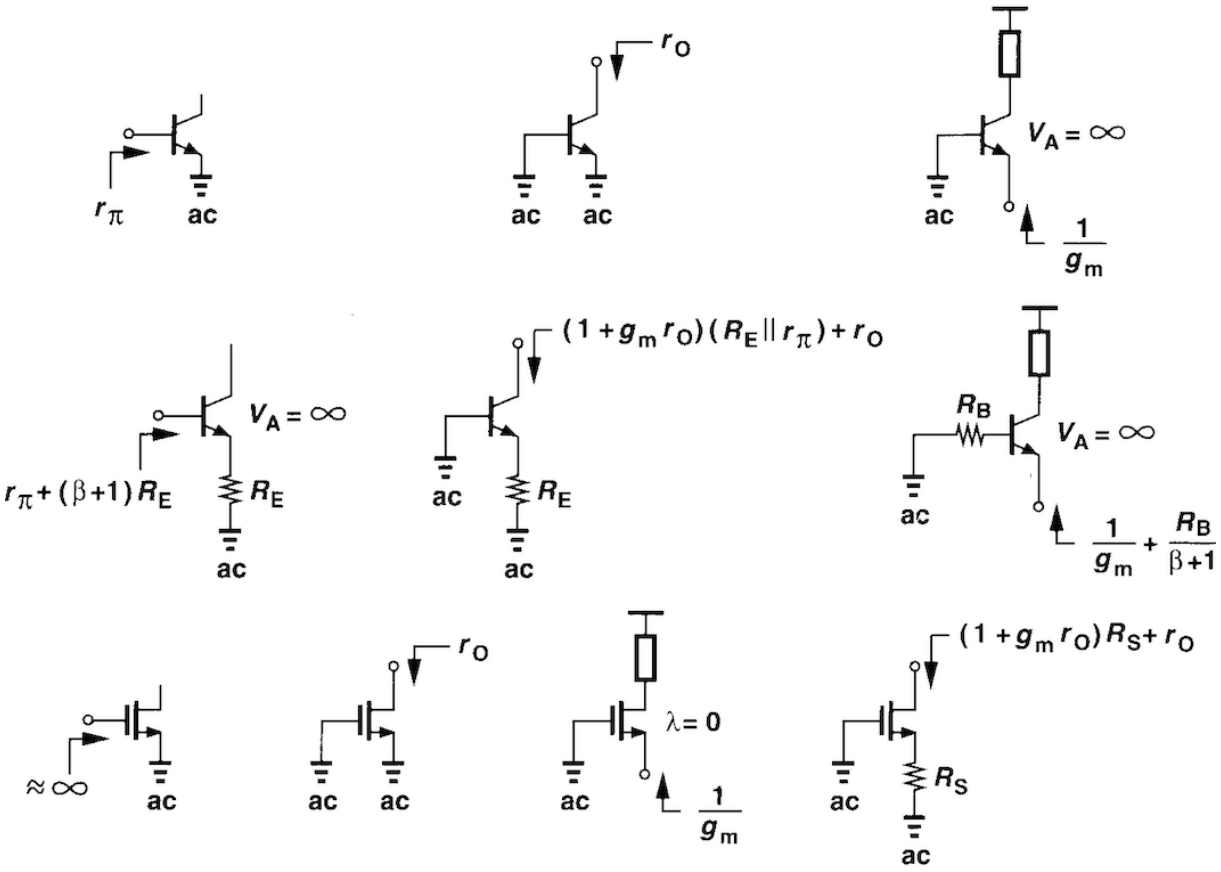
g) Derive an expression for the open-loop output impedance [3]

h) Derive an expression for the closed-loop output impedance [2]

i) Calculate the closed-loop gain and output impedance given A_1=100dB, $I_S=6\times10^{-16}$A and R_M=10Ω. [5]

[Question 3 Total = 30]

Input and Output Impedances



Voltage Gain Equations