IMPERIAL COLLEGE LONDON

EE3-11
EE9-AO8

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2014

MSc and EEE PART III/IV: MEng, Beng.and ACGI

Corrected Copy

ADVANCED ELECTRONIC DEVICES

Tuesday, 21 January 10:00 am

Time allowed: 3:00 hours

There are FIVE questions on this paper.

Answer Question One and THREE other questions.

Question One carries 40 marks. All other questions carry 20 marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : K. Fobelets, K. Fobelets

Second Marker(s) : S. Lucyszyn, S. Lucyszyn

Special instructions for invigilators

Q1 is compulsory

Special instructions for students

Q1 is compulsory.

Constants

permittivity of free space:	$\varepsilon_o = 8.85 \times 10^{-12}$ F/m
permeability of free space:	$\mu_o = 4\pi \times 10^{-7}$ H/m
intrinsic carrier concentration in Si:	$n_{i\,Si} = 1.45 \times 10^{10}$ cm^{-3} at $T = 300$K
intrinsic carrier concentration in Ge:	$n_{i\,Ge} = 2.0 \times 10^{13}$ cm^{-3} at $T = 300$K
intrinsic carrier concentration in GaAs:	$n_{i\,GaAs} = 1.79 \times 10^{6}$ cm^{-3} at $T = 300$K
intrinsic carrier concentration in InAs:	$n_{i\,InAs} = 1 \times 10^{15}$ cm^{-3} at $T = 300$K
dielectric constant of SiO_2:	$\varepsilon_{ox} = 4$
dielectric constant of Si:	$\varepsilon_{Si} = 12$
dielectric constant of Ge:	$\varepsilon_{Ge} = 16$
dielectric constant of GaAs:	$\varepsilon_{GaAs} = 13$
dielectric constant of InAs:	$\varepsilon_{InAs} = 15$
electron affinity of Si	$\chi_{Si} = 4.05$ eV
electron affinity of Ge	$\chi_{Ge} = 4.0$ eV
electron affinity of GaAs	$\chi_{GaAs} = 4.1$ eV
electron affinity of InAs	$\chi_{InAs} = 4.9$ eV
electron affinity of AlAs	$\chi_{AlAs} = 3.6$ eV
bandgap of Si	$E_G = 1.1$ eV
bandgap of Ge	$E_G = 0.66$ eV
bandgap of GaAs	$E_G = 1.42$ eV
bandgap of InAs	$E_G = 0.36$ eV
bandgap of AlAs	$E_G = 2.22$ eV
effective density of states of Si:	$N_{C\,Si} = 2.8 \times 10^{19}$ cm^{-3}
	$N_{V\,Si} = 1.04 \times 10^{19}$ cm^{-3}
effective density of states of Ge:	$N_{C\,Ge} = 1.0 \times 10^{19}$ cm^{-3}
	$N_{V\,Ge} = 5.0 \times 10^{18}$ cm^{-3}
effective density of states of GaAs:	$N_{C\,GaAs} = 4.7 \times 10^{17}$ cm^{-3}
	$N_{V\,GaAs} = 9.0 \times 10^{18}$ cm^{-3}
effective density of states of InAs:	$N_{C\,InAs} = 8.7 \times 10^{16}$ cm^{-3}
	$N_{V\,InAs} = 6.6 \times 10^{18}$ cm^{-3}
thermal voltage:	$kT/e = 0.026$V at $T = 300$K
charge of an electron:	$e = 1.6 \times 10^{-19}$ C (1 eV)

Workfunction of metals

metal	ϕ (eV)
Al	4.08
Ni	5.01
Ti	4.33
W	4.6

Formulae

$f(E)=\dfrac{1}{1+\exp\left(\dfrac{E-E_F}{kT}\right)}$	Fermi distribution
$n_i=\sqrt{N_V N_C}\exp\left(\dfrac{-E_G}{2kT}\right)$	Intrinsic carrier concentration
$n=N_c e^{-\frac{(E_c-E_F)}{kT}}$	Concentration of electrons
$p=N_v e^{\frac{(E_v-E_F)}{kT}}$	Concentration of holes
$\dfrac{dE}{dx}=\dfrac{\rho(x)}{\varepsilon}$	Poisson equation in 1 dimension
$E=-\dfrac{dV}{dx}$	Relationship between electric field and electrostatic potential
$\left.\begin{array}{l} J_n(x)=e\mu_n n(x)E(x)+eD_n\dfrac{dn(x)}{dx} \\ J_p(x)=e\mu_p p(x)E(x)-eD_p\dfrac{dp(x)}{dx}\end{array}\right\}$	Drift and diffusion current densities in a semiconductor
$-\dfrac{\hbar^2}{2m}\dfrac{d^2\psi(x)}{dx^2}+V(x)\psi(x)=E\psi(x)$	Schrödinger's equation in one dimension
$D=\dfrac{kT}{e}\mu$	Einstein relation
$I_{DS}=\dfrac{\mu C_{ox}W}{L}\left((V_{GS}-V_{th})V_{DS}-\dfrac{V_{DS}^2}{2}\right)$	Drift current in a MOSFET
$V_{th}=\phi_m-\phi_s+2\times\phi_F+\gamma\times\sqrt{2\times\phi_F}$	Threshold voltage
$\phi_F=\dfrac{kT}{e}\ln\left(\dfrac{N_A}{n_i}\right)$	Fermi potential (difference between intrinsic and Fermi level)
$\gamma=\dfrac{\sqrt{2e\varepsilon_s N_A}}{C_{ox}}$	Body effect coefficient
$J=\dfrac{eD_n n_p}{L_n}\left(e^{\frac{eV}{kT}}-1\right)+\dfrac{eD_p p_n}{L_p}\left(e^{\frac{eV}{kT}}-1\right)$	Diode diffusion current density
$V_{bi}=\dfrac{kT}{e}\ln\left(\dfrac{N_A N_D}{n_i^2}\right)$	Built-in voltage pn diode
$W_{depl}(V)=\left[\dfrac{2\varepsilon(V_{bi}-V)}{e}\left(\dfrac{1}{N_A}+\dfrac{1}{N_D}\right)\right]^{1/2}$	Total depletion width under bias V
$S=\dfrac{dV_{GS}}{dLog(I_{DS})}$	Sub-threshold swing

1. Compulsory question.

a) Sketch the energy band diagram (E_c, E_v, E_i, E_F) from the gate into the substrate for an n-channel MOSFET (nMOS) with $\phi_m < \phi_s$. ϕ_m is the workfunction of the metal and ϕ_s of the Si substrate. All contacts are grounded. [5]

b) The surface charge density underneath the gate oxide is given by the expression:

$$n_s = N_A e^{\left(\frac{V_S - 2\phi_F}{V_T}\right)}$$

with V_s the surface potential, V_T the thermal voltage and ϕ_F the Fermi potential.

i) Give the expression for V_s at the onset of depletion. [1]

ii) Give the expression for V_s at the onset of inversion. [1]

iii) Give the expression for n_s in both cases i) and ii). [3]

c) The curve fits to the current-voltage measurements of an *ideal* long channel MOSFET in strong inversion in the triode (V_{DS} = 0.01V) and the saturation region (V_{DS} = 1V > $V_{GS} - V_{th}$) gives the following equations:

Triode: $I_{DS} = 8.85\ 10^{-13} V_{GS} - 4.425\ 10^{-13}$

Saturation: $I_{DS} = 4.425\ 10^{-11} V_{GS}^2 - 3.9825\ 10^{-11} V_{GS} + 8.960625\ 10^{-12}$

Note that these equations are only valid for $V_{GS} \geq V_{th}$.

Calculate DIBL (drain induced barrier lowering). [5]

d) Sketch the energy band diagram (E_c, E_v, E_F, E_G) through the 4-layer structure: Ti – Ge – GaAs - Al. Include the influence of the metals (Ti and Al). The workfunction of Ge is ϕ_{Ge} = 4.33 eV and of GaAs is ϕ_{GaAs} = 4.33 eV. You can assume that the electron affinity rule is valid. [5]

e) Figure 1.1 gives the velocity-field curves for 3 materials: m1, m2 and m3.

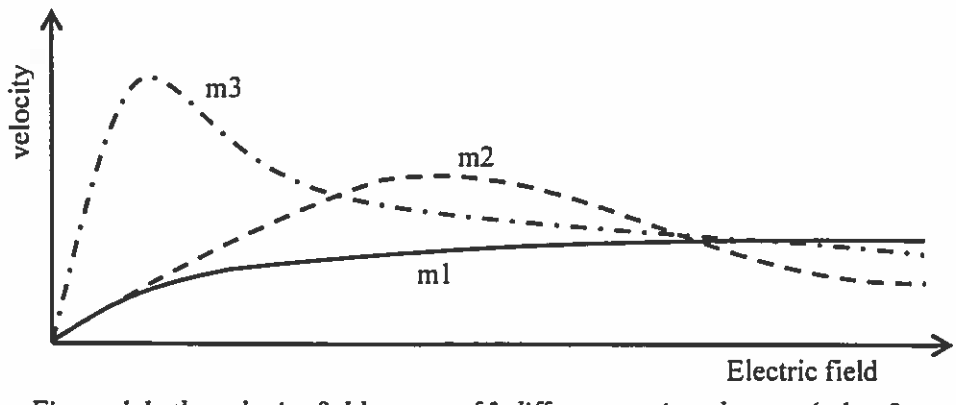


Figure 1.1: the velocity field curves of 3 different semiconductors (m1, m2, m3).

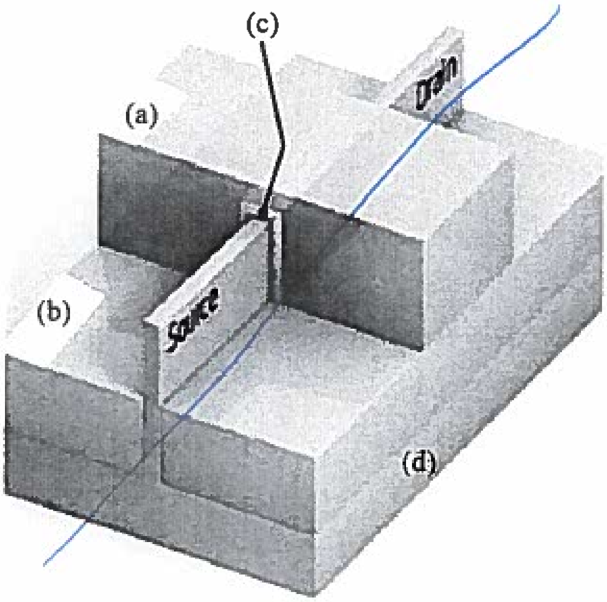
i) Rank (< , >, =) the materials in order of decreasing mobility ($\mu 1$, $\mu 2$, $\mu 3$) [3]

ii) Rank (<, >, =) the materials in order of decreasing saturation velocity ($v_{sat}1$, $v_{sat}2$, $v_{sat}3$) [2]

f) A MESFET is fabricated using n-type GaAs. The GaAs layer underneath the gate has a doping concentration of $N_D = 10^{15}$ cm^{-3}. Choose the *best* gate metal from the set given in the constants list on page 2 for this MESFET. Explain your choice briefly. Assume the interface state density is zero. [5]

g) How does the gate leakage current compare between a GaAs MESFET and a GaAs JFET? Explain your answer briefly. [5]

h) Figure 1.2: 3D drawing of the FET.



use drawing on the next page.

Figure 1.2: 3D image of a FET, taken from Electronics News 25 September 2012.

i) What type of FET is drawn in figure 1.2? [1]

ii) Define each region (a), (b), (c) and (d). [4]

Advanced Electronic Devices – Figure for question 1 h) in better grey scales

h) Figure 1.2: 3D drawing of the FET.

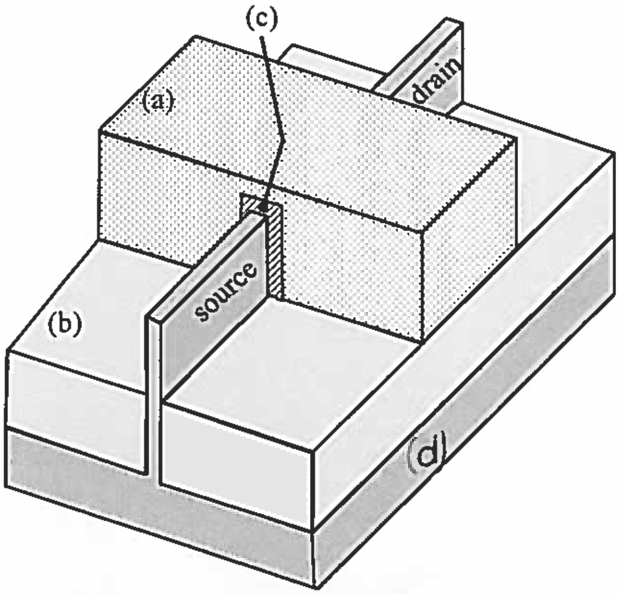


Figure 1.2: 3D image of a FET, taken from Electronics News 25 September 2012.

2. MOSFET

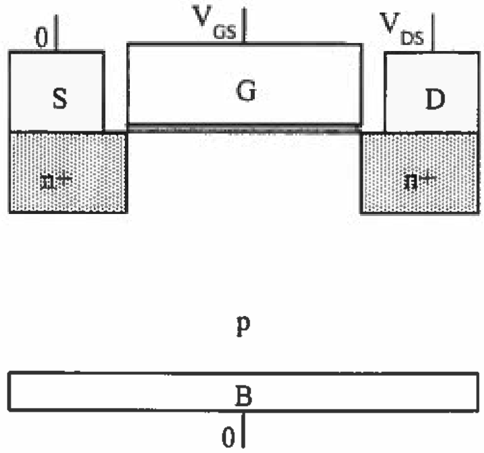


Figure 2.1: Schematic material cross section of an n-channel enhancement mode MOSFET. The metal contacts are given as rectangular boxes.

Material parameters: $\phi_m = \phi_{p\text{-}Si}$. The gate voltage, V_{GS} is at threshold. A small drain voltage, $V_{DS} = 0.26$ V is applied. The doping density in the different regions is: n+: $N_D = 10^{20}$ cm^{-3} and p: $N_A = 10^{16}$ cm^{-3}.

Initial assumptions:

1. The n+ regions implant depth is larger than the maximum depletion width caused by the gate, $t_j > W_{max}$.
2. The width of all depletion regions can be assumed to be independent of the perpendicular electric field. E.g. $W_{max}(V_{GS})$ is assumed to be independent of V_{DS}.
3. Doped (implanted) regions and depletion regions can all be assumed to be rectangular.
4. The width of the gate is large.

a) Calculate the following depletion widths:

W_{max}, W_{DB}, W_{SB} (respectively, the maximum depletion width caused by the gate voltage, the drain-bulk and source-bulk depletion width). Give any approximation you make. [8]

b) Sketch the region of the material cross section of the MOSFET of figure 2.1 relevant for demonstrating charge sharing. Add the different relevant depletion widths (W_{max}, W_{DB}, W_{SB}) to this sketch and ensure their relative magnitudes are consistent. [4]

c) Derive the expression of the threshold voltage shift, ΔV_{th} due to charge sharing in terms of the depletion widths. Give any approximations you make. [8]

3. III-V FETs

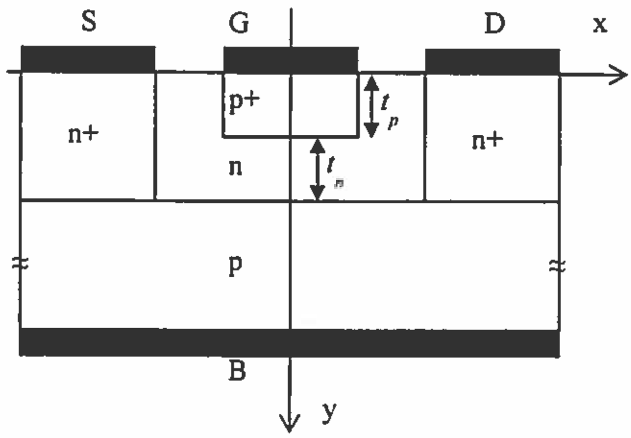


Figure 3.1: Material cross section of a GaAs JFET. Drain, source and bulk contact are grounded. The doping density in the different regions is: n+: $N_D = 10^{20}$ cm^{-3}, p+: $N_A = 10^{20}$ cm^{-3}, n: $N_D = 10^{17}$ cm^{-3}, p: $N_A = 5\ 10^{17}$ cm^{-3}.

a) Sketch the energy band diagram (E_c, E_v, E_F) from the gate into the substrate for the depletion mode JFET of figure 3.1 for $V_{DS} = V_{GS} = V_{BS} = 0$V. Ensure that the relative dimensions of the different parameters involved in this sketch are correct. [5]

b) Sketch the energy band diagram (E_c, E_v, E_F) of the JFET in figure 3.1 from the source to the drain through the channel when the channel is completely pinched off at $V_{DS} = V_{BS} = 0$V. Identify the regions by their carrier concentration. [5]

c) Derive the expression for the pinch-off voltage V_p for $V_{DS} = V_{BS} = 0$V in terms of material parameters. Take the differences in doping concentration into account in your reasoning, but do not use their value in the expression of V_p. [10]

4. SOI

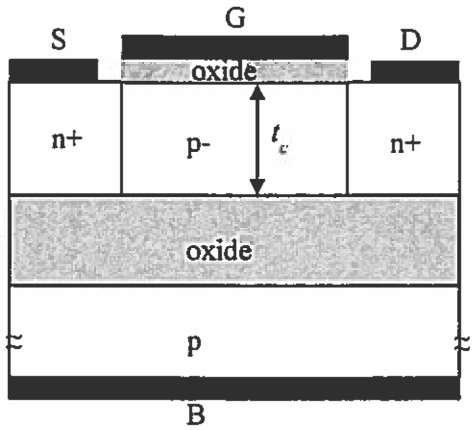


Figure 4.1: Material cross section of a MOSFET on SOI. Source and bulk contact are grounded. The doping density in the different regions is: n+: $N_D = 5\ 10^{19}\ cm^{-3}$, p-: $N_A = 10^{15}\ cm^{-3}$, p: $N_A = 10^{17}\ cm^{-3}$.

a) Explain the reason for the occurrence of the kink effect in partially depleted SOI MOSFETs at higher drain voltages. [5]

b) Give three advantages and two disadvantages of using fully depleted SOI for CMOS. [5]

c) Derive an expression for the workfunction of the metal as a function of the MOSFET material parameters and t_c that ensures that the MOSFET in figure 4.1 is fully depleted at $V_{GS} = V_{DS} = V_{BS} = 0V$. Do not substitute the doping values in the derived equation. Write down the reasoning behind your derivation. [10]

5.

a) By drawing appropriate material cross sections (identify neutral and depleted regions), demonstrate that reducing the source and drain Ohmic contact implantation depth, t_j (junction depth) reduces ΔV_{th} caused by charge sharing. [5]

b) Reducing t_j (junction depth), decreases the externally measured transconductance g_m. Derive an expression, as a function of material parameters, that describes the influence of t_j on the externally measured g_m. [8]

c) Industry is using SiGe to circumvent the problem associated with a reduction of the junction depth.

   i) What is this method called? [2]

   ii) How can this method be used to also increase the mobility? [2]

   iii) Sketch a material cross section in which this method (i & ii) is used. [3]