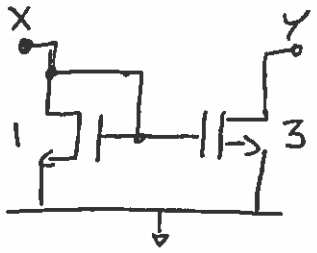
1. a) State two advantages of representing signals in the current-mode rather than voltage mode domain when trying to achieve low-power operation.

- With current mode we can achieve a larger dynamic range as the SNR of the input signal is no longer dependent on the supply voltage. [1]
- Computation can occur using the physical primitives of devices which can be more efficient. [1]

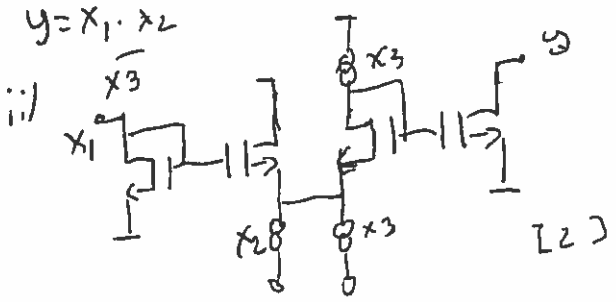
[Total 2 points]

b) Sketch current mode topologies that implement the following functions, where x represents an input current, z represents an input voltage, A and B are constants and y the output current. Identify A and B in equations (iii), (iv) and (vi).

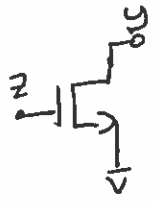
i) $y = 3x$ [2]



ii) $y = x_1.x_2/x_3$ [2]



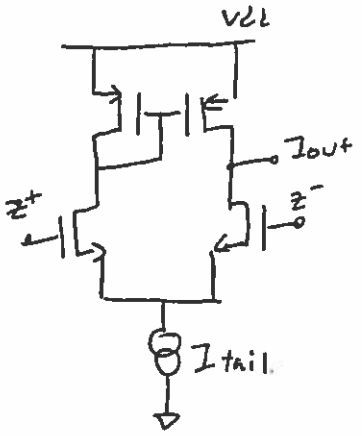
iii) $y = A \exp\left(\frac{z}{B}\right)$ [2]



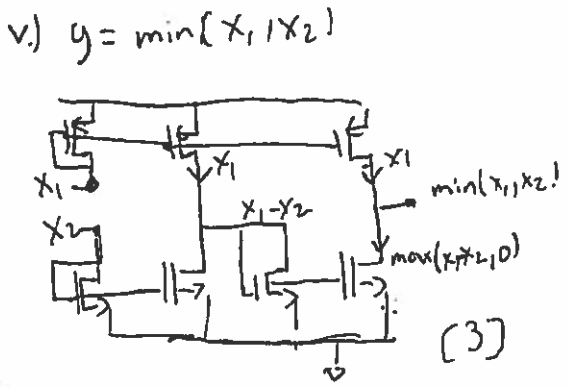
Weak - Inversion

$I_{DS} = I_0 \exp\left(\frac{V_{GS}}{nU_t}\right)$

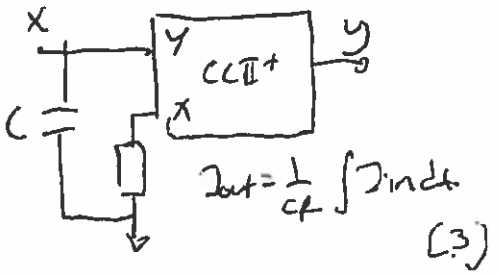
iv) $y = A \tanh\left(\frac{z}{B}\right)$ [3]



v) $y = \min(x_1, x_2)$ [3]



vi) $y = A\int x\,dt$ [3]



c) Equation 1.1, below, shows the noise resource equation which represents the output noise from a cascade of M amplifiers of gain G. Each amplifier i contains n_i devices of area A_i and a bias current I_i.

$$v_{no}^2 = \sum_{i=1}^{i=M} v_{ni}^2 G_i^2 = \sum_{i=1}^{i=M} \left(n_i \frac{K_w}{(I_i / n_i)^p} \cdot \Delta f + n_i \frac{K_f}{(A_i / n_i)} \cdot \ln\left(\frac{f_h}{f_l}\right) \right) G_i^2 \qquad (1.1)$$

i) What does equation 1.1 tell us about where the most emphasis should be given in order to reduce noise and why when trying to detect very small signals using a M amplifier cascade?

In an amplifier cascade more emphasis should be given to the first stage as the noise from the first stage is multiplied by all the subsequent stages in the cascade.

Total output noise is given by $v_{no}^2 = \sum_{i=1}^{i=M} v_{ni}^2 G_i^2$ where $G_i = \prod_{k=i}^{k=M} g_k$.

[1]

ii) Propose two methods to improve noise performance for a fixed supply current.

For a fixed current we can increase the area of our input transistors to reduce 1/f noise and we can also compute more slowly to limit our bandwidth and thus our thermal noise.

[2]

2. a) State and derive the translinear principle (TLP) for a loop of MOS transistors working in weak inversion. Give all assumptions you make.

[bookwork]
In a closed loop containing an even number of forward biased junctions, arranged so that there are an equal number of clockwise facing and counterclockwise facing polarities, the product of the current densities in the clockwise direction is equal to the product of the current densities in the counterclockwise direction.
[2 points for definition]
Number of Clockwise Junctions (Voltage Rises)=Number of Anticlockwise Junctions (Voltage drops)

$$\sum_{n\in CW} V_n = \sum_{n\in CCW} V_n$$

$$V_n = nU_T \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right)$$

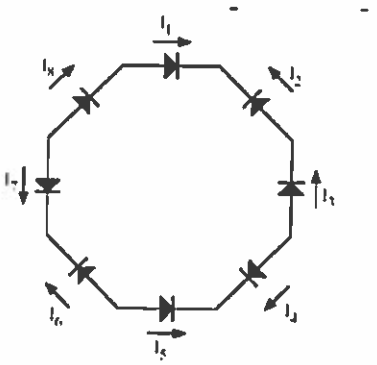
$$\sum_{n\in CW} nU_T \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right) = \sum_{n\in CCW} nU_T \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right)$$

$$\sum_{n\in CW} \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right) = \sum_{n\in CCW} \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right)$$

$$\prod_{n\in CW} \frac{I_n}{\lambda_n I_{DO}} = \prod_{n\in CCW} \frac{I_n}{\lambda_n I_{DO}}$$

$$\prod_{n\in CW} \frac{I_n}{\lambda_n} = I_{DO}^{CW-CCW} \prod_{n\in CCW} \frac{I_n}{\lambda_n}$$

$$\prod_{n\in CW} \frac{I_n}{\lambda_n} = \prod_{n\in CCW} \frac{I_n}{\lambda_n}$$



Assumptions: Temperature and saturation currents are all the same.
[3 points for derivation]

[Total 5points]

b) Show how short channel effects in MOS transistors operating in weak inversion, lead to multiplicative errors in output currents of translinear circuits.

- Short channel effects of MOS transistors induce an Error due to early effect/channel length modulation

$$I_{DS(wi)} = \lambda \cdot I_{D0} \exp\left(\frac{V_{GS}}{nU_t}\right)\left(1-\exp\left(\frac{-V_{DS}}{U_t}\right)\right) = \lambda \cdot \gamma \cdot I_{D0} \exp\left(\frac{V_{GS}}{nU_t}\right)$$ [2]

- Appear like an area mismatch

$$\prod_{n\in CW} \frac{I_n}{\lambda_n \gamma_n} = \prod_{n\in CCW} \frac{I_n}{\lambda_n \gamma_n}$$ [1]

[Total 3 points]

c) The translinear circuit, shown in figure 2.1, is used to solve the quadratic equation:

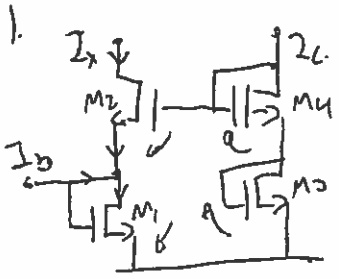
$$x^2 + bx + c = 0 \qquad (2.1)$$

i) Derive the circuit's function to show it does indeed represent equation 2.1.

[2]

ii) Derive the equation for the output current I_x which gives the positive root of the quadratic equation. (Hint: $c=-I_c^2$).

c).



Translinear loop M3-M4 = M2-M1

$I_4 . I_3 = I_2 . I_1$

$I_c . I_c = I_x . (I_x + I_b)$

$I_c^2 = I_x^2 + I_b I_x$

$I_x^2 + I_b I_x - I_c^2 = 0$

represents $x^2 + bx + c = 0$

where $b = I_b$ and $c = -I_c^2$

$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \Rightarrow I_x = \frac{-I_b + \sqrt{I_b^2 + I_c^2}}{2}$

(4)

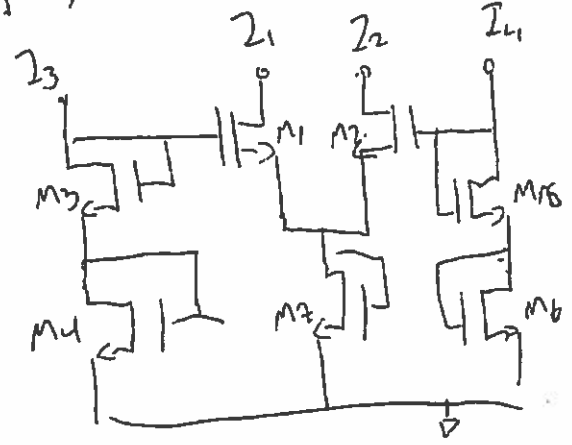
[2 points for showing it solves the quadratic equation and 2 points for showing the solution]

d)

i) For the circuit shown in Figure 2.2, show that the output current is given by:

$$I_{out} = I_1 - I_2 = \frac{I_3^2 - I_4^2}{\sqrt{I_3^2 + I_4^2}}$$

d) i)



$T_{L1} = M_3 - M_4 - M_1 - M_7$

$T_{L2} = M_6 - M_5 - M_2 - M_7$

$I_{M1} \cdot I_{M3} = I_{M1} \cdot I_{M7}$

$I_{M5} \cdot I_{M6} = I_{M2} \cdot I_{M7}$

$I_3 \cdot I_3 = I_1 \cdot I_7$

$I_4 \cdot I_4 = I_2 \cdot I_7$

$I_3^2 = I_1 \cdot I_7$ and $I_7 = I_1 + I_2$

$I_4^2 = I_2 \cdot I_7$

$I_7 = \frac{I_3^2}{I_7} + \frac{I_4^2}{I_7}$

$I_1 = \frac{I_3^2}{I_7}$ $I_2 = \frac{I_4^2}{I_7}$

$I_7^2 = I_3^2 + I_4^2$

$I_1 - I_2 = \frac{I_3^2 - I_4^2}{I_7}$

$I_7 = \sqrt{I_3^2 + I_4^2}$

$I_{out} = \frac{I_3^2 - I_4^2}{\sqrt{I_3^2 + I_4^2}}$ [5]

ii) State the function of this circuit for $I_3 = I_A|\cos \omega t|$ and $I_4 = I_A|\sin \omega t|$. [5]

[3]

$I_{out} = \frac{I_A^2(\cos^2 \omega t - \sin^2 \omega t)}{\sqrt{(\cos^2 \omega t + \sin^2 \omega t)}} = \frac{I_A^2(\cos 2\omega t)}{1}$

$I_{out} = I_A^2(\cos 2\omega t)$ => frequency doubler [3]

3. a) The transfer function of a biquad filter is defined in state space representation by the following equations:

$$\dot{X}_1 = -\omega_0 X_2 + \omega_0 U_1$$

$$\dot{X}_2 = \omega_0 X_1 - \frac{\omega_0}{Q} X_2 + \omega_0 U_2$$

$$Y = X_2$$

whereby Y is the output; U_1 and U_2 are the inputs; and X_1 and X_2 are the states.

i) Show that these state equations can be used to implement either a lowpass or a bandpass transfer function (represented in the Laplace domain) and explain the role of the two inputs U_1 and U_2.

3.a) i) $\dot{X}_1 = -\omega_0 X_2 + \omega_0 u_1$

$\dot{X}_2 = \omega_0 X_1 - \frac{\omega_0}{Q} X_2 + \omega_0 u_2$

$Y = X_2$

$sX_1 = -\omega_0 X_2 + \omega_0 u_1 \Rightarrow X_1 = \frac{-\omega_0 X_2 + \omega_0 u_1}{s}$

$sX_2 = \omega_0 X_1 - \frac{\omega_0}{Q} X_2 + \omega_0 u_2$

$sX_2 = \omega_0\left(\frac{-\omega_0 X_2 + \omega_0 u_1}{s}\right) - \frac{\omega_0}{Q} X_2 + \omega_0 u_2$

$s^2 X_2 = -\omega_0^2 X_2 + \omega_0^2 u_1 - \frac{\omega_0}{Q} s X_2 + s\omega_0 u_2$

$s^2 X_2 + \frac{s\omega_0}{Q} X_2 + \omega_0^2 X_2 = \omega_0^2 u_1 + s\omega_0 u_2$

$X_2\left(s^2 + \frac{s\omega_0}{Q} + \omega_0^2\right) = \omega_0^2 u_1 + s\omega_0 u_2$

$Y = X_2 = \frac{\omega_0^2 u_1 + s\omega_0 u_2}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2}$

$y = \frac{\omega_0^2}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2}$ if $u_2 = \phi$ Low pass

$y = \frac{s\omega_0}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2}$ if $u_1 = \phi$ Band pass

[4]

ii) By using the mappings below show how these linear equations can be mapped to non-linear log-domain design equations. You may assume $I_1=I_2=I_\omega$. Give any other assumptions you make.

$$X_1 = I_1 \exp\left(\frac{V_1}{nU_t}\right) \qquad X_2 = I_2 \exp\left(\frac{V_2}{nU_t}\right)$$

$$U_1 = I_{U1} \exp\left(\frac{V_{U1}}{nU_t}\right) \qquad U_2 = I_{U2} \exp\left(\frac{V_{U2}}{nU_t}\right)$$

---

iii)

① $\dot{X}_1 = -\omega_0 X_2 + \omega_0 U_1$

② $\dot{X}_2 = \omega_0 X_1 - \frac{\omega_0}{Q} X_2 + \omega_0 U_2$.

$X_1 = I_1 \exp\left(\frac{V_1}{nU_t}\right)$ [6]

$X_2 = I_2 \exp\left(\frac{V_2}{nU_t}\right)$

$U_1 = I_{U1} \exp\left(\frac{V_{U1}}{nU_t}\right)$

$U_2 = I_{U2} \exp\left(\frac{V_{U2}}{nU_t}\right)$

$\dot{X}_1 = \frac{I_1}{nU_t} \exp\left(\frac{V_1}{nU_t}\right) \dot{V}_1$

$\dot{X}_2 = \frac{I_2}{nU_t} \exp\left(\frac{V_2}{nU_t}\right) \dot{V}_2$

Equation ① Assume $I_1 = I_2 = I_\omega$ and I_{U1} and $I_{U2} = I_0$

$$\frac{I_1}{nU_t} \exp\left(\frac{V_1}{nU_t}\right) \dot{V}_1 = -\omega_0 \cdot I_2 \exp\left(\frac{V_2}{nU_t}\right) + \omega_0 I_{U1} \exp\left(\frac{V_{U1}}{nU_t}\right)$$

$$\dot{V}_1 = -nU_t \omega_0 \frac{I_2}{I_1} \exp\left(\frac{V_2 - V_1}{nU_t}\right) + nU_t \omega_0 \frac{I_{U1}}{I_1} \exp\left(\frac{U_1 - V_1}{nU_t}\right)$$

$\because I_\omega = C_n V_T \omega_0$.

$$C\dot{V}_1 = -I_\omega \frac{I_2}{I_1} \exp\left(\frac{V_2 - V_1}{nU_t}\right) + I_\omega \frac{I_{U1}}{I_1} \exp\left(\frac{V_{U1} - V_1}{nU_t}\right)$$

$$\rightarrow C\dot{V}_1 = -I_\omega \exp\left(\frac{V_2 - V_1}{nU_t}\right) + I_0 \exp\left(\frac{V_{U1} - V_1}{nU_t}\right)$$

Equation (2)

$$\frac{I_2}{nU_t}\exp\left(\frac{V_2}{nU_t}\right)\dot{V}_2 = \omega_0 I_1 \exp\left(\frac{V_1}{nU_t}\right) - \frac{\omega}{Q}\cdot I_2 \exp\left(\frac{V_2}{nU_t}\right) + \omega_0 I_{u2}\exp\left(\frac{V_{u2}}{nU_t}\right)$$

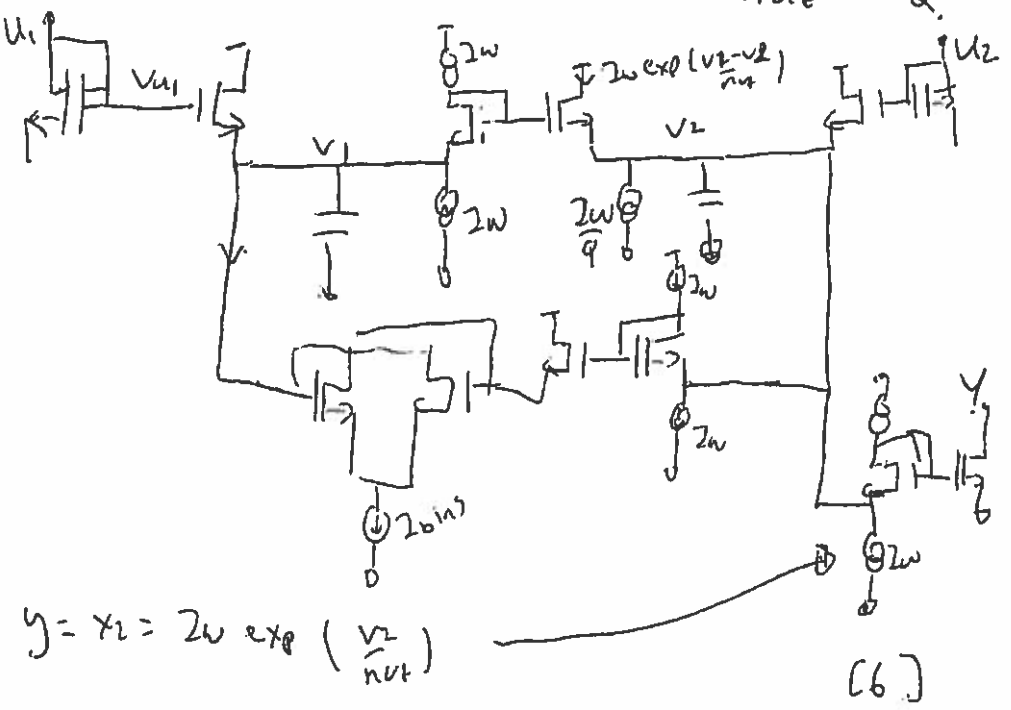
$$C\dot{V}_2 = I_\omega \exp\left(\frac{V_1 - V_2}{nU_t}\right) + I_0 \exp\left(\frac{V_{u2}-V_2}{nU_t}\right) - \frac{I_\omega}{Q}$$

[3 points for equation 1, 3 points for equation 2, Total 6 points]

iii) With these log-domain design equations, sketch a schematic of the final log domain filter using MOS transistors operating in weak inversion.

$$C\dot{V}_1 = -I_\omega \exp\left(\frac{V_2 - V_1}{nU_t}\right) + I_0 \exp\left(\frac{V_{u1}-V_1}{nU_t}\right)$$

$$C\dot{V}_2 = I_\omega \exp\left(\frac{V_1 - V_2}{nU_t}\right) + I_0 \exp\left(\frac{V_{u2}-V_2}{nU_t}\right) - \frac{I_\omega}{Q}$$



also $y = x_2 = 2w \exp\left(\frac{V_2}{nU_t}\right)$

[6]

[6]

iv) Given the biquad filter has cut-off frequency, $\omega_0 = 2\pi.10000$ rad/s, select a suitable current for I_1 given that the filter capacitor is C = 10 pf , n = 1.23 and U_t = 25mV.

$I_i = CnU_t\,\omega_0 = 10pf \times 1.23 \times 25mV \times 2\pi.10000\ rad/s = 19nA$

[1]

b) The log-domain filter is classed as a companding filter. Explain why companding is advantageous in such filters.

Companding can increase the usuable dynamic range through compression of the input signal, processing in the non-linear domain and then expansion. Large signals get compressed, small signals get expanded above the noise floor of the filter resulting in an overall increase in usable dynamic range of a fixed dynamic range of the filter.

[3]

4. a) Figure 4.1 shows a NMOS sampling switch to be used in a switched capacitor circuit. The parameters of M1 are $(W/L)_1 = 10\mu m/1\mu m$, $C_{ox} = 7\ fF/\mu m^2$, $V_{th} = 0.7$ V, CK = $V_{DD} = 3$ V and $C_H = 1$ pf. The total charge in the inversion layer, when the switch is on, is given by:

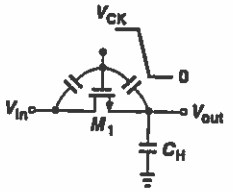
$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{th})$$

i) Explain the errors caused due to charge injection and clock feed. Derive equations that show how the output voltage will change due to these errors, assuming the charge injection is split equally between the source and the drain.

- Charge injection: When a MOSFET is conducting, there is a charge in the inversion layer defined by $Q_{ch} = WLC_{ox}(V_{GS} - V_{th})$. When the MOSFET turns off this charge must escape through the source and drain terminals of the device. When the charge is deposited on the hold capacitor it causes a change, ΔVout in output voltage giving (assuming an equal split):

$$\Delta V_{out} = \frac{Q_{ch}}{2C_H} = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{th})}{2C_H}$$ [2]

- Clock Feedthrough: The MOSFET gate source/drain overlap capacitances couple clock transition changes on the hold capacitor causing a change in the output voltage:



$\Delta V_{out} = \frac{V_{CK} W C_{ov}}{W C_{ov} + C_H}$ where C_{ov} is the overlap capacitance. [2]

[Total 4 points]

ii) Using the output voltage equations derived in 4i), calculate the total change in output voltage due to charge injection and the total change due to clock feed-through. Based on your result, specify which is more significant. You may assume the overlap capacitance $C_{ov} = 0.08$ fF and an input voltage $V_{in} = 0$ V.
Charge injection: ΔVout= 10 x 1 x 7f (3-0-0.7)/2x1p =80.5mV [1]
Clock feedthrough: ΔVout = 3 x 10x10^{-6} x 0.08 x 10^{-15} / 3x10 x 10^{-6} x 0.08 f + 1p =2.4nV [1]
Therefore charge injection is the most significant.

[Total 2 points]

iii) Show that the output voltage contribution due to charge injection results in a non-unity gain error and constant offset. Plot a graph indicating the value of the offset and the slope.

$$V_{out} = V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{th})}{2C_H}$$

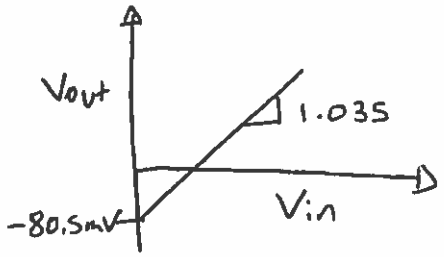
$$V_{out} = V_{in}(1 + \frac{WLC_{ox}}{2C_H}) - \frac{WLC_{ox}(V_{DD} - V_{th})}{2C_H}$$

$$\frac{WLC_{ox}}{2C_H} = 35mV$$

$$V_{out} = V_{in}(1.035) - 80.5mV$$

Slope = 1.035, Y-intercept=-80.5mV [2]

Graph:

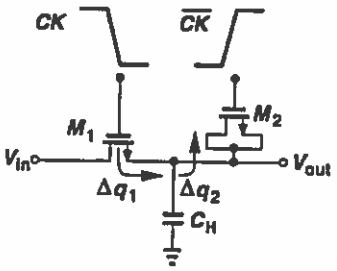


[1]

[Total 3 points]

iv) Propose a single method that reduces both charge injection and clock feed-through. Draw schematics and show equations to justify your answer.

Including a dummy transistor can remove both charge injection and clock feed-through:



Charge injection from M1 is absorbed to create the channel of M2. For this to occur $\Delta q_1 = \Delta q_2$ where

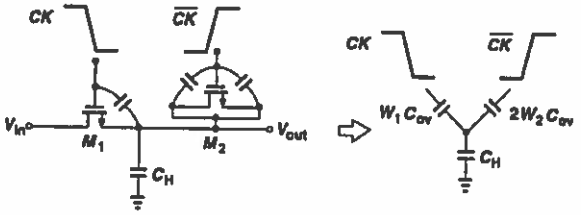
$$\Delta q_1 = \frac{W_1 L_1 C_{ox}}{2}(V_{CK} - V_{in} - V_{TH1}).$$

and

$$\Delta q_2 = W_2 L_2 C_{ox}(V_{CK} - V_{in} - V_{TH2})$$

Therefore we can choose $W_2 = 0.5W_1$, $L_2 = L_1$ to ensure $\Delta q_1 = \Delta q_2$ and compensate for charge injection. [2]

Because $W_2 = 0.5W_1$ clock feedthrough also gets suppressed:



- Total charge in V_{out} is zero since

$$-V_{CK}\frac{W_1 C_{ov}}{W_1 C_{ov} + C_H + 2W_2 C_{ov}} + V_{CK}\frac{2W_2 C_{ov}}{W_1 C_{ov} + C_H + 2W_2 C_{ov}} = 0.$$

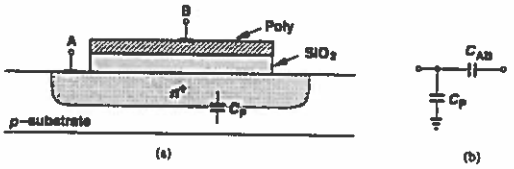
[2]

[Total 4 points]

b) Figure 4.2 shows a circuit diagram of a switched capacitor non-inverting amplifier.

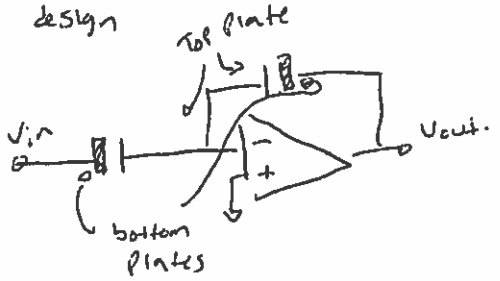
i) Explain the necessity of bottom plate sampling in this design and draw a schematic of the amplifier indicating which sides of the capacitors are the bottom plates.

Capacitors implemented in CMOS have a top polysilicon later and a bottom plate, which is a heavily doped n+ region. Therefore the bottom plate has a parasitic junction capacitance, Cp, to the substrate which is usually about 10-20% the oxide capacitance:



(a) Monolithic capacitor structure, (b) circuit model of (a) including parasitic capacitance to the substrate.

Since the input capacitance of the opamp affects speed and precision in SC circuits, it needs to be well defined. Therefore we always connect the top plate to the input of the opamp, and therefore at the high impedance node, and the bottom plate at a low impedance node, which in this design is the input and output. This mimises the effect of the parasitic but also avoids injection of substrate noise. [3]
In this design:

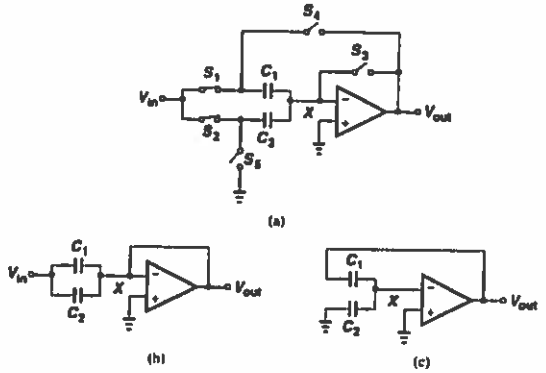


[1]

[Total 4 points]

ii) Draw an equivalent circuit of Figure 4.2, which has a gain of 2 and a lower gain error. Explain its operation.

Switched capacitor multiply by two circuit. Absence of capacitor in feedback during sampling phase leads to lower gain error



$$Q_1 = C_1 \cdot V_{in}$$
$$Q_2 = C_2 \cdot V_{in}$$
$$C_1 = C_2 = C$$
$$V_{out} \cdot C = Q_1 + Q_2$$
$$V_{out} = 2 \cdot V_{in}$$

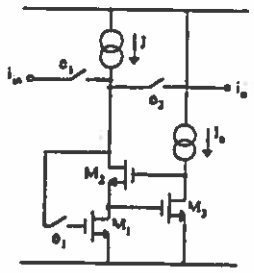
[2 points for circuit , 1 point for equations, Total 3 points]

5. a) Figure 5.1 depicts a switched current memory cell.

i) State two limitations of the circuit shown in figure 5.1 and draw an improved schematic which compensates for these and has improved output resistance.

The switched current memory cell is susceptible to charge injection from the switch in addition to the drain source voltage variations between the sampling and readout phases which will cause an error in the output current. Increasing the output impedance through cascoding reduces the dependency of I_D on V_{DS}. This is achieved using a regulated cascode: [2]

Regulated Cascode Cell



$$R_o = g_{m2}g_{m3}r_{ds1}r_{ds2}r_{ds3}$$

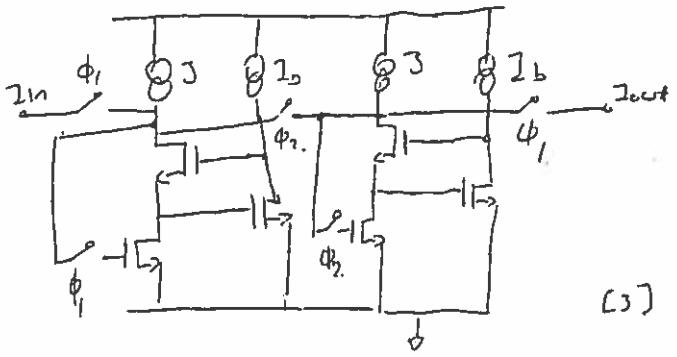
[2]

Charge injection effects from switch Φ1 can also be further reduced by operating M1 in the triode region since , $g_{m1}=2\beta V_{DS}$ and therefore error is independent of input signal.

[Total 4 points]

ii) Using your schematic from part 5.a.i, design a memory cell that is non-inverting.

For non-inverting just cascade two cells:



[3]

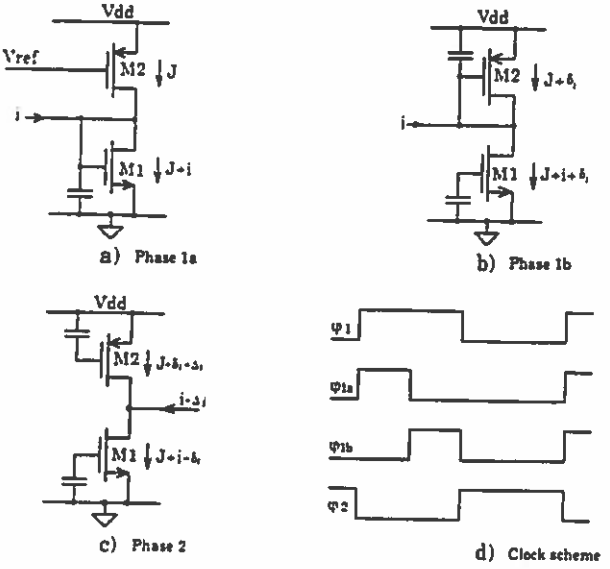
[Total 3 points]

iii) Figure 5.2 depicts a switched capacitor memory cell capable of error compensation. Explain its operation, stating the drain currents of M1 and M2 during each phase of the clock and derive the compensated output current.

S^2I memory cell provides error reduction using coarse and fine memory to store the charge injection then subtract it. [1]

S^2I memory cell operation

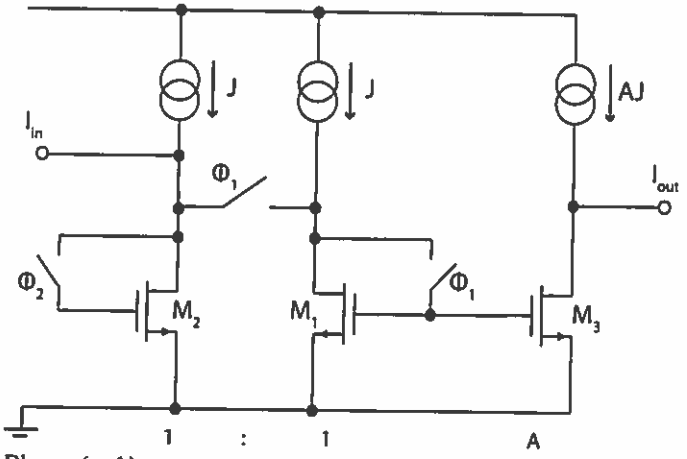
- Phase 1a: $I_{D1}=J+i$, $I_{D2}=J$
- Phase 1b: $I_{D1}=J+i+\delta_1$, $I_{D2}=J+\delta 1$
- Phase 2: $I_{D1}=J+i+\delta_1$, $I_{D2}=J+\delta_1+\Delta_1$
- $I_{out}=I_{D1}-I_{D2}=i-\Delta_1$
- Δ_1 Is an input independent charge injection [1 point for each phase and diagram]



[Total 4 points]

iv) Figure 5.3 depicts a switched current cell. Derive its input/output characteristic and identify which function this block performs. You are required to state the transfer function in the z-domain.

Switched current differentiator



Phase (n-1)

Φ2: $I_{D2}(n-1)=I_{in}(n-1)+J$

Phase (n)

Φ1: $I_{D1}(n)=I_{in}(n) - I_{in}(n-1)+J$

$I_{D3}(n)=AI_{in}(n) - AI_{in}(n-1)+AJ$

$I_{out}(n) = A(I_{in}(n)- I_{in}(n-1)$: This is a difference equation

Taking Z-transforms:

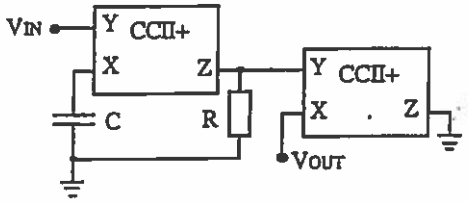
$$I_{out}(z) = A(I_{in}(z) - I_{in}(z)z^{-1})$$

$$\frac{I_{out}(z)}{I_{in}(z)} = A(1 - z^{-1})$$

[Total 5 points]

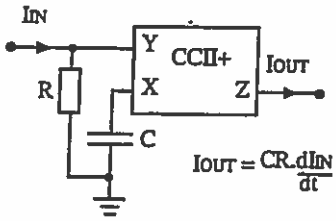
b) This question concerns current conveyors. Design, using CCII+ current conveyors, a voltage mode and a current mode differentiator.

Voltage mode differentiator:



$$V_{out} = RC\frac{dV_{in}}{dt}$$ [2]

Current mode differentiator:



[2]

[Total 4 points]

6. Figure 6.1 shows a voltage measurement system which uses an operational amplifier (OA) and a novel integrating analogue to digital converter to encode detected voltage signals. The detected signal are first converted to a current through a voltage to current converter (V/I) and then to a spike train through an integrate and fire neuron (I/F). The 8 bit counter is used to count the number of spikes in a fixed period T_{reset} which is then stored in memory. The whole system works off a 1 V supply.

a) Desribe a technique which allows detection of very small voltage signals which exist below the 1/f noise floor of the operational ampifier. Include diagrams showing the operation of this technique and how the frequency spectrum of the signal and noise is shaped in each stage.

We can use the chopper stabilization technique: We up-modulate our input signal using square wave modulation to a frequency which is above 1/f noise spectrum of our amplifier. We then amplify and then down modulate at the output with the same square wave signal. At the output however noise and offset get up-modulated which can then be removed using a low-pass filter.

[2]

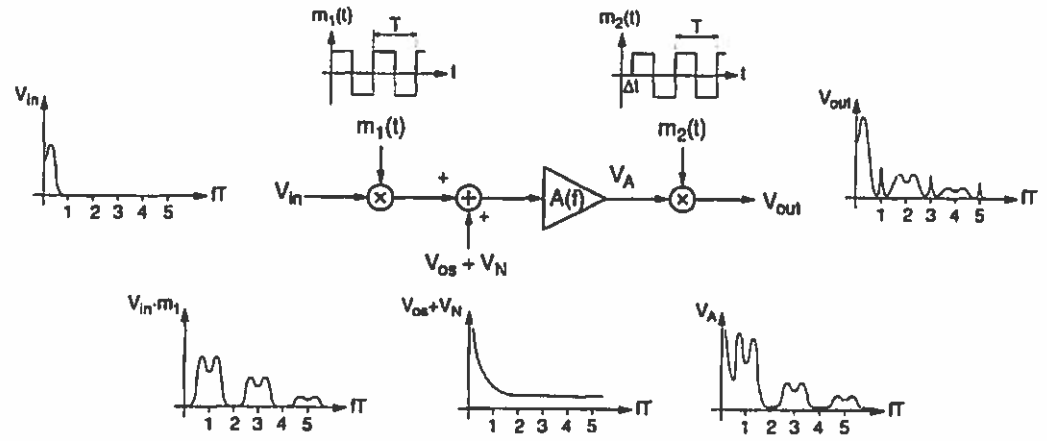


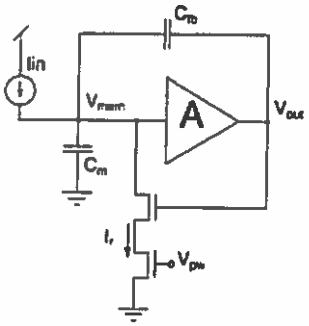
Fig. 9. The chopper amplification principle [19].

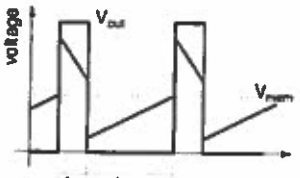
[3]

[Total 5 points]

b) Sketch an integrate and fire circuit which can be used in this design and describe its operation. Derive equations for the pulse width and frequency.

We can use an axon-hillock integrate and fire neuron. Current is used to charge the capacitor which resets the voltage after it passes the threshold of the amplifier causing a spike.





$$t_L = \frac{C_{fb} + C_m}{I_{in}} \Delta V_{mem} = \frac{C_{fb}}{I_{in}} V_{dd}$$

$$t_H = \frac{C_{fb} + C_m}{I_r - I_{in}} \Delta V_{mem} = \frac{C_{fb}}{I_r - I_{in}} V_{dd}$$

Frequency $\propto I_{in}$

Pulse width $\propto 1/I_r$ for $I_r \gg I_{in}$

[2 points for circuit and explanation, 1point for graph, 2 points for derivations]

[Total 5 points]

c)

i) Given that the maximum output current is limited to I_{out} = 100 nA, chose a suitable capacitor value for your integrate and fire circuit such that the spike frequency is always less than 5 kHz. You may assume the refractory current I_r=1nA.

V_{dd}=1V, I_{in}=100nA, I_r=1nA
$T_{total} = t_h + t_l$ = 1/5KHz
$C_{fd}.\ V_{dd}/I_{in} + C_{fd}.\ V_{dd}/(I_r - I_{in})$ = 1/5KHz
C_{fd}= 10pf

[3]

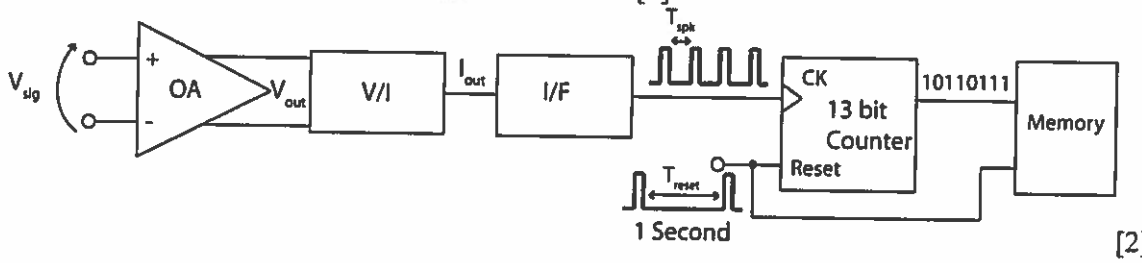
ii) Calculate the maximum allowable reset time T_{reset} such that the counter never overflows for this current.

8 bit counter means 2^8 counts therefore Maximum $T_{reset} = 2^8/5x10^3$ = 51.2 msec

[2]

d) Explain why this method of integration is more efficient in area when integrating over a very long period (time constant τ = 1 sec). Show how the system, shown in figure 6.1, can be modified to achieve this integration.

This method is more efficient since the integration time constant can simply be set by T_{reset} and selecting a suitable counter such that it does not overflow. Implementing a one second time constant in continuous time analogue would require a huge resistor and capacitor which could not be implemented on chip. Therefore we would require off-chip components. [2]
For T_{reset}=1 second we need n=12.28= 13bit counter. [1]



[2]

[Total 5 points]