EE4-16
EE9AC6

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2012

MSc and EEE PART IV: MEng and ACGI

Corrected Copy

ANALOGUE SIGNAL PROCESSING

Friday, 11 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P. Georgiou
Second Marker(s) : K. Fobelets

Special instructions for students

Unless otherwise stated the following parameters have the following definitions:

V_{DS} : Drain Source Voltage.

V_{GS} : Gate Source Voltage.

V_{TH} : Threshold Voltage.

U_t : Thermal Voltage.

n : Weak Inversion Slope factor.

g_m: Transconductance.

1.

a) State two advantages and two disadvantages of using analogue circuits for signal processing.

[4 marks]

b) The equation for weak inversion operation of a MOS transistor is defined as follows:

$$I_{DS(wi)} = I_{D0}\frac{W}{L}e^{\frac{V_{GS}}{nU_t}}\left(1-e^{\frac{-V_{DS}}{U_t}}\right)$$

Derive the transconductance and transconductance efficiency of the device assuming it is in weak inversion saturation and current I_{D0} is constant. State any assumptions you make.

[2 marks]

c) Figure 1.1 shows a common source amplifier with a diode-connected load. Both transistors are operating in weak inversion. The gain of this amplifier is given as:

$$Av = \frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{m2}}$$

whereby g_{m1} and g_{m2} are the transconductances of transistors M1 and M2 respectively.

Given that the lengths of M1 and M2 are sized at $L_1=L_2=1\mu m$, select suitable widths for M1 and M2 such that the gain of the amplifier Av = -10 and the area is kept to a minimum. Assume the minimum allowable width is $W=1\mu m$ and both NMOS and PMOS have the same I_{D0} current.

[4 marks]

d) Figure 1.2 shows a cascade of amplifiers whereby each stage uses the circuit from Figure 1.1. For the following question assume that the total stages M=2 and the constant P=1 for weak inversion operation.

(i) The total output noise of this system is given by the following noise resource equation:

$$v_{no}^2 = \sum_{i=1}^{i=M} v_{ni}^2 G_i^2 = \sum_{i=1}^{i=M}\left(n_i\frac{K_w}{(I_i/n_i)^p}\cdot\Delta f + n_i\frac{K_f}{(A_i/n_i)}\cdot\ln\left(\frac{f_h}{f_l}\right)\right)G_i^2$$

Calculate the total noise v^2_{no} at the output assuming the amplifier has a DC drain current $I_D=100nA$, $K_w=1x10^{-15}\ V^2\ C$, $K_f=3.5x10^{-18}\ Hz/F^2$, $\Delta F=100$ Hz, $f_h=100Hz$, $f_l=1Hz$.

(ii) Propose two methods with which the noise could be reduced even further.

[10 marks]

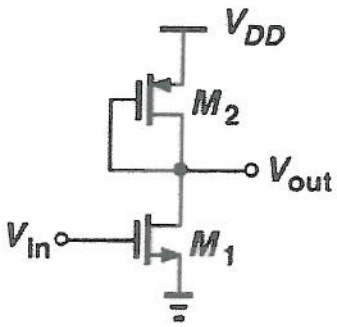


Figure 1.1

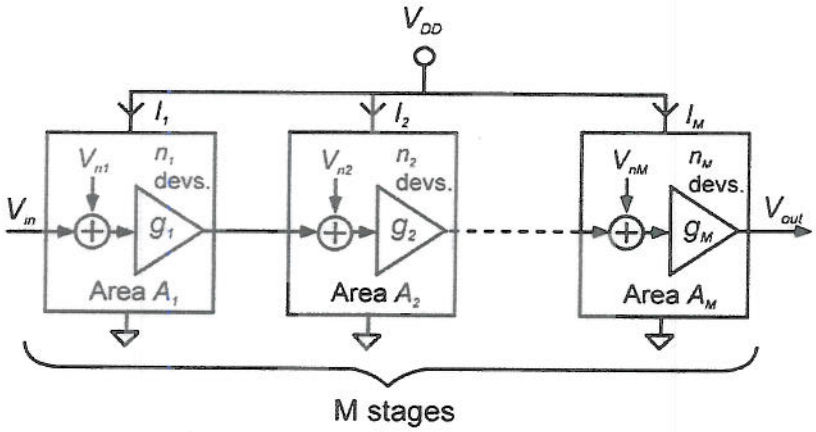


Figure 1.2

2.

a) State and derive the translinear principle (TLP) for a loop of MOS transistors working in weak inversion.

[4 marks]

b) List the three factors which could contribute to non-ideal behaviour in a translinear circuit.

[3 marks]

c) Figure 2.1 shows a translinear circuit made up of NMOS transistors biased in weak inversion.

(i) Derive I_{out} as a function of X by applying the translinear principle. Show all necessary steps.
(ii) What is the function of the circuit shown in Figure 2.1 ?

[5 marks]

d) The equation for a vector normaliser circuit is given as:

$$u = \frac{x}{\sqrt{x^2 + y^2}}$$

Synthesise a translinear circuit to provide this function minimsing the circuit where possible. You may only use Type A cells.
Hint: The function may be decomposed into the functions $u = \frac{x}{r}$ and $r = \sqrt{x^2 + y^2}$.

[8 marks]

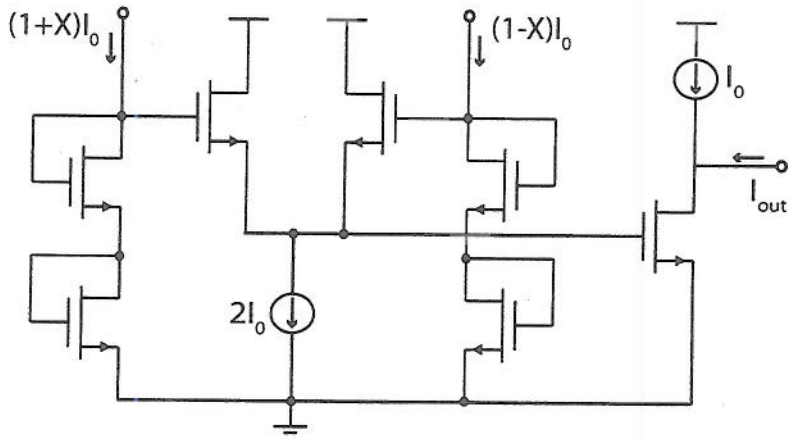


Figure 2.1

3.

a) Figure 3.1 shows a block diagram of a current-mode integrator, with an input X and an output Y. f() and g() represent non-linear functions which compress and expand the signal such that input-output relationship of the integrator is linear and given by:

$$Y = \tau \int X \cdot dt$$

Given that the expansive function is defined as $g(V_c)=\beta(V_g-V_{th})^2$, derive the function f(x) such that linear integration is achieved. All constants should be grouped to represent a current I_0, with the function f(x) composed of just I_{in}, I_{out} and I_0.

[5 marks]

b) The transfer function of a biquad filter is defined in state space representation by the following equations:

$$\dot{X}_1 = \frac{-\omega_0}{Q} X_1 - \omega_0 X_2 + \omega_0 U_1$$

$$\dot{X}_2 = \omega_0 X_1 - \omega_0 U_2$$

$$Y = X_1$$

whereby Y is the output and U_1 and U_2 are the inputs and X_1 and X_2 are the states.

(i) Show that this represents a low pass filter bi-quad. State any assumptions you make.

[2 marks]

(ii) By using the mappings below show how these linear equations can be mapped to non-linear log-domain design equations. State any assumptions you make.

$$X_1 = I_1 \exp\left(\frac{V_1}{nU_t}\right) \qquad X_2 = I_2 \exp\left(\frac{V_2}{nU_t}\right) \qquad U_2 = I_{U2} \exp\left(\frac{V_{U2}}{nU_t}\right)$$

[5 marks]

(iii) With these log-domain design equations, sketch a schematic of the final log domain filter using weak inversion MOS transistors.

[6 marks]

(iv) Given the biquad filter has cut off frequency, $\omega_0=2\pi.10000$ rad/s , select a suitable current for I_1 given that the filter capacitor is C=10pf , n=1.23 and U_t=25mV.

[2 marks]

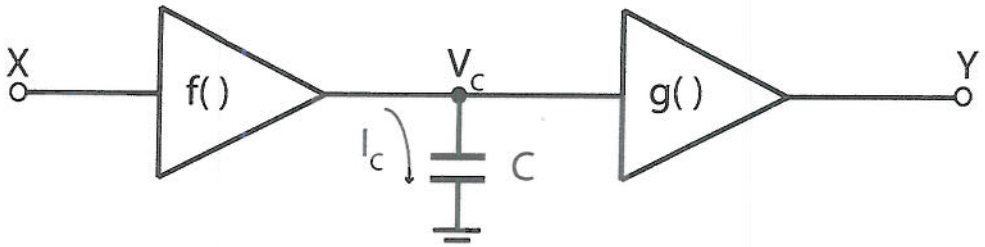


Figure 3.1

4. Figure 4.1 shows a NMOS sampling switch, M_1, connected to a hold capacitor, C_H, to be used in the switched capacitor circuit Figure 4.2. When the switch is on, CK=V_{DD}, current conduction is defined by triode region of operation as:

$$I_{D1} = (\mu_n C_{ox})(W / L)(V_{DD} - V_{in} - V_{TH})V_{DS}$$

a) State four non-desirable effects which could be caused by the switch M_1 and affect the output, V_{out}.

[4 marks]

b) Draw a sketch showing how the on resistance of the switch M_1 varies with the input, V_{in} at a fixed V_{DD}.

[2 marks]

c) Propose a method with which the switch resistance could be made less variable over the entire operating range. Sketch a diagram of the new switch.

[2 marks]

d) When M1 is ON, there is a charge in the inversion layer of the device defined as:

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH}),$$

this charge gets equally distriubuted to the source and drain of the device when the switch turns OFF.

Calculate the width and length of transistor M1 $(W/L)_1$, such that total error induced in the output, ΔV_{out}, does not exceed 10%. You may assume, V_{in}=1.65V, C_H=16pf , with oxide capcitance per unit micron C_{ox}=0.064 pF /u^2, V_{DD}=3.3V, V_{TH}=0.65V and a minimum length L_1=1μm.

[4 marks]

e) Figure 4.2 shows a circuit diagram of a unity gain sample and hold circuit.

(i) Derive the relationship between V_{out} and V_{in} confirming it is a sample and hold circuit. You may use Φ1 to represent the sampling phase (S_1 and S_2 closed, S_3 open) and Φ2 to represent the hold phase (S_3 closed, S_1 and S_2 open).

(ii) Draw the timing diagrams of switches S1, S2 and S3 during the sample and hold periods of operation such that any non-ideal effects due to switching are minimised.

(iii) Draw an improved circuit schematic of Figure 4.2 which allows cancellation of non-ideal effects due to the switches and includes all clock generation circuits.

[8 marks]

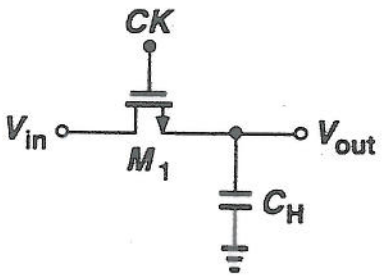


Figure 4.1

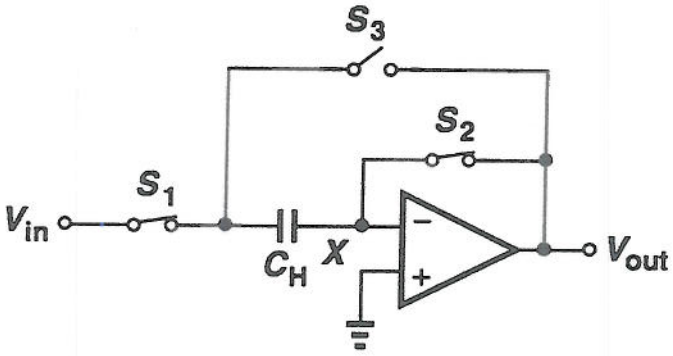


Figure 4.2

5.

a) Explain the principle of chopper stabilisation with diagrams showing the operation and how the frequency spectrum of the signal and noise is shaped in each stage.

[5 marks]

b) Figure 5.1 shows a multistage autozeroing amplifier.

(i) Explain how this amplifier removes any offset in the input stage and derive the input referred offset , $V_{os\text{-}res}$. You may use only two stages in your explanation.

[4 marks]

(ii) For your derivation in part b.i , assuming a three stage cascade of autozeroing amplifiers, each with a gain A=10 and an offset V_{os}=100mV, calculate the value of the storage capacitor, $C_1=C_2=C_3$, such that the total input referred noise $V_{os\text{-}res}$ <100μV. You may assume that a charge of $q_{inj}=6\text{x}10^{-12}$ C is inserted each time the switch closes.

[4 marks]

c) Figure 5.2 shows a switched capacitor correlated double sampling integrator.

(i) Derive the output voltage of the integrator V_{out} for both phases Φ_1 and Φ_2 showing how this removes any offset in the amplifier.

[5 marks]

(ii) Show, with the aid of a sketch, how the circuit in Figure 5.2 can be modified to accommodate wideband operation.

[2 marks]

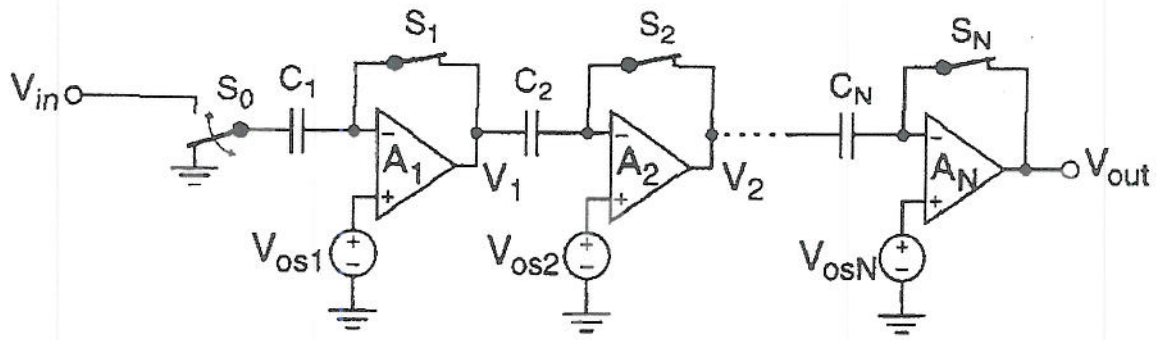


Figure 5.1

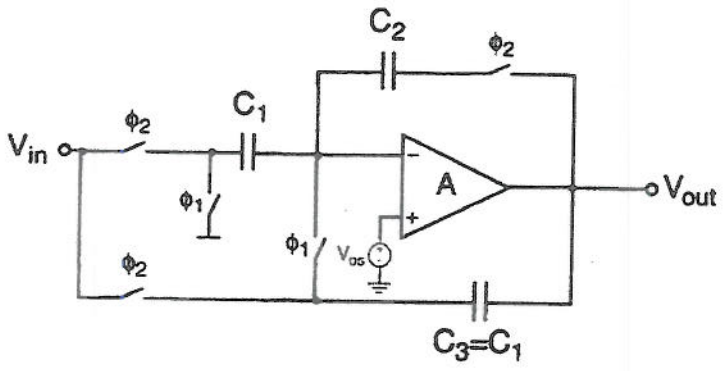


Figure 5.2

6. Figure 6.1 shows a differential pair, where transistors M_1 and M_2 are operating in the weak inversion region. Their associated currents are given by:

$$I_1 = I_0 exp\left(\frac{V_{G1} - V_{S1}}{nU_t}\right), I_2 = I_0 exp\left(\frac{V_{G2} - V_{S2}}{nU_t}\right)$$

a) Show that the output current I_1 can be represented by the following equation:

$$I_1 = \frac{I_B}{1 + exp\left(\frac{V_{G2} - V_{G1}}{nU_t}\right)}$$

[6 marks]

b) Figure 6.2 shows a generalised ion channel model of a neuron in the Hodgkin and Huxley formalism. The activation variable (s_∞), time activation (ds/dt), and ion-current of the channel (I_K), are given be the following equations:

Activation variable:

$$s_\infty(v_{mem}) = \frac{1}{(1 + \exp((v_s - v_{mem})/nU_t))}$$

Time activation:

$$\frac{ds}{dt} = \frac{s_\infty(v_{mem}) - k \cdot s}{\tau_s}$$

Ion-current:

$$I_K = g_K \cdot s \cdot (v_{mem} - v_K)$$

(i) Sketch a circuit topology which could implement the time activation variable s derive the time constant τ_s and gain k. Hint: The output of your circuit should be a current I_{out} which at steady state ($t=\infty$) is equal to $I_{out}=I_B.s$ when the input is $I_{in}=I_B.s_\infty$.

[6 marks]

(ii) The transconductance of the ion channel may be defined by the following equation:

$$g_K \cdot s \approx \frac{I_s}{2nU_t}$$

whereby g_K is a constant transconductance and $I_s=s.I_B$ is a current which is modulated by the activation variable s.

Using a suitable circuit which gives this relationship and the results of part a and b or otherwise sketch the full circuit schematic of the ion channel shown in Figure 6.2.

Hint: The input current I_s is equal to the output current I_{out} from the previous stage and the function $g_K.s$ can be generated from a similar circuit to Figure 6.1.

[8 marks]

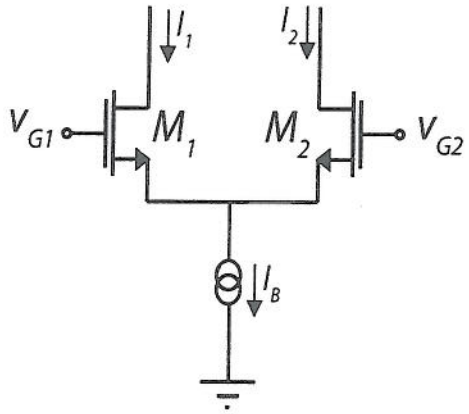


Figure 6.1

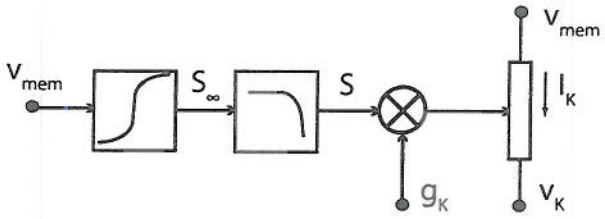


Figure 6.2

1.(a) Theory.

[4]

(b) Transconductance:

$$g_{m(wi)} = \frac{I_{DS(wi)}}{nU_t}$$

Transconductnace efficiency:

$$\frac{g_m}{I_{DS(wi)}} = \frac{1}{nU_t}$$

[2]

(c)Av=-gm1/gm2=W1.L2/L1.W2=W1/W2 for equal lengths.
For Av=-10 therefore W1=10um and W2=1um.

[4]

(d)
i) Student needs to realise that number of devices n=2 with a total area A= 10x1 +1x1=11u^2. Also the noise contribution of the first stage is multipled by 100 at the output.

The equation for the system can be written as:

$$v_{no}^2 = n_1 \frac{K_w}{(I_1/n_1)} \cdot \Delta f + n_1 \frac{K_f}{(A_1/n_1)} \cdot \ln\left(\frac{f_h}{f_l}\right)\left(Av_1.Av_2\right)^2 + n_2 \frac{K_w}{(I_2/n_2)} \cdot \Delta f + n_2 \frac{K_f}{(A_2/n_2)} \cdot \ln\left(\frac{f_h}{f_l}\right)\left(Av_2\right)^2$$

[4]

Assuming identical stages simplifies to:

$$v_{no}^2 = n_1 \frac{K_w}{(I_1/n_1)} \cdot \Delta f + n_1 \frac{K_f}{(A_1/n_1)} \cdot \ln\left(\frac{f_h}{f_l}\right)\left[\left(Av_1.Av_2\right)^2 + \left(Av_2\right)^2\right]$$

$$v_{no}^2 = 2\frac{K_w}{(100n/2)} \cdot 100 + 2\frac{K_f}{(11u^2/2)} \cdot \ln(100)\left[(100)^2 + (10)^2\right]$$

$$v_{no}^2 = (4\times10^9 K_w + 1.67\times10^{12} K_f)[10100]$$

$$v_{no}^2 = 100mV^2/Hz$$

[4]

ii) To reduce noise we need to reduce noise of the first stage. This can be done by increasing the bias current or increasing the total area of the devices.

[2]

2. (a) Theory: *In a closed loop containing an even number of forward biased junctions, arranged so that there are an equal number of clockwise facing and counterclockwise facing polarities, the product of the current densities in the clockwise direction is equal to the product of the current densities in the counterclockwise direction*

[2]

Derivation from notes:

$$\sum_{n\in CW} V_n = \sum_{n\in CCW} V_n$$

$$V_n = nU_T \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right)$$

$$\sum_{n\in CW} nU_T \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right) = \sum_{n\in CCW} nU_T \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right)$$

$$\sum_{n\in CW} \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right) = \sum_{n\in CCW} \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right)$$

$$\prod_{n\in CW} \frac{I_n}{\lambda_n I_{DO}} = \prod_{n\in CCW} \frac{I_n}{\lambda_n I_{DO}}$$

$$\prod_{n\in CW} \frac{I_n}{\lambda_n} = I_{DO}^{CW-CCW} \prod_{n\in CCW} \frac{I_n}{\lambda_n}$$

$$\prod_{n\in CW} \frac{I_n}{\lambda_n} = \prod_{n\in CCW} \frac{I_n}{\lambda_n}$$

[2]

(b) Area Mistmatch, Finite output resistance, Body effect with explanations.

[3]

(c) TLP 1: $(1+X)^2 I_0^2 = I_3 \cdot I_7$

TLP 2: $(1-X)^2 I_0^2 = I_4 \cdot I_7$

KCL A: $I_4 = 2 \cdot I_0 - I_3$

Rearranging: $I_7 = (1+X^2) \cdot I_0$

KCL B: $I_{OUT} = X^2 \cdot I_0$

This is an absolute circuit.

[5]

(d) Equation must be synthesised:

Can treat as two separate equations: $r = \sqrt{x^2 + y^2}, u = \frac{x}{r}$

Represent each variable as a ratio of currents:

$$x = \frac{I_x}{I_1}, y = \frac{I_y}{I_1}, r = \frac{I_r}{I_1}, u = \frac{I_u}{I_1}$$

Substitute these into the original equations:

$$\frac{I_u}{I_1} = \frac{I_x/I_1}{I_r/I_1} \quad I_u I_r = I_x I_1$$

$$\frac{I_r}{I_1} = \sqrt{\left(\frac{I_x}{I_1}\right)^2 + \left(\frac{I_y}{I_1}\right)^2} \quad I_r^2 = I_x^2 + I_y^2$$

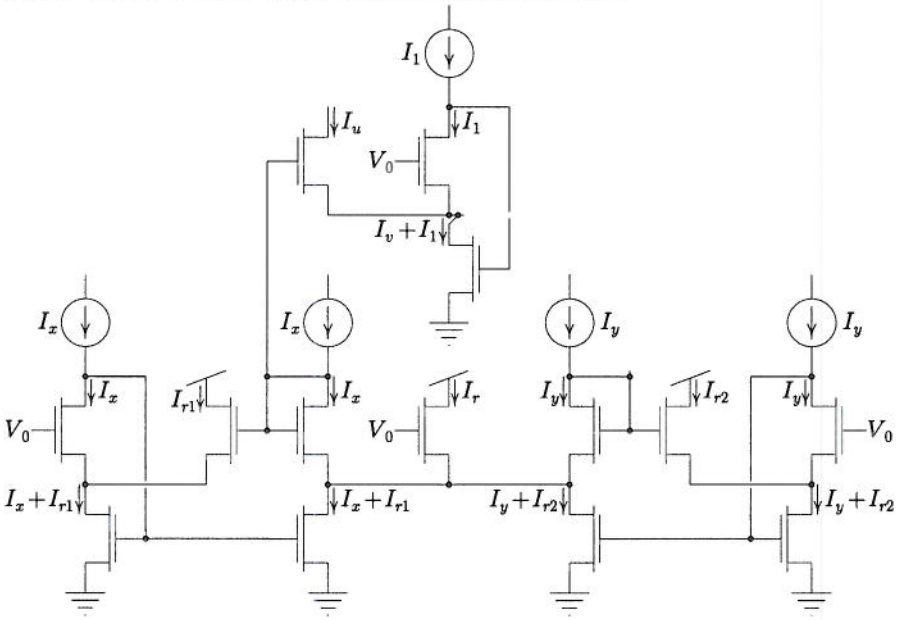
$$I_r = \underbrace{\frac{I_x^2}{I_r}}_{I_{r1}} + \underbrace{\frac{I_y^2}{I_r}}_{I_{r2}}$$

Derive the translinear circuits which need to be designed:

TLP: $I_{r1} I_r = I_x^2$
$I_{r2} I_r = I_y^2$
$I_u I_r = I_x I_1$

KCL: $I_r = I_{r1} + I_{r2}$

Final Circuit after removing redundant loops:



[8]

3.a

$$\frac{dY}{dt} = \tau X$$

$$\frac{dY}{dt} = \frac{d(g(V_C))}{dV_C} \cdot \frac{dV_C}{dt} = \frac{d(g(V_C))}{dV_C} \cdot \frac{I_C}{C} = \frac{d(g(V_C))}{dV_C} \cdot \frac{f(X)}{C}$$

$$\frac{d(g(V_C))}{dV_C} \cdot \frac{f(X)}{C} = \tau X$$

for linear integration.

$$Y = I_{out} = \beta(V_c - V_t)^2 = g(V_C)$$

$$\frac{dY}{dV_C} = \frac{I_{out}}{dV_C} = 2\beta(V_c - V_t) = 2\beta\frac{\sqrt{I_{out}}}{\sqrt{\beta}} = 2\sqrt{\beta I_{out}}$$

$$f(x) = I_C = X\tau C\left(\frac{dY}{dV_C}\right)^{-1} = I_{in}\tau C / 2\sqrt{\beta I_{out}} = I_{in}\sqrt{\frac{I_0}{I_{out}}}$$

$$I_0 = \left(\frac{C}{2\tau\sqrt{\beta}}\right)^2$$

[5]

b)

i) Setting U1=0 and representing in the laplace space it should simplify to:

$$\frac{Y}{U_2} = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$$

[2]

ii) Bookwork, should be able to derive:

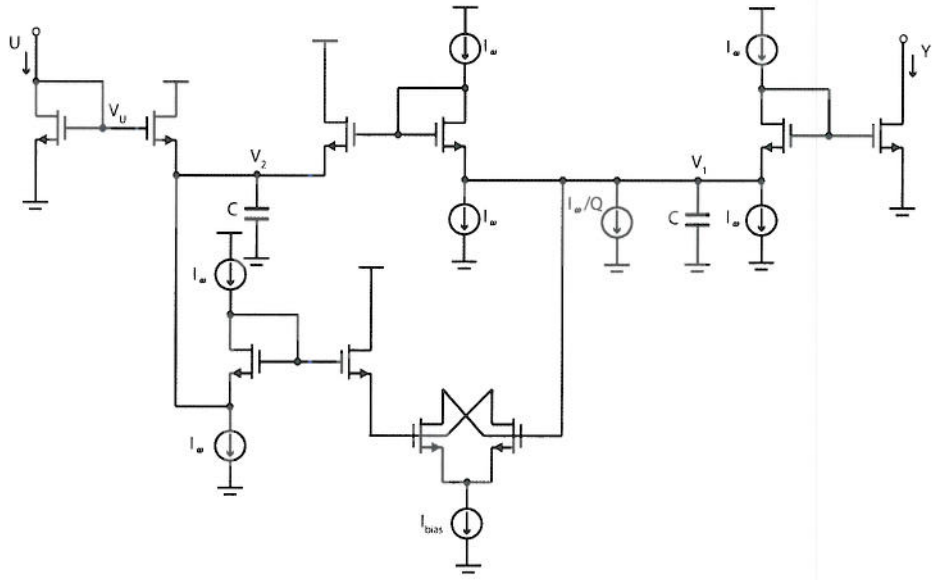
$$C\dot{V}_1 + \frac{I_\omega}{Q} + I_\omega \exp\left(\frac{V_2 - V_1}{nU_t}\right) = 0$$

$$C\dot{V}_2 - I_\omega \exp\left(\frac{V_1 - V_2}{nU_t}\right) - I_0 \exp\left(\frac{V_{U2} - V_2}{nU_t}\right) = 0$$

$$Y = I_\omega \exp\left(\frac{V_1}{nU_t}\right)$$

[5]

iii) Bookwork, should be able to design the following circuit:



[6]

iv)

$$I_\omega = C\omega_0 n U_t$$

I1=10px2π.100x1.23x25m=19.3nA.

[2]

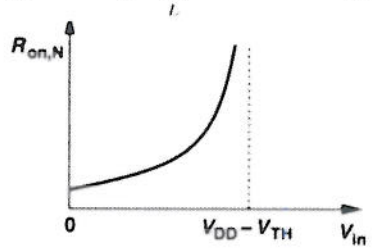
4.

a)

1. Channel Charge injection.
2. Clock Feed through.
3. Sampled Noise.
4. Leakage current.

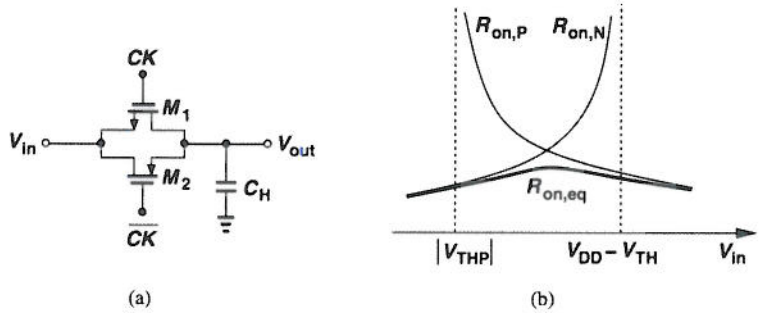
b) (Bookwork):

$$R_{on} = [\mu_n C_{ox}(W/L)(V_{DD} - V_{in} - V_{TH})]^{-1}$$



[2]

c) (Bookwork). Sketch of complementary swtich and how resistance is constant and lower overall over whole input range leading to higher speed.



[2]

[4]

d) Because charge gets equally distibuted, half of Qch will flow into CH causing an error according to:

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H}.$$

Assuming Vout=Vin, a 10% error leads to a ΔV=1.65x0.1=0.165V

Therefore solving for WL:
WL=0.165x2x16p/(0.064p x (3.3-1.65-0.65))=82.5 um^2

Therefore max allowable $(W/L)_1$ =82.5/1.

[4]

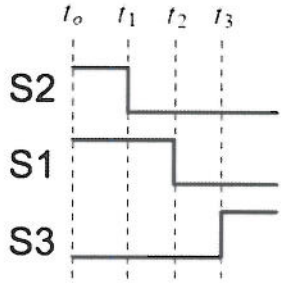
e) i) Sampling Φ1, S1 and S2 are on, S3 is off : QH(Φ1)=Vin(Φ1)CH since Vx=Vout=0
Holding Φ2, S3 is on, S1 and S2 are off: QH(Φ2)=Vout(Φ2)

Chare concevation means QH(Φ1)= QH(Φ2)

Therefore Vout(Φ2) =Vin(Φ1) and Vout(Φ1)=0.

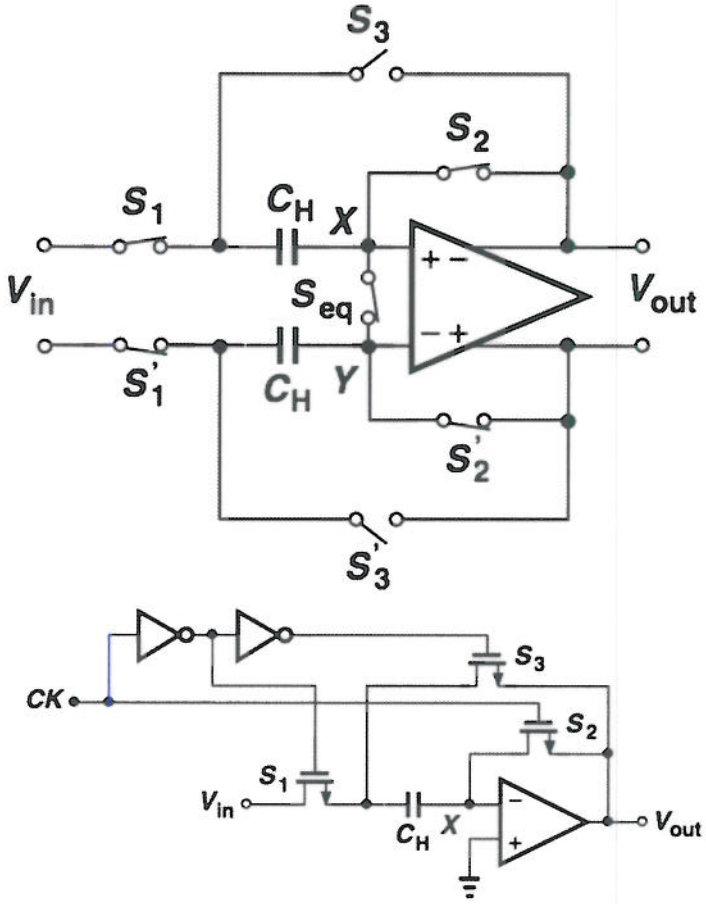
[1]

ii) Need to identify that opening S2 first reduces charge injection from theory.



[2]

iii) Differential circuit with timing circuit from notes, draw one circuit combining the two:



[5]

5.a. Theory. Need to explain with diagrams how 1/f noise is upmodulated the removed by low pass filtering.

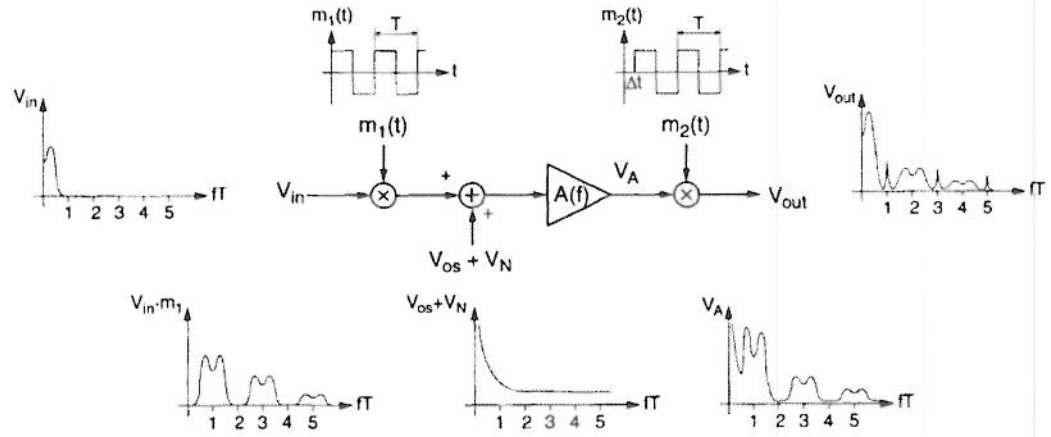


Fig. 9. The chopper amplification principle [19].

[5]

b) i) The amplifier removes offset by opening the switches sequentially. This is because no offset propagates because it is stored then subtracted.

- S_1 is released first, thus charge injection due to S_1 is stored on C_1.
- Charge $Q_2 = C_2(V_1 - V_{os2}A/(1+A))$.
- Then sequentially S_2 is released.
- $V_2 = A_2 (V_{os2} - (V_1 - Q_2/C_2 - q_{inj}/C_2)) = V_{os2} + A_2 q_{inj}/C_2$
- Neither offset nor charge injection of preceding stage propagates !
- Output offset is only affected by last stage:

$$V_{os\text{-}res} \cong \frac{V_{osN} + A_N \cdot \frac{q_{injN}}{C_N}}{A_1 A_2 \cdots A_N}$$

[4]

ii) Substitute values into Vos-res:
$100uV = (10mV + (10x6x10^{-12})/C)/10x10x10$
Rearranging gives C=667 pF.

[4]

c)
i) Need to derive relationship by considering the charges in each capacitor during Φ1 and Φ2 and show how offset is cancelled out in the process :

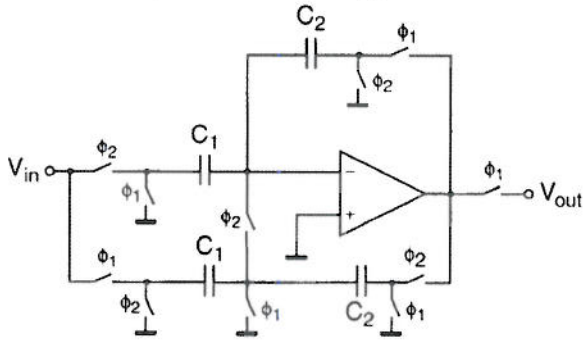
$$v_{out}^2(n) = v_{out}^2(n-1) - (C_1/C_2)v_{in}^2(n)$$

$$v_{out}^1(n) = v_{out}^2(n) + v_{os}$$

[5]

9.

ii) Bookwork, wideband integrator



[2]

10/10

6.a) New derivation:

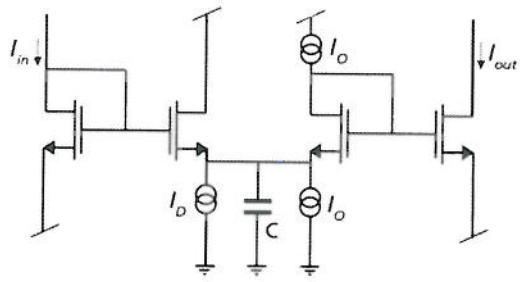
$$I_1 = I_0 exp\left(\frac{V_{G1} - V_s}{nU_t}\right), I_2 = I_0 exp\left(\frac{V_{G2} - V_s}{nU_t}\right)$$

$$I_B = I_1 + I_2 = I_0 exp\left(\frac{V_{G1} - V_s}{nU_t}\right) + I_0 exp\left(\frac{V_{G2} - V_s}{nU_t}\right)$$

$$I_1/I_B = 1/(1 + exp\left(\frac{V_{G2} - V_{G1}}{nU_t}\right)$$

[6]

b) (book work) Circuit is a first order log domain filter:

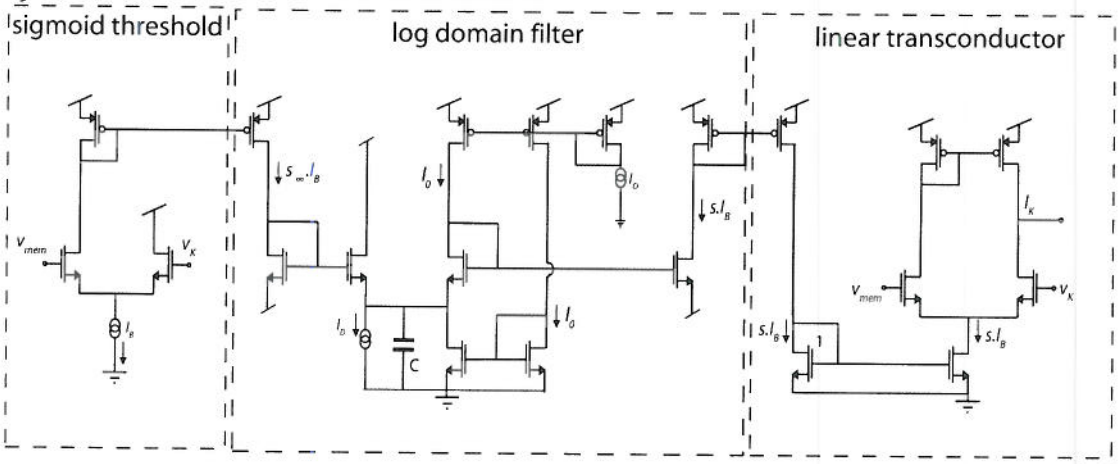


$$\frac{dI_{out}}{dt} = \frac{I_0 I_{in} - I_D I_{out}}{CnU_t}$$

$$I_{out} = I_B.s \qquad \tau_s = \frac{CnU_t}{I_0}$$

[6]

c) Full circuit architecure of ion channel:



[8]