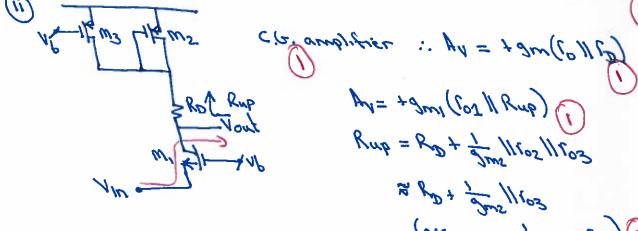
Analogue Electronics 2 (ES.2) 2014 - SOLUTIONS

91-BOOKNOORK/CALCULATION FOR NEW EXAMPLE

(1) (a) source degeneration is when a circuit element (eg. resistor) is connected between the source terminal (in a MOSTET) and the common node (i.e. GND for NMOS and NDO for PMOS).

Disadvantages (compared to (5)

:. Ay = + 9m1 (101) (Ro + gne 1103))



(c) (c) Lycc

Norther generation (c)

Sin Lord

(d) O output voltage range of a differential amplifier depends on the number of devices that are "stacked" which may limit the headroom. This is because all devices must remain in solvention (i.e. V65-VTH = VD6). For example,

using cascode devices will limit the off range. 3

The slew rate of an amplifier gives a measure on how fast the output can change. As this is fundamentally due to the output current charging and discharging the load, the SR is limited by the bias current

(on "drivelility"). (2)

(6) $V^{\Lambda}(0.7) = 18099 = 18_{100} = 500'000$ Vin R2 The out Av(c1)= - K1/2 (1- 1/2) (1+ R2) (2) ((005+1) 00000s -1)005-= :: E=0.1005°10 (f) The typical procedure to improve phase margin in opening. design is to add a compensation capacitance such as to limit the bandwichth so sufficient phase margin is achieved. By exploiting the Miller effect this capacitor value 2 JAME TO Since Vout = Av2 (-ve amphitication stage)

No. - The left was TE Hour a shouting capacitor placed across this will appear as:

Plants | Blants2 | C = Cm(1+ |Av2|) of the input con of t

(m (open bop gain) = 1 out = 1/m . lout 1/2

Vx = -9m3(103/1105)

Tout = Tout x (1/2) = 9m1

First I Tout = 101 (03 1105)

FRE = 101 - 101 + (R+Rm)

FRE = 101 - 101 + (R+Rm)

101 + RL + Rm

101 + RL + Rm

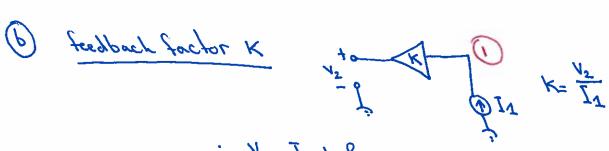
(ii) Row (OR) × 17 (OA). Row (OK) = 101 + Rm (O)

Need to replace hix

Re with a lest EVX

Voltage source SR

and: Rowl = ix



@ Transconductore amplifier : Voltage in, current out

Rout = so

.. - Ve feedback will Increase both

Rin and Road.

(a) Loop gain = (1 + RmGm) so either Rm can be increased or Gm(OL)

Ideally Rm should be hept Small: Reed to increase (m(or)

If bias current is increased eq. 155, this would increase sma but would also decrease (03, (05.1)

(and 100 gm3)

However can increase gms by increasing its (WIL).

@ Rm should ideally be kept small so majority of voltage drop is across the load.

- Given Vop=104 and lout=5mA

However Rm also needs to provide sufficient bias vollage to Sustain device My in saturation.

: V(Rm) > Vos (sat)

-3 Lets design for V(Rm) = 0.5 V 1

: Rm= 0.5V = 100 s ()

3 @ (1) Assuming perfect symmetry, sources of ditt. pair can be connected to AC. ground. (1)

VIN - HE MY Vout

VIN - HE MY

VOUT

(ii) with parasities associated with hodes x and voul.

Win Tike My

Cabi (DB)

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for (1) and (11) OK as Single diagram

Rout = Ruplikdown

grab = Just Cottod + Lot + Lod Rdaun= 9m3103(10511101) +103 + 1051161

: assuming souto so I

Rout & 3m2 lostod + 3m3 los (10211101)

 $V_{\text{by}} = V_{\text{m}} = V_{\text{m}}$

:. Av=-ours[3mtloslod + 0mglos (1011102)]

(c) $3m = \sqrt{2\mu(\omega_{R} \frac{h}{L} \frac{1}{D})}$ $3m_{3} = \sqrt{2(2\omega_{p})(2\omega_{0})} \frac{2\omega_{p}}{2\omega_{p}} = 3h_{p}$ 3m7=12(100H)(2)250h = 353h2

607 = 0.2(250m) = 20KIL 101 = 1 0.2 (200 M) = 25KR 103 = 1 0.1(250m) = 40Ks

105 = 1 = 200KR

316×(20×)(20×)+ (09 = 1 316×(40×)(25×1/200×) = -1688 = 64.568 :. h = - 4m (353 x (20x) (20x) +

Thomas = TR Bout Cont

Cx = (co)(1+ 3m1/3)+c081+c05+c085+c085+0

Rx = 101 11 10511 1 103 2 1 3m3 (assume grace) 1

Since CDB=CSB=B

cont = cost + chest + coss + ches 2 1

Rout = as in (6).

Rx = 1m3 = 31645 = 3.16KD

Pout = 422 KR (from @)

Cont = 5(0.2) + 2(0.2) = 1.4ff

: fpx = 2TT (3.16K) 319f = 157.9 MHZ

fort = 211(1.4ft)(455K) = 5.6d. 4 WHS