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EE3-01
EE9AC1

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2011

MSc and EEE PART III/IV: MEng, BEng.and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Tuesday, 10 May 2:30 pm

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : P. Georgiou

1. (a) Figures 1.1 and 1.2 show two popular biasing schemes typically used in analogue integrated systems. Briefly outline the main feature of each of these circuits.

[4]

For the bandgap voltage reference circuit of Figure 1.1, show that $\delta V_0 / \delta T = 0$ (where T is temperature) if $(R_2/R_3) ln\ [\ I_1/I_2\ ] = 29$ for $V_0 = 1.283\ V$. Assume the temperature coefficient of V_{BE} to be -2.5mV/°C, the collector current of transistor Q_3 is 100μA and the device saturation current is $I_S = 1.2\ x10^{-13}A$. Boltzmann's constant $k = 1.38\ x10^{-23} J/K$ and the electron charge is $q = 1.6\ x10^{-19}C$.

[7]

(b) Show that the circuit of Figure 1.2 can be developed into a current source with output current directly proportional to absolute temperature and virtually independent of supply voltage. Since it is likely that on power-up the output current will fall into a zero current state, sketch a suitable start-up circuit that ensures that this condition will not occur and explain the operation of the circuit.

[9]

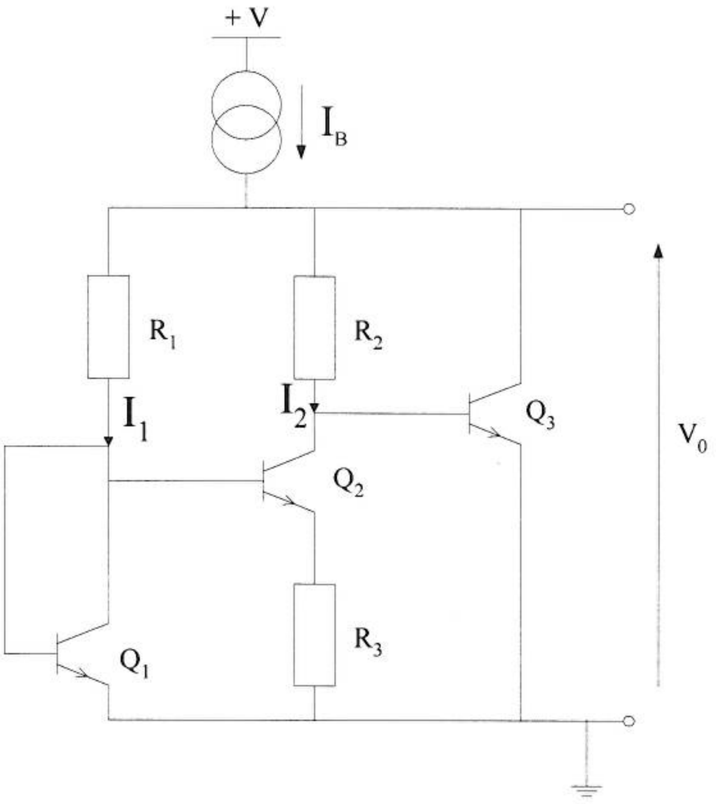

Figure 1.1

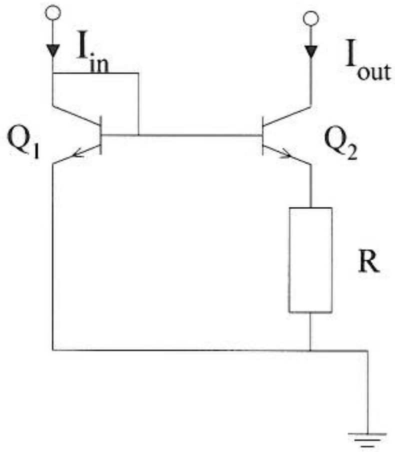

Figure 1.2

2. (a) Sketch a typical circuit diagram for a single-stage fully differential folded cascode CMOS op-amp. Briefly explain the concept of common-mode feedback with reference to your folded cascode op-amp and sketch a common-mode feedback circuit.

[8]

(b) Estimate the low-frequency differential voltage gain, slew rate and gain-bandwidth product of the two-stage CMOS op-amp shown in Figure 2. Aspect ratios of all devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

[10]

(c) Explain qualitatively why the addition of a resistor in series with compensation capacitor Cc improves amplifier stability.

[2]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	*Kp (μA/V2)*	$\lambda (V^{-1})$	$V_{T0} (V)$
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

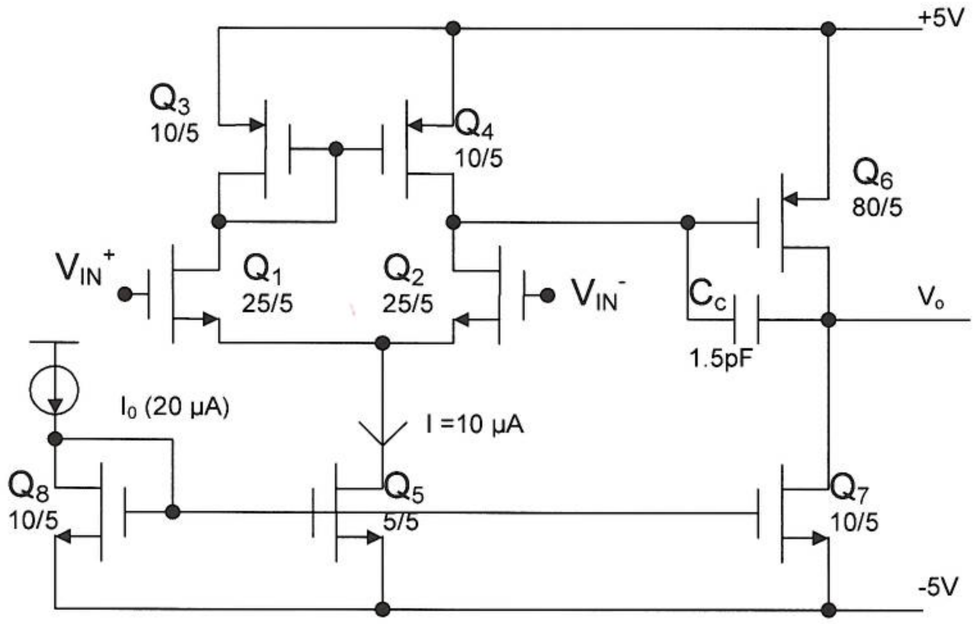

Figure 2

3. (a) Derive an expression for the fundamental limitation imposed on the Dynamic Range (DR) of any high performance A/D converter using the following parameters: V_{ref} is the reference voltage, k is the Boltzmann's constant, T is absolute temperature, R is switch resistance and f_c is the clock frequency of the switch. You may assume that the system settles in 10τ (where τ is the time constant), over one period of the clock frequency.

[8]

(b) A very high resolution analogue-to-digital converter is the oversampling converter sometimes referred to as the sigma-delta modulator. Explain its principles of operation using a diagram where necessary.

[12]

4. (a) Under what operating conditions does the MOSFET of Figure 4.1 realise a linear floating resistor between terminals *A* and *B* ? Explain why the bulk is not connected to the source.

[6]

(b) Discuss three sources of non-linearity in the single MOSFET resistor realisation of Figure 4.1 and suggest one suitable circuit design to help eliminate one or more of these non-linear terms. Show all necessary circuit analysis to confirm your design.

[6]

(c) Figure 4.2 shows a fully differential continuous time integrator using a balanced double differential linear active transresistor. Derive an expression for the time constant of the integrator. You may ignore all bulk effects, and assume all MOSFETs are operating in the triode region.

[8]

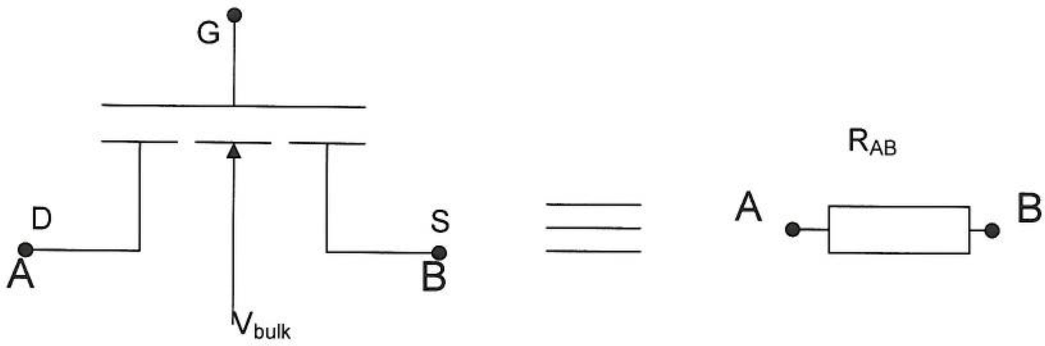

Figure 4.1

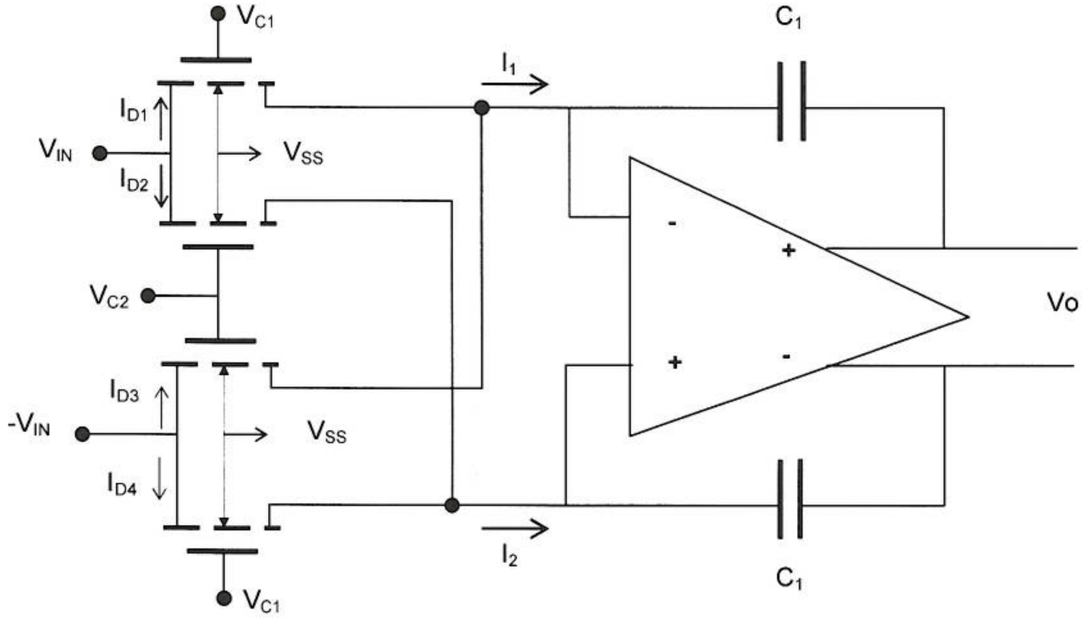

Figure 4.2

5. (a) With the aid of a suitable macromodel, explain the theoretical concept of current feedback and how it results in constant bandwidth amplification. Using a current-feedback op-amp, design a closed-loop non-inverting gain stage with a bandwidth of 10 MHz for a fixed voltage gain of 100. Assume an internal compensation capacitance of 4pF and that the open-loop transresistance gain of the amplifier is very much larger than the amplifier feedback resistor.

[15]

(b) The circuit shown in Figure 5 is a single bit cell of a current-mode algorithmic analogue to digital converter. Briefly describe the operation of the cell and give reasons why this converter is particularly suitable for mixed-analogue and digital VLSI.

[5]

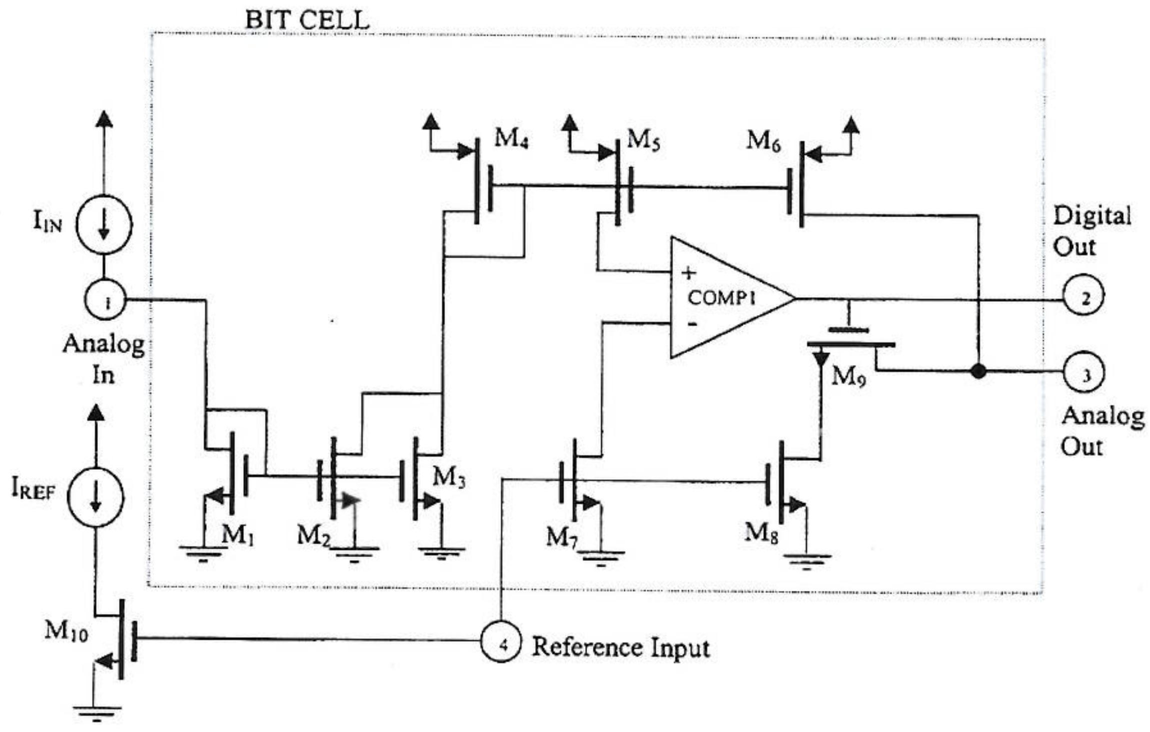

Figure 5

6. (a) Sketch circuits for both a Lossy and differential switched-capacitor integrator. Derive an expression for the transfer function of the differential integrator. Assume clock frequency much higher than the maximum input signal frequency. Also assume the switches are ideal.

[10]

(b) Figure 6 shows one section of a switched capacitor ladder filter. Based on this filter structure, design a 3rd-order Chebyshev low-pass filter with a cut-off frequency of 5 kHz and a 1.0 dB pass band ripple. Assume a clock frequency of 100 kHz. Passive component values for the LC prototype, normalised to 1 rad/s, are $C_1 = C_3 = 2.0236$, $L_2 = 0.994$. In your analysis assume all integrators to be lossless.

[10]

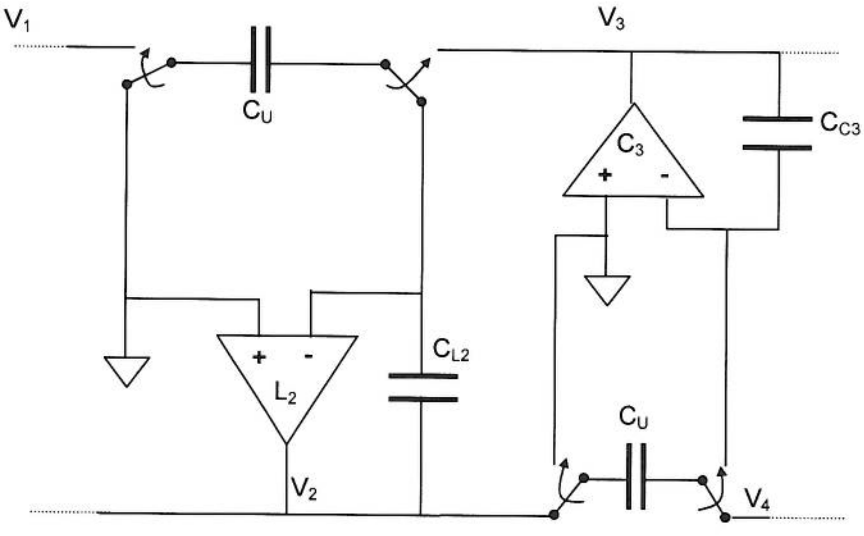

Figure 6

ANALOG - SOLUTIONS

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Q1/ Bandgap voltage reference circuit has almost zero temperature coefficient. Used mainly as stable voltage reference in ICs. 2

PTAT (proportional to absolute temperature) current generator. Output current usually insensitive to power supply voltage. Used as a biasing circuit in most precision ICs. 2

For BG reference :- $V_{BE1} = V_{BE2} + I_2 R_3 \quad (\beta \gg 1)$

Since
$$V_{BE1} - V_{BE2} = V_T \ln (I_1/I_2)$$
then $V_O = V_{BE3} + (R_2/R_3) V_T \ln (I_1/I_2)$

$V_T \ln [I_3/I_S]$ → assume room temp.

For $dV_O/dt = 0$, then $dV_{BE3}/dT = \dfrac{V_T}{T} \dfrac{R_2}{R_3} \ln \dfrac{I_1}{I_2}$

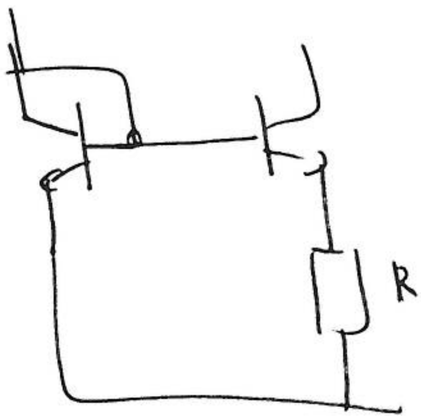
Since $\dfrac{dV_{BE}}{\partial t} = -2.5 mV/°C$, $\dfrac{V_T}{T} = \dfrac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}}$

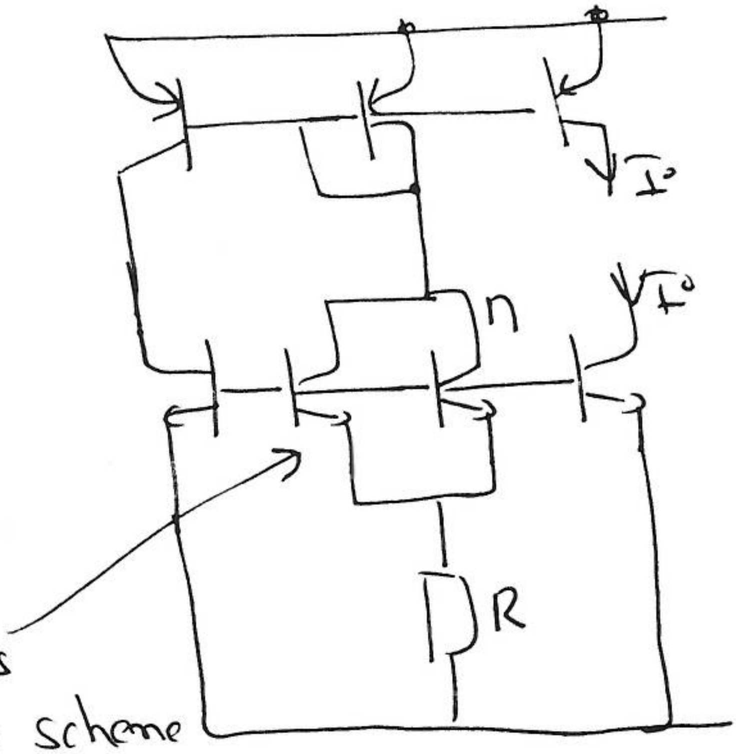
then $\left(\dfrac{R_2}{R_3}\right) \ln \left(\dfrac{I_1}{I_2}\right) = 29$ and so

$$V_O = 1.283 V$$ 3

CT

Question 1 continued. 2



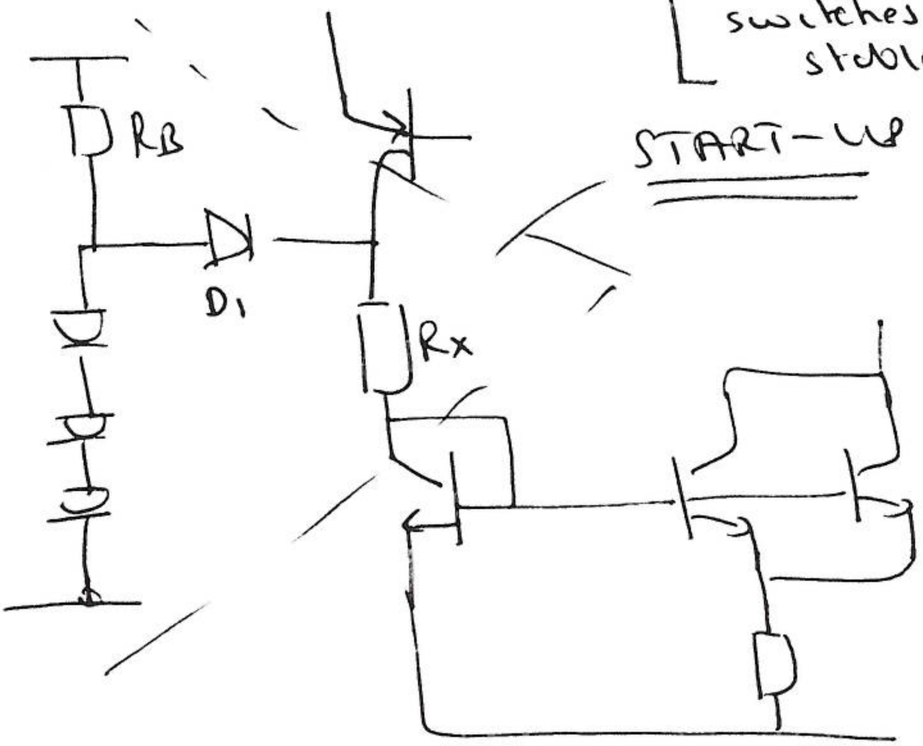


n - emitters
Self biassing scheme
requires Start up. 5

$$I_o = \frac{V_T}{R} \ln [n]$$

[D_1 - conducts on start-up
switches off in stable-state]

START-UP



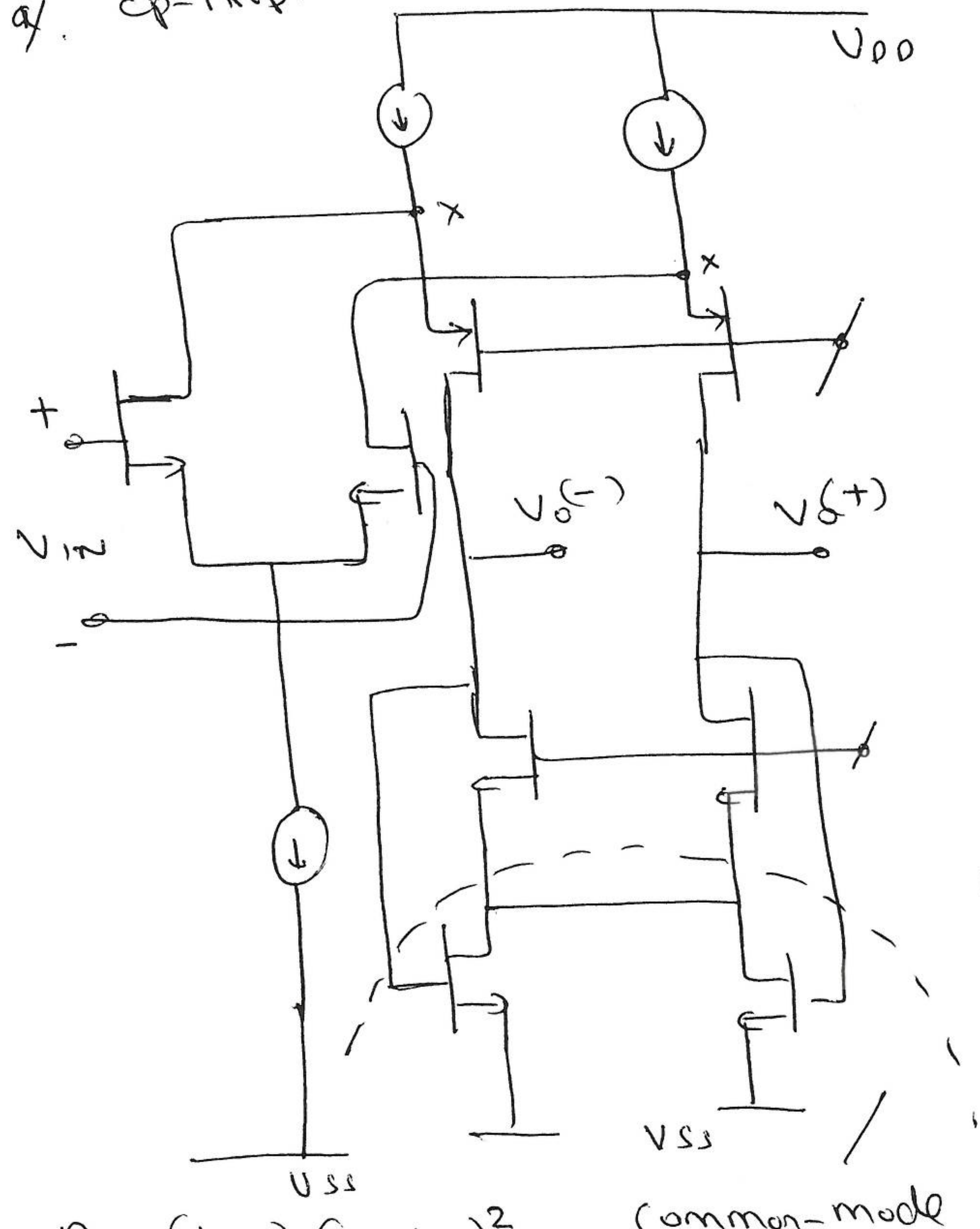
4

(5)

Qu. 2

Architecture of folded-cascode

a/. op-Amp.



4

$A \simeq (1/2)(g_m/g_o)^2$

(T

Qu2 Cont.

4

Single-stage because one current path from input to output.

Node X is low impedance and so very small voltage swing is generated. Only high impedance node is at the output. (2)

Not necessary to pole split since dominant pole at ~~output~~ output not two stages.

Diff output op-amps with high gain have no way of stabilisation since outputs are undefined (voltage that is).

Common-mode feedback - senses common-mode output and via negative feedback controls the current through the output stage to ensure stable quiescent operating point. Circuit shown in the figure. (2)

Qu 2 Cont

b/. OP-Amp

(2/2) $\boxed{A_{v1} = -g_{m2}/(g_{o2}+g_{o4})}$

$(g_{o2}+g_{o4}) = I_{D2}(\lambda_N+\lambda_P)$

$= 5\times10^{-6}\times0.05 = 2.5\times10^{-7}\,\Omega^{-1}$

$g_{m2} = 2\sqrt{\beta_2 I_D} \Rightarrow \beta_2 = \frac{k_N}{2}\left(\frac{W}{L}\right)_2$

$\beta_2 = 7.5\times10^{-5}\ A/V$

$\therefore\ g_{m2} = 3.87\times10^{-5}\,s$

(2/2) $\underline{\underline{A_1 = -154.9}}$

$A_2 = \boxed{-g_{m6}/(g_{o7}+g_{o6})}$

$(g_{o6}+g_{o7}) = I_{D6}(\lambda_{NP}+\lambda_N)$

$= 20\times10^{-6}\times0.05$

$= 10\times10^{-7}\,\Omega^{-1}$

(2/1) $g_{m6} = 1.13\times10^{-4}$, $A_2 = -113$.

$A_T = A_1A_2 = 17503$

CT

Qu 2 cont.

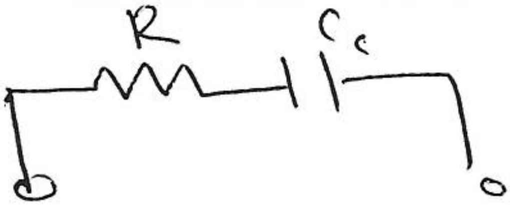
6

$$G.B_P = \frac{g_{m2}}{2\pi C_C} = 4.1\,\mathrm{MHz} \quad - (2)$$

$$S.R = I_0/C_C = \left(\frac{10}{1.5}\right) V/\mu s \quad - (2)$$

— TOTAL 10/10

Introduce R in series with C_c



provides feedforward compensation and eliminates RHP zero in the op-amps transfer function.

Zero is given by $Z = - - g_{m6}/C_c$

with R

$$Z = -\frac{1}{\left(1/g_{m6} - R\right) C_c}$$. Improves ϕ

by setting $Z = P_2$ = 2nd pole.

with R.

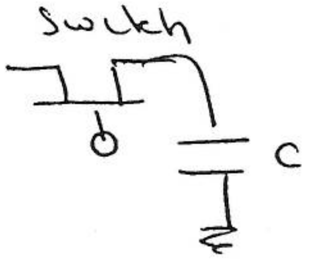
2/2

(T

Qu 3

Q3! Constraint

a.) Dynamic Range $\triangleq$ Vref / Noise $= 2^N$



Rms noise of switch driving Capacitor

$$= \sqrt{\frac{kT}{C}}$$

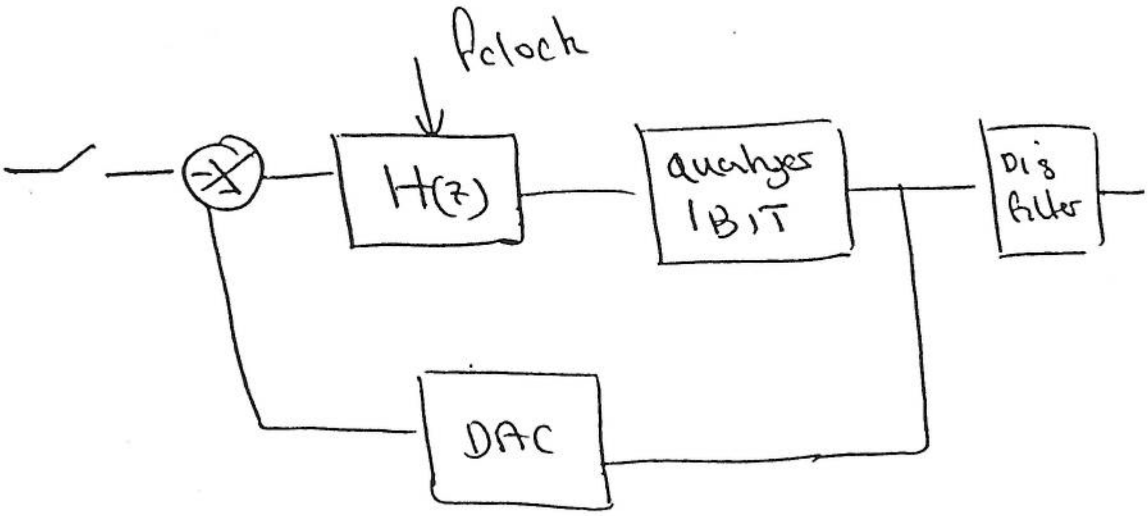
$$\therefore \; DR = \frac{V_{ref}}{\sqrt{\frac{kT}{C}}} = 2^N$$

Assume $f_c = 1/(10RC)$

then solving for C gives

$$DR = 2^N = V_{ref} / \sqrt{kT\,10RC}$$

b)



Basic idea is that coarse quantization noise gets shaped by $1/(Hz)$ via feedback

8/8

7.

Ct

8

Generally $H(z)$ is an Integrator so noise is shaped differentially. This reduces requirements upon component accuracy. The architecture includes a negative feedback loop producing the coarse estimate that oscillates about the true value of input, the digital filter averages this coarse estimate to produce a finer approximation. The feedback DAC and forward integrator force the quantization error to have a high frequency spectrum. The output of the digital filter is down sampled and gives a multibit digital representation. High frequency quantization noise is reduced. Noise shaped giving very high (S/N) at low frequency.

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CT

QUESTION 4

Q4

a) Assumption is that if ($V_{DS} \approx 0$) or ($V_{DS} << (V_{gs} - V_T)$) device acts in linear region. From

$$I_D = \frac{KW}{L}\left[(V_{GS}-V_T)V_{DS} - V_{DS}^2/2\right](1+\lambda V_{DS})$$

for $V_{DS} << (V_{gs} - V_T)$, then $\lambda V_{DS} << 1$

So $$I_D = \frac{KW}{L}(V_{GS}-V_T)V_{DS}$$

6/6

OR $R_{AB} = V_{DS}/I_D = L/(KW(V_{GS}-V_T)$

b) Three sources of Non-linearity

(i) limited due to V_{BS} changing V_T for negative V_{DS} due to body effect.
ie $V_T = V_{T0} + \gamma\left[\sqrt{-V_{BS}+2\phi_F} - \sqrt{2\phi_F}\right]$
γ = bulk threshold parameter
ϕ_F = Fermi-level potential

(ii) limited due to V_{DS} approaching ($V_{GS} - V_T$) hence saturation region for large positive V_{DS}.

(iii) For large values of V_{DS} the $V_{DS}^2/2$ term comes in making the resistor quite non-linear.

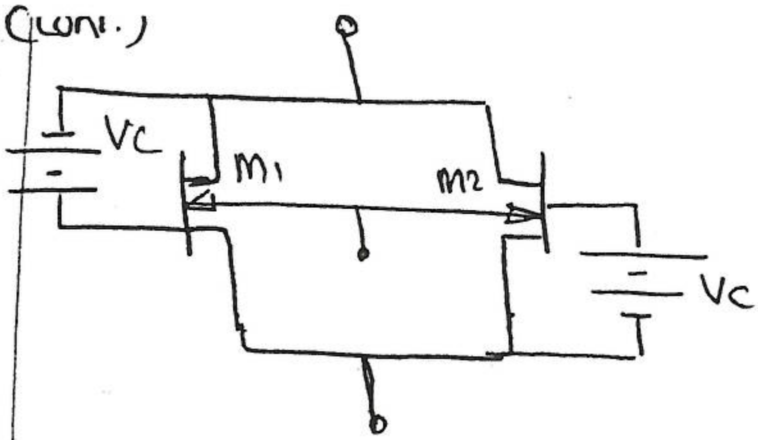
4/4

9

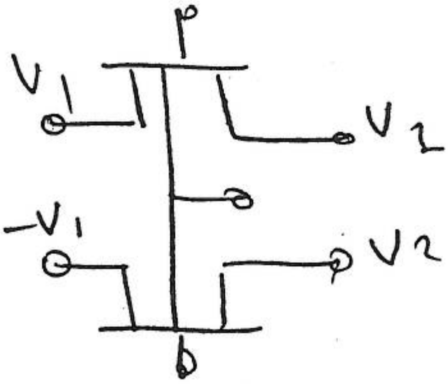
(T

Q4 (cont.)

10

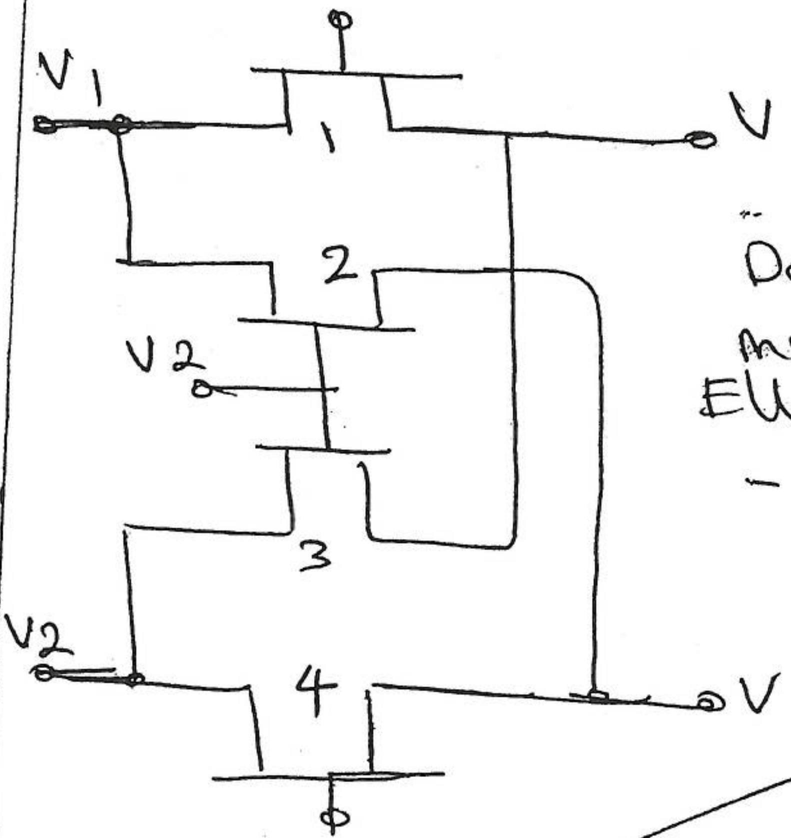


Parallel circuit - eliminates $V_{ds}^2/2$ term.



Differential scheme

Effects of V_{DS} cancelled.



Double differential MOS.
Eliminates
- V_{DS} and V_T term.

2/2

Any one of these will do!

15

Q4 cont,

Double differential integrator

$$I_{D1} = 2\beta\left[(V_{C1} - V - V_T)(V_1 - V) - \tfrac{1}{2}(V_1 - V)^2\right]$$

$$I_{D2} = 2\beta\left[(V_{C2} - V - V_T)(V_1 - V) - \tfrac{1}{2}(V_1 - V)^2\right]$$

$$I_{D3} = 2\beta\left[(V_{C2} - V - V_T)(V_2 - V) - \tfrac{1}{2}(V_2 - V)^2\right]$$

$$I_{D4} = 2\beta\left[(V_{C1} - V - V_T)(V_2 - V) - \tfrac{1}{2}(V_2 - V)^2\right]$$

Expanding it can be shown that :-

$$(V_1 - V_2)/(I_1 - I_2) = 1/2\beta(V_{C1} - V_{C2}) = R$$

Independent of both V_T and V_{DS} terms

Hence $\tau = 2CR = \left[\dfrac{C}{\beta(V_{C1} - V_{C2})}\right]$

8/8

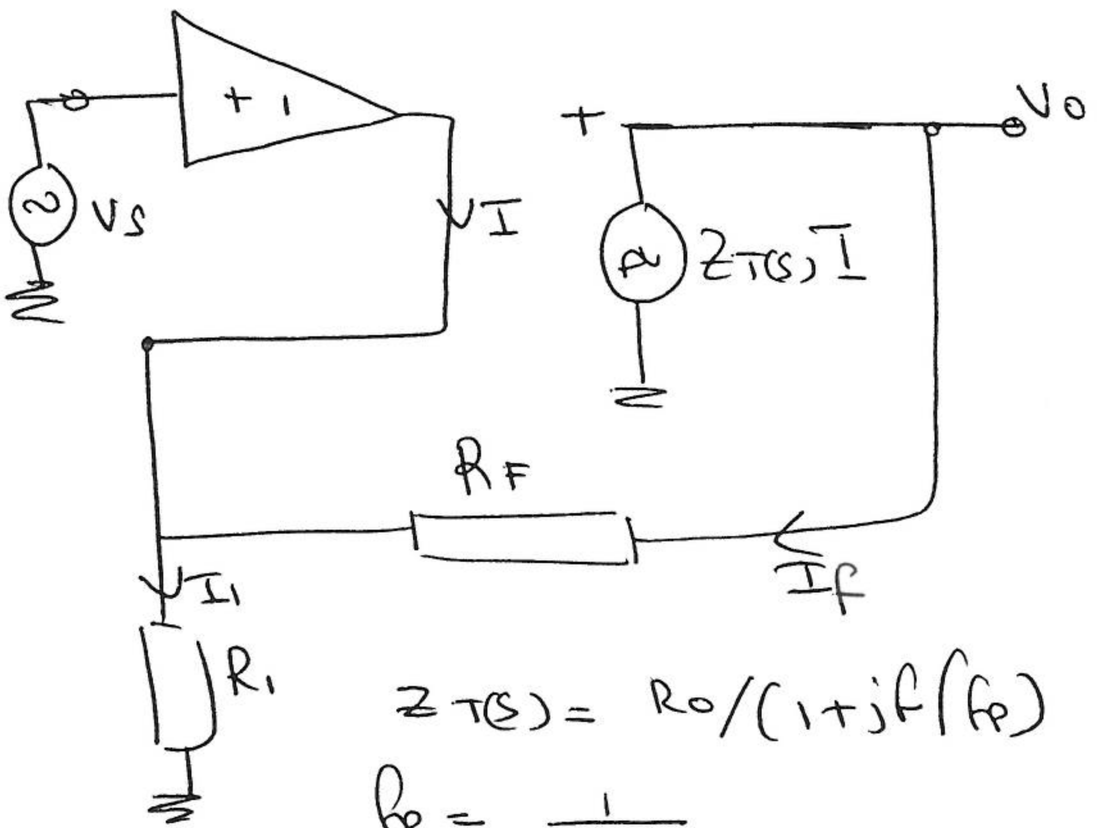
CT

Q5

Advantages of Current-mode

Higher frequency performance, wide dynamic range

lower power supply voltages 2



$Z_{T(s)} = R_o / (1 + jf/f_p)$

$f_p = \dfrac{1}{2\pi R_o C}$

C = compensation capacitor

3 equations

$I_f = (V_o - V_s) R_F$ — (1)

$I_1 = V_s / R_1$ — (2) 8

$V_o = Z_{T(s)} I = Z_{T(s)} [I_1 - I_f]$ — (3)

13

Q5 cont/d..

Subs ① and ② into ③ gives,

$$\left(V_o/V_s\right) = \left(1+R_F/R_1\right) Z_T(s)/\left(R_F+Z_T(s)\right)$$

Subs for $Z_T(s)$

$$\left(V_o/V_s\right)_{j\omega} = \overbrace{\left(1+R_F/R_1\right)\left[\frac{R_o}{R_o+R_F}\right]}^{\text{gain}} \times \frac{1}{\left(1+jf/\underbrace{f_p\left[\frac{R_o+R_F}{R_F}\right]}_{BW}\right)}$$

Assuming $R_o \gg R_F$

then

Closed loop gain $\simeq \left(1+R_F/R_1\right)$ — *

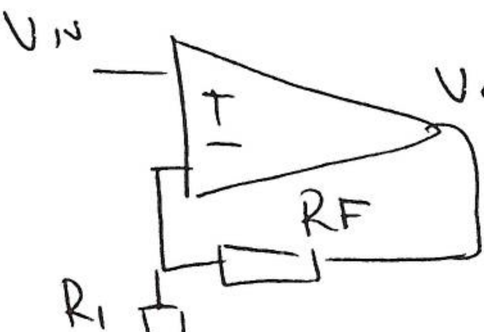
Closed loop Bandwidth $\simeq \dfrac{f_p R_o}{R_F} = \dfrac{1}{2\pi R_F C}$

L*.

Hence R_F sets the amplifier constant BW

and R_1 chosen to set the gain

—//—



$$BW = \frac{1}{2\pi R_F C} = 10\,MHz$$

∴ given $C = 4pF$

$R_F = 3.98\,k\Omega$ 5

Since $A = \left(1+R_F/R_1\right) = 100$

$R_1 = \dots 40\,\Omega$

Q5 cont/d..

Algorithmic Converter

$2I_{IN}$ on +ve terminal of comparator compared to Iref (-ve) terminal

If $2I_{IN}$ < Iref, comp output goes low

digital output = 0 and analogue output = $2I_{IN}$

If $2I_{IN}$ > Iref, comp output goes high

digital output = 1, analogue output $2I_{IN}$ - Iref

Analogue output consequently feeds into following 'bit' which performs exactly the same function.

The process is repeated as many times as necessary to achieve desired resolution.

Digital VLSI – small size, low-power supply voltages

less stringent upon analogue accuracy

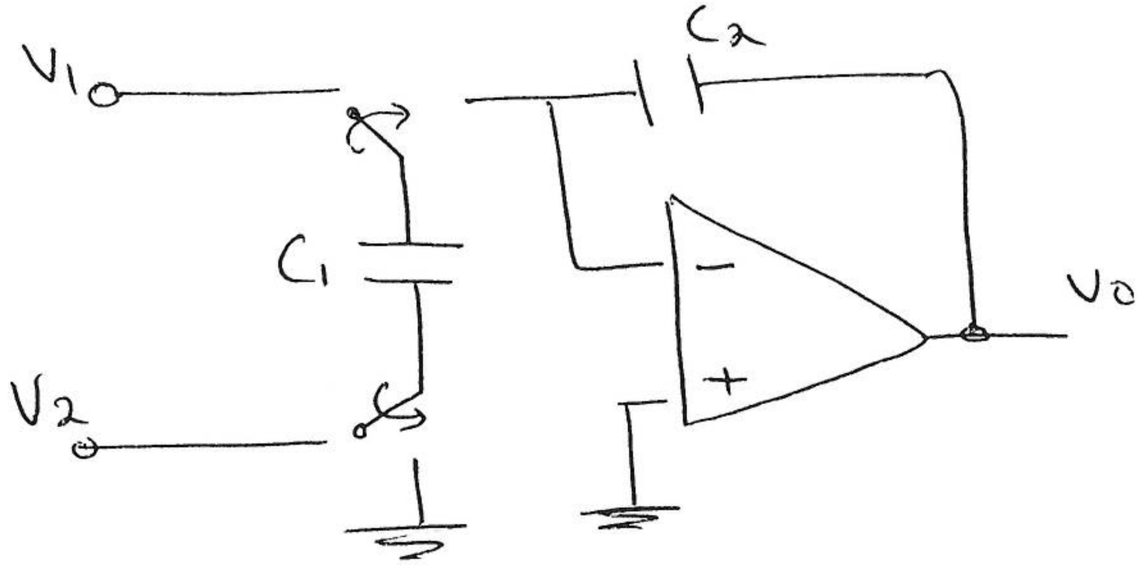
5

rx

15

Qu6/.

a) Differential integrator



During ϕ_1 $\quad Q = C_1[V_1 - V_2]$

$I_{av} = f_c C_1 [V_1 - V_2]$

f_c = clock frequency

During $\phi_2 \Rightarrow \quad I_{av} = -f_c(V_1 - V_2)C_1$

$\therefore V_0 = \frac{-1}{jwC_2} f_c C_1 [V_1 - V_2]$

$\therefore \frac{V_0}{(V_1 - V_2)} = -\frac{f_c}{jw}\frac{C_1}{C_2} \approx \tau = \frac{C_2}{C_1 f_c}$

5/5

LT

Q6 **Lossy Integrator**

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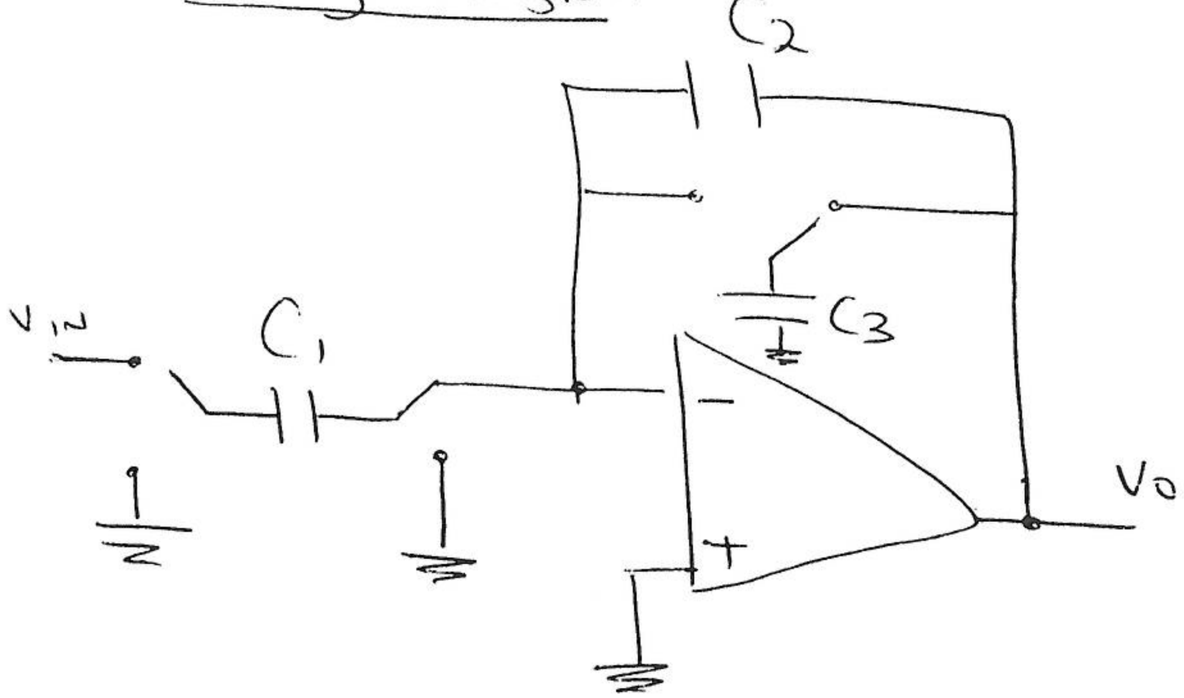


During ϕ_1 $\quad Q = C_1 V_{IN} \Rightarrow I_{av} = f_c C_1 V_{IN}$

During ϕ_2

$$I_{av} = -\left[f_c C_3 V_o + j\omega C_2 V_o\right]$$

$$\therefore f_c C_1 V_{IN} = -\left[f_c C_3 V_o + j\omega C_2 V_o\right]$$

$$V_{IN} = -\left[\frac{C_3}{C_1} V_o + \frac{j\omega C_2 V_o}{C_1 f_c}\right]$$

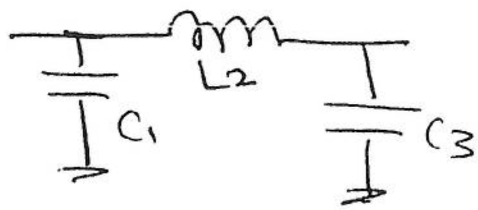
5/5

$$\therefore \frac{V_o}{V_{IN}} = -\frac{C_1}{C_3}\left(\frac{1}{\left(1 + \frac{C_2}{C_3} j\omega / f_c\right)}\right)$$

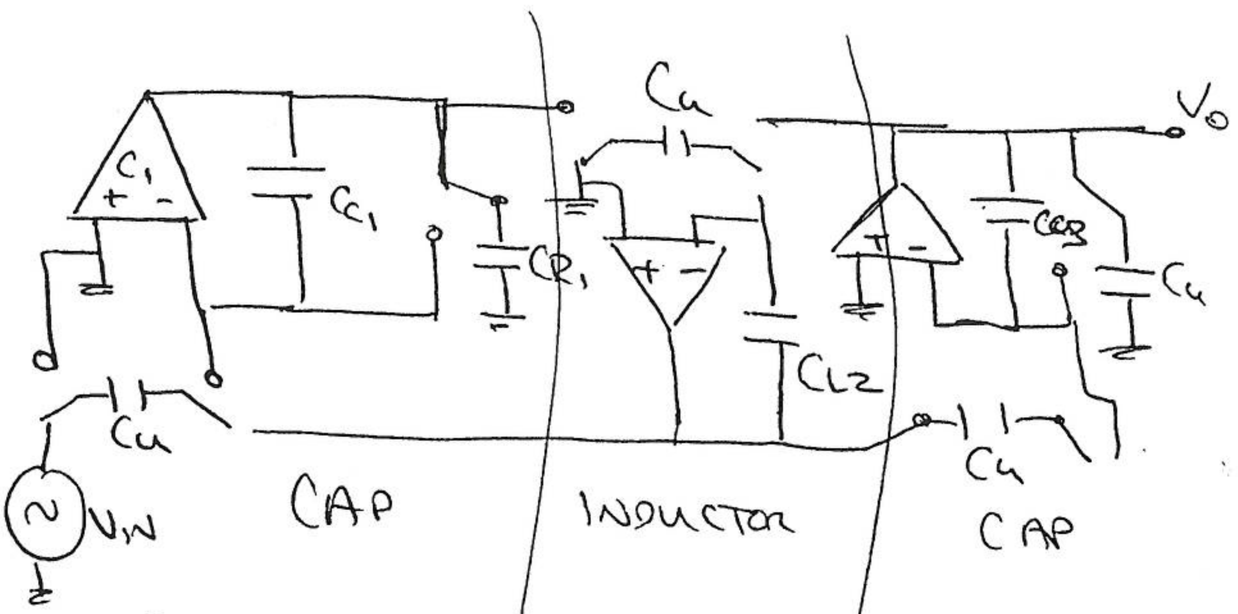
$$\therefore \tau = \left(C_2 / C_3\right)\frac{1}{f_c}$$

(VI)(a)

Q 6 Section of LCR prototype.



General transformation Rules (Not really required but the bright students may include)



3/4

Conversion into differential integrates.

Inductor transformation

$(L_2/R_S) f_c = C_{L2}/C_u$

Capacitor Transformation.

$C_3/C_u = f_c R_S C_3$

where RS is normalising dummy scaling resistor. Assuming $R_S = 1$

$C_{C1}/C_u = f_c C_1$

$C_{C3}/C_u = f_c C_3$ general transformation

$C_{L2}/C_u = f_c L_2$

(T

Q6 con...

18/18

Table values of C_1, L_2 and C_3 are normalized to 1 rad/s $\div 2\pi f_p$

$f_p = 5$ kHz

$C_L = C_3 = 2.0236 / (2\pi\ 5\times10^3)$
$= 6.44 \times 10^{-5}$ F

$C_{L2} = 0.994 / (2\pi\ 5\times10^3)$
$= 3.164 \times 10^{-5}$ F

For termination R_s

assume $C_{LL} = C_{R1} = C_{Ro} = 1$pF

then $\begin{bmatrix} C_{L1} = C_{L3} = 6.44\text{pF} \\ C_{L2} = 3.164\text{pF} \end{bmatrix}$

6/6

Total 20/20