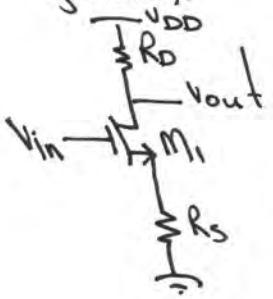
SAMPLE 1 WORKED SOLUTIONS

(1) (a) Source degeneration is when a circuit element (eg. resistor) is connected between the MOSFET source terminal and the common node (eg. V_{dd} or ground).



Advantage (over CS)

- Output impedance is increased (from $R_D \| r_{o1}$ to $R_D \| (r_{o1} + R_S + g_{m1} r_{o1} R_S)$).
- Large-signal operation is linearised (i.e larger small-signal region).

Disadvantages (over CS)

- Reduced headroom
- Reduced voltage gain $= -\dfrac{R_D}{\frac{1}{g_m} + R_S}$ (from $-g_m R_D$)

(b) (i) $A_v = \dfrac{v_{out}}{v_{in}} = \dfrac{(R_E + \frac{1}{g_{m2}} \| r_{o2}) \| r_{o1}}{(R_E + \frac{1}{g_{m2}} \| r_{o2}) \| r_{o1} + 1/g_{m1}}$ (if $\lambda > 0$)

or

$= \dfrac{R_E + \frac{1}{g_{m2}}}{R_E + \frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$ (if $\lambda = 0$)

* question should state if $\lambda = 0$ or $\lambda > 0$

(ii) $A_v = \dfrac{v_{out}}{v_{in}} = \dfrac{v_{out}}{v_x} \times \dfrac{v_x}{v_{in}}$

$\dfrac{v_{out}}{v_x} = g_{m1} \cdot (g_{m2} r_{o2} R_E + R_E + r_{o2}) \| r_{o1}$

$\dfrac{v_x}{v_{in}} = \dfrac{1/g_{m1}}{1/g_{m1} + R_S}$

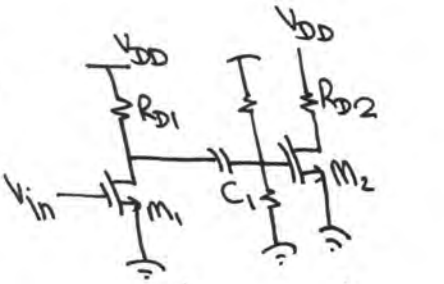
$A_v = \dfrac{(g_{m2} r_{o2} R_E + R_E + r_{o2}) \| r_{o1}}{1/g_{m1} + R_S}$

* if $\lambda > 0$

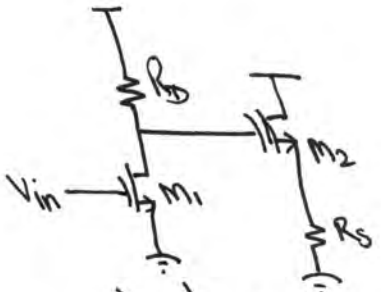
or

$A_v = \dfrac{v_{out}}{v_{in}} = \dfrac{R_E}{1/g_{m1} + R_S}$ if $\lambda = 0$*

(c)



Capacitive coupling



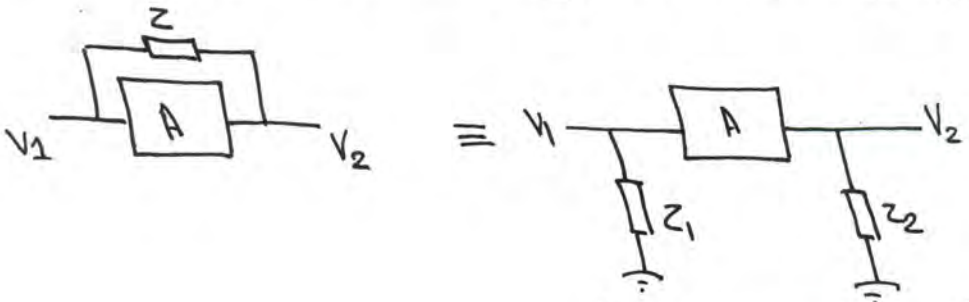
direct coupling.

Capacitive coupling is when amplifier stages are cascaded by using a capacitor for ac coupling, i.e. biasing each stage independently.

Direct coupling is when the amplifier stages are directly connected and the circuit must therefore be designed to be biased correctly as a whole.

In IC design, constraints in large capacitance realisation means that capacitive coupling is undesirable for low frequency signals.

(d)



where $Z_1 = Z\left(\frac{1}{1+A}\right)$

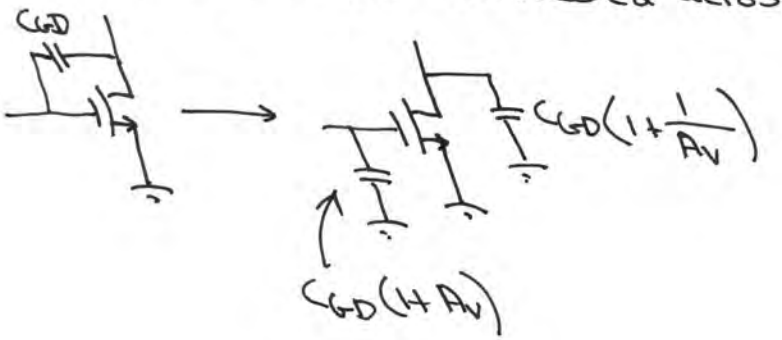
$Z_2 = Z\left(\frac{1}{1+1/A}\right)$

If $A = \frac{V_2}{V_1}$

If the impedance is a capacitor $\therefore C_1 = C(1+A)$

$C_2 = C\left(1+\frac{1}{A}\right)$

~~The~~ Miller's theorem is extremely useful in resolving floating capacitances, in particular connected across an amplifying device.



(e) ~~Gain~~ 4 advantages are:

1. gain desensitisation
2. extension of bandwidth
3. modification in input/output impedance
4. linearity improvement

for (1) for example in op-amp → open-loop gain may vary by +/- 20%. however when operated in closed loop (eg. non-inverting amplifier) $\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + \frac{R_2}{R_1+R_2} A_0}$ and if $A_0 \gg 1 \Rightarrow \frac{V_{out}}{V_{in}} \approx 1 + \frac{R_2}{R_1}$

for (2) if we consider a one-pole amplifier:

$$A_1(s) = \frac{A_0}{1 + s/\omega_0}$$

if we substitute into a closed-loop system:

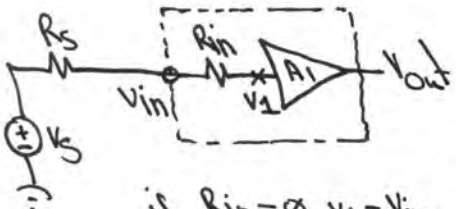
$$\frac{Y}{X} = \frac{\frac{A_0}{1+s/\omega_0}}{1 + \frac{kA_0}{1/s\omega_0}} = \frac{A_0}{1 + kA_0 + s/\omega_0}$$

$$= \frac{\frac{A_0}{1+kA_0}}{1 + \frac{s}{(1+kA_0)\omega_0}}$$

$\therefore$ closed-loop BW $= (1+kA_0)\omega_0$

(f) voltage amplifier : $R_{in} = \infty$ ideally

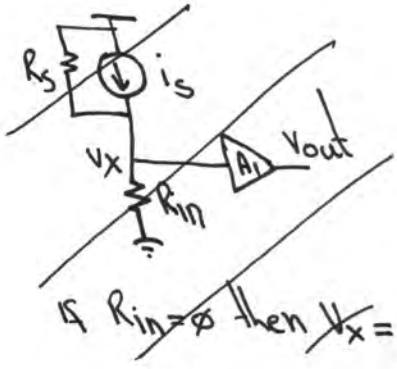
transimpedance amplifier $R_{in} = 0$ ideally



if $R_{in} = 0$, $v_1 = v_{in}$, and $V_{out} = A_1 V_s$

otherwise:

$$V_{out} = \left(\frac{V_s R_{in}}{R_{in} + R_s}\right) A_1$$



if $R_{in} = 0$ then $V_x =$

(g) The transit frequency (f_T) is defined as the frequency at which the current gain of a transistor becomes unity. This gives a measure of the maximum "speed" of the transistor.

$$f_T = \frac{1}{2\pi} \cdot \frac{g_m}{C_{BE}}$$ → if $C_{BE} = 2.2pf$ and $I_C = 5mA$

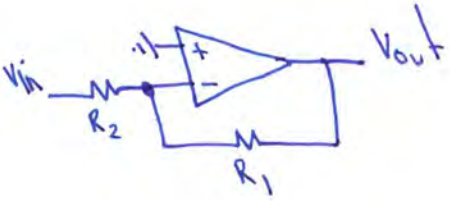
$$f_T = \frac{1}{2\pi} \frac{I_C}{V_T . C_{BE}} = \frac{1\,(5mA)}{2\pi\,(26mV)(2.2pf)}$$

$$= 13.91\,GHz$$

(h) $A_V(o.L) = 106dB = 10^{\left(\frac{106}{20}\right)} = 200{,}000$

$A_V(c.L) = 250$

As inverting amplifier



$\therefore \frac{R_1}{R_2} = 250$

$$\frac{V_{out}}{V_{in}} = -\frac{R_1}{R_2}\left(1 - \frac{1}{A_0}\left(1 + \frac{R_1}{R_2}\right)\right)$$

$$\frac{V_{out}}{V_{in}} = -250\Big(1 - \underbrace{\frac{1}{200000}\left(1 + 250\right)}_{\varepsilon}\Big)$$

$\varepsilon = 0.126\%$

(i) (PVT) Remember

P = Process variation

V = Power supply variation

T = temperature

} Three challenges of designing on chip reference (bias generator) circuits are the sensitivity (or dependance) on P, V and T.

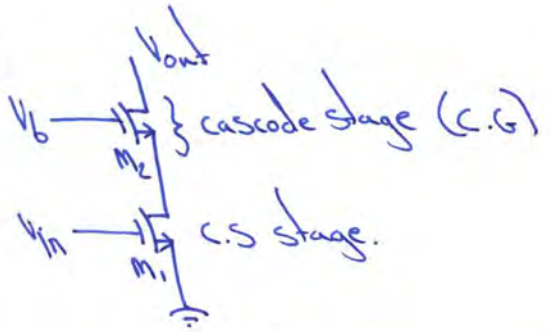
To overcome apply design techniques as follows:

Process: make bias generator dependant on relative component ratio's not absolute values.

Temperature: use combination of components with +ve and -ve temp. coefficient to cancel out

Power supply: Do not derive reference from P.S

(j)



A cascode stage can boost the output impedance of a C.S stage from (r_{o1}) to $(g_{m2} r_{o1} r_{o2} + r_{o1} + r_{o2})$ and thus, if ~~$V_{out} = i_{out} \cdot R_{out}$~~

~~$\Rightarrow A_v = \frac{V_{out}}{V_{in}} = G_m$~~

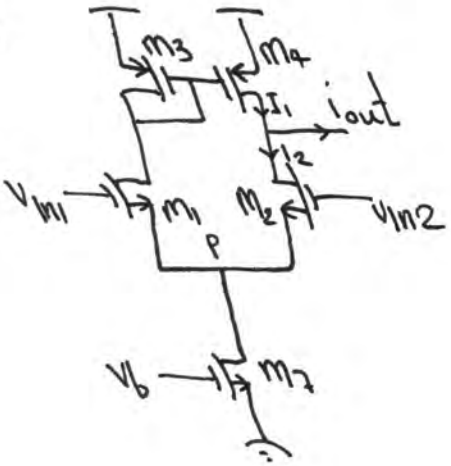
$V_{out} = i_{out} \times R_{out}$ where $i_{out} = G_m V_{in}$

$V_{out} = G_m V_{in} R_{out}$

$\frac{V_{out}}{V_{in}} = G_m R_{out}$ $\therefore$ by increasing R_{out}, A_v is increased.

Drawbacks: (1) Reduced headroom therefore require higher supply voltage.
(2) An additional device is required.

(2) (a)



$i_1 = g_{m1} v_{in1}$ (assuming P is ac gnd)

$i_2 = g_{m2} v_{in2}$

$i_{out} = g_{m1}(v_{in1} - v_{in2})$ (assuming $M_1 = M_2$)

$R_{out} = r_{o4} \| r_{o2}$

$\therefore V_{out} = i_{out} R_{out} = g_{m1}(v_{in1} - v_{in2})[r_{o2} \| r_{o4}]$

$A_v = \frac{V_{out}}{v_{in1} - v_{in2}} = g_{m1}(r_{o2} \| r_{o4})$

(b) $\frac{V_{out}}{V_y} = -g_{m5}(r_{o5} \| r_{o8})$ C.S stage.

$A_v = \frac{V_{out}}{v_{in1} - v_{in2}} = -g_{m1} g_{m5} (r_{o2} \| r_{o4})(r_{o5} \| r_{o8})$

(c) $\left(\frac{W}{L}\right)_6 = \frac{4}{2}$ $\left(\frac{W}{L}\right)_7 = \frac{10}{2}$ $\left(\frac{W}{L}\right)_8 = \frac{20}{2}$

$\frac{V_{DD} - V_{GS}}{8K} = I_6$, $I_6 = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_6 (V_{GS} - V_{TH})^2$

$\frac{V_{DD} - V_{GS}}{8K} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_6 (V_{GS} - V_{TH})^2$

$1.8 - V_{GS} = 4000(200\mu)\,2\,(V_{GS} - 0.4)^2$

$1.8 - V_{GS} = 1.6(V_{GS}^2 + 0.16 - 0.8 V_{GS})$

$1.6V_{GS}^2 - 1.28V_{GS} + V_{GS} + 0.256 - 1.8 = 0$

$1.6V_{GS}^2 - 0.28V_{GS} - 1.544 = 0$

$V_{GS6} = 1.074\text{V}$

$\therefore I_D = \frac{1.8 - 1.074}{8K}$

$= 90.9\mu\text{A}$

$\therefore$ Power $= I_{total} \times V_{DD}$

$I_{total} = I_6 + I_7 + I_8$

$= 90.9\mu(1 + 2.5 + 5)$

$= 772\mu A$

Power $= IV = 772\mu(1.8) = 1.4\,mW$

(d) $\left(\frac{W}{L}\right)_{1,2} = \frac{250}{1}$

$\left(\frac{W}{L}\right)_{3,4} = \frac{4}{4}$

$\left(\frac{W}{L}\right)_5 = \frac{40}{4}$

$A_v = g_{m1} g_{m5} (r_{o2} \| r_{o4})(r_{o5} \| r_{o8})$

$g_{m1} = \sqrt{2 I_D \frac{W}{L} \mu_n C_{ox}}$

$= \sqrt{2(2.5)90.9\mu 200\mu(250)}$

$= 4.8\,mS$

$g_{m5} = \sqrt{2 I_D \frac{W}{L} \mu_n C_{ox}} = \sqrt{2(5)90.9\mu(100\mu)10}$

$= 0.953\,mS$

$r_{o2} = \frac{1}{\lambda_n I_{D2}} = \frac{1}{0.1(0.5)(90.9\mu)2.5} = 88k\Omega$

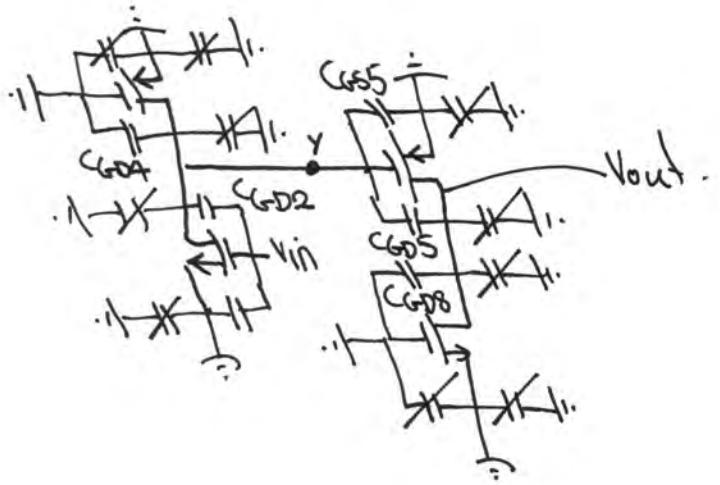
$r_{o4} = \frac{1}{\lambda_p I_{D2}} = 44k\Omega$

$r_{o8} = \frac{1}{\lambda_n I_{D8}} = \frac{1}{0.1(0.5)(90.9\mu)} = 22k\Omega$

$r_{o5} = \frac{1}{\lambda_p I_{D5}} = 11k\Omega.$

$\Rightarrow A_v = (29.33k)(7.3k)0.953m \times 4.8m = 98.39$

$= 39.859\,dB$



(e) At node Y: $C_y = C_{GD4} + C_{GD2}\left(1 + \frac{1}{A_{V1}}\right) + C_{GS5} + C_{GD5}(1 + A_{V2})$ ($\frac{1}{A_{V1}}$: small)

At node out: $C_{out} = C_{GD5}\left(1 + \frac{1}{A_{V2}}\right) + C_{GD8}$ ($\frac{1}{A_{V2}}$: small)

$$\rightarrow C_y = C_{GD4} + C_{GD2} + C_{GS5} + C_{GD5}(1 + g_{m5}(r_{O5} \| r_{O8}))$$
$$= 4(0.2) + 250(0.2) + 40(4)\tfrac{2}{3}(12) + 40(0.2)(1 + 6.96)$$
$$= 1.39\,pf.$$
$$C_{out} = C_{GD5} + C_{GD8} = 40(0.2) + 20(0.2) = 12ff$$

$$R_y = r_{O2} \| r_{O4} = 29.33k \text{ (from (d))}$$

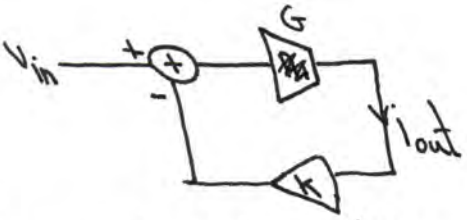
$$R_{out} = r_{O5} \| r_{O8} = 7.3k \text{ (from (d))}$$

(f) $\therefore f_{py} = \frac{1}{2\pi(29.33k)1.39p} = 3.9\,Mhz.$

$$f_{Pout} = \frac{1}{2\pi(7.3k)12ff} = 1.82\,Ghz.$$

f_{py} is the dominant pole

(3) (a)



(i) Gain of CE is negative and therefore the +ve terminal of amp. is used.

(ii) Gain of EF is positive and therefore the -ve terminal of amp. is used.

Both are +ve feedback.

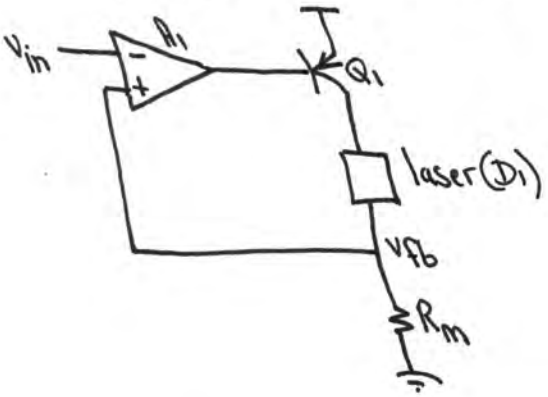
(b) Voltage in, current out:

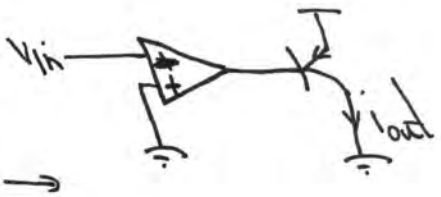
∴ transconductance amplifier

(c) Ideal transconductance amplifier has high input impedance and high output impedance

∴ topology (i) common source is preferrable as higher o/p impedance.

(d)

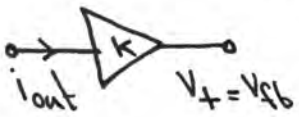




$$i_{out} = -V_{in}(A_1) \times -g_{m1}$$

$$\Rightarrow \frac{i_{out}}{V_{in}} = g_{m1}A_1 \quad (\text{open loop})$$

(e) Feedback factor (K) takes i_{out} as it input and gives V_+ as its o/p (V_{fb})



$$\therefore K = \frac{V_{fb}}{i_{out}} = \frac{\cancel{i_{out}} \times R_m}{\cancel{i_{out}}} = R_m.$$

∴ loop gain = ~~G~~ × K

$$= g_{m1}A_1R_m$$

(f) $$\frac{i_{out}}{V_{in}}(\text{closed-loop}) = \frac{G}{1+KG} = \frac{g_{m1}A_1}{1+g_{m1}A_1R_m}$$

(g) $$\frac{V_{out}}{i_{out}} = R_{out} = R_m + r_{o1}$$

(h) $$R_{out}(\text{closed-loop}) = (R_m + r_{o1})(1 + g_{m1}A_1R_m)$$

(i) * Note: this section cannot be solved as I_C and V_A are not given.

→ if $I_C = 20mA$, $V_A = 10V$ } $g_m = \frac{I_C}{V_T}$ and $r_o = \frac{V_A}{I_C}$ → $\frac{i_{out}}{V_{in}} = \frac{1}{10}S$

→ $R_{out}(\text{closed}) = 390\ \Omega$