EE4-16
EE9-AC6

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2013

MSc and EEE PART IV: MEng and ACGI

ANALOGUE SIGNAL PROCESSING

Monday, 13 May 10:00 am

Time allowed: 3 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible — First Marker(s): P. Georgiou
Second Marker(s): K. Fobelets

Special instructions for students

Unless otherwise stated the following parameters have the following definitions:

V_{DS} : Drain Source Voltage.

V_{GS} : Gate Source Voltage.

V_{TH} : Threshold Voltage.

U_t : Thermal Voltage.

n : Weak Inversion Slope factor.

g_m: Transconductance.

1. a) Compare analogue and digital signal processing with regards to power consumption and computational capability.

[4]

b) The differential pair transconductor shown in Figure 1.1 has MOS transistors which are operating in the weak-inversion region of operation with a slope factor n = 1.23.

i) Briefly explain what the weak-inversion region of operation for a MOS transistor is, indicating the mechanism of current conduction and gate bias considerations.

[2]

ii) Show that the output current $I_{out} = I_1 - I_2$ of the differential pair transconductor may be given by equation 1. Show all your steps in derivation.

$$I_{out} = I_{tail} \tanh\left(\frac{V_{GS1} - V_{GS2}}{2nU_t}\right) \quad (1)$$

[4]

iii) Show that the small signal transconductance is given by $g_m = I_{tail}/2nU_t$ and thus derive the transconductance efficiency of the circuit in Figure 1.1

[2]

c) Figure 1.2 shows a cascade of amplifiers where each stage uses the circuit from Figure 1.1. The total noise at the output is given by equation 2. The total stages M = 2 and the constant P = 1 for weak inversion operation. Also assume that the total noise contribution is due to the two input devices of the differential pair ($n_i = 2$) and the gain of each stage is given by $G_i = -g_m R_{out}$, where g_m is the transconductance derived in question 1.b.iii and $R_{out} = 1\ M\Omega$.

i) Given the tail current of the differential pair I_{tail}=100nA, calculate the minimum area A_1 required by the first stage, such that the total contribution of the noise at the output from the first stage is less than 100 $\mu V/\sqrt{Hz}$. You may assume $K_w = 1x10^{-15}\ V^2C$, $K_f = 3.5x10^{-18}\ Hz/F^2$, ΔF =100 Hz, f_h = 100Hz, f_l = 1Hz and the transconductance is constant over a given input voltage.

$$v_{no}^2 = \sum_{i=1}^{i=M} v_{ni}^2 G_i^2 = \sum_{i=1}^{i=M} \left(n_i \frac{K_w}{(I_i/n_i)^p} \cdot \Delta f + n_i \frac{K_f}{(A_i/n_i)} \cdot \ln\left(\frac{f_h}{f_l}\right) \right) G_i^2 \quad (2)$$

[4]

ii) Propose suitable gate widths and lengths for transistors M1 and M2 for a typical 0.35um process.

[2]

iii) Given that the system shown in Figure 1.2 operates on a Bluetooth signal at 2.4 GHz, but conveys audio information at 44 kHz, propose one method to reduce the power consumption requirements before quantizing the analogue signal.

[2]

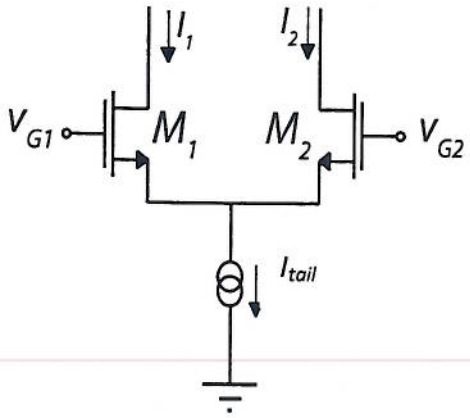

Figure 1.1

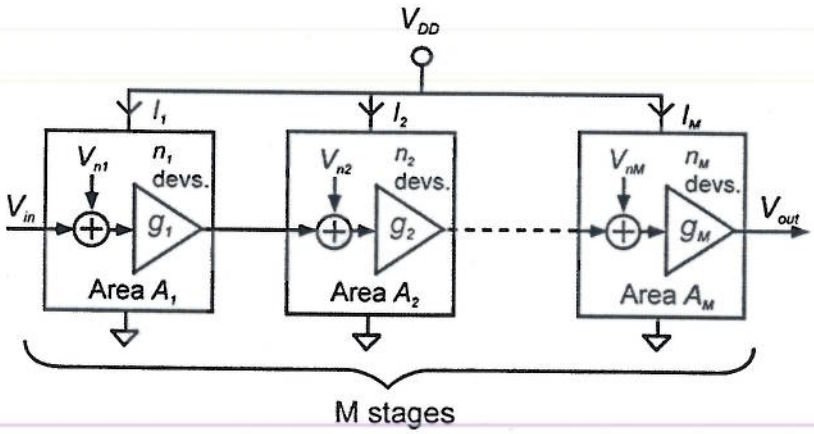

Figure 1.2

2. a) Explain why MOSFETs operating in weak-inversion make suitable translinear elements and state two limitations when using these in translinear circuits which may apply specifically to weak inversion operation.

[4]

b) Figure 2.1 shows a translinear circuit.

i) Derive the transfer function I_{out} of this circuit using the translinear principle. You may assume that currents I_1 and I_2 are input currents and I_4 is a static bias.

[5]

ii) Write down an expression for the output current I_{out} when I_{in}= Asin(ωt) and I_1 and I_3 are derived as:

$$I_3 = \left|\frac{dI_{in}}{dt}\right|, \qquad I_1 = \left|\int I_{in}\, dt\right|$$

[3]

iii) What is the function of this circuit when the inputs are applied as in 2.b.ii ?

[1]

c) Synthesise using Type A translinear cells, a multiplier circuit that implements the following function:

$$z^+ - z^- = (x^+ - x^-)y$$

Draw the complete circuit including all biasing schemes and remove redundant loops.

[5]

d) Explain one advantage of a Gilbert gain cell over a conventional translinear multiplier.

[2]

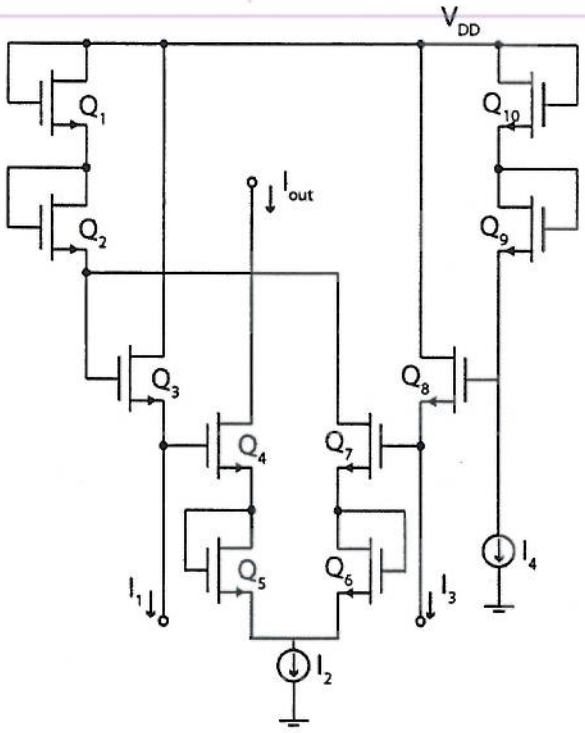

Figure 2.1

3. a) Explain the principle of companding, illustrating how the dynamic range changes through the signal processing chain.

[4]

b) Figure 3.1 shows a block diagram of a current-mode companding integrator, with an input X and an output Y. f() and g() represent non-linear functions which compress and expand the signal such that the input-output relationship of the integrator is linear and given by:

$$Y = \tau \int X \cdot dt$$

Given that the expansive function is defined as $I_{out} = g(V_c) = I_0 \sinh(V_c/nU_t)$, derive the function f(x) such that linear integration is achieved. All constants should be grouped to represent a current I_1, with the function f(x) composed of just I_{in}, I_1 and I_{cosh}, whereby $I_{cosh} = I_0 \cosh(V_c/nU_t)$.

[6]

c) The transfer function of an oscillator may be defined in state space representation by the following equations:

$$\dot{X}_1 = -\omega_0 X_1 + \omega_0 X_2$$
$$\dot{X}_2 = -2\omega_0 X_1 + \omega_0 X_2 + \omega_0 U$$
$$Y = X_1$$

where Y is the output, U is the input and X_1 and X_2 are the states.

(i) By using the mappings below show how these linear equations can be mapped to non-linear log-domain design equations. You may use the following mapping for constant currents, $I_1 = I_2 = I_\omega$ and $I_U = I_O$.

$$X_1 = I_1 \exp\left(\frac{V_1}{nU_t}\right) \qquad X_2 = I_2 \exp\left(\frac{V_2}{nU_t}\right) \qquad U = I_U \exp\left(\frac{V_U}{nU_t}\right)$$

[5]

(ii) With these log-domain design equations, sketch a schematic of the final log domain filter using weak inversion MOS transistors.

[5]

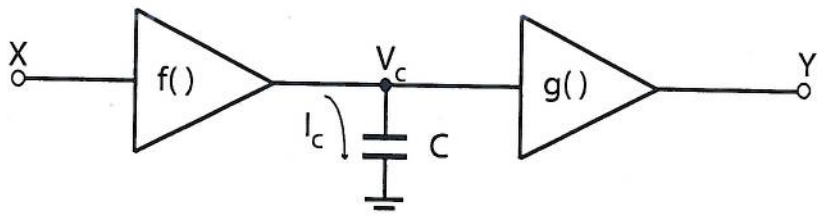

Figure 3.1

4. a) Figure 4.1 shows a conventional second-generation positive current conveyor, CCII+.

i) Explain it's operation principle and describe how impedances at each of its three ports, X, Y, Z, differ from a standard operational amplifier.

[4]

ii) Draw the circuit of a CMOS implementation of a bi-directional CCII+.

[3]

iii) Propose a method to increase it's output impedance.

[1]

iv) Using the current conveyor in Figure 4.1, draw the schematics of a current mode integrator and a voltage mode integrator, each with a time constant, τ =1s. You may assume R = 100KΩ.

[4]

v) Figure 4.2 shows a voltage mode Sallen key filter. Using the adjoint principle transform this to it's current mode equivalent using CCII+ blocks.

[4]

b) Sketch a current mode circuit that can implement the following hyperbolic functions:

$$I_1 - I_2 = I_{DC} \sinh\left(\frac{V_1 - V_2}{nU_t}\right)$$

$$I_1 + I_2 = I_{DC} \cosh\left(\frac{V_1 - V_2}{nU_t}\right)$$

[4]

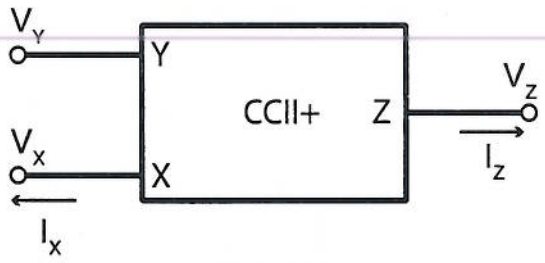

Figure 4.1

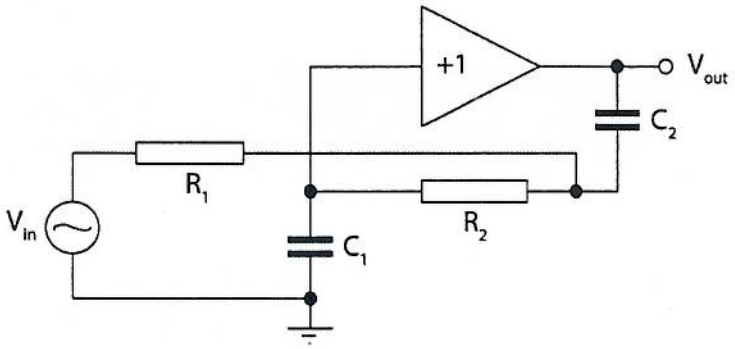

Figure 4.2

5. This question relates to discreet time integrators.

a) Figure 5.1 shows a discreet time RC integrator.

i) Derive the time constant of integration. [2]

ii) Assuming $C_1 = C_2$, select a suitable clock frequency to give a time constant $\tau = 1\mu s$. [2]

iii) For the circuit Figure 5.1, when CK goes low all of the channel charge, Q_1, of transistor M_1 is injected into C_1. This causes an error voltage ΔV_{C1} in C_1 defined by:

$$\Delta V_{C1} = \frac{Q_1}{C_1}$$

Then transistor M_2 turns ON. The channel charge of M_2 is split equally between C_1 and C_2. Estimate the total amount of charge injection and therefore error voltage ΔV_{C2} from switches M_1 and M_2 which appears on the output capacitor C_2 after CK goes high again, that is after one integration cycle. [4]

b) Figure 5.2 shows an autozeroing switched capacitor integrator capable of removing any offset in the amplifier. Derive the output voltage of the integrator during phase Φ_1 and Φ_2 indicating how the offset is removed by showing the charge on each capacitor during each phase. [5]

c) Figure 5.3 shows a schematic of switched current integrator.

i) Derive the transfer function of the switched current integrator and show that in the z-domain this may be represented as $H(z) = A/(z-1)$. [5]

ii) Explain one limitation of the switched current technique that doesn't exist in its voltage mode equivalent. [2]

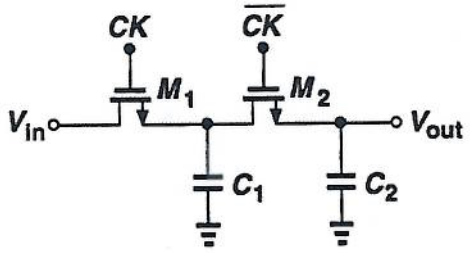

Figure 5.1

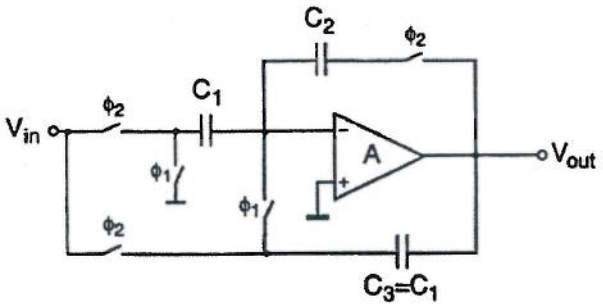

Figure 5.2

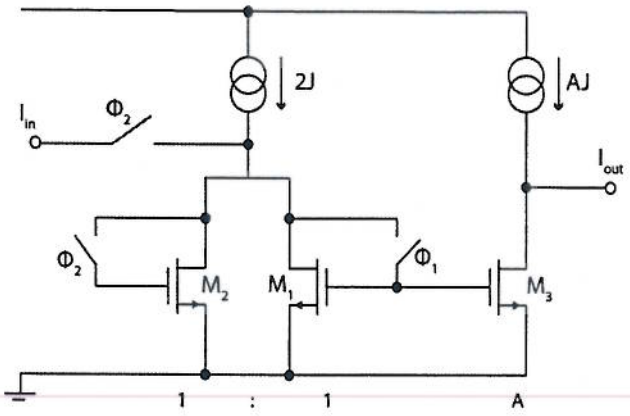

Figure 5.3

6. Figure 6.1 shows a biomedical system used to measure the similarity between two EEG channels by recording action potentials from the human brain. The front end consists of a differential operational amplifier (OA) connected to a voltage-to-current (V/I) converter. This then connects to a current rectifier followed by a peak detector that detects the envelope of the converted current I_{out1}. The similarity between the envelopes of the two channels, I_{env1} and I_{env2}, is detected using a current mode correlator to derive an output signal I_{corr}.

a) Explain one method to make the input signals V_{sig1} and V_{sig2} immune to 1/f noise in the operational amplifier, and draw a block diagram of this method illustrating how the frequency spectrum of the signal changes during each stage.

[5]

b) Draw a schematic of a suitable front end for this system using the method described in 6.a. You may use the OA symbol as in Figure 6.1 and do not need to show the schematics of this amplifier.

[5]

c) Figure 6.2 shows a suitable circuit that can be used as a current mode peak detector. Explain it's principle of operation.

[5]

d) The system in Figure 6.1 uses a V/I converter with improved linearity over a conventional differential pair. Sketch suitable schematics for the V/I converter and the current correlator used in this system.

[5]

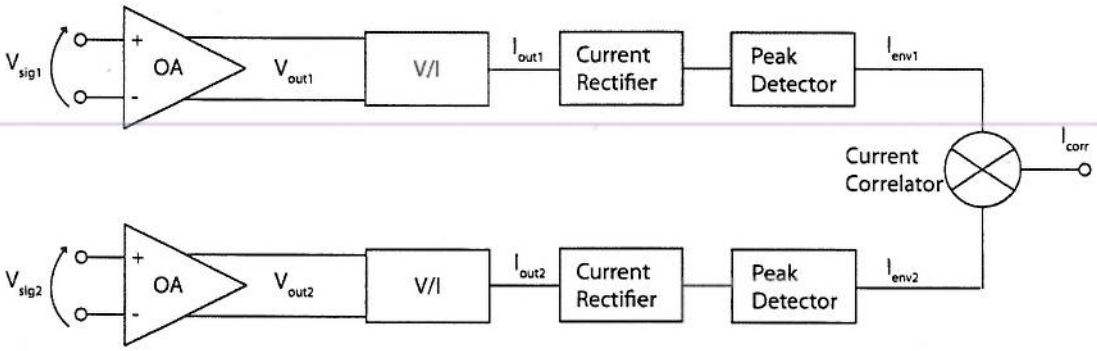

Figure 6.1

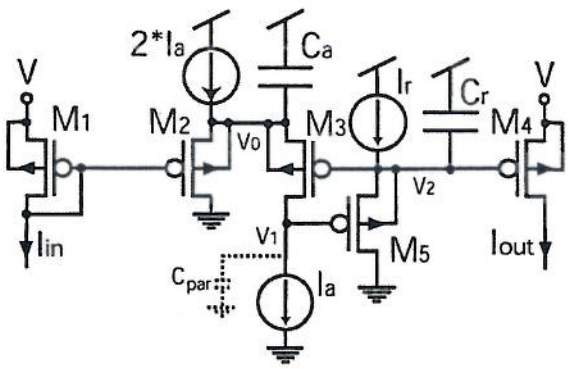

Figure 6.2

6. Figure 6.1 shows a biomedical system used to measure the similarity between two EEG channels by recording action potentials from the human brain. The front end consists of a differential operational amplifier (OA) connected to a voltage-to-current (V/I) converter. This then connects to a current rectifier followed by a peak detector that detects the envelope of the converted current I_{out1}. The similarity between the envelopes of the two channels, I_{env1} and I_{env2}, is detected using a current mode correlator to derive an output signal I_{corr}.

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[5]

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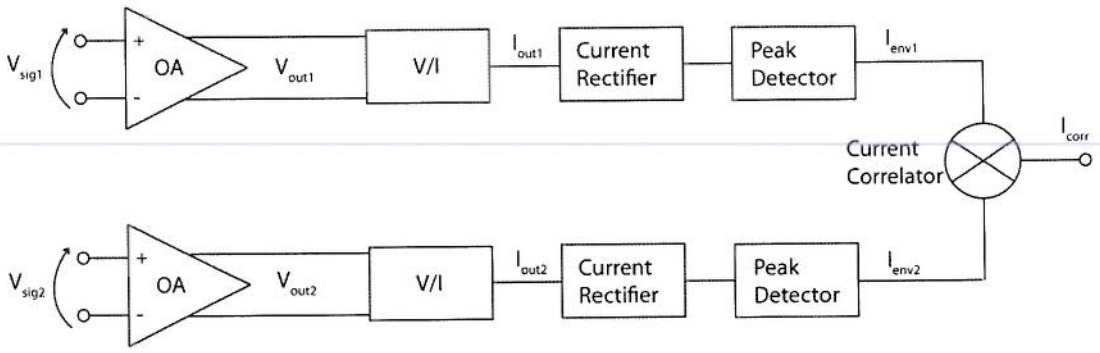


Figure 6.1

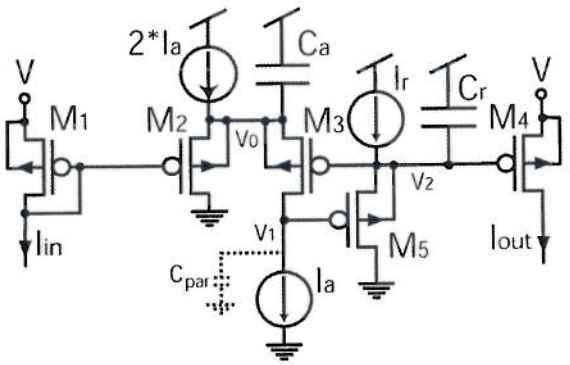


Figure 6.2

1. a) Compare analogue and digital signal processing with regards to power consumption and computational capability.

[4]

[bookwork]

- Analogue - Power consumption depends on supply and biasing current [1]
- Analogue - Computational capabilities arise from the physics of devices [1]
- Digital - Power consumption is dynamic and dependent on the clock [1]
- Digital - Computation arises from well described Boolean logic [1]

b) The differential pair transconductor shown in Figure 1.1 has MOS transistors which are operating in the weak-inversion region of operation with a slope factor n=1.23.

i) Explain what is the weak-inversion region of operation.

[2]

Weak inversion (sub-threshold) ($V_{GS}<V_t$):

- Exponential relationship with drain current (show equation) [1]
- Current flows by Diffusion [1]

ii) Show that the output current I_{out} of the differential pair transconductor may be given by equation 1, showing all your derivation.

$$I_{out} = I_{tail} \tanh\left(\frac{V_{GS1} - V_{GS2}}{2nU_t}\right) \quad (1)$$

[4]

Mathematical derivation:

$$I_1 = I_0 \exp\left(\frac{V_{GS1}}{nU_t}\right)$$

$$I_2 = I_0 \exp\left(\frac{V_{GS2}}{nU_t}\right)$$

$$I_{tail} = I_1 + I_2 = I_0(e^{V_{GS1}/nU_t} + e^{V_{GS2}/nU_t})$$

$$I_{out} = I_1 - I_2 = I_0(e^{V_{GS1}/nU_t} - e^{V_{GS2}/nU_t})$$

$$V_{inD} = V_{GS1} - V_{GS2}$$

$$\frac{I_{out}}{I_{tail}} = \frac{e^{V_{GS1}/nU_t} - e^{V_{GS2}/nU_t}}{e^{V_{GS1}/nU_t} + e^{V_{GS2}/nU_t}} = \frac{e^{V_{inD}/nU_t} - 1}{e^{V_{inD}/nU_t} + 1} = \tanh\left(\frac{V_{inD}}{2nU_t}\right)$$

iii) Derive the small signal transconductance and transconductance efficiency of the circuit in Figure 1.1

[2]

Transonductance: $g_m = \frac{I_{tail}}{2nU_t}\sec^2\left(\frac{V_{inD}}{2nU_t}\right) \approx \frac{I_{tail}}{2nU_t}$

Transconductance efficiency: $g_m/I_{tail}=1/2nU_t$

c) Figure 1.2 shows a cascade of amplifiers whereby each stage uses the circuit from Figure 1.1 and the total noise at the output is given by equation 2. For the following question assume that the total stages M=2 and the constant P=1 for weak inversion

operation. Also assume that the total noise contribution is due to the two input devices of the differential pair (n_i=2) and the gain of each stage is given by G_i=-$g_m R_{out}$, where g_m is the transconductance derived in section 1.b.iii and R_{out}=1 MΩ.

i) Given the tail current of the differential pair I_{tail}=100nA, calculate the minimum area required by the first stage A_1 such that the total contribution of the noise from the first stage at the output is less than 100uV/√Hz. You may assume K_w=1x10^{-15} V^2 C, K_f=3.5x10^{-18} Hz/F^2, ΔF=100 Hz, f_h=100Hz, f_l=1Hz and the transconductance is constant over a given input voltage.

$$v_{no}^2 = \sum_{i=1}^{i=M} v_{ni}^2 G_i^2 = \sum_{i=1}^{i=M} \left(n_i \frac{K_w}{(I_i / n_i)^p} \cdot \Delta f + n_i \frac{K_f}{(A_i / n_i)} \cdot \ln\left(\frac{f_h}{f_l}\right) \right) G_i^2 \quad (2)$$

[4]

Solution:
I_{tail}=100nA
g_m=I_{tail}/2nU_t = 100nA/(2x1.23x0.026) = 1.56 uS [1]
Voltage gain G_i=-$g_m R_{out}$ =1.56uS x 1 MΩ = -1.56
Input noise requirement for two stages: V_{n1}xG_1xG_1 < 100uV/√Hz

$$V_{n1} < 41.15 < \left(n_i \frac{K_w}{(I_i / n_i)^p} \cdot \Delta f + n_i \frac{K_f}{(A_i / n_i)} \cdot \ln\left(\frac{f_h}{f_l}\right) \right) \quad [2]$$

Solving for A_1 gives A=1.73 (um)^2 [1]

ii) Propose suitable widths and lengths for transistors M1 and M2 for a typical 0.35um process.

[2]

Area=1.72(um)^2, so A=1.31um, L=1.31um is a possible solution. [2]

iii) Given the system shown in Figure 1.2 operates on a Bluetooth signal at 2.4GHz, but conveys audio information at 44KHz, propose one method to reduce the power consumption requirements before quantizing the analogue signal.

[2]

Using a mixer you can downcovert the 2.4GHz signal to 44KHz. This will reduce the quantiser requirements from 4.8Gsamples/sec to just 88Ksamples/sec assuming we are sampling at nyquist. [2]

2. a) Explain why MOSFETs operating in weak-inversion make suitable translinear elements and state two limitations which may apply specifically to weak inversion operation.

[4]

[bookwork]
MOSFETs in weak inversion have an exponential relationship between VGS and IDS. The trancoductance is therefore linear with VGS. Through the logarithmic relationship we can therefore multiply currents in a KVL loop. [2]

Drawbacks:
Currents need to be limited to below 100nA. [1]
Temperatures must be equal to get rid of thermal voltage terms. [1]

b) Figure 2.1 shows a translinear circuit.
i) Derive the transfer function I_{out} of this circuit using the translinear principle. You may assume that currents I_1 and I_2 are inputs current and I_4 is a static bias.

[4]

Translinear Loop: $I_{Q1}.I_{Q2}.I_{Q3}.I_{Q4}.I_{Q5}=I_{Q6}.I_{Q7}.I_{Q8}.I_{Q9}.I_{Q10}$ [1]
Also $I_{Q1}=I_{Q2}=I_{out}-I_2$, $I_{Q4}=I_{Q5}=I_{out}$, $I_{Q6}=I_{Q7}=I_2$, $I_{Q10}=I_{Q9}=I_4$
Substituting yields:
$I_{out}=I_4\sqrt{(I_3/I_1)}$ [3]

ii) Write down an expression for the output current I_{out} when $I_{in}=A\sin(\omega t)$ and I_1 and I_3 are derived as:

$$I_3 = \left|\frac{dI_{in}}{d_t}\right|, \qquad I_1 = \left|\int I_{in}\, dt\right|$$

[3]

$I_3 = \left|\frac{dI_{in}}{d_t}\right| = A\omega cos(\omega t)$, [0.5]
$I_1 = |\int I_{in}\, dt| = \frac{A}{\omega}\cos(\omega t)$ [0.5]
$I_{out}=I_4 \times \omega$ [2]

iii) What is the function of this circuit when the inputs are applied as in 2.b.ii ?

[1]

The circuit monitors the frequency of the input [1]

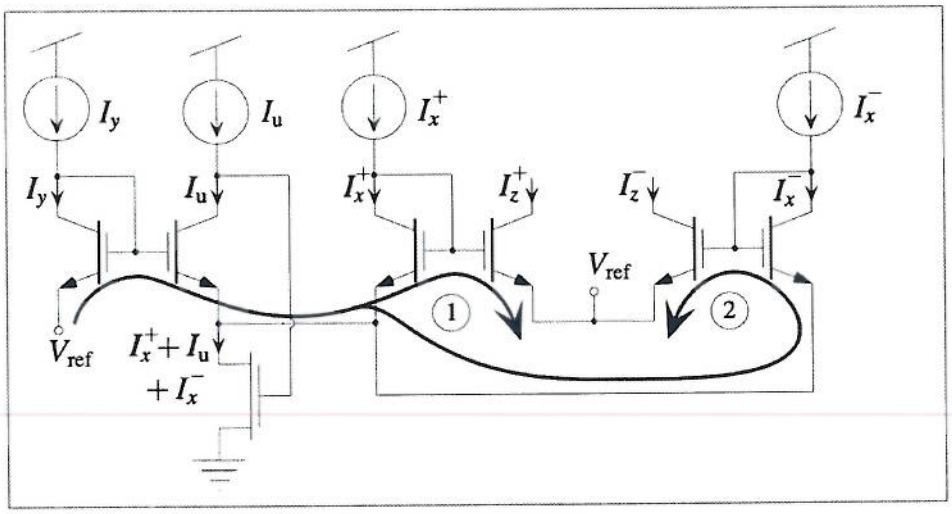
c) Synthesise using Type A cells a translinear circuit that implements the following function:

$$z^+ - z^- = (x^+ - x^-)y$$

Draw a complete circuit including all biasing schemes and removing redundant loops.

[5]

Solution:

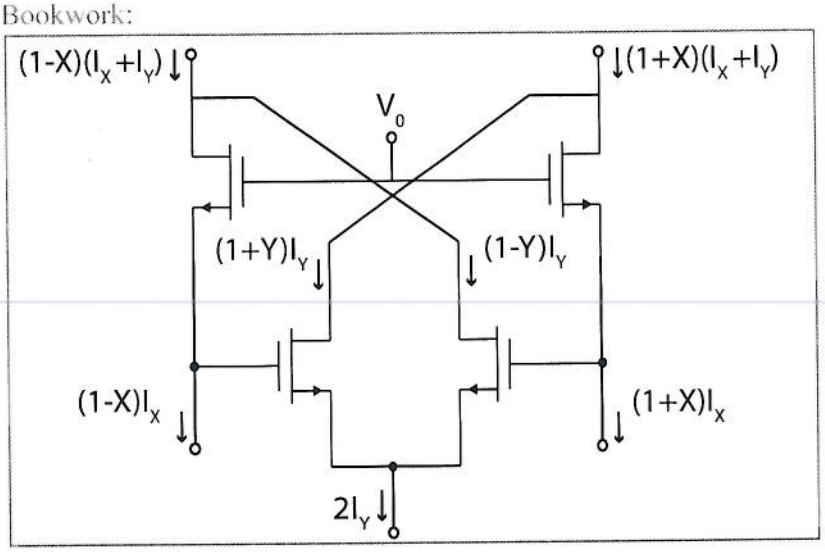


[2] For synthesis equation
[2] For circuit
[1] For removing redundancies.

d) Draw the circuit of the gilbert gain cell and explain it's advantage over a conventional translinear multiplier.

[3]

Bookwork:



Drawing of Circuit [2]
Advantage: Reuses current to provide more gain [1]

3.a) Explain the principle of companding illustrating how the dynamic range changes through the signal processing chain ?

[4]

[Bookwork]
Definition [2]
Diagram [2]

b) Figure 3.1 shows a block diagram of a current-mode companding integrator, with an input X and an output Y. f() and g() represent non-linear functions which compress and expand the signal such that input-output relationship of the integrator is linear and given by:

$$Y = \tau \int X \cdot dt$$

i) Given that the expansive function is defined as $I_{out}=g(V_c)=I_0\sinh(V_c/nUt)$, derive the function f(x) such that linear integration is achieved. All constants should be grouped to represent a current I_1, with the function f(x) composed of just I_{in}, I_1. and I_{cosh}, whereby $I_{cosh}=I_0\cosh(V_c/nU_t)$.

[6]

New derivation:

$$Y = I_{out} = I_0 \sinh(V_c / nU_t) = g(V_C)$$

$$\frac{d(g(V_c))}{dV_C} = \frac{dY}{dV_C} = \frac{dI_{out}}{dV_C} = \frac{I_0}{nU_t}\cosh(V_C / nU_t) = \frac{I_{Cosh}}{nU_t}$$

$$f(x) = I_C = X\tau C\left(\frac{dY}{dV_C}\right)^{-1} = X\tau C\frac{nU_t}{I_{\cosh}} = X\frac{I_1}{I_{\cosh}} \qquad X = I_{in}, \quad I_1 = \tau \cdot CnU_t$$

$$I_C = f(I_{in}) = \frac{I_{in}I_1}{I_{\cosh}}$$

c) The transfer function of an oscillator may be defined in state space representation by the following equations:

$$\dot{X}_1 = -\omega_0 X_1 + \omega_0 X_2$$

$$\dot{X}_2 = -2\omega_0 X_1 + \omega_0 X_2 + \omega_0 U$$

$$Y = X_1$$

whereby Y is the output and U is the input and X_1 and X_2 are the states.

(i) By using the mappings below show how these linear equations can be mapped to non-linear log-domain design equations. You may use the following mapping for constant currents, $I_1=I_2=I_\omega$ and $I_U=I_O$.

$$X_1 = I_1 \exp\left(\frac{V_1}{nU_t}\right) \qquad X_2 = I_2 \exp\left(\frac{V_2}{nU_t}\right) \qquad U = I_U \exp\left(\frac{V_U}{nU_t}\right)$$

[5]

Appliction of taught methodology.
Should apply state space mapping and derive the following KCL equations:

$$C\dot{V}_1 = -I_\omega - I_\omega \exp\left(\frac{V_2 - V_1}{nU_t}\right)$$

$$C\dot{V}_2 = -2I_\omega \exp\left(\frac{V_1 - V_2}{nU_t}\right) + I_\omega + I_0 \exp\left(\frac{V_U - V_2}{nU_t}\right)$$

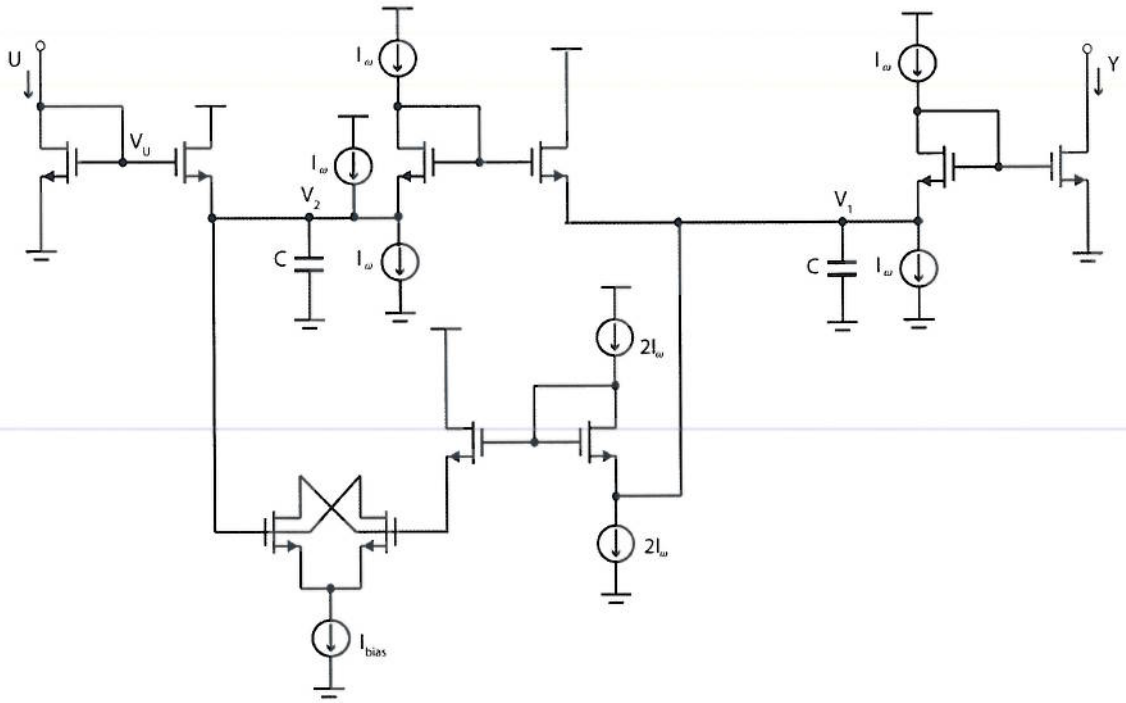
$$Y = I_\omega \exp\left(\frac{V_1}{nU_t}\right)$$

[5]

(ii) With these log-domain design equations, sketch a schematic of the final log domain filter using weak inversion MOS transistors.

[5]

Drawing of log domain circuit.



4.a) Figure 4.1 shows a conventional second-generation positive current conveyor, CCII+.

i) Explain it's principal of operation and describe how impedances at each of it's three ports differ from a standard operational amplifier.

[4]

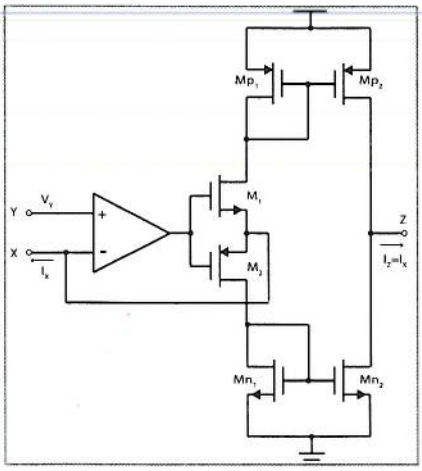
[bookwork]

- Current-voltage characteristics
  $V_X=V_Y$, $I_Z=\pm I_X$, $I_Y=0$
  $Z_Y \rightarrow \infty$, $Z_X \rightarrow 0$, $Z_Z \rightarrow \infty$
- Voltage-follower between Y-input and X-output
- Current-follower between X-input and Z-output [4]

ii) Draw the circuit of a CMOS implementation of a bi-directional CCII+ .

[3]

Schematic:



[3]

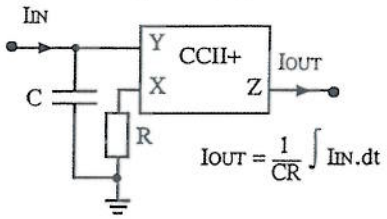
iv) Propose a method to increase it's output impedance.

[1]

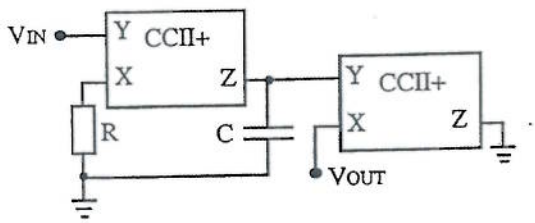
We can use cascaded current mirrors to increase output impedance at the expense of dynamic range. [1]

iii) Using the current conveyor in Figure 4.1 draw the schematics of current mode integrator and a voltage mode integrator each with a time constant, τ =1 second. You may assume R=100KΩ.

Current integrator [2]:



Voltage integrator [2]:

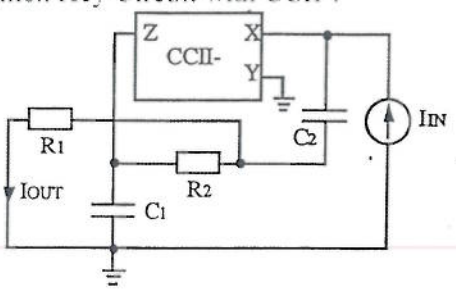


[4]

iv) Figure 4.2 shows a voltage mode sallen key filter. Using the adjoint principle transform this to it's current mode equivalent using CCII+ blocks.

[4]

Sallen Key Circuit with CCII-:



[2]

Student also needs to realize the CCII- block required can be implemented using two CCII+ blocks. [2]

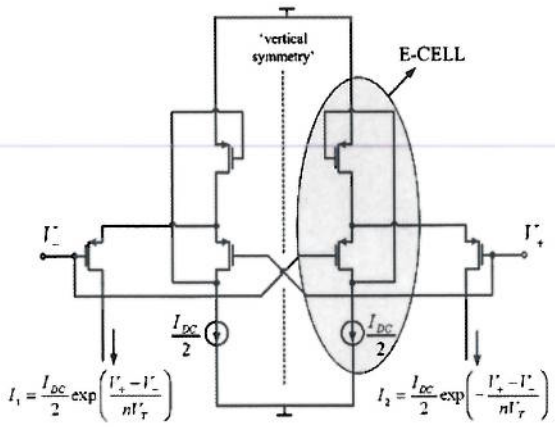
b) Design a single circuit current mode circuit that can implement the following trigonometric functions:

$$I_1 - I_2 = I_{DC} \sinh\left(\frac{V_1 - V_2}{nU_t}\right)$$

$$I_1 + I_2 = I_{DC} \cosh\left(\frac{V_1 - V_2}{nU_t}\right)$$

[4]

[bookwork]



$$I_1 - I_2 = I_{DC} \sinh\left(\frac{V_1 - V_2}{nU_t}\right)$$

$$I_1 + I_2 = I_{DC} \cosh\left(\frac{V_1 - V_2}{nU_t}\right)$$

5. This question relates to discreet time integrators.

a) Figure 5.1 shows a discreet time RC integrator.

i) Derive it's time constant of integration.

Switches M1, M2 and C1 for a resistor R, and time constant $\tau = RC_2$ where

$$R = \frac{1}{C_1 f_{CK}}$$

[2]

ii) Assuming $C_1=C_2$, select a suitable clock frequency to give a time constant $\tau = 1\mu s$

[2]

$\tau = C_2/C_1 \cdot f_{ck}$ which results in $f_{ck}=1MHz$

iii) If all of the channel charge, Q_1, of transistor M_1 is injected into C_1, estimate the total amount of charge injection from switches M_1 and M_2 which appears in the output capacitor C_2 after one integration cycle, assuming that the channel charge Q_2 of switch M_2 is split equally between C_1 and C_2.

[4]

[New application of taught theory]
Charge in Q_1 is injected into C_1 when CK goes low and M_1 turns off.
M_2 Turns on so charge $Q_1/2$ appears between both capacitors C_1 and C_2.
Charge is absorbed by M_2 to create channel but is injected back equally between C_1 and C_2 when CK goes high again. So the remaining charge injection on C_2 is $Q_1/2$.

b) Figure 5.2 shows an autozeroing switched capacitor integrator capable of removing any offset in the amplifier.

i) Derive the output voltage of the integrator during phase Φ1 and Φ2 showing how the offset is removed showing the charge on each capacitor.
[Derivation from notes]
Student should conclude to the following equations showing at each phase how the offset V_{os} gets subtracted.

$$v_{out}^{\Phi 2}(n) = v_{out}^{\Phi 2}(n-1) - (C_1/C_2)v_{in}^{\Phi 2}(n)$$

$$v_{out}^{\Phi 1}(n) = v_{out}^{\Phi 2}(n) + v_{os}$$

[4]

c) Figure 5.2 shows a schematic of switched current integrator.

i) Derive the transfer function of the switched current integrator and show that in the z-domain this may be represented as H(z)= A/(z-1).

[4]

[derivation from notes]
ii) Explain one limitation of the switched current technique that doesn't exist in its voltage mode equivalent.

[2]

VDS variations of memory transistors are an issue causing mismatch, need to be compensated [2].

iii) Propose one method to overcome this limitation and show it's schematic.

[2]

Increased output resistance through cascoding [1]
Schematic of a cascode [1]

6. Figure 6.1 shows a biomedical system used to measure the similarity between two EEG channels by recording action potentials from the human brain. The front end consists of a differential operational amplifier (OA) connected to a voltage-to-current (V/I) converter. This then connects to a current rectifier followed by a peak detector that detects the envelope of the converted current I_{out1}. The similarity between the envelopes of the two channels, I_{env1} and I_{env2}, is detected using a current mode correlator to derive an output signal I_{corr}.

a) Explain one method to make the input signals V_{sig1} and V_{sig2} immune to 1/f noise in the operational amplifier, and draw a block diagram of this method illustrating how the frequency spectrum of the signal changes during each stage.

[5]

[bookwork]
Student needs to identify that chopping can be used and explain the principle of chopper stabilization with the following diagrams.

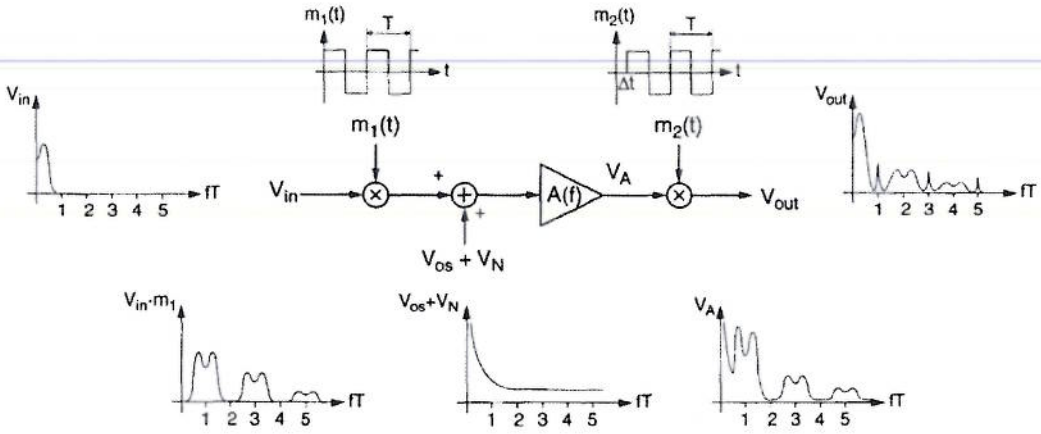
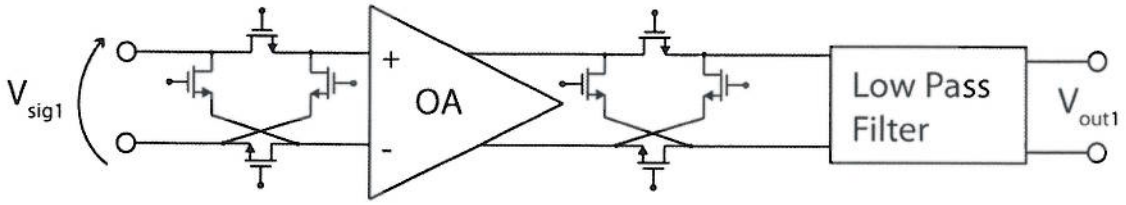


Fig. 9. The chopper amplification principle [19].

b) Design a suitable front end for this system using the method described in part 6.a. You may use the operational amplifier as in Figure 6.

[5]

[Application of theory].
Student needs to add chopping switches in input and output and low pass filter block.



c) Figure 6.2 show a suitable circuit that can be used as a current mode peak detector. Explain it's principal of operation.

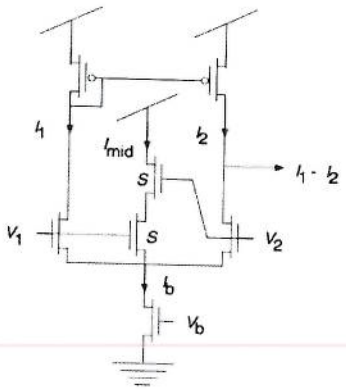
[5]

[bookwork]

d) The system in Figure 6.1 uses a V/I converter with improved linearity over a conventional differential pair. Sketch suitable schematics for the V/I converter and the current correlator used in this system. [5]

[Application of Known Theory]

V/I = Bump transconductor[3]



Current correlator = Two transistor correlator [2]