

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2010

MSc and EEE PART III/IV: MEng, BEng and ACGL

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Friday, 14 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for
candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : S. Lucyszyn

1. Figure 1 (a, b c, and d) show four popular biasing schemes typically used in analogue integrated circuits.

(a) Briefly explain the function of each of the circuits in Figure 1 (a, b, c and d) and derive expressions for the constant output parameter in each case, clearly indicating component design requirements and any approximations you have made. You may ignore bulk effects in the CMOS circuits.

[16]

(b) Design the constant current generator of Figure 1(c) to give an output current of $5 \mu\text{A}$. Assuming R is a polysilicon resistor with a temperature coefficient of $1500 \text{ ppm}/^\circ\text{C}$, calculate the fractional temperature coefficient of the circuit at room temperature.

[4]

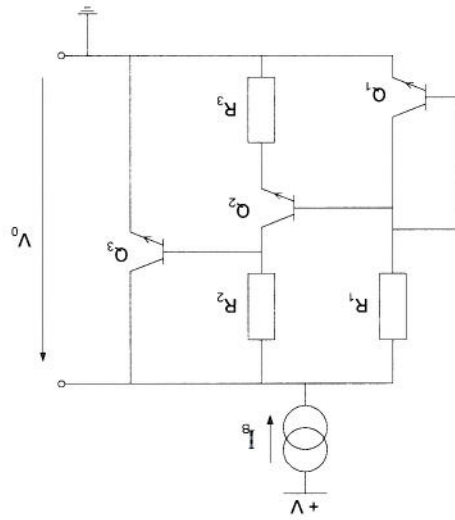


Figure 1(a)

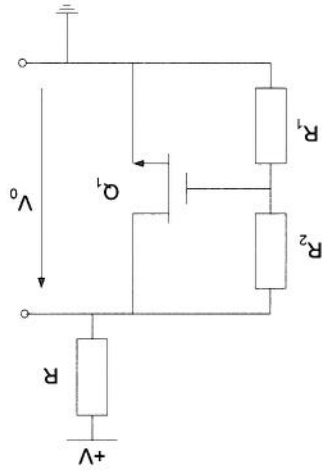


Figure 1(b)

Figure 1(d)

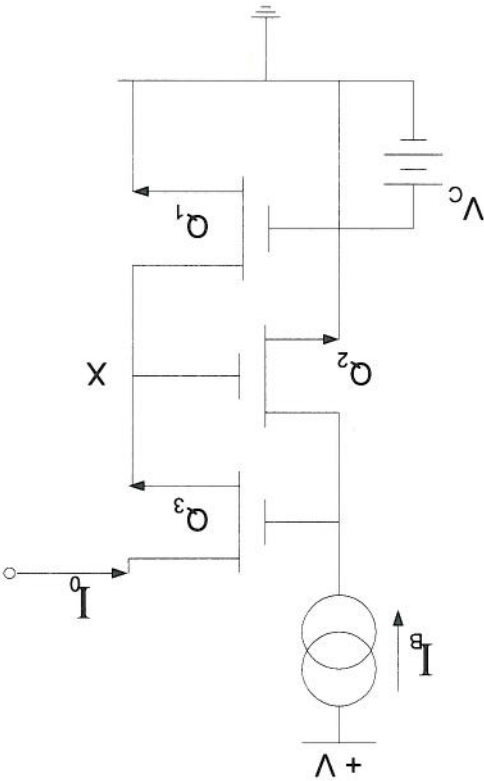
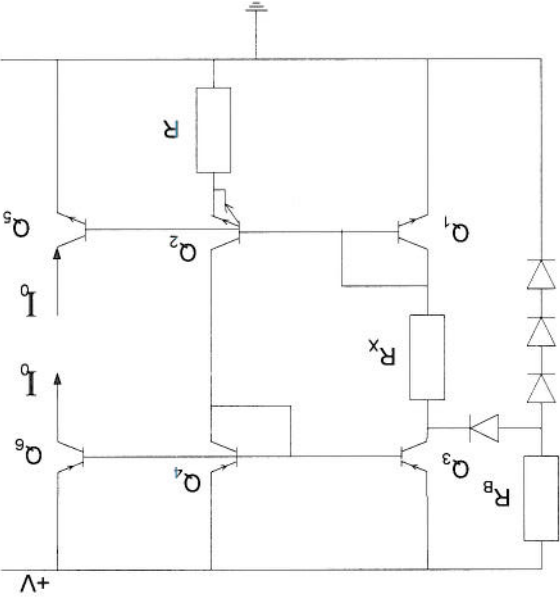


Figure 1(c)



2. (a) Two high-performance analogue-to-digital converters are the current-mode algorithmic converter and the sigma-delta converter. Sketch a typical architecture for ONE of these converter types and explain its principles of operation.

[10]

- (b) Assume that the maximum resolution of any sampled-data converter is limited by switch noise (kT/C). Calculate the maximum resolution of a stereo-audio system running at a sample rate of 40 kHz. Assume a MOSFET switch aspect ratio (W/L) = 1/8, transconductance parameter $k_p = 20 \mu A/V^2$ and a device threshold voltage $V_T = 1$ V. The on voltage of the switch is a 5 V reference (i.e. $V_{GSon} = V_{ref} = 5$ V). You may also assume that the switch settles in 10τ (where τ = time constant) over one period of the clock frequency.

Boltzmanns constant $k = 1.38 \times 10^{-23}$ J/K and the ambient temperature is 300 K.

[10]

3. Figure 3 shows a partially-designed two-stage CMOS op-amp required to give a voltage gain of approximately 80 dB, a slew-rate of 5 V/ μ s and a gain-bandwidth product of 3 MHz.
- (a) Given that the technology is a fixed 5 μ m double metal CMOS process, design the channel widths of transistors Q1, Q2 and Q6 for the op-amp to meet the above performance specifications. Aspect ratios of all other devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below. [15]
- (b) Give a reason why the introduction of a single integrated resistor in series with the compensation capacitor should significantly improve the amplifier's phase margin. [5]

CMOS TRANSISTOR MODEL PARAMETERS				
MODEL PARAMETERS				
	Kp (μ A/V ²)	λ (V ⁻¹)	V_{T0} (V)	
PMOS	20	0.03	-0.8	
NMOS	30	0.02	1.0	

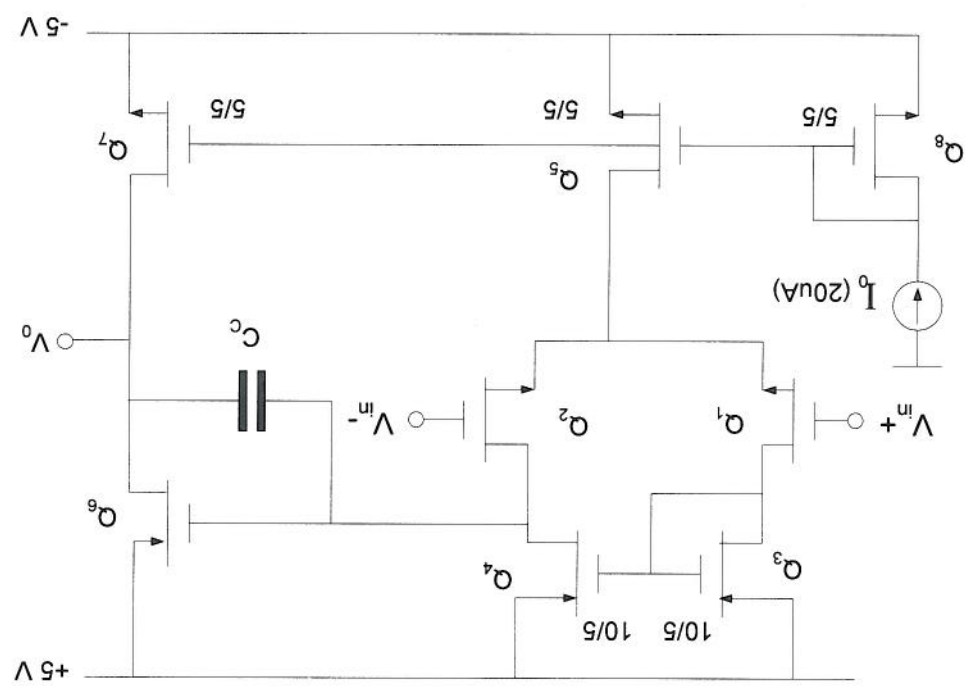


Figure 3

4. Figure 4 shows the basic design of an analogue sampled-data precision integrator.

- (a) Derive an expression for the transfer function of the integrator. Assume that the integrator is driven by non-overlapping clocks and that the switches are ideal.

[10]

- (b) (i) Sketch the basic design of a 3rd-order Chebyshev low pass switched-capacitor ladder filter.

The filter is to have a cut-off frequency of 5kHz. Assume a clocking frequency of 100 kHz. The values of integration capacity for the capacitor based sections are 6.44pF and inductive section is 3.164pF. All other switched capacitors are 1pF.

(ii)

From the circuit, estimate normalised passive component values for the original double-terminated LC prototype of the filter. All values should be normalised to 1 rad/s. You may assume that the clocking frequency is so high that the integrators can be assumed lossless.

[10]

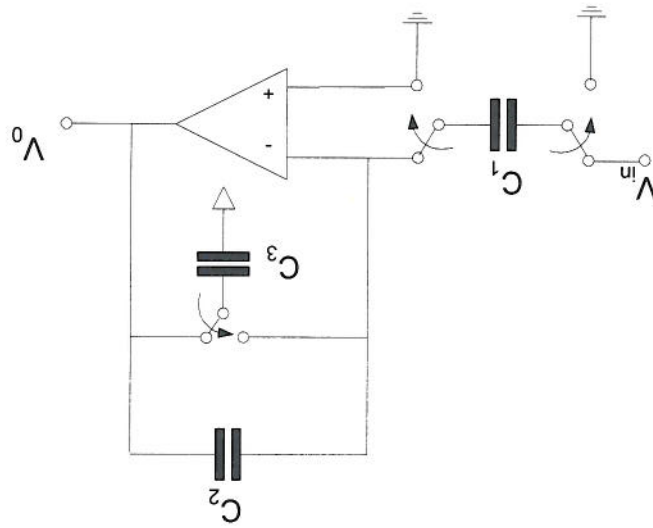


Figure 4

5. (a) Give two advantages of current-mode analogue signal processing compared to traditional voltage-mode processing.

[4]

- (b) With the aid of a suitable macromodel, explain the theoretical concept of current feedback and how it results in constant bandwidth amplification. Using a current-feedback op-amp, design a closed-loop non-inverting gain stage with a bandwidth of 10 MHz for a fixed voltage gain of 100. Assume an internal compensation capacitance of 4pF and that the open-loop transresistance gain of the amplifier is very much larger than the amplifier feedback resistor.

[16]

6. Figure 6 shows the basic design of an integrated circuit precision integrator.

- (a) Derive an expression for the time constant of the integrator. [10]

- (b) Why is it important for the MOSFETS in Figure 6 to operate in their triode region? Discuss the three key sources of non-linearity in the triode region. [4]

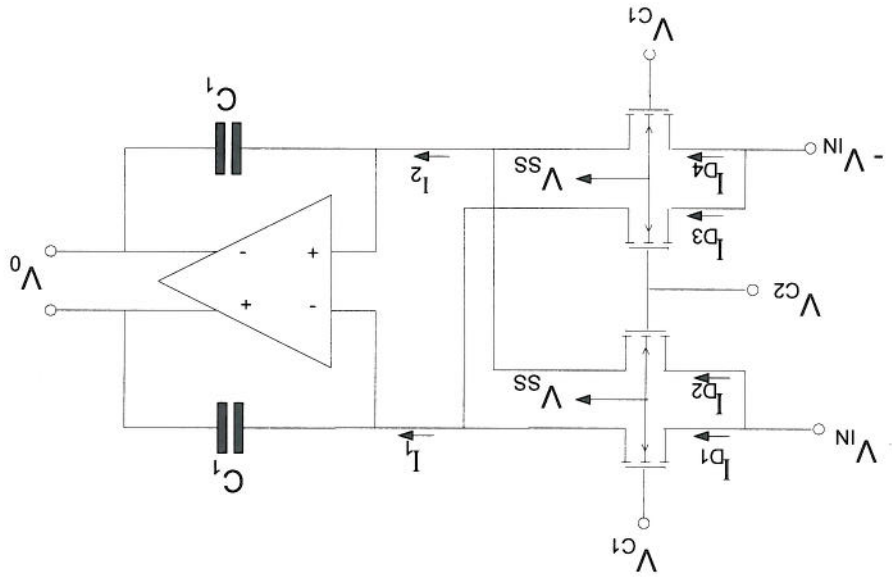


Figure 6

- (c) Sketch suitable fully differential folded cascade op-amp architecture for Figure 6. Why is it important for the amplifier to have common-mode feedback? [6]

Exam Solutions

E3.01
AC1

Analogue integrated circuit and system

2010

1 marker. C. Townsend
2 marker. S. Lucyshyn

①

①

a) Bandgap reference. Output voltage reference independent of temperature. Assume $V_{BE} = -2.5 \text{ mV}/^\circ\text{C}$ and $\beta \gg 1$

$$V_{BE3} - V_{BE2} = V_T \ln(I_1/I_2) = I_2 R_1$$

$$\text{Thus } V_O = V_{BE3} + (R_2/R_3) (V_T \ln I_1/I_2)$$

for $dV_O/dT = 0$, then $(R_2/R_3) \ln(I_1/I_2) \approx 24.5$, $V_O = 1.25 \text{ V}$

b) V_{GS} multiplier. Can replace shaded diodes with a single resistor for biasing purposes.

$$V_O = V_{GS} [1 + R_2/R_1]$$

$$\approx (1 + R_2/R_1) [V_T + \sqrt{I_0/R}] \quad (7)$$

c) PTH (proportional to absolute temperature)

current (current source/sink). The output current is virtually independent of the power supply voltage. Diode chain R_3 and R_4 form automatic offsetting circuitry.

ensures correct behavior in correct output state.

Modules - Assuming matched devices $\beta \gg 1$

$$\frac{I_{O1}}{I_{O2}} = \Delta V_{BE}/R = [V_T \ln(I_{O1}/I_{O2}) (I_{S3}/I_{S1})]/R$$

$$(I_{S3} = 2I_{S1}) \text{ then } I_{O2} = (V_T \ln 2) R$$

(4)

Question 4 - continued.

Fig 4d >

Regulated cascode circuit,
 since drain source voltage of Q1 is
 regulated by the feedback circuit
 Q2 the current has a very high
 output impedance equivalent to that
 of a double cascode.

$$\text{Analysis, } I_D = \beta (V_G - V_T)^2$$

assume FET Q1 is saturated

$$b) I_D = (V_{TM}^2) / R$$

assuming $V_T = 25 \text{ mV}$ at 300°K
 then $R = 3.465 \text{ k}\Omega$.

$$T_{CF} = \frac{1}{V_T} \frac{\partial V_T}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T}$$

$$= \frac{1}{T} - \left(\frac{1}{R} \frac{\partial R}{\partial T} \right)$$

$$= \left(\frac{1}{300} \right) - \left(1500 \times 10^{-6} \right)$$

$$= 1.833 \text{ ppm}/^\circ \text{C}$$

(4)

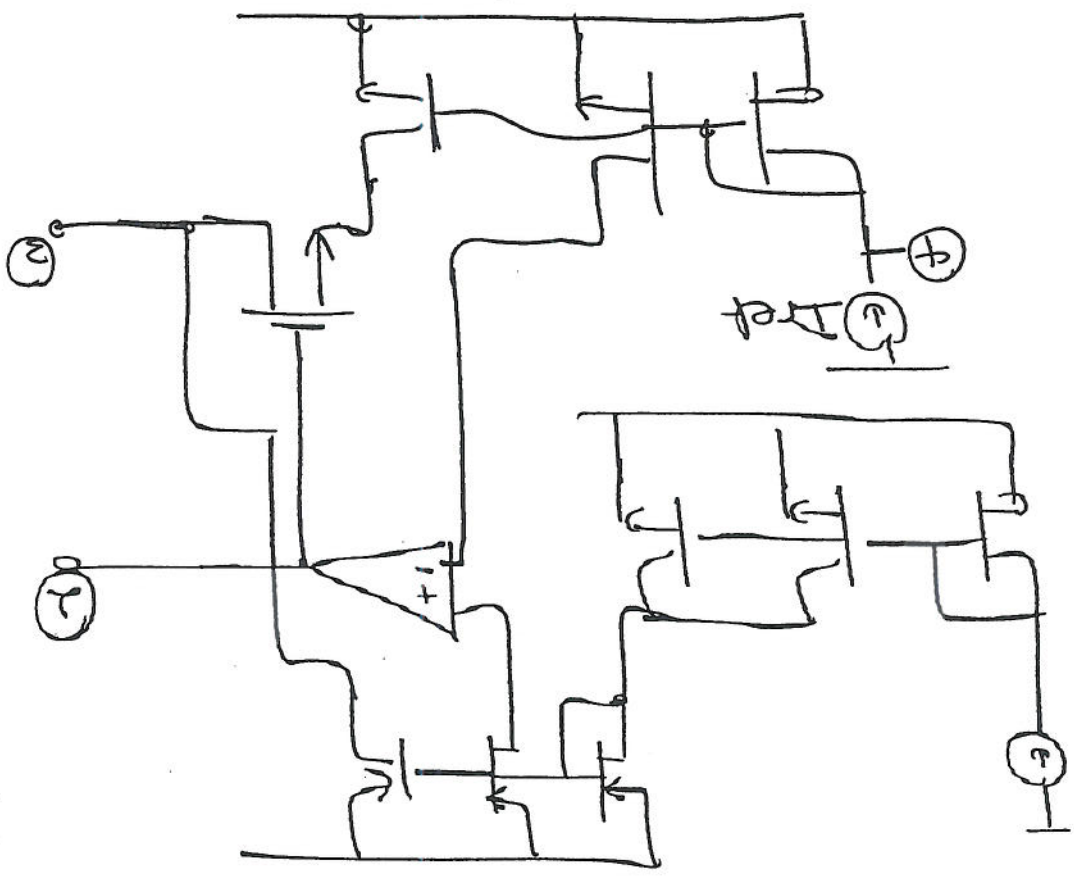
CT

(2)

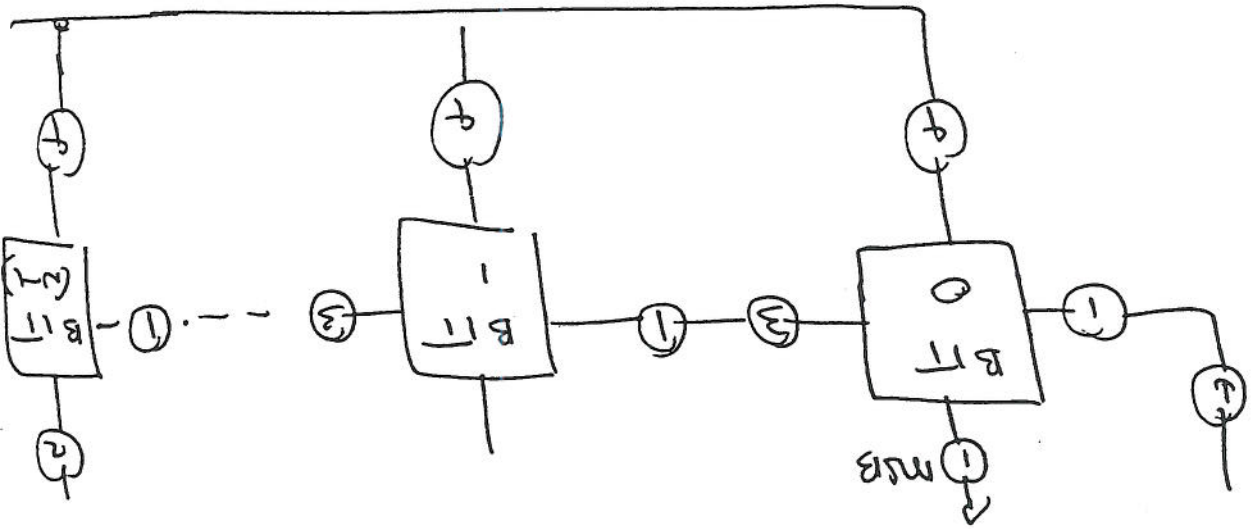
Question 2

High gain CMOS

1 Bit



Bit C Architecture



Question 2 - Cont

If $2I_{in} < I_{ref}$

Comp sees low, digital output = 0
and creates output $2I_{in}$

If $2I_{in} > I_{ref}$, comp output goes high, digital = 1

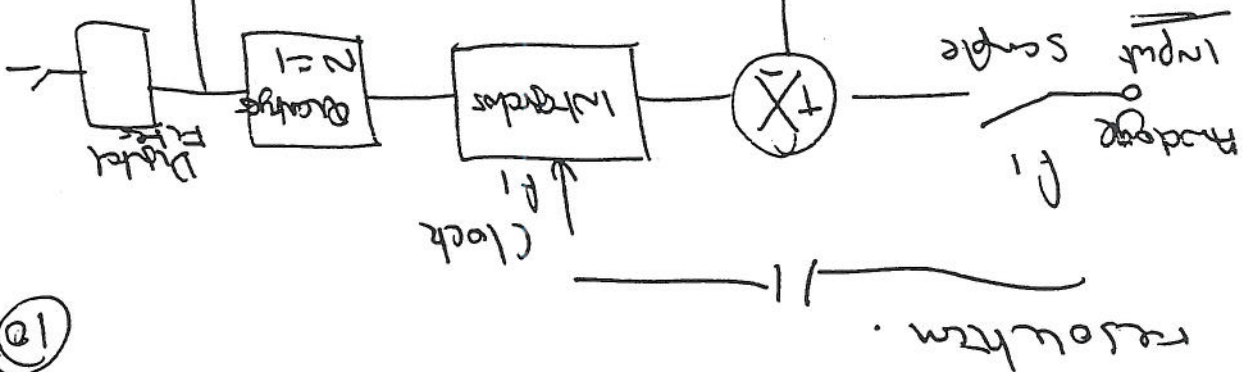
analog output $(2I_{in} - I_{ref})$

Analog output continuously feeds into following 'bit' which

performs exactly the same function.

The process is repeated as many times as needed to achieve desired

(10)



modulus
Σ-D
CT

Question 2 - Cont

Coarse quantization at high sampling rate combined with negative feedback and digital filters achieve increased resolution at lower sampling rates.

It means of trading resolution in time for resolution in amplitude according

we need for precision analogue components.

Negative feedback produces coarse estimate that oscillate about the true value of the input, the digital filter averages the coarse estimate to give a finer approximation.

Feedback $P/D + \text{integrator} \rightarrow$

quantization error to have a high frequency spectrum, filtered

out by digital filter.

Noise shaped out all high frequency

noise filtered away very high

(S/N) at low frequency.

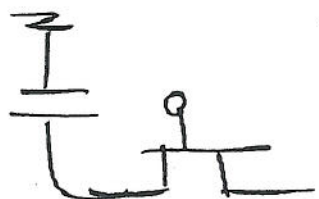
(10)

(1)

Question 2 cont

$$D_A \approx V_{ref} / I_{noise} = I_{N}$$

switch



$$\sqrt{\frac{C}{kT}}$$

Capacitor

RMS noise of switch

$$\text{Assume } f_c = \frac{1}{10 R \cdot C}, \text{ then}$$

Solution for C gives

$$D_A = I_N = V_{ref} / \sqrt{kT \cdot 10 \cdot R \cdot f_c}$$

$$R_{ov} = \frac{1}{I_N (V_{DD} - V_T) (A \beta \times 4)}$$

$$\beta = \left[\frac{k v}{A L} \right]$$

Can now find D_R at 40 kHz

(10)

3 // Specs $A = 80dB$, $s.e. = 5\sqrt{Hz}$, $C_B = 3MHz$

a) $A_1 = g_{m2}/(g_{m4} + g_{m2}) \Rightarrow (g_{m2}/g_{m4})$

$= 102 (1.2 + 1.6)$

$= 10 \times 10^{-6} [0.05]$

$= 5 \times 10^{-7} \mu^{-1}$

$g_{m2} = 2\sqrt{I_{D2} I_{D1}} \Rightarrow \text{but } G.B = g_{m2} \cdot 2\pi C_c$

require C_c . From $s.B = I_{D1}/C_c$

When $C_c = 4pF \Rightarrow g_{m2} = 7.54 \times 10^{-5}$

$\therefore A_1 = -150.8$

From $g_{m2} = g_{m1} = 2\sqrt{I_{D1} I_{D2}}$

$B_2 = B_1 = 1.42 \times 10^{-4} = K W \cdot 2L$

$\therefore (W/L)_2 = (W/L)_1 = 9.46$

$= 47/5$

Since $A_1 = 150.8$, $A_2 = 10^4 / (150.8) = 66$

$A_2 = g_{m6}/(g_{m4} + g_{m6})$

$(906 + 907) = 101 (1.6 + 1.7)$

(3) cont

$$(506 + 907) = 20 \times 10^{-6} (0.05) = 1 \times 10^{-2}$$

$$\text{avg } \omega_n = 6.63 \times 10^{-5}$$

$$\Rightarrow \beta \omega = \left(\frac{\omega_n}{2} \right)^2 \frac{1}{100} = 5.5 \times 10^{-5}$$

$$\text{Then } \omega_{\text{avg}} (\omega/L)^6 = 5.5 = 27/5$$

1/1

b)

R

C

provide feedback

Comparison of elements RHP

zero from transfer

function of OR-RHP.

with $R \Rightarrow \text{zero} = \omega_n / C$,

with R

$$Z = \frac{1}{1}$$

$$(1/\omega_n - R) C$$

(1)

$$R = 1/\omega_n \rightarrow \text{remove zero}$$

improve ϕ

(2) $R \Rightarrow$ non dominant pole cancels

with zero

$$\omega_n > 1/\omega_n$$

or

Q4 - lossy integrator.

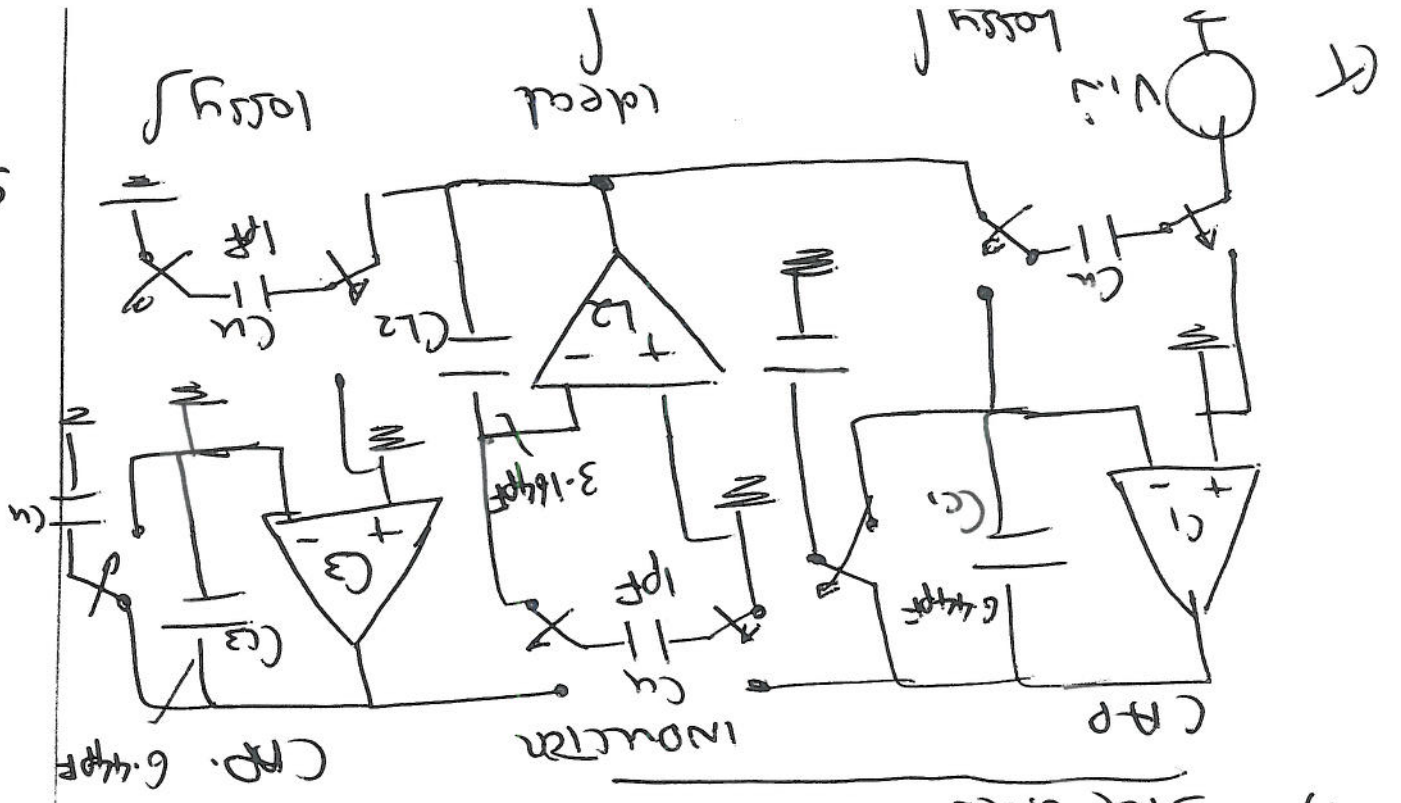
During ϕ_1 of switch, $I_{out} = C \cdot V_{in} / T$
 $\phi_2 - C \cdot V_{in} / T = V_{out} [3\omega C] + \frac{1}{(3V_0)}$
 Transfer & charge

frequency yields

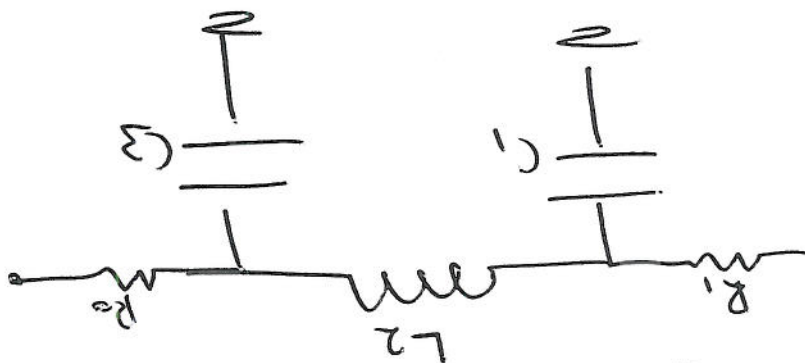
$$V_{out}/V_{in} = -C_1/C_3 \left[\frac{1}{(1 + j\omega \frac{C_3}{C_2})} \right]$$

$$H_p = \frac{1}{2 \pi \frac{C_3}{C_2}} \cdot \frac{1}{(1 + jf/f_c)}$$

b) 3rd order SC low pass



Q4 cont Doubly Terminated Ladder.



(converters into different network)

$$\left. \begin{aligned} C_1/C_2 &= f_c C_1 \\ C_3/C_2 &= f_c C_3 \\ C_1/C_2 &= f_c L_2 \end{aligned} \right\} \text{general transformation}$$

$$R_1 = R_2 = 1 \Omega = R_0.$$

Assuming $f_c = 100 \text{ kHz}$, $C_2 = 1 \text{ pF}$

$$\text{When } C_1 = C_3 = 0.44 \times 10^{-5} \text{ F}$$

$$C_2 = 3.164 \times 10^{-5} \text{ F}$$

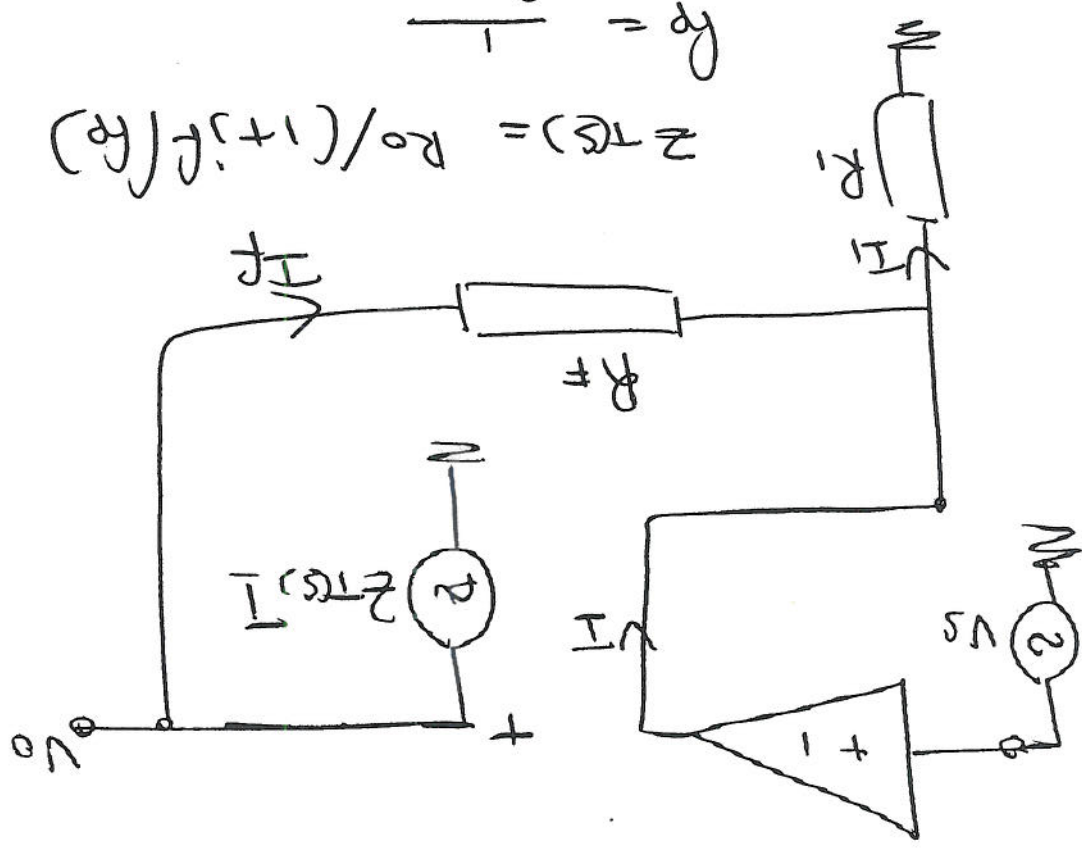
Normalized $2 \pi f$

$$\text{where } f = 5 \text{ kHz}$$

$$\text{Then } C_1 = C_3 = 2.0236 \times 10^{-5} \text{ F}$$

$$C_2 = 0.994 \times 10^{-5} \text{ F}$$

Advantages of Current-mode
 1) High frequency performance, wide dynamic range
 2) Lowers power supply voltages



$$Z_{TS} = R_O / (1 + jf/f_p)$$

$$f_p = \frac{1}{2\pi R_O C}$$

C = compensation capacitor

3 equations

$$I_F = (V_O - V_S) R_F \quad \text{--- (1)}$$

$$I_1 = V_S / R_I \quad \text{--- (2)}$$

$$V_O = Z_{TS} I = Z_{TS} [I_1 - I_F] \quad \text{--- (3)}$$

(if

2

1

2

Subs ① and ② into ③ gives,

$$(V_o/V_s) = (1 + R_F/R_1) \cdot Z(s) / (R_F + Z(s))$$

subs for $Z(s)$

$$(V_o/V_s)_{sw} = \underbrace{(1 + R_F/R_1) \left[\frac{R_o}{R_o + R_F} \right]}_{\text{gain}}$$

$$\times \frac{(1 + j\omega/R_o [R_o + R_F])}{R_F}$$

Assuming $R_o \gg R_F$ BW

then
closed loop gain $\approx (1 + R_F/R_1) - *$
closed loop bandwidth $\approx \frac{1}{R_F}$

$$A_F \approx \frac{1}{R_F}$$

L*

Hence R_F sets the amplifier
cutoff BW

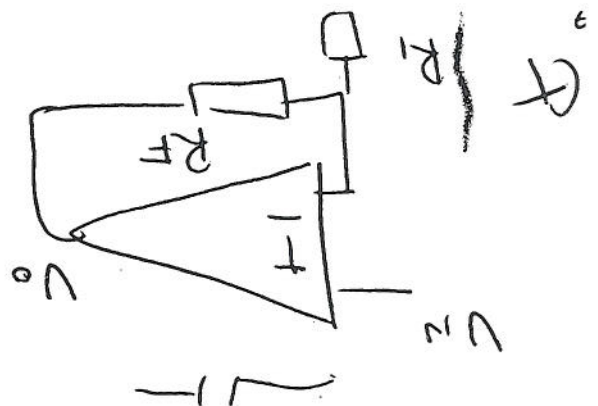
and R_1 chosen to set the gain

$$BW = \frac{1}{2\pi R_F C} = 10 \text{ MHz}$$

\therefore Given $C = 4 \text{ pF}$

$$R_F = 3.98 \text{ k}\Omega$$

$$\text{Since } A = (1 + R_F/R_1) = 100$$



Source: $A = (1 + R_F/R_1) = 100$

(T)

- (iii) Log values, $V_{DS}^2/2$ term makes region non-linear.
- (ii) V_{DS} approaching $(V_{DS} - V_T)$ here 3 checks for positive V_{DS} effect.
- (i) V_{DS} changing V_T due to body

3 sources of non-linearity

$$\pm 0 = \frac{L}{2W} [(V_{GS} - V_T)W - V_{DS}^2] (1 \pm 1/V_{GS})$$

when $V_{DS} < C(V_{GS} - V_T)$ region shows a square law characteristic. avoid non-linear effects in saturation linear triode region important to

6)

$$\beta = \frac{KW}{2L}$$

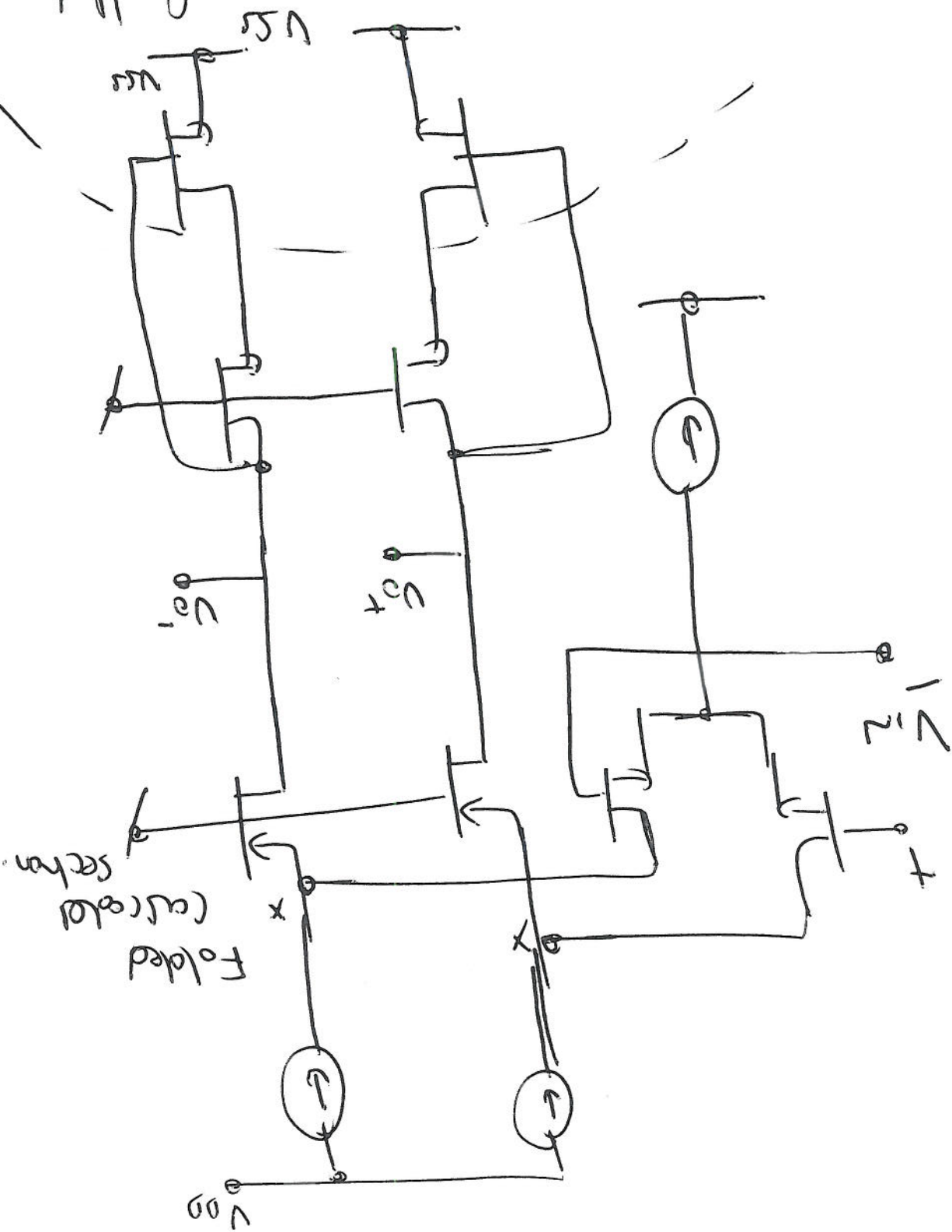
$$r_c = \frac{2\beta(V_{GS} - V_{DS})}{C}$$

Expected shunt to give full derivation.

$$\beta = \frac{(I_1 - I_2)}{V_{IN} - (-V_{IN})} = \frac{2\beta(V_{GS} - V_{DS})}{1}$$

6) a) Flaring intrinsic R.C network Double mos resistors

6 c)



$A = \frac{1}{2} \left(\frac{g_m}{g_D} \right)^2$
 (common-mode feedback) is necessary to
 reduce output differential
 offset or to ensure
 rejection of common-signal
 at output.

(7)

