IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2008

EEE/ISE PART I: MEng, BEng and ACGI

**ANALYSIS OF CIRCUITS**

Wednesday, 28 May 10:00 am

Corrected Copy

Time allowed: 2:00 hours

**There are FOUR questions on this paper.**

**Q1 is compulsory.**
**Answer Q1 and any two of questions 2-4.**
**Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).**

**Any special instructions for invigilators and information for candidates are on page 1.**

Examiners responsible First Marker(s) : D.G. Haigh, D.G. Haigh
Second Marker(s) : P.D. Mitcheson, P.D. Mitcheson

1 a) Use source transformations to determine the voltage v in the circuit in Figure 1 (a).

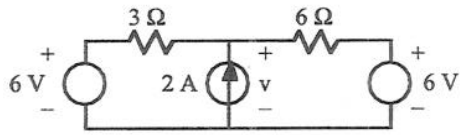



Figure 1(a)

[4]

b) Use the principle of superposition to find current $i$ in the circuit in Figure 1(b).

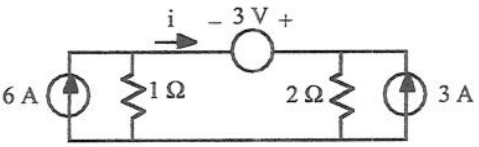



Figure 1(b)

[4]

c) Derive both the Thevenin and the Norton equivalent circuits for the sub-circuit in Figure 1(c); an approach based on determining short-circuit current and the Thevenin resistance is recommended.

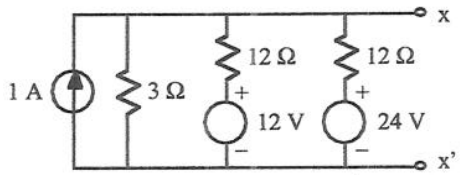



Figure 1(c)

[4]

d) Use nodal analysis to determine the nodal voltages $v_1$ and $v_2$ in the circuit of Figure 1(d).

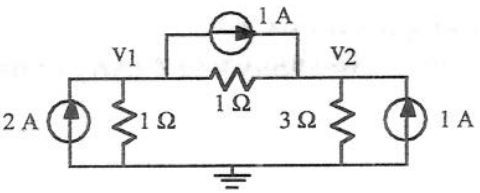



Figure 1(d)

[4]

e) In the circuit of Figure 1(e), the switch remains in position 1 for a long time before moving to position 2 at time $t = 0$ s. Find (i) capacitor voltage $v_c(t)$ at $t =$ 0 s before the switch moves, (ii) final value of $v_c(t)$ for $t \to \infty$, (iii) the time constant for $t \geq 0$ s and (iv) an equation for $v_c(t)$ as a function of time.

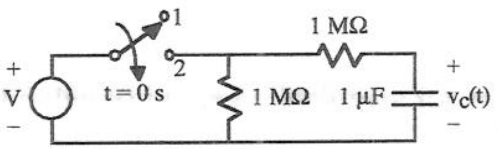
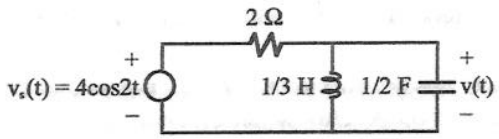



Figure 1(e)

[4]

f) Write the voltage $v_s(t) = 4\cos 2t$ in phasor form. Write the impedance of a 1/3 H inductor and a 1/2 F capacitor at a frequency of 2 rad/sec. Hence, use the phasor method to determine the voltage $v(t)$ in Figure 1(f).

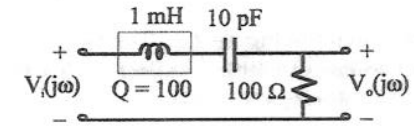
Figure 1(f)




[4]

g) In the bandpass filter circuit of Figure 1(g), the inductor symbol represents a lossy inductor that has a Q-factor of 100 at the filter resonant frequency. Determine (i) the resonant frequency of the filter circuit in rad/sec, (ii) the equivalent resistance in series with the inductor that represents its loss and (iii) the gain of the filter circuit $V_o(j\omega)/V_i(j\omega)$ at its resonant frequency.

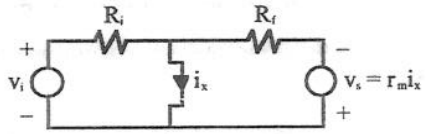
Figure 1(g)




[4]

h) Figure 1(h) shows a circuit containing a dependent source that is a current-controlled voltage source, for which the controlling variable is $i_x$. Write an expression for current $i_x$ as a function of the voltages $v_i$ and $v_s$ and hence determine an expression for $v_s$ in terms of $v_i$.

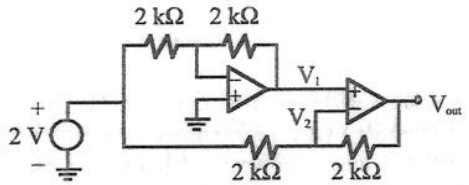
Figure 1(h)




[4]

i) The circuit in Figure 1(i) contains two operational amplifiers that we treat here as ideal. Determine the voltages $v_1$ and $v_2$ and the output voltage $v_{out}$.

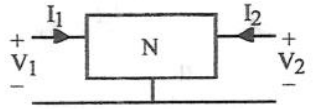
Figure 1(i)




[4]

j) A linear 2-port circuit with its 2-port admittance description is given in Figure 1(j). The circuit is loaded at port 2 by a resistor $R_L$ (not shown). Determine the voltage gain $V_2/V_1$ for the loaded circuit in terms of the y-parameters ($y_{11}$, $y_{12}$, $y_{21}$ and $y_{22}$) and the load resistance ($R_L$).

Figure 1(j)




$$I_1 = y_{11}V_1 + y_{12}V_2$$
$$I_2 = y_{21}V_1 + y_{22}V_2$$

[4]

2 a) Write two expressions, one relating voltage $v_L(t)$ and current $i_L(t)$ for an inductor and the other relating voltage $v_C(t)$ and current $i_C(t)$ for a capacitor.

Hence or otherwise, obtain circuit models for the inductor and for the capacitor that are appropriate for DC steady-state analysis of a circuit containing these elements.

Use the DC steady state models for the inductor and for the capacitor in order to carry out DC steady-state analysis on the circuit in Figure 2.1 in order to find the values of voltage v and current i.

[8]

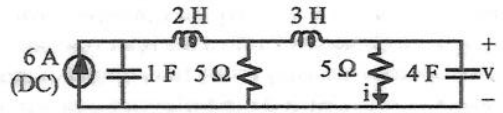



Figure 2.1 Circuit for Question 2(a)

b) Consider the circuit in Figure 2.2. The switch spends a long time in position 1, allowing all voltages to settle. At time $t = 0$ s, the switch moves to position 2. Determine the following for $t \geq 0$:

i) The time constant that governs the capacitor voltage $v(t)$

ii) The initial value of $v(t)$ for $t = 0$

iii) The final value of $v(t)$ for $t \to \infty$

iv) An expression for $v(t)$ as a function of $t$

v) The value of $v(t)$ at $t = 2$ ms

After 2 milli-seconds, the switch returns to position 1.

vi) Determine the time constant that governs the capacitor voltage $v(t)$ for $t \geq$ 2 ms.

[16]

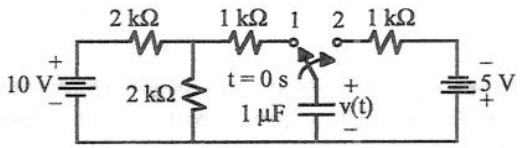



Figure 2.2 Circuit for Question 2(b)

c) Two digital logic gates are inter-connected as shown in Figure 2.3(a). The voltage at node 'x' is modelled very approximately by RC circuits for the voltage pull-up and for the voltage pull-down as in Figures 2.3(b) and (c), respectively. Given that the voltage at node 'x' moves between the allowed logic levels in a time equal to 1.75 time constants, determine the minimum clock period and maximum clock rate for this part of the system.

[6]

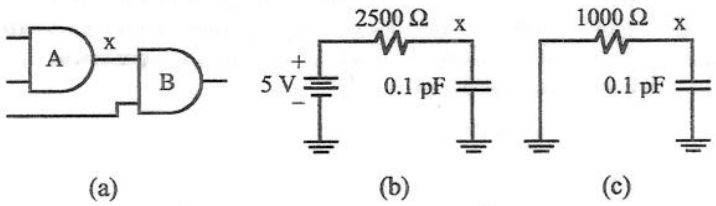



Figure 2.3 Circuit for Question 2(c)

3 a) Give a general definition for *impedance* of an element.

State expressions for the impedance of an inductor of value $L$ at a frequency $\omega$ and for the impedance of a capacitor of value $C$ at a frequency $\omega$.

Give a general definition for *reactance*.

Give expressions for the reactance of an inductor and of a capacitor. Sketch them versus frequency using linear scales for reactance and for frequency and then using logarithmic scales for reactance and for frequency.

For a sub-circuit consisting of a *series* combination of inductor $L$ and capacitor $C$, write expressions for the impedance and for the reactance of the subcircuit.

Sketch the magnitude of the reactance versus frequency for the series LC sub-circuit using logarithmic scales for reactance and for frequency.

[12]

b) For the RC circuit in Figure 3.1, determine the frequency response function $H(j\omega) = V_o(j\omega)/V_i(j\omega)$.

Given that, in Figure 3.1, $R = 1$ kΩ and $C = 1$ nF, determine the frequency where the phase response is zero and determine the amplitude response at that frequency.

For the same circuit, sketch the amplitude and phase responses versus frequency.

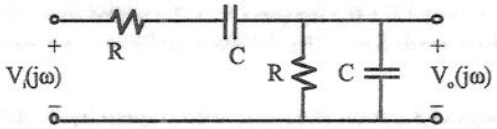



Figure 3.1 Circuit for Question 3(b)

[8]

c) Figure 3.2 shows a generic structure that can generate many types of 2nd order filter by assigning each of the three impedances $Z_1$, $Z_2$ and $Z_3$ to be either an inductor $L$, a capacitor $C$ or a resistor $R$.

Assign element types $L$, $C$ and $R$ to the three impedances in Figure 3.2 in order to realise 2nd order filters of the following three types:

i) 2nd order lowpass filter

ii) 2nd order bandpass filter

iii) 2nd order highpass filter

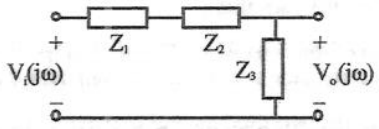



Figure 3.2 Circuit for Question 3(c)

[6]

d) Give one example, for each, of the use in systems for (i) bandpass and (ii) lowpass filters.

[4]

4. a) State two possible advantages of using operational amplifiers (op-amps) as elements for analogue circuit design, rather than designing at transistor-level.

[4]

b) Design and show circuits using one or more op-amps and any other necessary elements with their values in order to realise the following requirements, following the advised constraints below:

i) $V_{out} = 5\ V_{in}$

ii) $V_{out} = -5\ V_{in}$

iii) $V_{out} = -5\ V_{in}$ to $5\ V_{in}$, adjustable by means of a potentiometer

$V_{out}$ and $V_{in}$ are input and output voltages, respectively. The constraints on the design are 1) to try to not use unnecessary elements, and 2) to design in order to avoid problems in interfacing with preceding and following circuits by using practical element values and ensuring that each circuit has reasonably high input impedance and reasonably low output impedance.

[7]

c) The *first cut* of a circuit design using op-amps may be done assuming that the op-amps are ideal, in which case the op-amps may be modelled as nullors comprising a nullator and a norator.

Show the nullor model for the op-amp. For the nullator and norator that comprise the nullor op-amp model, give the defining equations in terms of their voltage and current.

The first cut design of a circuit is usually then *refined* by taking into account the non-ideal behaviour of practical op-amps. State two non-ideal performance limitations of a practical op-amp that are very significant and therefore should usually be considered at this stage.

[7]

d) Op-amps are attractive and popular for design. However, in some situations, transistor level design is more appropriate. State two situations where this is likely to be the case.

[4]

e) Small-signal models for transistors are used in order to derive by circuit analysis (and by computer circuit analysis programs, such as SPICE) the small-signal response of a circuit containing them.

Draw the topology, excluding capacitances and output resistance, of small-signal models for the bipolar transistor and for the field-effect transistor.

Label the elements in these two models and express the element parameters in terms of device constants and bias voltages or currents.

Given an AC small-signal equivalent circuit for a circuit containing transistors, state a suitable method of by-hand circuit analysis that would allow you to obtain the frequency response function $H(j\omega) = V_{out}(j\omega)/V_{in}(j\omega)$.

[8]