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EE2-2

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2012

EEE PART II: MEng, BEng and ACGI

CORRECTED - Q2

ANALOGUE ELECTRONICS 2

Wednesday, 30 May 2:00 pm

Time allowed: 1 hour 30 minutes

There are THREE questions on this paper.

ALL questions are compulsory.
Question 1 carries 40% of the marks and Questions 2 and 3 carry 30% each.

Any special instructions for invigilators and information for candidates are on page 1.

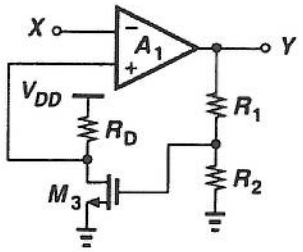
Basic expressions for voltage gain, input and output resistance for single stage amplifiers are given on the last page.

Examiners responsible — First Marker(s): T.G. Constandinou; Second Marker(s): K. Harris

1. This question consists of 6 sub-questions. Each item can be answered in a few words or a short paragraph with use of a diagram and/or expression where helpful. Please answer all sub-questions.

a) Explain the difference between an *ideal voltage amplifier* and an *op-amp*. [5]

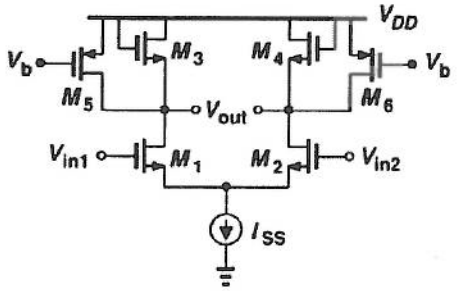
b) Calculate the *loop gain* and *closed-loop gain* of the circuit shown below. Assume the op-amp has an open-loop gain of A_1, but is otherwise ideal. Also assume $\lambda=0$ for M3. [5]



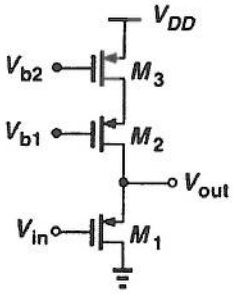
c) Describe the *common base* amplifier. Draw a schematic for the common base amplifier and comment on the relative levels of its input and output impedances. Describe and justify whether the common base amplifier is better described as a transimpedance amplifier or a unity-gain current amplifier? [5]

d) The LM741 op-amp is quoted as having a *Gain-Bandwidth Product (GBP)* of 1MHz. Explain the meaning on GBP. If a LM741 were configured with feedback to give a closed loop gain of 50, what would its *bandwidth* be? [5]

e) Derive expressions (by inspection) for the *voltage gain* of the amplifier circuits shown below (assuming $\lambda\neq0$, i.e. including r_O). State any assumptions made if simplifying the expressions. [10]

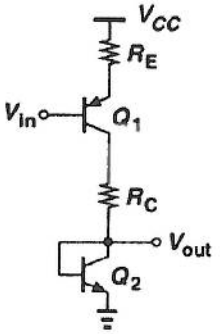


(i)

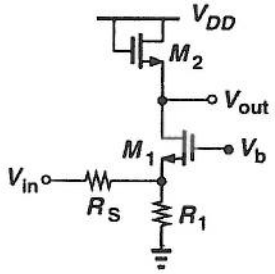


(ii)

f) Derive expressions (by inspection) for the *input impedance* and *output impedance* of the circuits shown below (assuming $V_A=\infty$ and $\lambda=0$, i.e. excluding r_O). State any assumptions made if simplifying the expressions. [10]



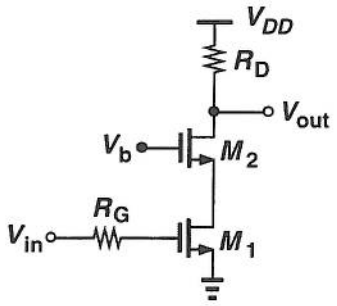
(i)



(ii)

2. The circuit shown below is a two-stage amplifier consisting of a common source amplifier (M_1) followed by a common gate (M_2) stage (often referred to as a cascode).

Use the following parameters: V_{DD}=1.8V, $(W/L)_1$=25μm/0.18μm, $(W/L)_2$=50μm/0.18μm, $I_{D1}=I_{D2}$=1mA, $C_{GS}=(2/3)(WL)C_{ox}$, C_{ox}=12fF/μm^2, $\mu_n C_{ox}$=200μA/V^2, λ=0, $C_{SB}=C_{DB}$=0 and $C_{GD}=C_0W$, where C_0=0.2fF/μm denotes the gate-drain capacitance per unit width.



a) Compare the frequency responses of a common source and common gate amplifier.

[4]

b) Redraw the circuit above to: (i) identify any nodes that are associated with poles and (ii) include all the parasitic device capacitances (within M_{1-1}).

[10]

c) Redraw the circuit drawn in your answer to (b) to remove any redundant capacitances and lump together any parallel capacitances. Determine expressions for the different pole frequencies using Miller's theorem where appropriate.

[8]

d) Determine an expression for the DC (low frequency) gain of the amplifier.

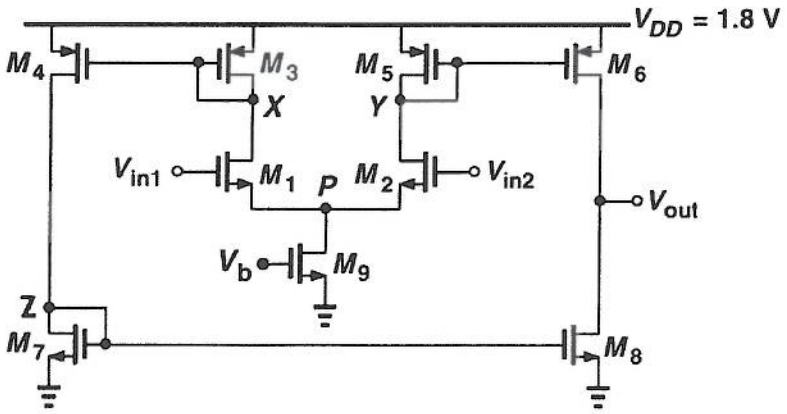
[2]

e) Evaluate the DC gain and pole frequencies, for $R_D=R_G$=2kΩ.

[6]

3. The circuit shown below is called a *fully-balanced Operational Transconductance Amplifier (OTA)*. The circuit operates as follows: Device M9 provides the bias current (sink) to the differential pair M_1/M_2. The two tail currents (I_{D1} and I_{D2}) are then copied by the active current mirrors M_3/M_4, M_5/M_6 and M_7/M_8 such as to subtract current I_1 from I_2 at the output node. This output current (i.e. I_2 - I_1) is typically delivered to an external load. Mirrors M_5/M_6 and M_7/M_8 can be scaled 1:K to provide additional current gain.

Assume all devices are in saturation and $\lambda>0$ (i.e. $R_{out}<\infty$). Where required, use the following values: $\mu_nC_{ox}=200\mu A/V^2$, $\mu_pC_{ox}=100\mu A/V^2$, $V_{TH,n}=0.4V$, $V_{TH,p}=-0.5V$, $\lambda_n=0.1V^{-1}$, $\lambda_p=0.2V^{-1}$.



a) This OTA can be used as a voltage amplifier, provided that the load resistance is large. Determine an expression for the voltage gain of the OTA, i.e. $A_v=V_{out}/(V_{in2}-V_{in1})$ given that $(W/L)_6=K(W/L)_5$ and $(W/L)_8=K(W/L)_7$.

[5]

b) Given that $I_{bias}=I_{D9}=10\mu A$, $(W/L)_{1,2}=50/0.5$, $(W/L)_{3,4,5}=6/3$, $(W/L)_6=60/3$, $(W/L)_{7,9}=3/3$, and $(W/L)_8=30/3$, evaluate the Voltage Gain (in dB) and Power Consumption.

[8]

c) How would any variation in the bias current impact the voltage gain? In practice why is it challenging to make stable, well-defined bias currents on-chip?

[6]

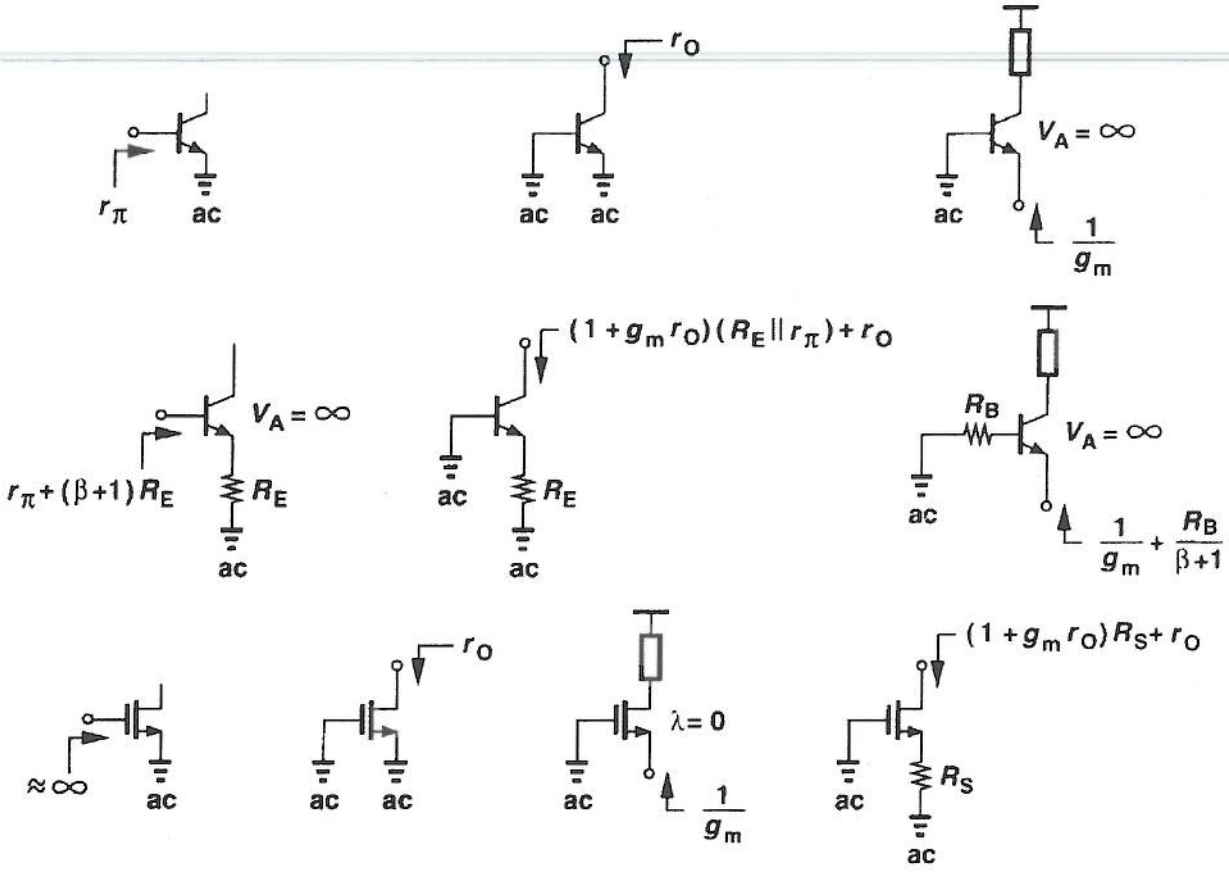
d) Determine expressions for the impedances seen 'looking into' nodes X, Y, Z and V_{out} (i.e. the equivalent impedances between each of these nodes and ground). Comment on these impedance expressions (i.e. are they low, moderate or high). How would this impact the amplifier's high frequency response?

[6]

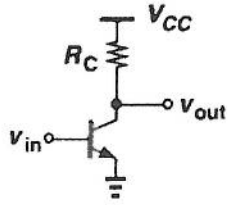
e) This OTA can be converted into a *voltage amplifier* simply by adding a 2nd stage to the output. Sketch a possible circuit for this (without using any resistors) and justify your choice. Describe how this would change the overall voltage gain and output impedance?

[5]

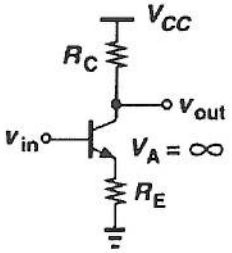
Input and Output Impedances



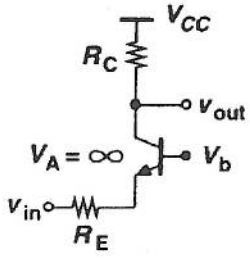
Voltage Gain Equations



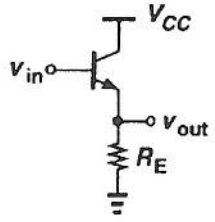
$$A_v = -g_m (R_C \| r_O)$$



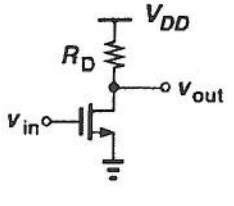
$$A_v = -\frac{R_C}{\frac{1}{g_m} + R_E}$$



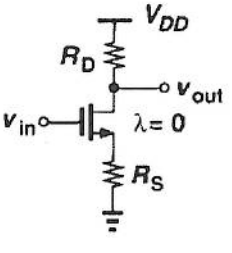
$$A_v = \frac{R_C}{\frac{1}{g_m} + R_E}$$



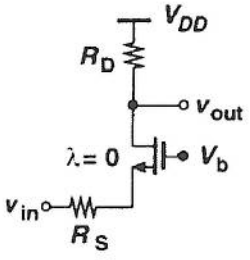
$$A_v = \frac{R_E \| r_O}{\frac{1}{g_m} + R_E \| r_O}$$



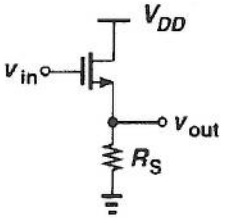
$$A_v = -g_m (R_D \| r_O)$$



$$A_v = -\frac{R_D}{\frac{1}{g_m} + R_S}$$



$$A_v = \frac{R_D}{\frac{1}{g_m} + R_S}$$



$$A_v = \frac{R_S \| r_O}{\frac{1}{g_m} + R_S \| r_O}$$

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2012

EEE PART II: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 2 (SOLUTIONS)

Wednesday, 30 May 2:00 pm

Time allowed: 1 hour 30 minutes

There are THREE questions on this paper.

ALL questions are compulsory.
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Any special instructions for invigilators and information for candidates are on page 1.

Basic expressions for voltage gain, input and output resistance for single stage amplifiers are given on the last page.

Examiners responsible
First Marker(s): T.G. Constandinou
Second Marker(s): K. Harris

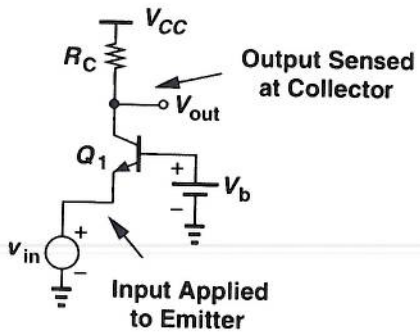
1. (a) An op-amp is a voltage amplifier with infinite voltage gain. The op-amp is also a difference amplifier with inverting and non-inverting inputs. A real op-amp has certain non-ideal characteristics compared to an ideal voltage amplifier- such as finite gain, finite output impedance (ideally zero) and non-infinite input impedance (although almost if MOSFET input). [5]

[Many students here missed out fact that an op-amp has differential inputs. Also comparing the ideal-characteristics of a voltage amplifier with the non-ideal characteristics of a real op-amp.]

1. (b) Loop gain = $KA_1 = g_{m3}R_D * A_1 * R_2/(R_1+R_2)$
Closed loop gain = $A_1 / (1+KA_1) = A_1 / [1 + g_{m3}R_D * A_1 * R_2/(R_1+R_2)]$ [5]

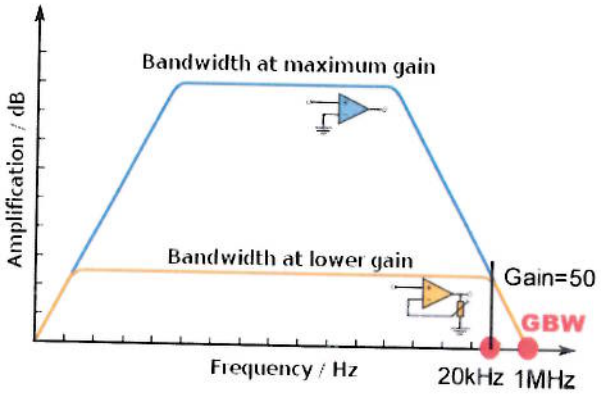
[Some answers did not include both the Loop and Closed loop gain – although clearly specified in the question.]

1. (c) A common base (CB) amplifier takes its input from the emitter terminal and passes its output though the collector terminal. The base terminal is at an ac ground (i.e. DC bias). It is best to describe a CB amplifier as a unity-gain current amplifier as its current gain very close to 1 – i.e. $A_v=\beta/\beta+1$. Voltage gain is similar to a CE amplifier but positive gain (i.e. $+g_m * (R_C \parallel r_o)$). It has low input impedance (approximately $1/g_m$) and moderate output impedance (r_o). [5]



[Several students drew a common gate instead of common base topology. Also, majority of students simply stated it is better described as a unity-gain current amplifier without properly justifying- see answer above.]

1. (d) For devices such as op-amps (generally designed to have a simple one-pole frequency response), the gain–bandwidth product indicates the frequency at which the gain falls to unity. For an amplifier in which negative feedback reduces the gain to below the open-loop gain, the gain–bandwidth product of the closed-loop amplifier will be approximately equal to that of the open-loop amplifier. This quantity is commonly specified for operational amplifiers, and allows circuit designers to determine the maximum gain that can be extracted from the device for a given frequency (or bandwidth) and vice versa. If the GBP of a 741 is 1 MHz, it means that the gain of the device falls to unity at 1 MHz. The same device when wired for a gain of 50 will work only up to 20kHz, in accordance with the GBW product formula. [5]



[Although it was not explicitly stated to use a diagram, many students did include this and it helped explain their answer. In general, the students that did not include a diagram failed to properly explain the GBW trade-off.]

1. (e) (i) Draw half-circuit assuming perfect symmetry (LHS and RHS) so common-source node is an ac ground. M_1 = CS amplifier, M_3 = diode connected load, M_5 = CS load.

$A_v = V_{out}/(V_{in1}-V_{in2}) = -g_{m1}(r_{o1} \parallel r_{o3} \parallel r_{o5} \parallel (1/g_{m3}))$

$A_v \approx -g_{m1}/g_{m3}$

Assuming $(1/g_{m3}) << r_{o1}, r_{o3}, r_{o5})$

[5]

[Several students did not state all assumptions.]

1. (e) (ii) From formula sheet use expression for a source follower.

$A_v = (r_{o1} \| R_E)/(r_{o1} \| R_E + 1/g_{m1})$, where $R_E = g_{m2}r_{o2}r_{o3} + r_{o2} + r_{o3} \approx r_{o1}/(r_{o1} + 1/g_{m1})$

Assuming $(r_{01} << R_E)$

[5]

[Several students did not state all assumptions.]

1. (f) (i) $R_{in} = r_{\pi 1} + (\beta+1)R_E$

$R_{out} = r_{down} \| r_{up} \approx r_{down} = r_{\pi 2} \parallel (1/g_{m2})$

(since $r_{up} = R_C$ + emitter degeneration r_{out} = infinite)

[5]

[For R_{in}, some students incorrectly stated the observed emitter resistance as $R_E/(\beta+1)$ instead of $(\beta+1)R_E$]

1. (f) (ii) $R_{in} = R_S + (R_1 \parallel (1/g_{m1}))$

$R_{out} = 1/g_{m2}$

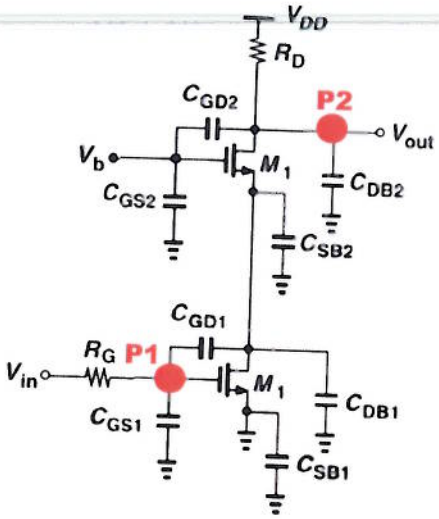
[5]

[Several students included r_0 in these expressions, although it was explicitly stated that r0 is excluded.]

2. (a) Common Source (CS) and Common Gate (CG) amplifiers have similar low frequency voltage gain ($g_m R_D$) except that CS is inverting and CG is non-inverting. However, CG amplifier has better high frequency response than the CS due to the parasitic capacitances. In case of the CS amplifier, the gate drain capacitance appears across the input/output terminal and is therefore subject to Miller multiplication (at the input). This significantly impacts the amplifier bandwidth by lowering the frequency of the input pole (since the input-referred capacitance is C_{GD} multiplied by the gain). In the case of the CG amplifier since the gate is at AC ground, there is no Miller effect. [4]

[Several students missed the "simple" explanation. The key here was to identify that in the case of a CS amplifier there is a floating (non-grounded) capacitor whereas for the CG amplifier this isn't the case. Then to infer that floating capacitors across an amplifying element are subjected to the Miller effect, which results in the floating capacitance being observed as a larger input (grounded) capacitance- scaled by the gain. This then limits the high frequency performance.]

2. (b)

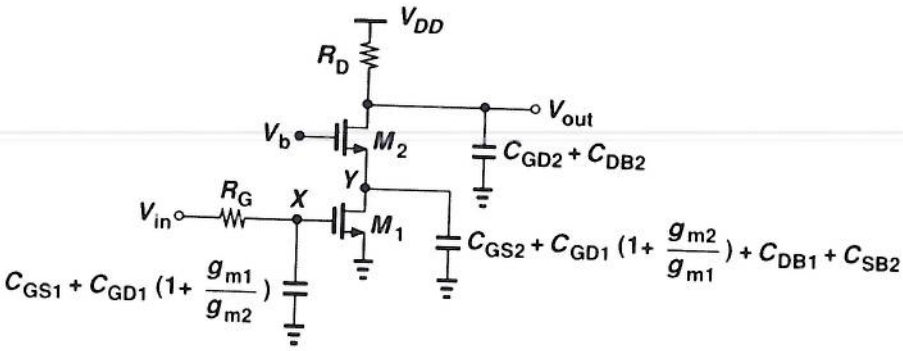


Note, node between CS and CG amplifiers may also be identified but must be discarded due to low impedance.

[10]

[Several students missed the fact that node between CS and CG amplifiers is a low impedance node and thus will not dominate high frequency performance.]

2. (c)



$F_{p1}=1/[2\pi*R_G*(C_{GS1}+C_{GD1}(1+A_{v1}))]$
$F_{p2}=1/[2\pi*R_D*(C_{DB2}+C_{GD2})]$

[8]

2. (d) $A_v=A_{v1}*A_{v2} = -(g_{m1}/g_{m2}) * (g_{m2}R_D) = -g_{m1}R_D$

[2]

2. (e) $g_{m1}=\sqrt{(2I_{D1}(W/L)_2*\mu_nC_{ox})} = \sqrt{(2*1m*25/0.18*200\mu)} = 7.5mS$
$g_{m2}=\sqrt{(2I_{D2}(W/L)_1*\mu_nC_{ox})} = \sqrt{(2*1m*50/0.18*200\mu)} = 10.5mS$

$A_v = -g_{m1}R_D = 7.5mS * 2000 = 15$

$C_{GS1} = (2/3) * (WL) * Cox = (2/3) * (25 * 0.18) * 12f = 36fF$
$C_{GD1} = C_0W_1 = 0.2fF/\mu m * 25\mu m = 5fF$
$C_{GD2} = C_0W_2 = 0.2fF/\mu m * 50\mu m = 10fF$

[Several students here incorrectly calculated C_{GS1}, C_{GD1} and C_{GD2}, even though the expression was given in the question].

$F_{p1}=1/[2\pi*R_G*(C_{GS1}+C_{GD1}(1+A_{v1}))] = 1/[2\pi*2K*(36f+5f(1+7.5/10.5))] = 1.785GHz$
$F_{p2}=1/[2\pi*R_D*(C_{DB2}+C_{GD2})] = 1/[2\pi*2K*(0+10f)] = 7.958GHz$

[6]

3. (a) Assuming perfect symmetry, eg. $g_{m1}=g_{m2}$, $Av=g_{m1}K(r_{o6}||r_{o8})$

[5]

[Most the students here failed to identify that M_3-M_4, M_5-M_6 and M_7-M_8 were active current mirrors and thus to use the current mirror ratio's to scale the current. Many students attempted to evaluate the impedances of nodes X and Y and determine corresponding voltage gain expressions, which were followed through to the output.]

3. (b) from W/L's => K=10 (i.e. $(W/L)_6 / (W/L)_5 = (W/L)_8 / (W/L)_7 = 10$

$g_{m1} = \sqrt{(2 * \mu_n C_{ox} * (W/L) * I_D)} = \sqrt{(2 * 200\mu * (50/0.5) * 5\mu)} = 0.45mS$
$r_{06} = 1/\lambda_p I_D = 100\mu(0.2) = 50k\Omega$
$r_{04} = 1/\lambda_n I_D = 100\mu (0.1) = 100k\Omega$

$A_v = 10(100k\Omega \parallel 200k\Omega) * 0.63mS = 300$
$A_v(dB) = 20\log_{10}(300) = 49.5dB$

Power consumption = $[I_{bias}(M_9) + 0.5 * I_{bias}(M_7) + K * I_{bias}(M_8)] * V_{DD}$
Power consumption = $6.5 * I_{bias} * V_{DD} = 6.5 * 10\mu A * 1.8 = 117\mu W$ [8]

3. (c) Any variation in the bias current would effect g_m by $\sqrt{\Delta I_D}$ and also the r_o of the devices (M_4 and M_6) – inversely proportional. Therefore $\Delta A_v = (\sqrt{\Delta I_D}) / \Delta I_D = 1 / \sqrt{(ID)}$. So a 10% increase in bias current would result in a $(1/\sqrt{(1.1)})$ => 4.65% decrease in voltage gain. In general it is challenging to make stable, repetitive, current sources on chip due to process variation, mismatch, power supply and temperature sensitivity- all which effect the intrinsic device characteristics. [6]

3. (d) $R_X = r_{o1} \parallel r_{03} \parallel (1/g_{m3}) \approx 1/g_{m3}$
$R_Y = r_{o2} \parallel r_{05} \parallel (1/g_{m5}) \approx 1/g_{m5}$
$R_Z = r_{o4} \parallel r_{o7} \parallel (1/g_{m7}) \approx 1/g_{m7}$
$R_{out} = r_{o6} \parallel r_{o8}$
[4]

Note that R_X, R_Y, R_Z are all low impedance nodes which means the poles associated with these nodes will be at very high frequencies. However Rout has relatively high impedance so the frequency response will be dominated by this pole associated with this node. If the amplifier becomes unstable it can be compensated by simply adding a capacitor to the output node (to ground). This is called load compensation. [2]

[Most students failed to identify that R_X, R_Y and R_Z are in fact (relatively) low impedance nodes due to the diode-connected devices.]

3. (e) Can add a PMOS common source amplifier (gate connected to current output) with an NMOS current sink load (taking input from V_B (as to M_9)). As the output is relatively high impedance we require an amplifier topology with very high input impedance (thus gate of a MOSFET is ideal). A CS amplifier can additionally provide voltage gain (compared to a source follower). The gain will be increased by $g_m(r_{outNMOS} \parallel r_{outPMOS})$. Note that the input terminals to the OTA will be reversed (i.e. +ve and –ve inputs). Source follower could also be used, however voltage gain will remain the same (wont be boosted any further). [5]

[Many students did not provide a complete answer here, although the answer is simple. Most answers included a sketch of a single CS device (with no load, i.e. drain floating)- however, this isn't a complete 2nd stage (as specified).]