E3.14
AO7

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2009

MSc and EEE PART III/IV: MEng, BEng.and ACGI

Corrected copy

POWER ELECTRONICS AND MACHINES

Tuesday, 12 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	T.C. Green, P.D. Mitcheson
	Second Marker(s) :	G. Strbac, G. Strbac

Information for candidates

Boltzmann's constant:	1.38×10^{-23} m^2 kg s^{-2} K^{-1}
Charge on the electron :	1.6×10^{-19} C

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1.

(a) Show that for an isolated flyback converter operating in discontinuous mode, the on-time required to store an energy, E in the magnetic core is:

$t_{on} = \frac{\sqrt{2EL_1}}{V_1}$ where L_1 is the primary inductance and V_1 is the input voltage,

and the diode conduction time required to discharge that energy is

$t_d = \frac{\sqrt{2EL_1}}{V_2} k_N$ where k_N is the secondary to primary turns ratio and V_2 is the output voltage.

[5]

(b) An isolated flyback converter is to be designed around a magnetic core that has the following ~~tow~~ two properties: Number of turns

- The inductance is given by $L = k_L N^2$ where $k_L = 7 \times 10^{-9}\,\text{H}$
- The peak stored energy before saturation is 250 μJ

The circuit is to step down 100 V to 10 V and provide an output power of 20 W. Determine the following:

(i) The maximum operating frequency to avoid saturation when operating at 20 W [2]

(ii) The number of turns on the primary to keep the on-time to less than 40% of the period at 20 W. [4]

(iii) The number of turns on the secondary to ensure discontinuous conduction with 10% of the period having no conduction. State whether the result should be rounded up or down to obtain the appropriate integer number of turns. [4]

(c) Explain the advantages and disadvantages of the double-switched flyback SMPS of figure Q1 over the single-switched version. [5]

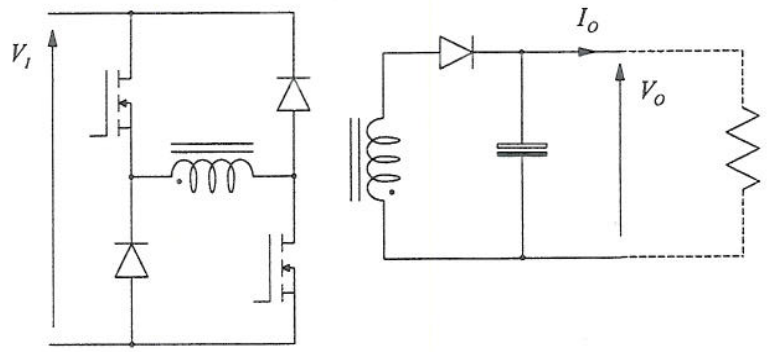

Figure Q1

2.

(a) Figure Q2 (overleaf) shows the circuit of a Ćuk switch-mode power supply (SMPS) and the current paths that exist when the MOSFET is on and when the MOSFET is off.

(i) Derive (stating any assumptions made) the ratio of output voltage to input voltage of this circuit when operating in continuous conduction mode. [4]

(ii) Describe any advantages or disadvantages the Ćuk circuit has over other SMPS. [3]

(b) Describe the steps needed to form a linear state-space model of a switch-mode power supply. [5]

(c) It is desired to form a state-space model of the Ćuk SMPS shown in figure Q2. The chosen state variable are i_{L1} , i_{L2} , v_{C1} and v_{C2}. The input voltage can be treated as constant. The series resistance of the capacitor and the voltage drops of the semi-conductors can be ignored.

(i) Find the four differential equations that apply to the state variables during the **on-time**. [3]

(ii) Find the four differential equations that apply to the state variables during the **off-time**. [2]

(iii) Use Equation Q2 to find the average model that applies to the circuit. [3]

$$\dot{\tilde{\mathbf{x}}} \cong \mathbf{A}\tilde{\mathbf{x}} + \mathbf{E}\tilde{\delta}$$

$$\text{where} \quad \mathbf{A} = \Delta\,\mathbf{A}_{\mathrm{On}} + (1-\Delta)\mathbf{A}_{\mathrm{Off}}$$

$$\mathbf{E} = (\mathbf{A}_{\mathrm{On}} - \mathbf{A}_{\mathrm{Off}})\mathbf{X} + (\mathbf{B}_{\mathrm{On}} - \mathbf{B}_{\mathrm{Off}})\mathbf{U} \qquad \text{Equation (Q2)}$$

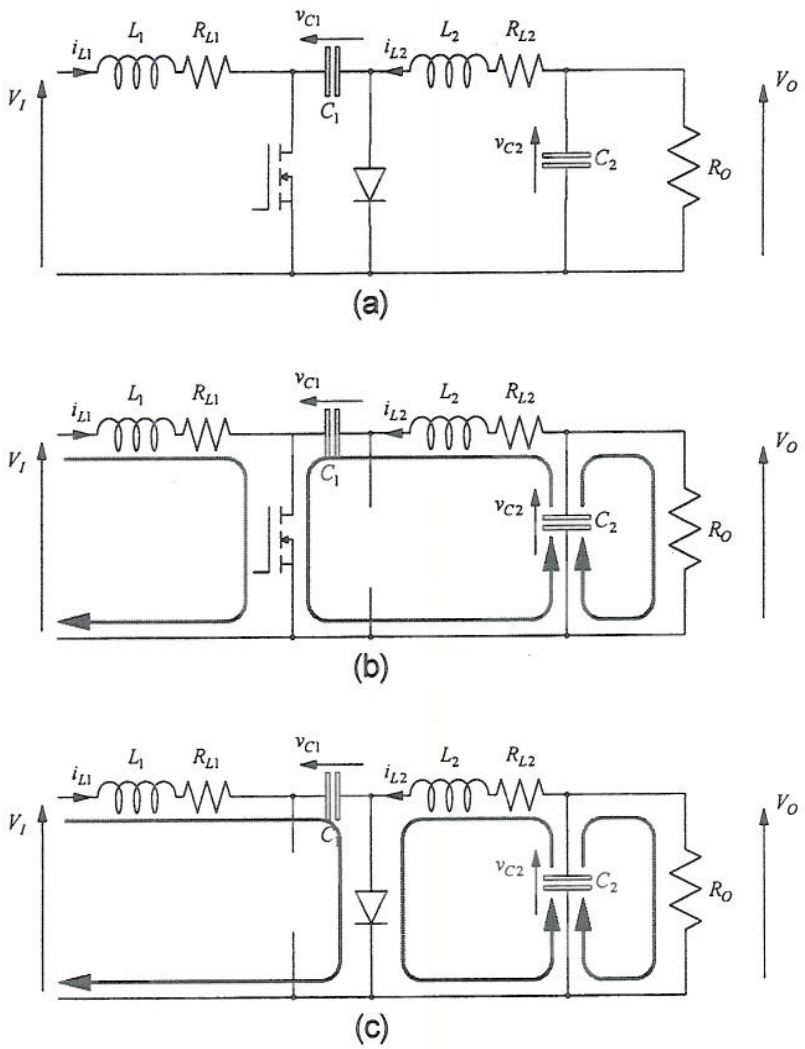

Figure Q2 (a) Ćuk switch-mode power supply; (b) conduction paths in on-state; (c) conduction paths in off-state

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3.

(a) Figure Q3 shows the waveform of AC side current of a rectifier and its relationship to the AC voltage.

(i) Calculate the RMS value of the current [4]

(ii) Calculate the fundamental component of the current [4]

(iii) Calculate the power factor of the current [2]

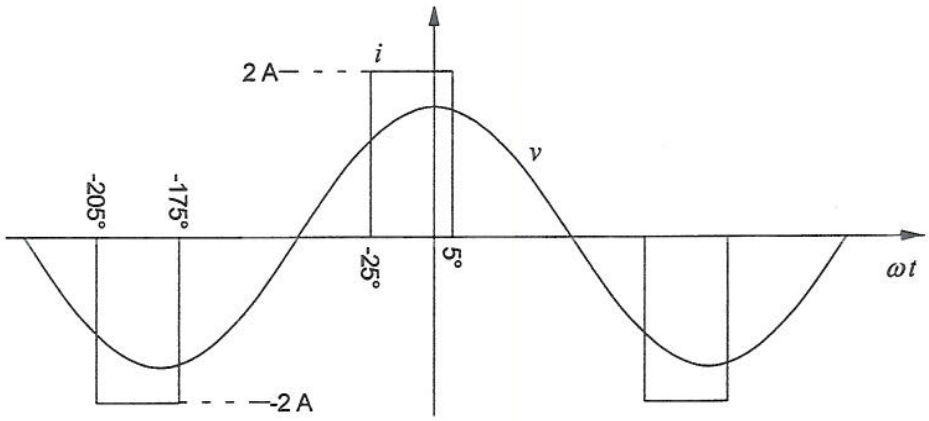


Figure Q3

(b) Describe why circuits that draw non-sinusoidal currents from the AC mains should not be used. [3]

(c) Describe a power converter circuit and its operation (including any modulator needed and control scheme) for use as a 3-phase AC to DC converter that maintains a sinusoidal AC current. [7]

4.

(a) The circuit of Figure Q4 below shows an IGBT switching an inductive load with a snubber circuit added.

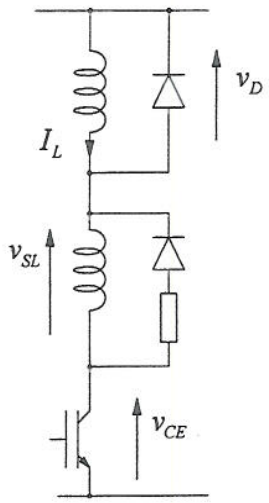


Figure Q4 – inductive load and snubber

(i) Explain the purpose of the snubber and draw the waveforms of IGBT current, V_{CE}, V_D and V_{SL} at turn on assuming that V_{CE} has fallen to zero before the collector current reaches I_L. [4]

(ii) The circuit has an average main inductor current of 10 A and the power supply rail is 500 V. The fall time of V_{CE} is 100 ns and the snubber inductor is 25 μH. Calculate the turn on loss in the IGBT. [4]

(b)

(i) Explain why power MOSFETS are built using a cell-based double-diffused vertical structure instead of the single diffused lateral structure normally used for signal devices. [5]

(ii) Explain why MOSFETS are the favoured switching device for low voltage applications and IGBTs become favourable at higher voltages. [3]

(c) A power device manufacturer is designing a new range of power MOSFETS and IGBTs using their latest fabrication processes. Table Q4 shows some of the expected properties of the devices in terms of the rated current and blocking voltage.

MOSFET:	**IGBT:**
$R_{DSon} = 9 \times \sqrt{V_{block}} / I_{rated}$	$R_{drift} = 8.92\sqrt{V_{block}} / I_{rated}$
	$J_s = 2 \times 10^{-12}$ A/cm^2

Table Q4 Parameters for new devices

where R_{DSon} is the drain source resistance of the MOSFET, R_{drift} is the resistance of the *n*- region of the IGBT, V_{block} is the rated blocking voltage of the devices, I_{rated} is the maximum rated current of the devices and J_s is the reverse saturation current density of the *pn* junction at the collector if the IGBT. The *pn* junction at the collector of the IGBT is assumed to obey the Shockley equation. R_{drift} can be assumed to contribute the only ohmic resistance between the IGBT's collector and emitter.

The manufacturer expects to achieve a current density in the MOSFET of 50 A/cm^2 and a current density of 100 A/cm^2 in the IGBT.

If the devices are operating at their rated currents at junction temperatures of 80^{0}C, estimate the rated blocking voltage at which the IGBT achieves lower conduction loss than the MOSFET. State which equivalent circuit model you are using for the IGBT.

[4]

5. You are required to design a low-loss power converter with the following characteristics:

Input voltage: 20 – 25 V
Output Voltage: 12 V
Output Power: 100 W
Input to Output Isolation: Not required

The following components are to be used in the design:

- 100 μH inductor, ESR = 50 mΩ
- IRF IRL2703 MOSFET, R_{DSon}=40 mΩ and when switching, the voltage rise and fall times are 80 ns and the current rise and fall times are 40ns
- Diode, whose voltage drop can be approximated as 0.7 V when conducting and has negligible reverse recovery charge
- Capacitor, negligible series resistance and inductance

(a) In the first instance, a simple buck power converter topology is chosen.

(i) Calculate limits on the duty cycle based on the operating conditions of the converter. You may assume no losses in the converter for this calculation. [1]

(ii) Calculate the maximum conduction losses in the circuit at rated output current. You may assume that the effect of ripple current on the losses is negligible. [3]

(iii) Calculate a suitable switching frequency for the converter assuming a maximum inductor current ripple of 5% is allowed at rated output current. Give your answer to 3 significant figures. [3]

(iv) Calculate the MOSFET switching losses and the worst case efficiency of the converter. [4]

(b) It is then proposed that in order to reduce losses, the converter is converted to a soft-switched design, as shown in Figure Q5 (overleaf).

(i) Explain how this converter topology is able to reduce the losses below that in the buck circuit in part (a). [3]

(ii) Using the same MOSFET switching frequency and input voltage range as in the hard switched converter, calculate the limits on the resonant frequency of this circuit. [2]

(iii) Choose a suitable value of resonant inductor to ensure that the MOSFET can be turned off under a low loss condition. [2]

(iv) Explain 2 potential disadvantages of using this circuit over the hard-switched case. [2]

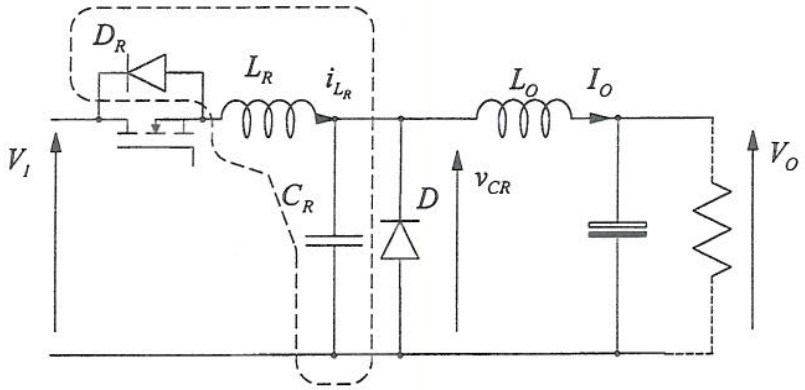


Figure Q5

6.

(a) Figure Q6 (overleaf) shows a slip-compensated speed control scheme for an induction machine. Describe the operation of the system including the role of the slip speed signal, the role of the slip limiter and the way in which the frequency and voltage commands for the inverter are determined. [5]

(b) The nameplate of a 2-pole-pair induction machine gives the following basic information for its operation on a fixed frequency supply. This information is taken to represent its maximum or rated operation for the conditions given.

Phase Voltage 230 V
Frequency 50 Hz
Rated Speed 1,450 rpm
Rated Power 5.0 kW

Determine the following for when the machine is used at variable frequency in a slip-compensated drive system using reasonable approximations where necessary.

(i) The maximum torque available. [2]

(ii) The maximum air-gap flux linkage. [2]

(iii) The slip-speed limit (in rad/s) that should be imposed to obtain maximum torque. [2]

(iv) The frequency of stator voltage needed to achieve rotation at 2,500 rpm. [2]

(v) The DC-link voltage needed for maximum torque at 2,500 rpm. [2]

(c) The drive system in Figure Q6 will regenerate on occasion. Describe what arrangements should be made in the DC-link circuit to facilitate this. [5]

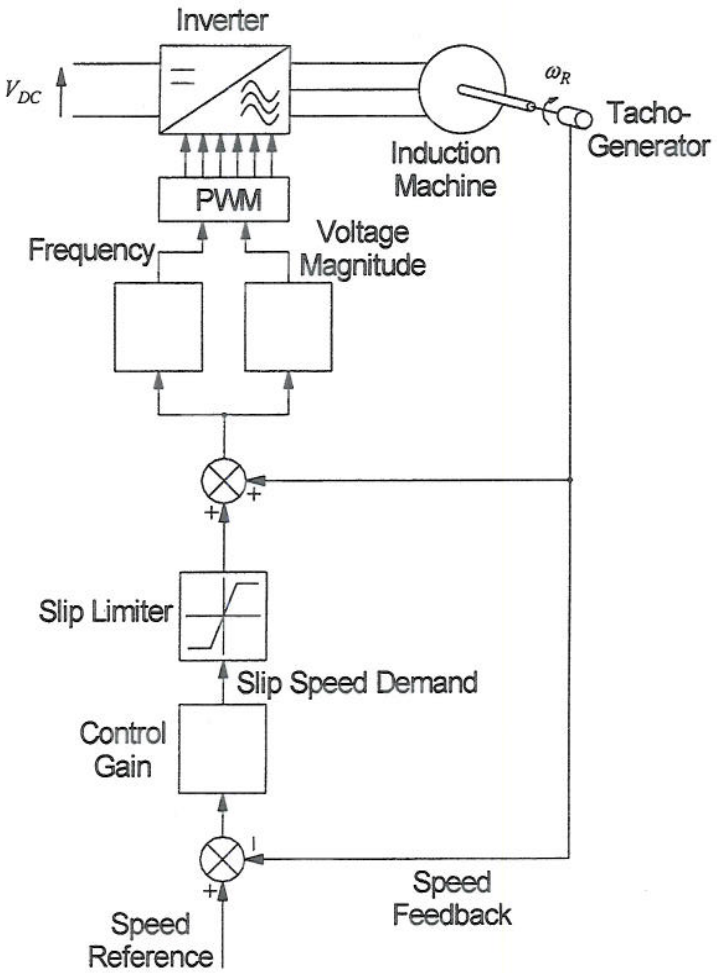

Inverter
V_{DC}
ω_R
Tacho-
Generator
Induction
Machine
PWM
Frequency
Voltage
Magnitude
+
+
Slip Limiter
Slip Speed Demand
Control
Gain
+
Speed
Feedback
Speed
Reference

Figure Q6

Master

[3.14]

A07

Answers Power Electronics + Machines 2009

1.

(a) Show that for an isolated flyback converter operating in discontinuous mode, the on-time required to store an energy, E in the magnetic core is:

$t_{on} = \frac{\sqrt{2EL_1}}{V_1}$ where L_1 is the primary inductance and V_1 is the input voltage,

and the diode conduction time required to discharge that energy is

where k_N is the secondary to primary turns ratio and V_2 is the output voltage.

[5]

Consider the rise of current during the on time and then the stored energy in an inductor

$$\frac{di}{dt} = \frac{V_1}{L_1}$$

$$\hat{i} = \frac{V_1}{L_1} t_{on}$$

$$E = \tfrac{1}{2} L_1 \hat{i}^2 = \tfrac{1}{2} \frac{V_1^2}{L_1} t_{on}^2$$

$$t_{on} = \frac{\sqrt{2EL_1}}{V_1}$$

The analysis can apply to the decay of current in the secondary side and the required result is obtained by noting that inductance is proportional to square of number of turns.

$$\frac{di_2}{dt} = \frac{V_2}{L_2}$$

$$\hat{i}_2 = \frac{V_2}{L_2} t_d$$

$$E = \tfrac{1}{2} L_2 \hat{i}_2^{\,2} = \tfrac{1}{2} \frac{V_2^2}{L_2} t_d^2$$

$$t_d = \frac{\sqrt{2EL_2}}{V_2}$$

$$\frac{L_1}{L_2} = \frac{N_1^2}{N_2^2} = \frac{1}{k_N^2}$$

$$t_d = \frac{\sqrt{2EL_1}}{V_2} k_N$$

(b) An isolated flyback converter is to be designed around a magnetic core that has the following tow properties:

- The inductance is given by $L = k_L N^2$ where $k_L = 7 \times 10^{-9}$
- The peak stored energy before saturation is 250 μJ

[3.14]

The circuit is to step down 100 V to 10 V and provide an output power of 20 W. Determine the following:

(i) The maximum operating frequency to avoid saturation when operating at 20 W [2]

Power is energy transfer per second which here is the maximum stored energy in the core times the frequency.

$$f = \frac{P}{E^{Max}} = \frac{20}{250 \times 10^{-6}} = 80\ kHz$$

(ii) The number of turns on the primary to keep the on-time to less than 40% of the period at 20 W. [4]

The on-time is

$$t_{on} = \frac{0.4}{f} = \frac{0.4}{80 \times 10^3} = 5\ \mu s$$

Now find inductance.

$$E = \tfrac{1}{2}\frac{V_1^2}{L_1} t_{on}^2$$

$$L_1 = \tfrac{1}{2}\frac{V_1^2}{E^{Max}} t_{on}^2$$

$$= \frac{100^2 \times \left(5 \times 10^{-6}\right)^2}{2 \times 250 \times 10^{-6}}$$

$$= 0.5\ mH$$

And so the number of turns is

$$N_1^2 = \frac{L_1}{k_L} = \frac{0.5 \times 10^{-3}}{7 \times 10^{-9}}$$

$$N_1 = 267.3$$

Take next largest integer (to ensure smaller not larger flux) which *is 287 truns*

(iii) The number of turns on the secondary to ensure discontinuous conduction with 10% of the period having no conduction. State whether the result should be rounded up or down to obtain the appropriate integer number of turns. [4]

The diode conduction time must be less than (1 - 0.4 - 0.1) of the period

$$t_d = \frac{1 - 0.4 - 0.1}{f} = \frac{0.5}{80 \times 10^3} = 6.25 \mu s$$

Now find secondary inductance

[3.14]

$$L_2 = \frac{1}{2}\frac{V_2^2}{E^{Max}} t_d^2$$

$$k_N^2 = \frac{L_2}{L_1} = \left(\frac{V_2}{V_1}\frac{t_d}{t_{on}}\right)^2$$

$$k_N = \left(\frac{0.5}{10 \times 0.4}\right) = 0.125$$

$$N_2 = k_N N_1 = 0.125 \times 267 = 33.375$$

Rounding down to 33 turns gives a smaller inductance, shorter diode conduction time and therefore maintains discontinuous conduction.

(c) Explain the advantages and disadvantages of the double-switched flyback SMPS of figure Q1 over the single-switched version. [5]

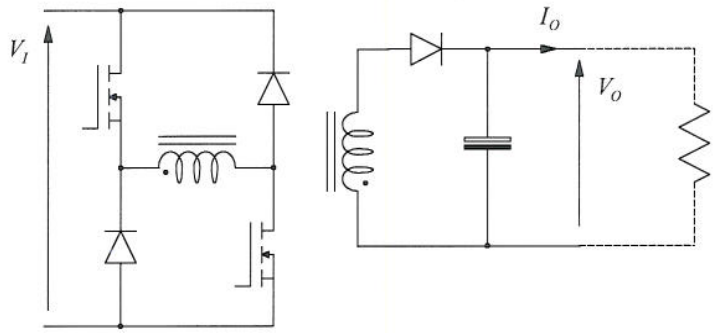
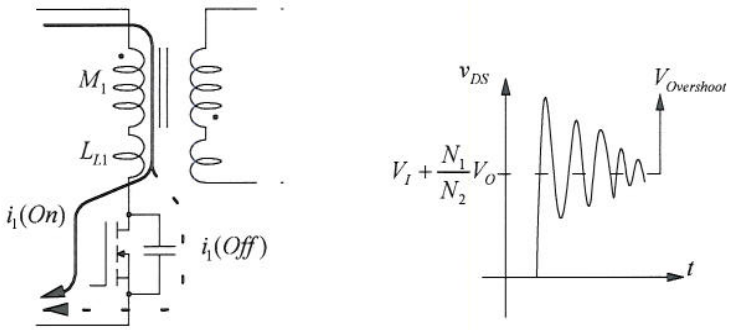


Figure Q1

Main points are:

- *Single-switched circuit has no explicit path for discharging the primary leakage inductance and so the drain-source capacitance is over charged beyond the expected* $V_I + V_O N_1/N_2$ *to value set by the trapped energy. A lightly damp oscillation ensues.*



[3.14]

- *In the double switched circuit, the diodes of the "asymmetric half bridge" form a path to discharge the primary leakage energy back to the supply. The diodes clamp the transistor voltages to a maximum of the input voltage.*
- *So, the trade off is between two transistors with well defined maximum voltage versus a single transistor with a substantially higher maximum voltage which is subject to variation in leakage energy and drain-source capacitance* .

[3.14]

2.

(a) Figure Q2 shows the circuit of a Ćuk switch-mode power supply (SMPS) and the current paths that exist when the Mosfet is on and when the Mosfet is off.

(i) Derive (stating any assumptions made) the ratio of output voltage to input voltage of this circuit when operating in continuous conduction mode. [4]

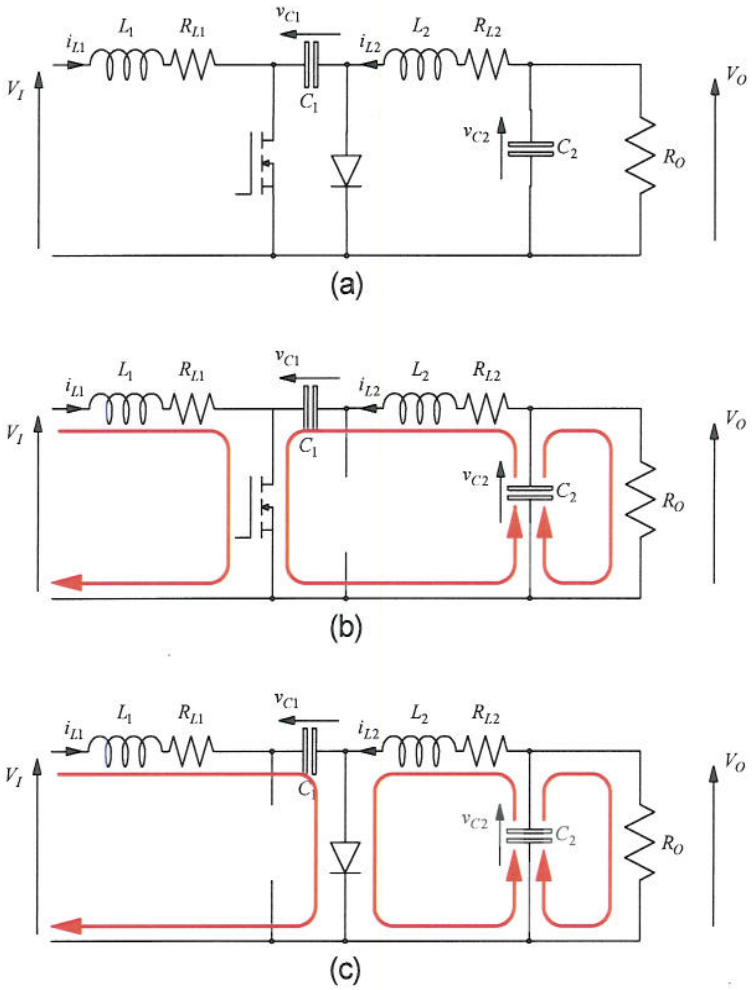


Figure Q2 (a) Ćuk switch-mode power supply; (b) conduction paths in on-state; (c) conduction paths in off-state

[Book work]

- *We assume that the capacitors are large enough for us to be able to neglect the small change in their voltage that occurs within a switching cycle.*
- *We will also assume that the voltage drops across semiconductors and parasitic resistances are negligible.*
- *The derivation relies on the fact that in steady-state the net change in inductor current over a switching cycle is zero.*

Inductor L_1

$$0 = \Delta i_{L_1}^{On} + \Delta i_{L_1}^{Off}$$

$$0 = \frac{V_1}{L_1} \cdot \delta T + \frac{V_I - V_{C1}}{L_1}(1-\delta)T$$

$$\frac{V_{C_1}}{V_I} = \frac{1}{1-\delta}$$

Inductor L_2

$$0 = \Delta i_{L_2}^{On} + \Delta i_{L_2}^{Off}$$

$$0 = \frac{V_{C_1} + V_O}{L_2} \cdot \delta T + \frac{V_O}{L_2}(1-\delta)T$$

$$\frac{V_O}{V_{C_1}} = -\delta$$

Voltage Ratio

- We now have voltage transfer ratios for the input to C_1 and from C_1 to the output. Their combination gives the overall result required.

$$\frac{V_O}{V_I} = \frac{V_O}{V_{C_1}} \cdot \frac{V_{C_1}}{V_I}$$

$$= -\frac{\delta}{1-\delta}$$

(ii) Describe any advantages or disadvantages the Ćuk circuit has over other SMPS. [3]

[Book work and interpretation]

- *With continuous current in both input and output inductors, the ripple currents are small and the up-stream and down-stream conducted emissions are small. From an EMC point of view this is a good circuit. In contrast, other circuits have an input current switched/chopped (buck SMPS), and output current switched/chopped (boost) or both.*
- *The Cuk SMPS offers voltage inversion and both step-up and step-down operation. This the same characteristic as the buck-boost.*
- *The better EMC properties are bought at a price of an extra inductor and an extra capacitor.*

(b) Describe the steps needed to form a linear state-space model of a switch-mode power supply. [5]

[Summary of material in notes - answer may be supplemented by equations]

- *Switch-mode circuits are piece-wise linear*
- *State-space models of each state can be formed using the same state vector for each*
- *If the switching between states is at a high frequency compared with the rates of change of the state variable, then the change of state vector over a switching cycle can be approximated by rates of change due to the two states weighted by the duty-cycle for the on-state and complement of the duty-cycle for the off-state.*

[3.14]

- *The resulting model contains products of the duty-cycle and the state vector and/or state matrices*
- *The model is then linearised for perturbations around an operating point.*
- *Transfer functions can be found from the state-space model in the normal way*

(c) It is desired to form a state-space model of the Ćuk SMPS shown in figure Q2. The chosen state variable are i_{L1} , i_{L2} , v_{C1} and v_{C2}. The input voltage can be treated as constant. The series resistance of the capacitor and the voltage drops of the semi-conductors can be ignored.

(i) Find the four differential equations that apply to the state variables during the **on-time**. [3]

$$v_I = i_{L1}R_{L1} + L_1\frac{di_{L1}}{dt}$$

$$v_{C2} + v_{C1} = i_{L2}R_{L2} + L_2\frac{di_{L2}}{dt}$$

$$\frac{dv_{C_1}}{dt} = \frac{-i_{L2}}{C_1}$$

$$\frac{dv_{C_2}}{dt} = \frac{-(i_{L2} + i_O)}{C_2}$$

$$i_O = \frac{v_{C2}}{R_O}$$

(ii) Find the four differential equations that apply to the state variables during the **off-time**. [2]

$$v_I - v_{C1} = i_{L1}R_{L1} + L_1\frac{di_{L1}}{dt}$$

$$v_{C2} = i_{L2}R_{L2} + L_2\frac{di_{L2}}{dt}$$

$$\frac{dv_{C_1}}{dt} = \frac{i_{L1}}{C_1}$$

$$\frac{dv_{C_2}}{dt} = \frac{-(i_{L2} + i_O)}{C_2}$$

$$i_O = \frac{v_{C2}}{R_O}$$

(iii) Use Equation Q2 to find the average model that applies to the circuit. [3]

$$\dot{\tilde{\mathbf{x}}} \cong \mathbf{A}\tilde{\mathbf{x}} + \mathbf{E}\tilde{\delta}$$

$$\text{where} \quad \mathbf{A} = \Delta\,\mathbf{A}_{\mathbf{On}} + (1-\Delta)\mathbf{A}_{\mathbf{Off}} \qquad \text{Equation (Q2)}$$

$$\mathbf{E} = (\mathbf{A}_{\mathbf{On}} - \mathbf{A}_{\mathbf{Off}})\mathbf{X} + (\mathbf{B}_{\mathbf{On}} - \mathbf{B}_{\mathbf{Off}})\mathbf{U}$$

[3.14]

$$\mathbf{x} = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix}$$

$$\mathbf{A_{On}} = \begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{R_{L2}}{L_2} & \frac{1}{L_2} & \frac{1}{L_2} \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & -\frac{1}{C_2} & 0 & -\frac{1}{R_O C_2} \end{bmatrix} \quad \mathbf{B_{On}} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\mathbf{A_{Off}} = \begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ 0 & -\frac{R_{L2}}{L_2} & 0 & \frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_2} & 0 & -\frac{1}{R_O C_2} \end{bmatrix} \quad \mathbf{B_{Off}} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\mathbf{A} = \Delta \begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{R_{L2}}{L_2} & \frac{1}{L_2} & \frac{1}{L_2} \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & -\frac{1}{C_2} & 0 & -\frac{1}{R_O C_2} \end{bmatrix} + (1-\Delta) \begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ 0 & -\frac{R_{L2}}{L_2} & 0 & \frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_2} & 0 & -\frac{1}{R_O C_2} \end{bmatrix}$$

$$= \begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & -\frac{(1-\Delta)}{L_1} & 0 \\ 0 & -\frac{R_{L2}}{L_2} & \frac{\Delta}{L_2} & \frac{1}{L_2} \\ \frac{(1-\Delta)}{C_1} & -\frac{\Delta}{C_1} & 0 & 0 \\ 0 & -\frac{1}{C_2} & 0 & -\frac{1}{R_O C_2} \end{bmatrix}$$

[3.14]

$$\mathbf{E}=\left(\begin{bmatrix} -\frac{R_1}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{R_2}{L_2} & \frac{1}{L_2} & \frac{1}{L_2} \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & -\frac{1}{C_2} & 0 & -\frac{1}{R_O C_2} \end{bmatrix} - \begin{bmatrix} -\frac{R_1}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ 0 & -\frac{R_2}{L_2} & 0 & \frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_2} & 0 & -\frac{1}{R_O C_2} \end{bmatrix}\right)\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \left(\begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}\right)[V_I]$$

$$=\begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ -\frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \end{bmatrix}$$

$$=\begin{bmatrix} \frac{V_{C1}}{L_1} \\ \frac{V_{C1}}{L_2} \\ -\frac{I_{L1}+I_{L2}}{C_1} \\ 0 \end{bmatrix}$$

3.

(a) Figure 6 shows the waveform of AC side current of a rectifier and its relationship to the AC voltage.

(i) Calculate the RMS value of the current [4]

(ii) Calculate the fundamental component of the current [4]

(iii) Calculate the power factor of the current [2]

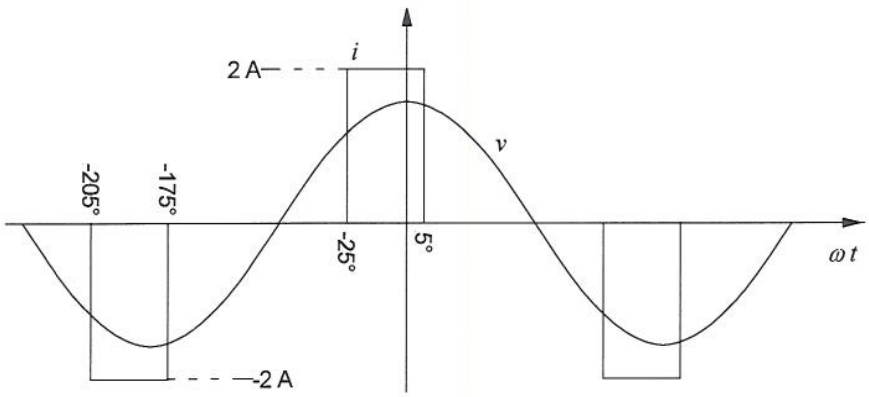


Figure Q3

[Calculation following established method]
RMS Current

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_{-\pi}^{\pi} i^2(\omega t).d\omega t} = \sqrt{\frac{I^2}{\pi}[\omega t]_{-25°}^{5°}}$$

$$= 2\sqrt{\frac{5-{}^{-}25}{180}} = 0.816$$

Fundamental Current

$$I_{A1} = \frac{1}{\pi}\int_{-\pi}^{\pi} i(\omega t)\cos(\omega t).d\omega t = \frac{2}{\pi}\int_{-55°}^{5°} I\cos(\omega t).d\omega t$$

$$= \frac{2}{\pi} I[\sin(\omega t)]_{-25}^{5} = \frac{2\times 2}{\pi}[\sin(5°) - \sin(-25°)] = 0.649\,A$$

$$I_{B1} = \frac{1}{\pi}\int_{-\pi}^{\pi} i(\omega t)\sin(\omega t).d\omega t = \frac{2}{\pi}\int_{-25°}^{5°} I\sin(\omega t).d\omega t$$

$$= \frac{2}{\pi} I[-\cos(\omega t)]_{-10}^{30} = \frac{2\times 2}{\pi}[-\cos(5°) + \cos(-25°)] = -0.114\,A$$

$$I_1 = 0.659\angle -9.9°$$

$$I_{1RMS} = \frac{0.659}{\sqrt{2}} = 0.466 \quad A$$

Displacement factor is $\cos(-9.9°) = 0.985$

[3.14]

Distortion factor is $\frac{I_1}{I_{RMS}} = \frac{0.466}{0.816} = 0.571$

Power factor is 0.565

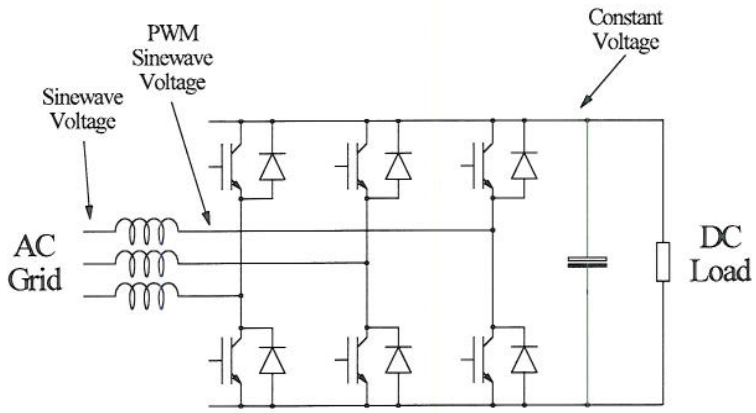
(b) Describe why circuits that draw non-sinusoidal currents from the AC main should not be used. [3]

[Bookwork]
The harmonic components of current do not transfer real power but do contribute to losses in the supply lines and transformers of the distribution system leading to inefficient operation. Utility operators may penalise low power factor (and therefore low distortion factor).

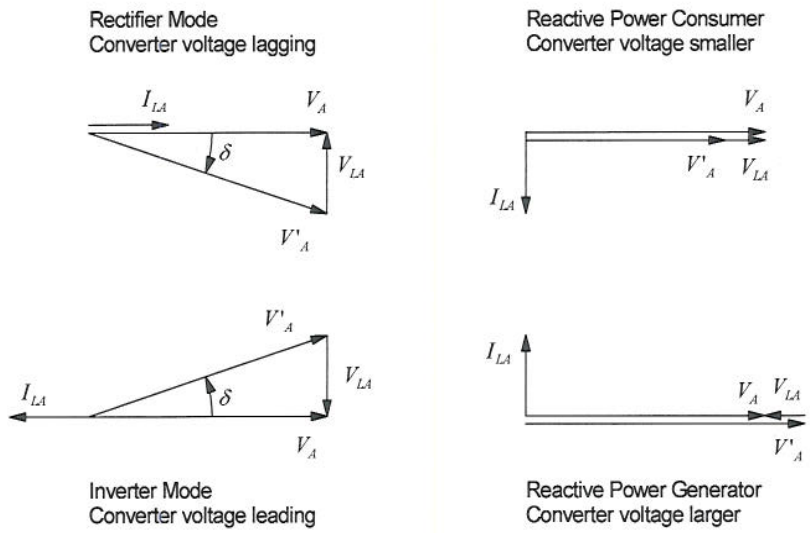
The harmonic current flows cause harmonic voltage drops in the distribution system and cause other consumers to be supplied with a distorted voltage waveform. This may cause mal-operation of equipment. EMC regulations, such as EN 61000, prohibit equipment from drawing harmonic current.

(c) Describe a power converter circuit and its operation (including any modulator needed and control scheme) for use as a 3-phase AC to DC converter that maintains a sinusoidal AC current. [7]

[Bookwork]
Circuit is that of an voltage source inverter connected to the grid voltage via coupling inductors. Once the inverter is pre-charged, it can synthesise (using PWM) a set of sinusoidal voltages of similar magnitude and angle to the grid voltages. A small voltage difference is set up across the coupling inductors and this determines the current flow. Provided that the voltages are sinusoidal then the currents will be sinusoidal also.



The following demonstrates that angle differences leads to in-phase current and real power exchange; magnitude differences leads to quadrature current and reactive power exchange.

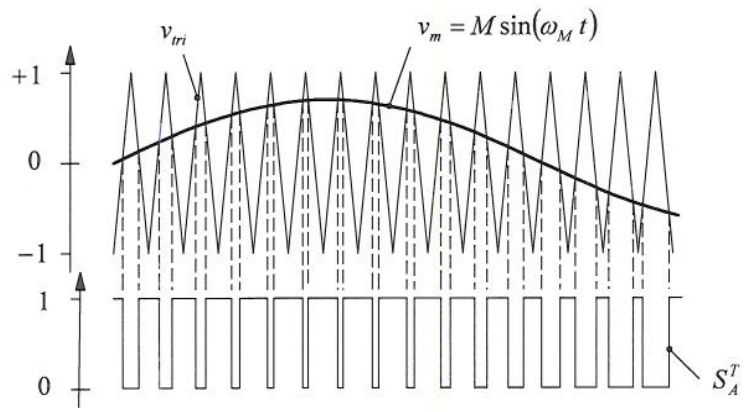


A sinusoidal reference signal of unit magnitude is established for each phase voltage. The signals are compared with a common triangle wave carrier to generate the commutation signals.

$$v_m = M\sin(\omega_M t) \quad \text{where } 0 \le M \le 1$$

$$\delta = \tfrac{1}{2} + \tfrac{1}{2}m \qquad \text{(Eqn 2.1)}$$

where M *is known as the depth of modulation and sets the magnitude of the* AC *voltage being synthesised and* v_m *is the instantaneous modulating signal.*



The resulting phase voltages are

$$v_A = \tfrac{1}{2}V_{DC} + \tfrac{1}{2}V_{DC}M\sin(\omega t) + \text{carier and sideband terms}$$

$$v_B = \tfrac{1}{2}V_{DC} + \tfrac{1}{2}V_{DC}M\sin\left(\omega t - \tfrac{2\pi}{3}\right) + \text{carier and sideband terms}$$

$$v_C = \tfrac{1}{2}V_{DC} + \tfrac{1}{2}V_{DC}M\sin\left(\omega t + \tfrac{2\pi}{3}\right) + \text{carier and sideband terms}$$

The DC terms are common mode and can be ignored.

The reference signals are often generated by a look up table. The frequency with which the look-up table is scanned dictates the AC supply frequency. The amplitude can be attenuated by multiplying the samples by a scaling factor.

[3.14]

4.

(a) The circuit of Figure Q4 below shows an IGBT switching an inductive load with a snubber circuit added.

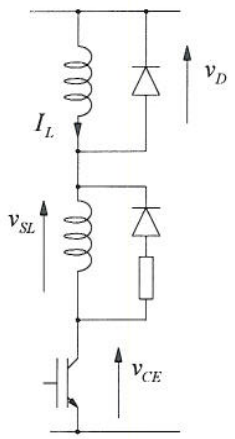


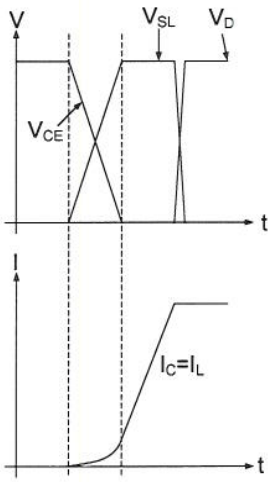
Figure Q4 – inductive load and snubber

(i) Explain the purpose of the snubber and draw the waveforms of IGBT current, V_{CE}, V_D and V_{SL} at turn on assuming that V_{CE} has fallen to zero before the collector current reaches I_L.

[4]

[bookwork]
This is a turn on snubber. The purpose of this snubber is to reduce the turn-on losses of the transistor by allowing V_{CE} to fall before the collector current has time to rise substantially, thus reducing the overlap between V_{CE} and I_C, thus reducing the switching loss at turn on.

The waveforms are as follows:



(ii) The circuit has an average main inductor current of 10 A and the power supply rail is 500 V. The fall time of V_{CE} is 100 ns and the snubber inductor is 25 μH.

Calculate the turn on loss in the IGBT.

[4]

[3.14]

[calculation]
The turn off loss in the IGBT is given by:

$$E = \int_0^{100n} I_c(t) \times V_{CE}(t)dt$$

Where VCE is given by:

$$V_{CE} = 500 - 5 \times 10^9 t$$

The snubber current (and thus collector current) is given by:

$$I = \frac{1}{L}\int_0^{t1} V_s dt \quad \text{where } V_s = 5 \times 10^9 t$$

$$I = 1 \times 10^{14} t^2$$

Thus, the power loss is:

$$E = \int_0^{100n} 1 \times 10^{14} t^2 \times (500 - 5 \times 10^9 t)dt$$

$$E = 1 \times 10^{14} \int_0^{100n} 500t^2 - 5 \times 10^9 t^3)dt$$

$$E = 1 \times 10^{14} \left[\frac{500}{3} t^3 - \frac{5 \times 10^9}{4} t^4 \right]_0^{100n}$$

Which gives an energy loss per switch off of 4.1μJ. [4]

(b)

(i) Explain why power MOSFETS are built using a cell-based double-diffused vertical structure instead of the single diffused lateral structure normally used for signal devices.

[5]

[Largely bookwork although it requires some thought to construct the argument]
Cells are used so that there is sufficient channel area to conduct high current (i.e. good use is made of the surface of the wafer. [1]

A power MOSFET could be (and sometimes is) made laterally, but to achieve high blocking voltages, this type of structure would utilise a lot of silicon area in order to achieve the required length. Building the device with the drain on the back side of the wafer allows the volume (not just the area) of the wafer to be utilised. [2]

A double diffusion is required to create a vertical MOSFET structure due to the fabrication steps that are used. (it is necessary to put a p region (which is inverted to form the channel) and an n region (the source) in series with the n- bulk of the wafer and thus 2 diffusions are required. [2]

[3.14]

(ii) Explain why MOSFETS are the favoured switching device for low voltage applications and IGBTs become favourable at higher voltages.

[3]

[Bookwork]
A High Blocking Voltage Requires a long lightly doped drift region to support the formation of a long depletion layer. This adds significant series resistance between source and drain of a MOSFET and the situation worsens as the voltage increases. In the IGBT, this n- region is conductivity modulated and so when current is flowing between the IGBT collector and emitter, the effective resistance of the drift region is reduced. [2]

The MOSFET is still preferred at lower voltages because it switches faster than an IGBT (for a given rated current) because minority carriers do not have to be removed at turn off or built up at turn on. [1]

(c) A power device manufacturer is designing a new range of power MOSFETS and IGBTs using their latest fabrication processes. Table Q4 shows some of the expected properties of the devices in terms of the rated current and blocking voltage.

MOSFET:	**IGBT:**
$R_{DSon} = 9 \times \sqrt{V_{block}} / I_{rated}$	$R_{drift} = 8.92\sqrt{V_{block}} / I_{rated}$
	$J_s = 2 \times 10^{-12}$ A/cm^2

Table Q4 Parameters for new devices

where R_{DSon} is the drain source resistance of the MOSFET, R_{drift} is the resistance of the *n-* region of the IGBT, V_{block} is the rated blocking voltage of the devices, I_{rated} is the maximum rated current of the devices and J_s is the reverse saturation current density of the *pn* junction at the collector if the IGBT. The *pn* junction at the collector of the IGBT is assumed to obey the Shockley equation. R_{drift} can be assumed to contribute the only ohmic resistance between the IGBT's collector and emitter.

The manufacturer expects to achieve a current density in the MOSFET of 50 A/cm^2 and a current density of 100 A/cm^2 in the IGBT.

If the devices are operating at their rated currents at junction temperatures of 80^{0}C, estimate the rated blocking voltage at which the IGBT achieves lower conduction loss than the MOSFET. State which equivalent circuit model you are using for the IGBT.

[4]

[calculations]

Use the diode/MOSFET series model of the IGBT – valid enough for steady state

At 80^{0}C, or 353K, the thermal voltage is kT/q=30.4 mV [1]
Thus, the voltage across the pn junction is given by rearranging the Shockley equation:

[3.14]

$$V = V_t \ln\left(\frac{J}{J_s} + 1\right)$$

At a current density in the IGBT of 100 A/cm^2 this gives a voltage of 0.989 V. [1] The lowest conduction loss occurs when the voltage between drain and source (MOSFET) or collector and emitter (IGBT) is lowest. Thus, the cross over point is given as:

$$I_{rated} \times 9 \times \sqrt{V_{block}} / I_{rated} = I_{rated} \times 8.92 \times \sqrt{V_{block}} / I_{rated} + 0.959$$

Thus, V_{block}=143.7 V. [2]

[3.14]

5. You are required to design a low-loss power converter with the following characteristics:

Input voltage: 20 – 25 V
Output Voltage: 12 V
Output Power: 100 W
Input to Output Isolation: Not required

The following components are to be used in the design:

- 100 μH inductor, ESR = 50 mΩ
- IRF IRL2703 MOSFET, R_{DSon}=40 mΩ and when switching, the voltage rise and fall times are 80 ns and the current rise and fall times are 40ns
- Diode, whose voltage drop can be approximated as 0.7 V when conducting and has negligible reverse recovery charge
- Capacitor, negligible series resistance and inductance

(a) In the first instance, a simple buck power converter topology is chosen.

(i) Calculate limits on the duty cycle based on the operating conditions of the converter. You may assume no losses in the converter for this calculation. [1]

[basic calculation]
For Vin=20 V, δ=0.6, for Vin=25 V, δ=0.48 [1]

(ii) Calculate the maximum conduction losses in the circuit at rated output current. You may assume that the effect of ripple current on the losses is negligible. [3]

The conduction losses are given by:

$$I_{out}^{2}\delta R_{DSon} + (0.7I_{out})(1-\delta) + I_{out}^{2}R_{ESR}$$

For the values given:

$$Ploss = 2.78\delta + 5.83(1-\delta) + 3.472$$

$$Ploss = 9.302 - 3.05\delta$$

Thus, the maximum conduction loss occurs when the duty cycle is minimised (i.e. Vin is max).

*Thus, the maximum conduction loss is 9.302-3.05*0.48=7.8 W [3]*

(iii) Calculate a suitable switching frequency for the converter assuming a maximum inductor current ripple of 5% is allowed at rated output current. Give your answer to 3 significant figures. [3]

[3.14]

[basic calculation]

The ripple current in the converter is given by:

$$I_{ripple} = \frac{(Vin - Vout)}{L}\frac{\delta}{f}$$

For this converter, the ripple current is given by

$$I_{ripple} = \frac{(Vin - 12)}{0.0001}\frac{(12/Vin)}{f} = \frac{10000}{f}\left[12 - \frac{144}{Vin}\right]$$

Therefore for a fixed f, the worst case ripple is for a maximum Vin, i.e. Vin=25 V.

Therefore:

$$0.05 \times \frac{100}{12} = \frac{10000}{f}\left[12 - \frac{144}{25}\right]$$

Which gives f=149.8 kHz, or approximately 150 kHz [2]

(iv) Calculate the MOSFET switching losses and the worst case efficiency of the converter. [4]

The switching losses are given by:

$$P_{loss-sw} = 2 \times f \times \frac{1}{2} \times Iout \times Vin \times (t_i + t_v)$$

The worst case here is for Vin=25 V. Thus the worst case switching loss is:

$$P_{loss-sw} = 2 \times 150000 \times \frac{1}{2} \times 8.33 \times 25 \times (120n)$$

$$P_{loss-sw} = 3.74W$$

This corresponds to the worst case conduction loss.

Thus the total maximum los in the converter is 7.8+3.74=11.5 W

Thus the worst case efficiency is 100/(100+11.5)=0.89=89%

(b) It is then proposed that in order to reduce losses, the converter is converted to a soft switched design, as shown in Figure Q5

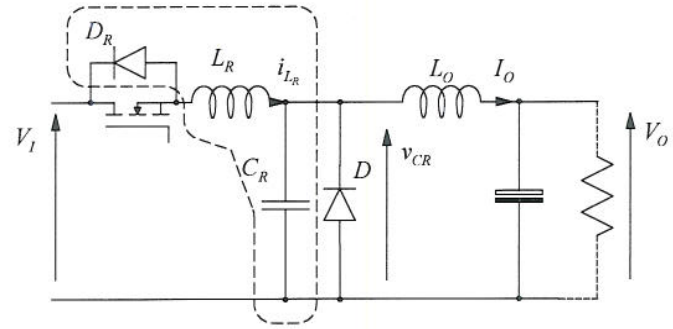


Figure Q5

(i) Explain how this converter topology is able to reduce the losses below that in the buck circuit in part (a). [3]

This converter is soft switched meaning the switching losses can be reduced. The MOSFET turns on into a series inductor and thus the rate of rise of current is limited (rather like a turn on snubber). This limits turn on losses. The resonant action between LR and CR can (if the circuit is properly designed), allow the MOSFET current to reverse. If the MOSFET is turned off during this time, the anti-parallel diode takes the current and clamps the MOSFET voltage to 0.7 V meaning that the MOSFET turns off (i.e. the current falls to zero) with almost zero voltage across it.

[3]

(ii) Using the same MOSFET switching frequency and input voltage range as in the hard switched converter, calculate the limits on the resonant frequency of this circuit. [2]

For this converter, the DC transfer function is given as:

$$\frac{Vout}{Vin} = \frac{2\pi f}{\omega_R}$$

Thus, for Vin=20 V, this gives ω_r=1.57 Mrads/s and for Vin=25 V, this gives ω_r=1.96 Mrads/s

(iii) Choose a suitable value of resonant inductor to ensure that the MOSFET can be turned off under a low loss condition. [2]

In order to allow the current to reverse and divert through the resonant diode at turn off, design the circuit such that:

$$\frac{Vin}{\omega_R L_R} = 1.2 I_{0\max}$$

Thus,

[3.14]

$$L_R = \frac{Vin}{\omega_R \times 1.2 \times 8.33}$$

Thus L_R=1.2μH

(iv) Explain 2 potential disadvantages of using this circuit over the hard-switched case. [2]

- *This circuit has a higher component count and thus cost*
- *control of the output voltage requires a change of clock frequency for the MOSFET rather than simply altering duty cycle – so the control is more complex.*

6.

(a) Figure Q6 shows a slip-compensated speed control scheme for an induction machine. Describe the operation of the system including the role of the slip speed signal, the role of the slip limiter and the how the frequency and voltage commands for the inverter are determined. [5]

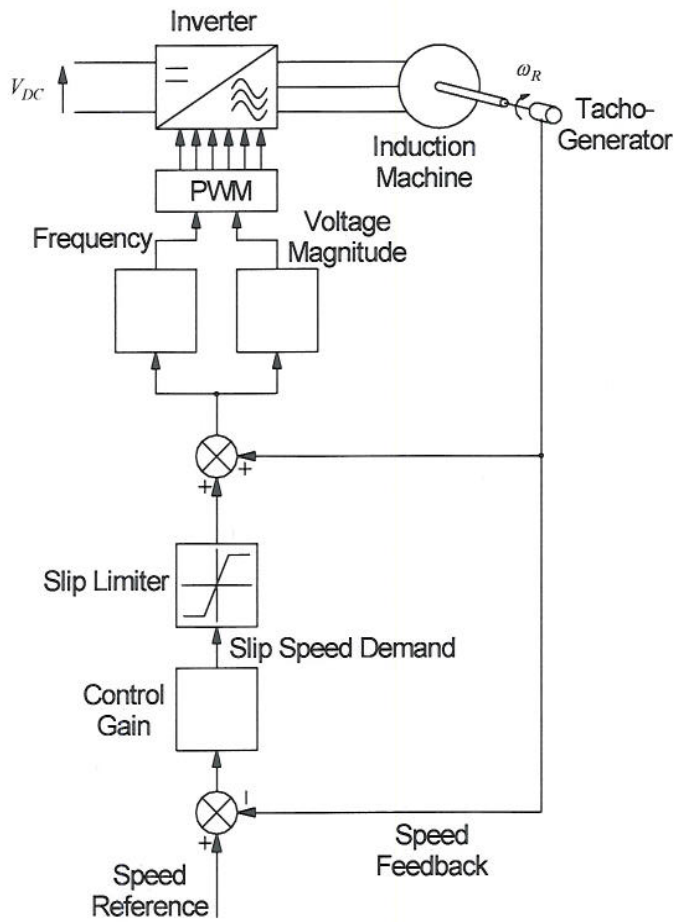


Figure Q6

[Bookwork - diagram has had detailed annotations removed here]
The speed error can be corrected by feedback. The speed error is applied to a controller (e.g. a PI controller) and the output of this used to set the torque developed by the machine. Torque is influenced by setting the slip frequency. The desired slip frequency is added to the measured rotor speed to form the required synchronous speed. The slip must be subject to a limit to prevent excessive currents from flowing. The slip limit is calculated as the frequency difference that exists when the machine is run under rated conditions. To ensure that the flux-linkage is held at its rated value, the applied voltage is varied in proportion to frequency except that (i) the voltage is held constant once it reaches the maximum value that can be formed from the available DC-link voltage and (ii) at low frequencies, where the stator resistance voltage drop is significant, a voltage boost is added.

(b) The nameplate of a 2-pole-pair induction machine gives the following basic information for its operation on a fixed frequency supply. This information is taken to represent its maximum or rated operation for the conditions given.

Phase Voltage 230 V

Frequency 50 Hz
Rated Speed 1,450 rpm
Rated Power 5.0 kW

Determine the following for when the machine is used at variable frequency in a slip-compensated drive system using reasonable approximations where necessary.

(i) The maximum torque available. [2]

$$T^{Max} = \frac{P}{\omega_R} = \frac{5000}{1450 \times \frac{2\pi}{60}} = 32.93\ Nm$$

(ii) The maximum air-gap flux linkage [2]

Approximate by ignoring stator voltage drop.

$$\psi_{AG}^{Max} \approx \frac{|V_S|}{\omega_E} = \frac{230}{2\pi 50} = 0.732\,Wb$$

(iii) The slip-speed limit (in rad/s) that should be imposed to obtain maximum torque. [2]

Again, consider operation at 50 Hz to represent rated operation and defines the maximum slip speed and current. It is clear that this is a 2-pole-pair machine since the rated speed is just below 1500 rpm for 50 Hz operation.

$$\omega_{Slip}^{Max} = \omega_S - \omega_R = \frac{2\pi 50}{2} - 1450 \times \frac{2\pi}{60} = 5.23\ rad/s$$

(iv) The frequency of stator voltage needed to achieve rotation at 2,500 rpm [2]

Approximate answer is sufficient. Approximation would be to ignore the slip and assume operation at synch speed.

$$f_E = \frac{P\omega_S}{2\pi} \equiv \frac{P\omega_R}{2\pi} = \frac{2 \times 2500 \times \frac{2\pi}{60}}{2\pi} = 83.3\ Hz$$

With the correction for slip

$$f_E = \frac{P\omega_S}{2\pi} \approx \frac{P(\omega_S - \omega_{Slip})}{2\pi} = \frac{2 \times \left(2500 \times \frac{2\pi}{60} - 5.23\right)}{2\pi} = 83.3 + 1.66 = 85.0\ Hz$$

(v) The DC-link voltage needed for maximum torque at 2,500 rpm [2]

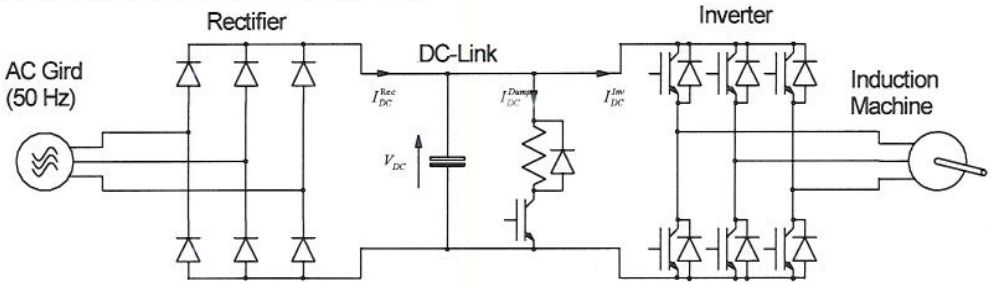
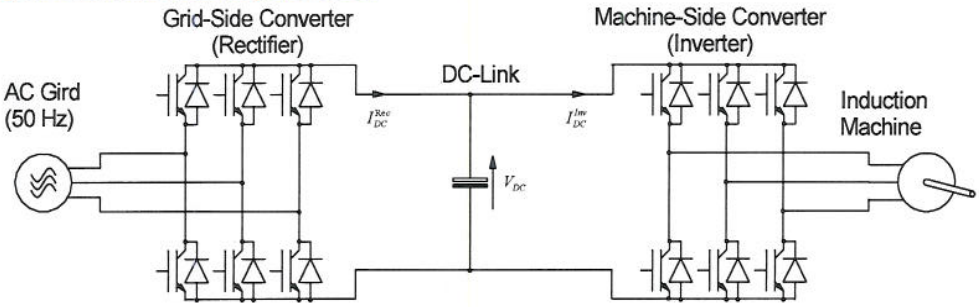
$$|V_S| = \omega_E \psi_{AG}^{Max} = 2\pi \times 85 \times 0.732 = 390.9\ V$$

$$V_{DC} = 2\sqrt{2}|V_S| = 1105\ V$$

In practice, an allowance would be made for voltage drops in inverter and control headroom. Choose perhaps 1200V.

(c) The drive system in Figure Q6 will regenerate on occasion. Describe what arrangements should be made in the DC-link circuit to facilitate this. [5]

The returned power causes the voltage of the DC-link capacitor to rise. It can not be processed by a diode rectifier. If a diode rectifier is used then a dump resistor is needed (switched on in the event of a voltage rise)



Alternatively, an AC/DC converter can be used at the grid-side and the bi-directional power flow possible with this converter allows the DC-link voltage to be managed under re-generation and motoring operation.