IMPERIAL COLLEGE LONDON

EE3-01
EE9AC1

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2012

MSc and EEE PART III/IV: MEng, BEng.and ACGI

Corrected Copy

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Monday, 30 April 2:30 pm

Time allowed: 3:00 hours

Correction
Q5b 2.45pm

There are SIX questions on this paper.

Answer FOUR questions.

Q4c(iv) 4.25pm

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : P. Georgiou

1. Figure 1 below shows a single stage of a differential amplifier.

(a)

(i) Draw a circuit schematic for the current source I_0 that ensures the differential gain is independent of temperature and power supply variation. Include any start up circuits that may be required.

[9]

(ii) For your design, show that the gain bandwidth product is independent of temperature.

[6]

(b) Draw a circuit schematic of a stable voltage reference that could provide the bias voltage V_s and is independent of temperature variation.

[5]

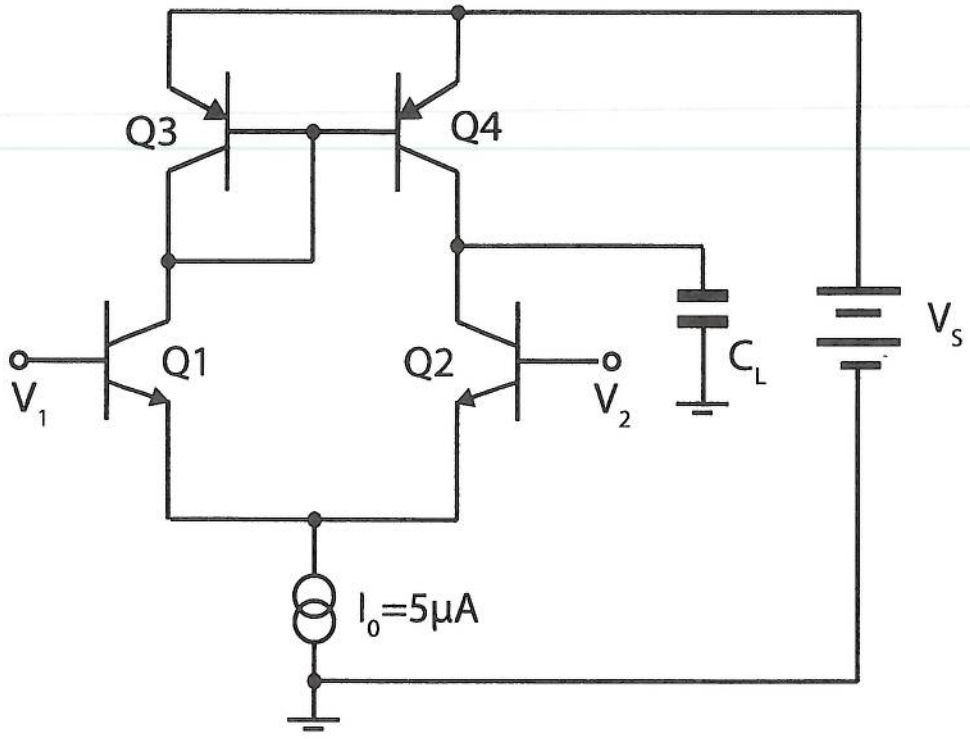

Figure 1.

2. (a). (i) Draw a circuit schematic for a 2-stage voltage mode operational amplifier.

[5]

(ii) Draw a circuit schematic for a single stage current feedback op-amp.

[5]

(b). Figure 2 below shows a 2-stage non-inverting amplifier, whereby Rf and R1 are the gain resistors and C_C is the compensation capacitor used internally for frequency compensation, which is connected from the output of the first stage to the output of the op-amp.

(i). The op-amp has a Gain Bandwidth Product of 1MHz and an input trans-conductance g_m=50.2mS. Calculate the value of the compensation capacitor C_C, assuming the Gain Bandwidth is determined by the first pole frequency.

[2]

(ii). Assuming now that the circuit in Figure 2 is a current feedback op-amp with a pole, $f_{C/L}$, at 10 KHz is given as:

$$f_{C/L} = \frac{1}{2\pi R_f C_C}$$

Calculate the value of R1 for the closed loop gain $A_{C/L}$=100 at this frequency.

[4]

(c). Explain why the slew-rate constraints of a current-feedback op-amp are significantly higher than a voltage mode op-amp.

[4]

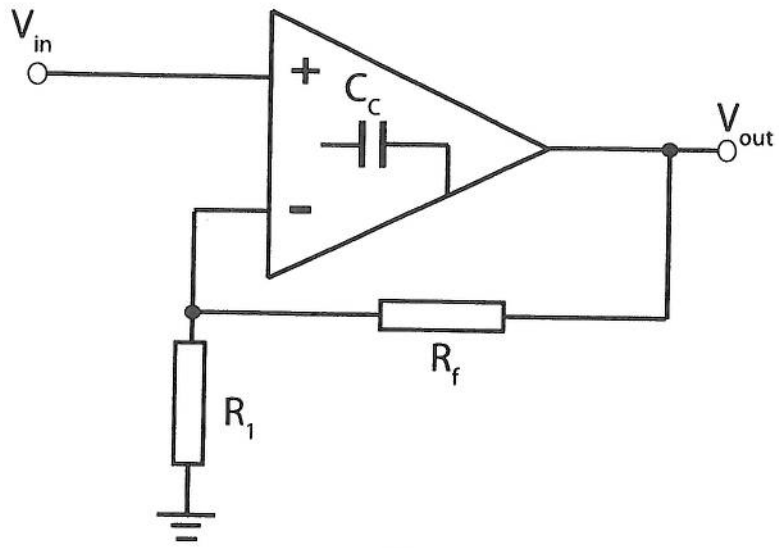

Figure 2.

3. (a). Figure 3 shows a two-stage CMOS op-amp.

(i) Estimate the low-frequency differential voltage gain and gain-bandwidth product of the amplifier. Aspect ratios of all devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

[8]

(ii) What is the main advantage and disadvantage of using a single-stage op-amp instead of a two-stage op-amp ?

[2]

(b).

(i) Show how the output transistors can be cascoded to increase the voltage gain.

[6]

(ii)State two advantages and two disadvantages of using a cascoded output stage.

[4]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	$Kp\ (\mu A/V^2)$	$\lambda\ (V^{-1})$	$V_{T0}\ (V)$
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

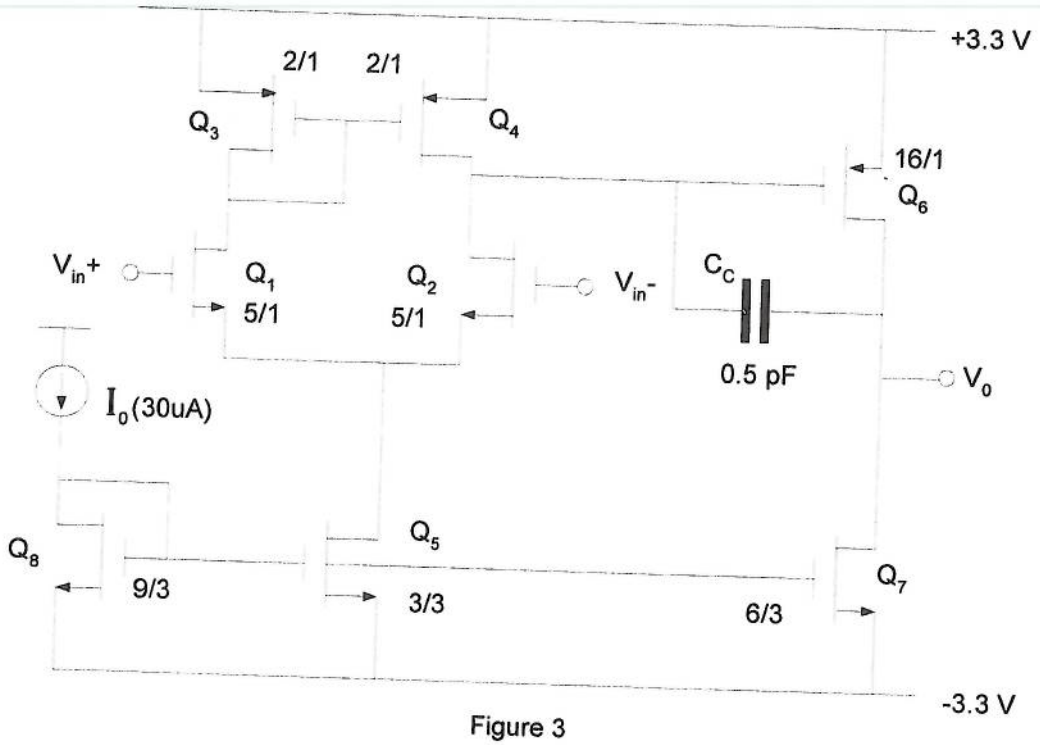

Figure 3

4. Figure 4 shows a differential opamp which is based upon a folded cascode design

(a). Explain what is meant by folded cascode.

[4]

(b). Sketch a circuit diagram of the folded cascode opamp including a circuit which ensures the common mode voltage is maintained at the output.

[6]

(c). (i) Derive the equation for the linear differential resistor of the circuit shown in Figure 4.

[5]

(ii) Assuming the time constant of the circuit is τ=10ms, calculate the value of feedback capacitor, C, assuming input transistors Q1 and Q2 are operating in the triode region and have W/L=5, K=20uA/V^2, Vg=1V, Vt=0.5V and node x is at a common mode of 0 V. You may neglect any body effects.

[5]

Corrected

4.25pm

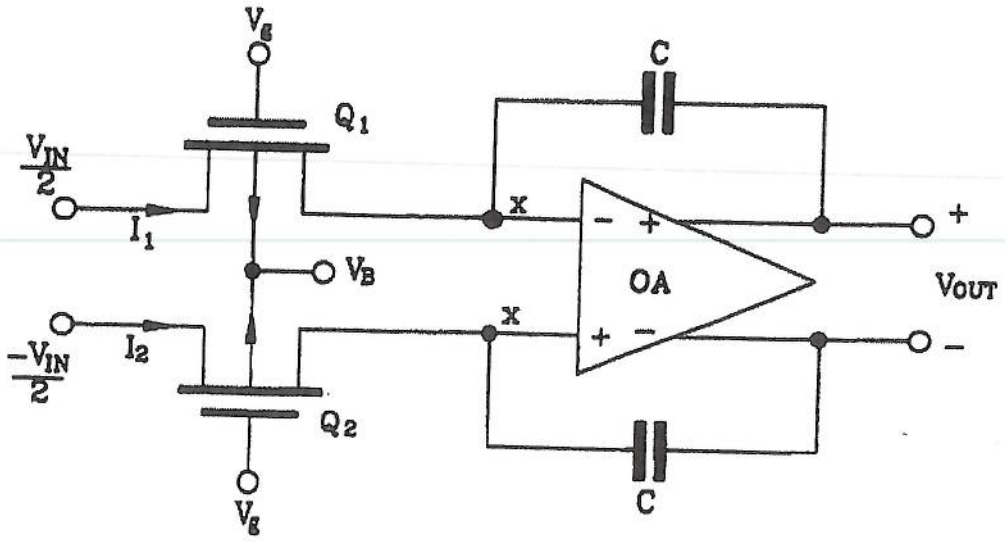

Figure 4.

5. (a) (i) Explain the principles of sigma delta modulation.

(ii) Sketch a typical circuit architecture of a sigma delta modulator. [5]

5

(b) Figure 4 shows one bit of an algorithmic data converter. [5]

connected
2.45pm

(i) Explain how the data conversion works.

(ii)Show how this can be cascaded to perform an 8-bit data conversion. [3]

(c) What noise limits the resolution of a sampled-data converters ? [4]

[3]

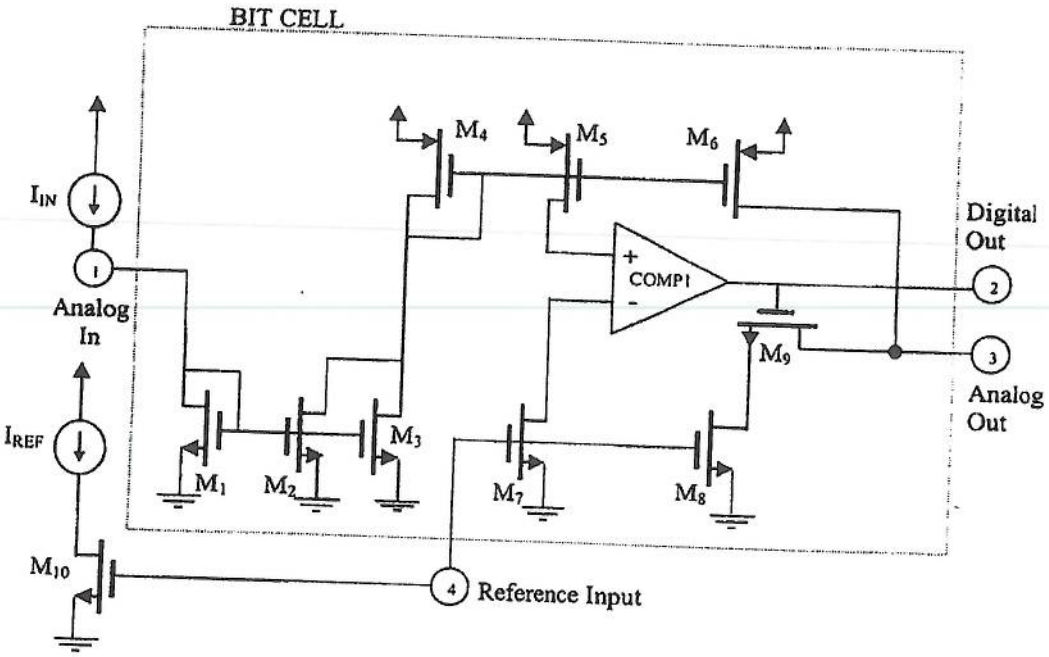

Figure 5.

6. (a) Sketch the basic design of a 3rd-order Chebyshev low pass switched-capacitor ladder filter using op-amps, capacitors and switches.

[5]

(b) For the circuit in part a. state the equations of the normalised passive component values and draw the equivalent RLC prototype.

[5]

(c) From the circuit, calculate normalised passive component values for the original double terminated LC prototype of the filter. The filter is to have a cut-off frequency of 5kHz and assume a clocking frequency of 100 kHz. The values of the integration capacitor for the capacitor-based sections are 5.06pF, and for the inductive based sections is 3.49pF. All other switched capacitors are 1pF. All values should be normalised to 1rad/s. You may assume that the clocking frequency is so high that the integrators can be assumed lossless.

[10]

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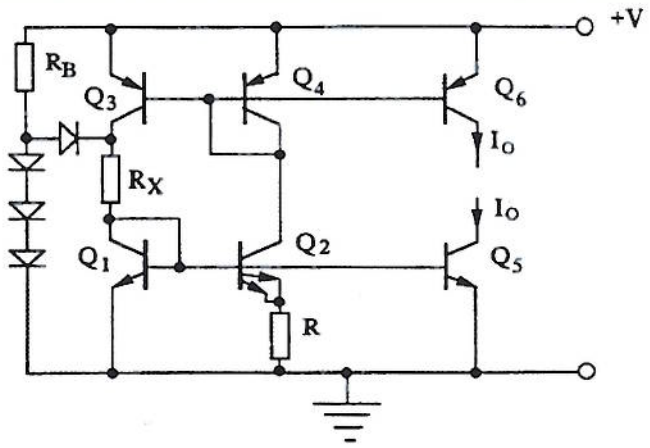
1/8

Answers to question 1:

1.a i) Self biased PTAT current source with start up circuit.



Drawing of PTAT [5]
Drawing of Startup Circuit [4]

ii) Prove that g_m is independent of temperature and therefore gain bandwidth.

$$GBW = \frac{g_{m2}}{2\pi C_c}$$

$$g_m = \frac{I_0}{V_t}$$

$$I_0 = (V_{be1} - V_{be2})/R = V_T \ln[I_{in}/I_0]/R$$

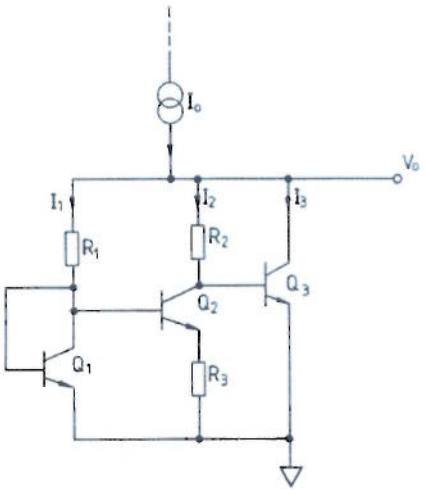
$$I_{in}/I_0 = 2$$

$$g_m = \frac{V_T \ln[2]/R}{2\pi V_t} = \frac{\ln[2]}{2\pi R}$$

$$GBW = \frac{\ln[2]}{2\pi RC_C}$$

[6]

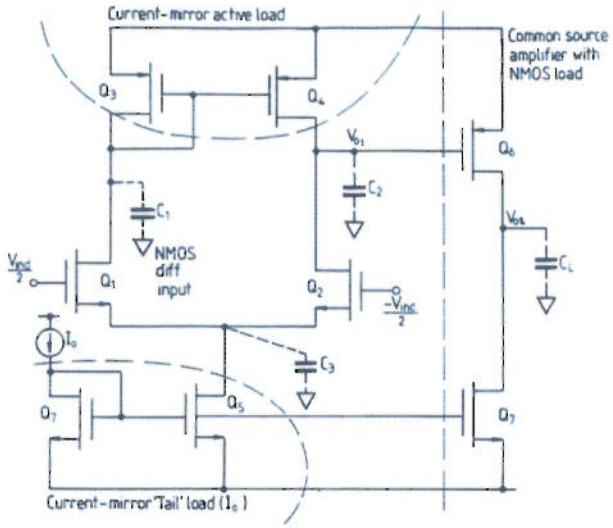
b. Bandgap voltage reference circuit.



[5]

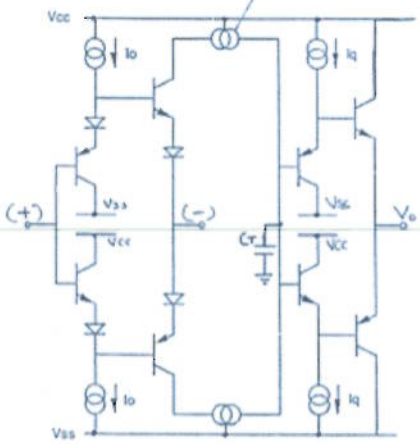
Answers to question 2:

2. a. 2 stage voltage mode op amp



[5]

Current feedback op amp



.

[5]

b. I. $GBW = \frac{g_m}{2\pi C_c} \Rightarrow C_c = \frac{g_m}{2\pi \cdot GBW} = \frac{8 \cdot 10^{-3}}{10^5} = 8pf$

[2]

II. Student needs to identify that for current feedback op-amps the gain is independent of bandwidth. Therefore:

$$f_{C/L} = \frac{1}{2\pi R_f C_C} \Rightarrow R_f = \frac{1}{2\pi f_{C/L} C_C} = \frac{1}{2\pi 10^3 8 \cdot 10^{-9}} = 1.99K\Omega$$

$A_{C/L}$ =(1+Rf/R1) therefore R1=1990 /100 -1 =20.1 Ω

[4]

c. The two inputs of the CFOA have very different impedance levels compared with the VOA.

SR=Zt[ΔIin/Δt] where Iin is the current into the low impedance (-ve) input.

Since there in no upper limit on $\Delta I_{in}/\Delta t$,the slew rate does not have a maximum value as in the case of a VOA. The large signal bandwidth is thus essentially the same as the small signal bandwidth.

[4]

Answers to question 3:

3. a.

$$Av1 = -gm2/(go2+go4)$$

$$(go2+go4) = I_{D2}(\lambda_N + \lambda_P) = 5\times10^{-6}\times0.05 = 2.5\times10^{-7}\Omega^{-1}$$

$$gm2 = 2\sqrt{\beta_2 I_D}$$

$$\beta_2 = \frac{K_N}{2}\left(\frac{W}{L}\right)_2 = 7.5\times10^{-5} A/V$$

$$gm2 = 3.87\times10^{-5} S$$

$$Av1 = -154.9$$

$$Av2 = -gm6/(go7+go6)$$

$$(go7+go6) = I_{D6}(\lambda_N + \lambda_P) = 20\times10^{-6}\times0.05 = 10\times10^{-7}\Omega^{-1}$$

$$gm6 = 2\sqrt{\beta_6 I_{D6}}$$

$$\beta_6 = \frac{K_N}{2}\left(\frac{W}{L}\right)_6 = 1.6\times10^{-4} A/V$$

$$gm6 = 1.13\times10^{-4} S$$

$$Av2 = -113$$

$$A_{total} = Av1\times Av2 = 17503$$

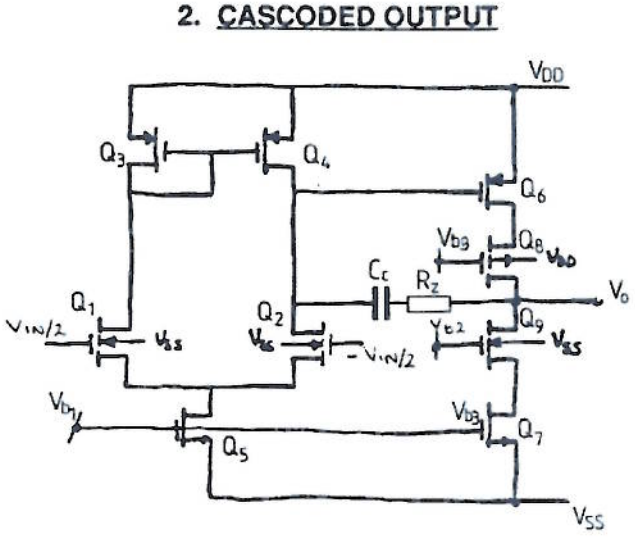
$$G.Bp = gm2/2\pi C_c = 12.32 MHz$$

[8]

In a 2-stage opamp the load contributes to the 2nd pole hence reducing load increases stability.
With a single-stage, the load forms the dominant pole hence reducing the load increases bandwidth.

[2]

c.



[6]

Cascoding output stage increases the output impedance by:
Go=[go6(go8/gm8) +go7(go9/gm9)]
Since Gain of output stage=gm6/[Go]=A_{V2}

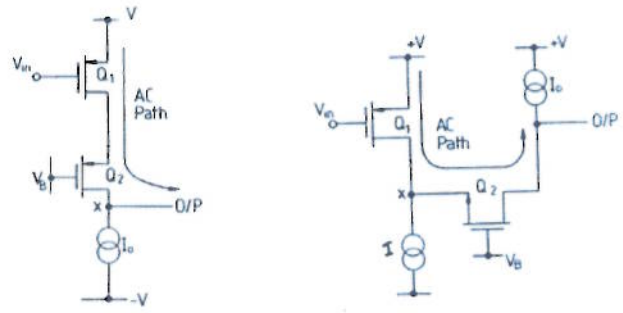
The overall gain therefore increases.

[4]

Answers to question 4:

4.a

Concept



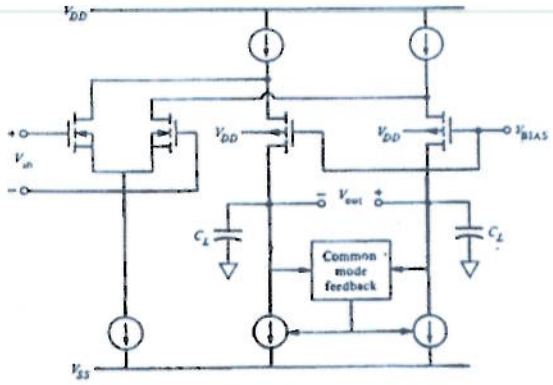
Conventional 'stacking' cascode

Folded cascode

In the folded cascode we are unstacking the conventional cascode and spreading it out. The AC current path is folded and this allow a reduction in power supply. The conventional cascode requires a 2-stage architecture and since the impedance at (x) is high requires internal compensation. The folded cascode can be used as a single stage architecture, node x is low impedance so the only high impedance node will be at the output.
Gain of the folded cascode Av=gm1/Go.

[4]

b.



[6]

c)

Circuit is a differential continuous time integrator with a balanced double differential linear active transresistor.

$$I_1 = 2\beta[(V_g - V_x - V_T)(V_{in}/2 - V_x) - 1/2(V_{in}/2 - V_x)^2]$$

$$I_2 = 2\beta[(V_g - V_x - V_T)(-V_{in}/2 - V_x) - 1/2(-V_{in}/2 - V_x)^2]$$

$$R = 2V_{in}/(I_1 - I_2)$$

$$R = \frac{1}{\beta(V_g - V_T)}$$

[5]

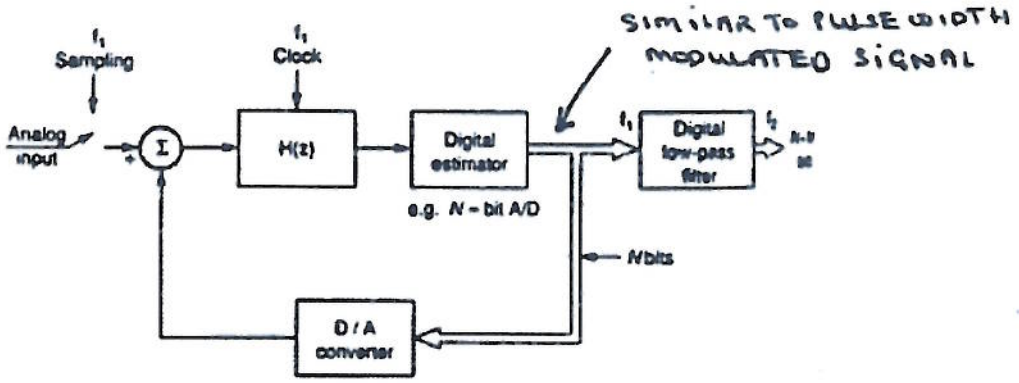
Time constant $\tau=RC=10ms$
$R=1/20ux5(1-0.5)=20\ K\Omega$
$C=\tau/R=10m/20K=5x10^{-7}\ f$

[5]

Answers to question 5:

5.a) Explain sigma delta operation (bookwork).

[5]



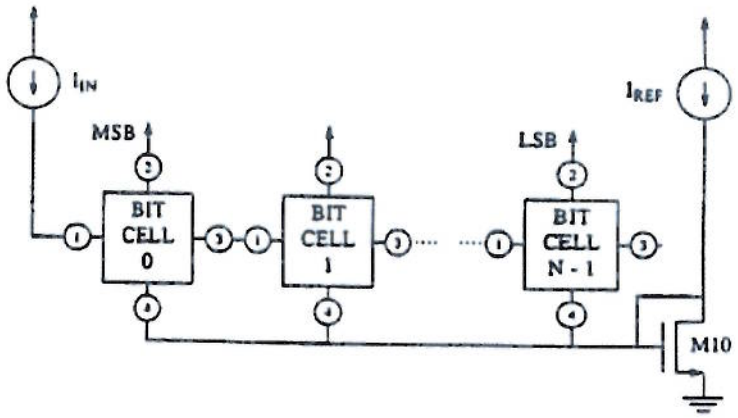
Typical oversampled Σ-Δ (modulator) converter architecture .

[5]

b)(i) Explain how the conversion works (bookwork)

[3]

Draw a cascade of blocks whereby N=8



[4]

c) KT/C noise limits the resolution of a sampled data converter.

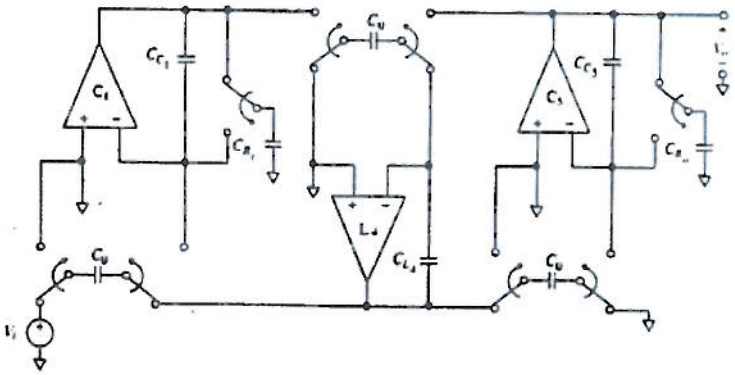
$$DR = 2^N = V_{ref}/Noise = V_{ref}/\sqrt{(kT.10Rf_c)}$$

[3]

8/8

Answers to question 6:

6.a. 3rd-order Chebyshev low pass switched-capacitor ladder filter.



[5]

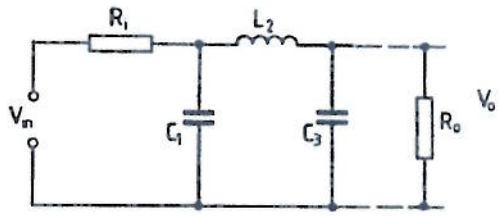
b. General transformation rules for ladder prototypes:

Inductor: $\frac{f_c L_2}{R_s} = \frac{C_{L2}}{C_u}$

Capacitor: $\frac{C_{c3}}{C_u} = f_c R_s C_3$

Resistor Rs=dummy scalar.

The circuit is equivalent to an RLC prototype



[5]

c. For switched capacitor equivalent:

C_{c1}=Cc3=5.08 pF

C_{L2}=3.49 pF.

C_u=1pF

Assume scaling Rs=Ri=Ro=1Ω

Therefore

L2= CL2/fc= $3.49/100\times10^3=3.49\times10^{-5}$ H

Normalised 1rad/sec we multiply by $2\pi f_0$

L2=$3.49\times10^{-5}\times2\pi\times5$ KHz =1.096 H

C1=C3=Cc3/fc = $5.08/100\times10^3=5.08\times10^{-5}$ f

Normalised value C1=C3=1.596