IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2014

EIE PART II: MEng, Beng and ACGI

Corrected Copy

COMPUTER ARCHITECTURE

Wednesday, 14 May 2:30 pm

Time allowed: 1:15 hours

There are TWO questions on this paper.

Answer TWO questions.

Answer ALL questions.

Use separate answer books for Sections A and B.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : W. Luk, D.B. Thomas
Second Marker(s) : D.B. Thomas, W. Luk

Section A (Use a separate answer book for this Section)

1 a Give one advantage and one disadvantage of a direct-mapped cache with one-word blocks.

b What is the total number of bits of storage required for a direct-mapped cache with α bytes of data and one-word blocks, given that the address size is β bits and each word contains γ bytes?

c Give one advantage and one disadvantage of a direct-mapped cache with multi-word blocks.

d Provide a diagram of a 128-kilobyte multi-word direct-mapped cache, given that each block contains 4 words, each word contains 4 bytes, and memory addresses are 32 bits. Show clearly on the diagram the tag size and the data size for an entry in the cache, and how a given address can be used to locate its entry in the cache. Show also the hardware for generating the hit signal and the corresponding data when a cache hit occurs.

e What is the total number of bits of storage required for a direct-mapped cache with α bytes of data and multi-word blocks, given that the address size is β bits, each block contains w words and each word contains γ bytes?

The five parts carry, respectively, 10%, 25%, 10%, 30% and 25% of the marks.

Section B (Use a separate answer book for this Section)

2a i) Give two examples, with justification, where the MIPS instruction set simplifies compiler design and implementation, compared to a CISC ISA.

ii) Give two examples where the MIPS instruction set has been balanced towards performance or architectural simplicity, at the expense of compiler or programmer convenience.

b The following code simulates a very simple processor with five instructions:

```
1  unsigned IM[65536], DM[65536];
2  unsigned pc=0, acc=0;
3
4  while(1){
5    unsigned instr=IM[pc];
6    pc=pc+1;
7
8    unsigned opcode=instr>>16, arg=instr&0xFFFF; // opcode=top 16 MSBs, argument=16 LSBs
9
10   if(opcode==0){
11     DM[arg]=acc;
12   }else if(opcode==1){
13     acc=DM[arg];
14   }else if(opcode==2){
15     acc=arg;
16   }else if(opcode==3){
17     acc=acc+DM[arg];
18   }else if(opcode==4){
19     acc=acc-DM[arg];
20   }
21 }
```

i) Describe the effect of the following two instructions: 0x2FFFF; 0x8000.

ii) What is the common name for this type of instruction set architecture?

iii) Suggest names and an assembly-style format for the five instructions.

iv) Give a minimal length sequence of instructions (in your assembly format) which reads the value at address 0x2000, multiplies it by 15, and stores it to address 0x2000. If necessary, use address 0x4000 as temporary storage.

v) Suggest a single instruction, along with code to add to the simulator, which would add data-dependent conditional branching to the processor.

The two parts carry, respectively, 30%, and 70% of the marks.