IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2010/2011

EEE PART II: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 2

SAMPLE PAPER 2 (ISSUED DECEMBER 2010)

Time allowed: 2.00 hours

There are THREE questions on this paper.

ALL questions are compulsory.
Question 1 carries 40% of the marks and Questions 2 and 3 carry 30% each.

Any special instructions for invigilators and information for candidates are on page 1.

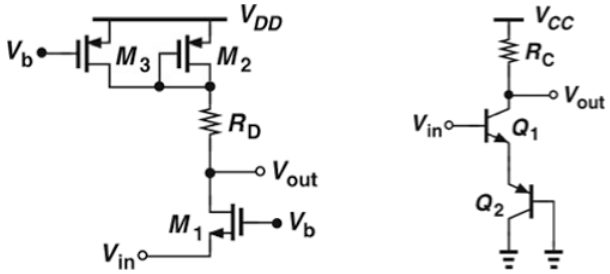
Basic expressions for voltage gain, input and output resistance for single stage amplifiers are given on the last page.

Examiners responsible	First Marker(s):	XXX
	Second Marker(s)	YYY

1. This question consists of 10 brief items. Each item can be answered in a few words or a short paragraph with use of a diagram and/or expression where helpful. Please answer all sub-questions, which carry equal marks.

a) Explain what is meant by *gain-bandwidth product*. A commercial op-amp (LM318) is quoted as having a gain-bandwidth product of 15MHz. What is the open-loop gain (in dB) of this amplifier at 100KHz? [4]

b) Derive expressions (by inspection) for the output impedance of the circuits shown below: [4]



(i) (ii)

c) Derive expressions (by inspection) for the voltage gain of the circuits shown above: [4]

d) With the aid of a diagram, describe how *Millers Theorem* simplifies the analysis of a common source amplifier at high frequency. [4]

e) Explain which amplifier topology (single stage) you would use as a *voltage buffer*. Explain your reasoning. [4]

f) Describe the *body effect* and explain how amplifiers can be designed to eliminate/reduce this. [4]

g) State (and explain) two challenges in analogue integrated circuit design (compared to designing circuits with discrete components). [4]

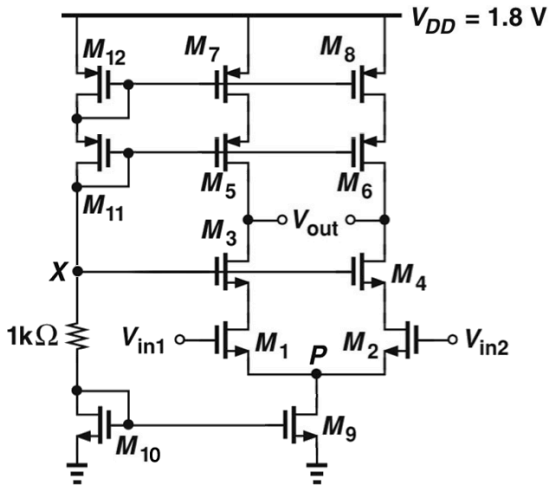
h) Describe with the use of a diagram, how to ensure a sufficient *phase margin* in the design of an amplifier. [4]

i) Explain what is meant by *Common-Mode Rejection (CMR)*? Why is it important in analogue design to achieve good CMR? [4]

j) Draw the *bode plot* (magnitude response only) for a single stage common-emitter amplifier having a capacitively-coupled input and resistive load. Include the parasitic capacitances. [4]

[Question 1 Total = 40]

2. The circuit shown below is called a fully differential telescopic cascode amplifier. The bias current to the differential pair $M_{1\text{-}2}$ and bias voltages required to bias the cascode amplifiers are generated by devices $M_{9\text{-}12}$.



Assume all devices are in saturation and $\lambda>0$ (i.e. $R_{out}<\infty$). Where required, use the following values: $|V_{TH}|=0.4V$, $\mu_n C_{ox}=200\mu A/V^2$, $\mu_p C_{ox}=100\mu A/V^2$, $\lambda_n=0.1V^{-1}$, $\lambda_p=0.2V^{-1}$.

a) Given that $V_X=0.9V$, $I_9=1mA$ and that all PMOS devices are identical, calculate $(W/L)_{5\text{-}12}$ for a power budget of 2.25mW. [5]

b) Draw the half circuit for the differential amplifier and derive the output impedance R_{out} stating any assumptions made. [5]

c) Derive the short-circuit transconductance G_m $(=i_{out}/v_{in})$ and use this and the answer to (b) to determine the differential voltage gain A_v $(=V_{out}/V_{in1}\text{-}V_{in2})$. [5]

d) Given that devices M_1 to M_4 are identical, calculate the (W/L)'s for $g_{m1\text{-}4}=10mS$. Use these values and the answers to (a) and (c) to calculate the differential voltage gain. [5]

This design is to be implemented into an integrated circuit in 0.18μm 1P4M CMOS technology. Assume this technology has the following devices available: 1.8v N/PMOS transistors, MIM (metal-insulator-metal) capacitors, metal resistors, poly resistors, high-resistance-poly resistors, where: $C_{MIM}=0.8fF/\mu m^2$, $R_{metal}=10m\Omega/\square$, $R_{poly}=50\Omega/\square$, $R_{highpoly}=5k\Omega/\square$. Also, the maximum current densities for metal and polysilicon are given as 1mA/μm and 0.1mA/μm respectively.

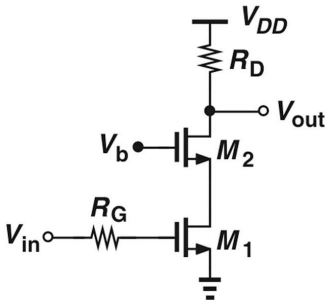
e) Design the resistor in this technology (i.e. select a resistor type and calculate the device dimensions: W and L). Explain your choice. [3]

f) Identify the device pairs/groups in the above circuit where matching is important. State three techniques that can be used to improve device matching. [4]

g) Identify three issues with the bias circuit used in this circuit when implementing this design as an integrated circuit. [3]

[Question 2 Total = 30]

3. We wish to design the MOS cascode amplifier shown below for an input pole of 5 GHz and an output pole of 10 GHz.



Assume M_1 and M_2 are identical and are of minimum length in 0.18μm CMOS technology, I_D=0.5mA, V_{GS}-V_{TH}=200mV (for both transistors), C_{GS}=(2/3)WLC_{ox}, C_{ox}=12fF/μm^2, C_{DB}≈0, C_{SB}≈0, $\mu_n C_{ox}$=200μA/V^2, λ=0 and C_{GD}=C_0W, where C_0=0.2fF/μm denotes the gate-drain capacitance per unit width.

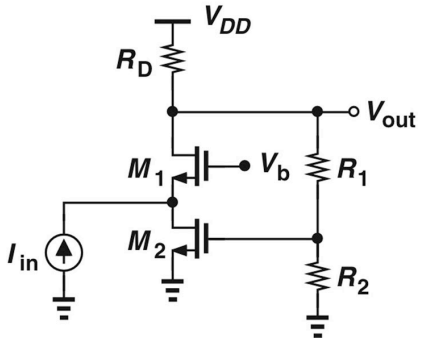
a) Redraw the circuit to include all the device parasitic capacitances. [3]

b) Determine which are redundant (i.e. either appear in parallel with other capacitances or have both terminals grounded) and redraw with reduced parasitic components (i.e. use lumped values). Use Miller's approximation to resolve any floating capacitors. [3]

c) Determine the device widths (W_1=W_2) and transconductances (g_{m1}=g_{m2}). [4]

d) Determine the maximum allowable values of R_G, R_D and the voltage gain. [5]

The circuit is reconfigured to take a current input and apply negative feedback in order to boost the output impedance. The new circuit is shown below.



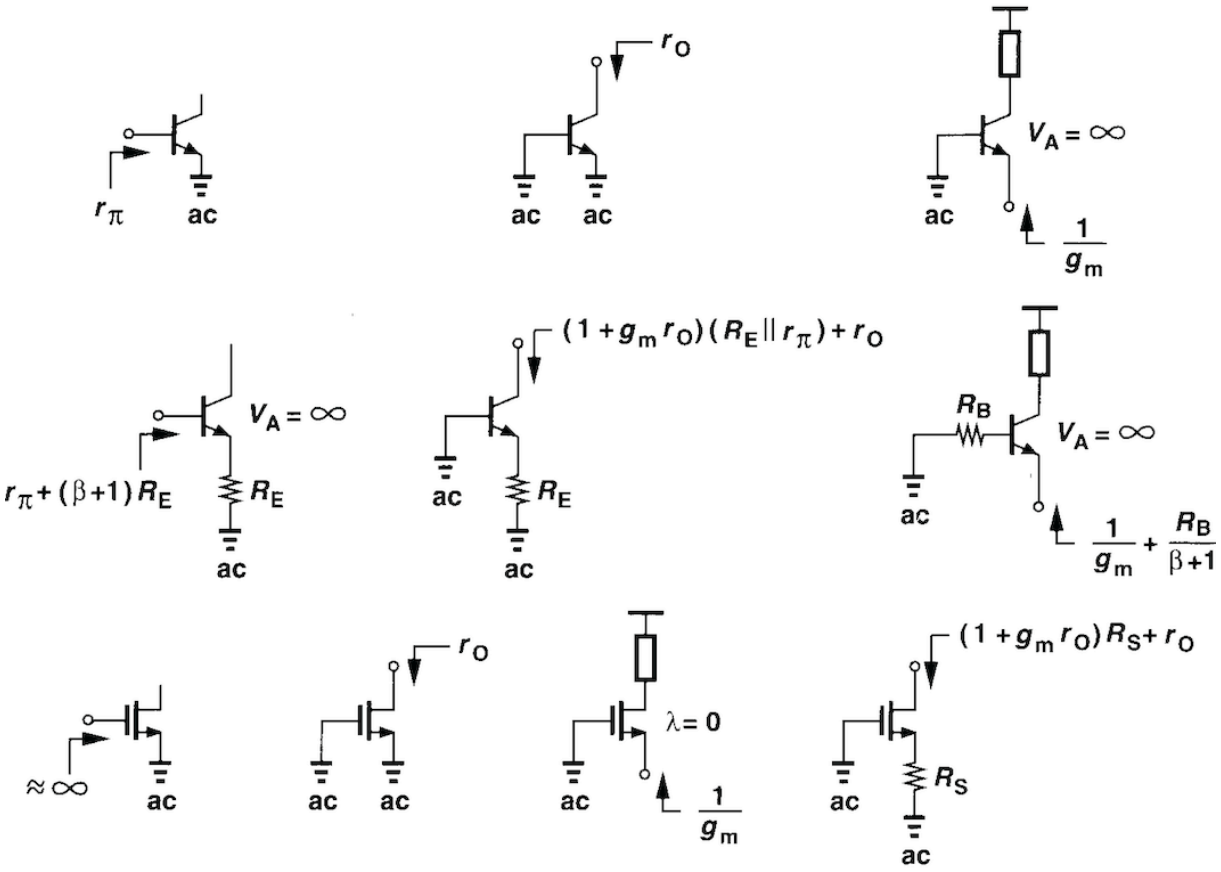
e) Identify the amplifier type and state the ideal input/output impedance levels for such an amplifier [3]

f) Identify the feedback network and break the loop to identify the open-loop gain considering the devices have finite output resistances (i.e. λ>0). [6]

g) Determine the closed-loop gain and input/output impedances. [6]

[Question 3 Total = 30]

Input and Output Impedances



Voltage Gain Equations