Model answer to Q 1(a): Calculated Example for New Application

The Active Denial System is a non-lethal electromagnetic weapon for crowd control. It generates enough incident radiation to penetrate human skin (i.e. 400 μm), just beyond the epidermis layer. One system has the following specifications (all variables have their usual meaning):

- fo = 95 GHz
- P_T = 100 kW
- R_{MAX} = 750 m
- Circular parabolic reflector antenna diameter, D = 2.2 m, with 75% efficiency.

At 95 GHz, dry human epidermis has the following approximate parameter values:

- Mass density, ρ_m = 1330 kg/m^3
- Specific heat capacity, c_p = 3590 J/kg.K
- Conductivity, σ = 39 S/m
- Dielectric constant, ε_r' = 5.79
- Voltage-wave reflection coefficient at the air-skin boundary, $|\rho|$ = 0.56

(i) Effective area of the antenna is $A_{eff} = \pi\left(\frac{2.2}{2}\right)^2 = 3.8\ m^2$

[1]

(ii) Directivity $Do = \frac{4\pi A_{eff}}{\lambda^2} = 4.79x10^6 = 66.8\ dBi$

[2]

(iii) Radiating far field range $R_{ff} = \frac{2D^2}{\lambda} = 3.1\ km$

[2]

(iv) Gain $G = Do\ x\ 0.75 = 3.59x10^6 = 65.6\ dBi$
But since we are in the near field assume a further gain reduction of 5 dB, corresponding to a gain of ~ 60 dBi. eg, IF THIS IS IGNORED

[2]

Model answer to Q 1(b): Calculated Example for New Application

(i) Effective Isotropically Radiated Power, EIRP = 10^5 x 10^6 = 10^{11} W = 110 dBW ×3.59 115.6dBW

[1]

(ii) Incident power density, $Pi = \frac{EIRP}{4\pi(750)^2} = 14{,}147\ W/m^2 = 1{,}415\ mW/cm^2$ ×3.59 5.08 W/cm²

Absorbed power density, $Pa = \frac{EIRP(1-|\rho|^2)}{4\pi(750)^2} = 9{,}711 W/m^2 = 971\ mW/cm^2$ 6.189 ×3.59 3.49 W/cm²

[2]

(iii) $|E|_{peak} = \sqrt{2\eta_o Pi} = 3{,}266\ V/m$
with the intrinsic impedance of free space, $\eta_o = 120\pi$

[2]

Model answer to Q 1(c): Calculated Example for New Application

(i) The Specific Absorption Rate (SAR) is the rate at which electromagnetic energy is imparted to an element of mass of a biological body.

$$SAR = \frac{\sigma|E|^2_{peak}}{\rho_m} = 312{,}785\ W/kg$$

1·123 MW/Kg

[3]

978°C

(ii) In 4 seconds the linear rise in temperature, $\Delta T = \frac{SAR\Delta t}{c_p} = 349\ ^{o}C$

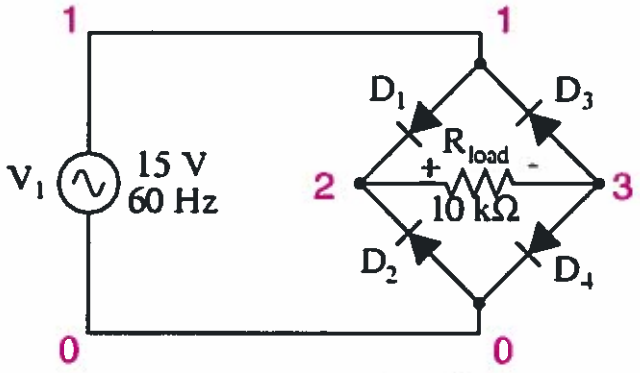
[3]

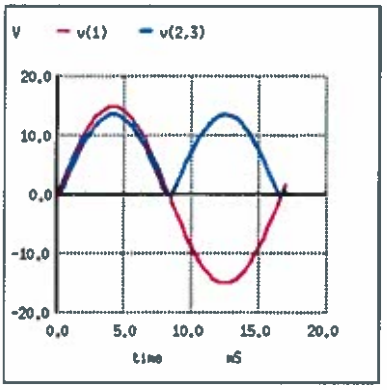
(iii) The traditional safety standard of 10 mW/cm2 applies to an indefinite time of exposure. It has been recognized that much higher levels are tolerable over short time periods. However, from 1b)(ii), the value of $Pi = 1{,}415\ mW/cm^2$ is well above the safety limit. Moreover, the 349 °C temperature rise clearly indicates that the skin would burn off.

[2]

Model answer to Q 2(a): Discussion in Class

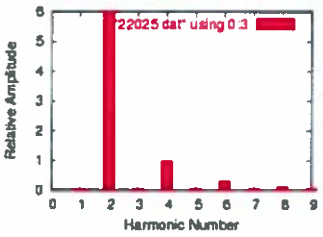
Draw a simple circuit topology that can be used as an even-order harmonic frequency multiplier and sketch typical plots of the input and out voltage waveforms and output frequency spectrum.





http://www.allaboutcircuits.com/vol_2/chpt_7/3.html

dc component = 8.273 V
1st harmonic = 0.070 V
2nd harmonic = 5.997 V
3rd harmonic = 0.072 V
4th harmonic = 1.013 V



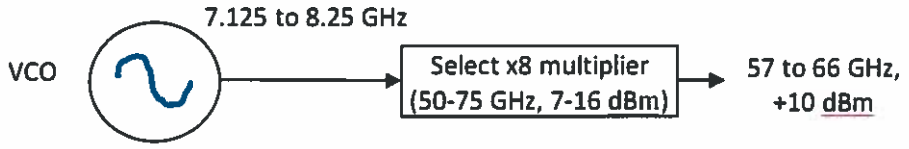
A full-wave bridge rectifier could be used to generate an output second harmonic component that has an amplitude 85 times that at the fundamental frequency. In practice the very high DC component will also need to be removed with the use of a DC blocking capacitor in series with the load.

[6]

Model answer to Q 2(b): Design and Calculated Example for New Application

The ultra-high speed 60 GHz wireless LAN defined, by the IEEE 802.11ad standard, has a 57 to 66 GHz operating frequency range within the European Union and a maximum permitted transmit power of +10 dBm. You are required to design the LO for a direct-conversion transmitter architecture. QuinStar Technology Inc. offers the following range of active frequency multiplier modules.

With a VCO and selecting the most appropriate module(s) available in Table 2.1, draw the block diagram of the LO that will have the least number of subsystem blocks to meet the IEEE 802.11ad specifications. Clearly identify each block and the frequency range of the VCO.



[2]

Model answer to Q 2(c): Calculated Example for New Application

For the design in 2(b), and assuming a linear decrease with increasing frequency of the power gain specified in dB, calculate the values of VCO output powers to meet the IEEE 802.11ad specifications.

From Table 2.1:

At 75 GHz, +4 dBm of input power produces +7 dBm of output power, resulting in conversion gain of 3 dB.

At 50 GHz, +6 dBm of input power produces +16 dBm of output power, resulting in conversion gain of 10 dB.

Using a straight line law, Gain [dB] = 24 - 0.28 x Output Frequency [GHz] or

= 24 – 2.236 x Input Frequency [GHz]

Therefore, to meet the IEEE 802.11ad specifications:

At 57 GHz, gain is 8.04 dB and the VCO output power should be +1.96 dBm

At 66 GHz, gain is 5.52 dB and the VCO output power should be +4.48 dBm

[6]

Model answer to Q 2(d): Discussion in Class

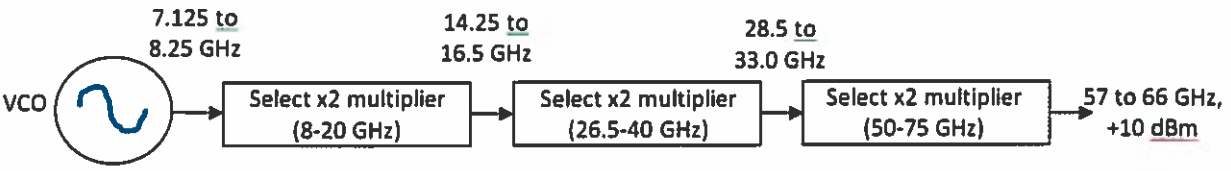
With reference to an equivalent circuit model, briefly describe the difference between *small-signal* and *large-signal* operation. Which of these describe the operation of the active devices listed in Table 2.1.

With *small-signal* operation, the intrinsic parasitic component values of active devices are not dependent on the RF signal power levels, while they are for large-signal operation. With the active frequency multipliers in Table 2.1, the function of harmonic generation exploits non-linear operation from the intrinsic parasitic components and so they must all be operating in the large-signal condition. This can be assumed by the relatively large levels of input power and low levels of conversion gain.

[3]

Model answer to Q 2(e): Calculated Example for New Application

With a VCO and using the modules available in Table 2.1, draw the block diagram of the LO that will have the most number of subsystem blocks to meet the IEEE 802.11ad frequency specifications only. Clearly identify each block and all associated frequency ranges. Using data from Table 2.1, briefly explain why this solution would not work in practice.

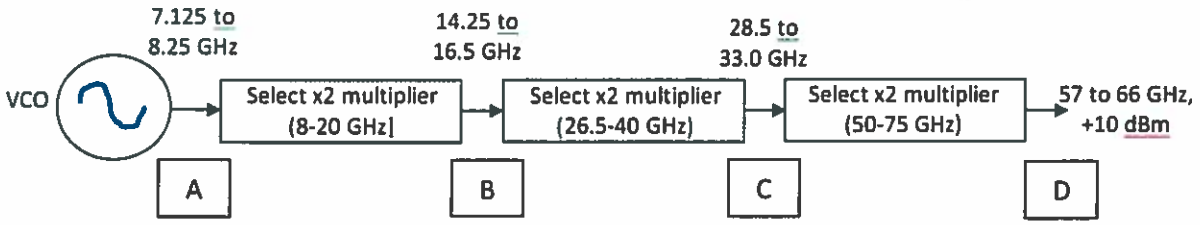


With each block, there is not enough information in Table 2.1 to determine the large-signal power gain and the associated input drive power required at each frequency. For example, for 66 GHz, +6 dBm of input power may be needed at 33 GHz, however this may not be available from the previous stage frequency multiplier because the gains that can be calculated from data in Table 2.1 are power and frequency dependent.

[3]

Model answer to Q 3: Calculated Example for New Application

To meet maximum permitted transmit power of +10 dBm and output frequency specifications for the IEEE 802.11ad wireless LAN standard, a chain of three frequency multiplier stages are used. The respective power gain, noise figure and second-order intercept point values are as follows:



	G [dB]	G	F [dB]	F	IP_2 [dBm]
Stage 1:	14.0	25.12	2.6	1.820	20.0
Stage 2:	8.0	6.31	3.1	2.042	15
Stage 3:	5.0	3.16	4.7	2.951	10

Use the following equations that the students should have learnt from lectures and tutorial questions.

$$So = G_{conversion} S_i \quad where \quad G_{conversion} = G_1 \cdot G_2 \cdot G_3$$

$$No = G_{conversion} F_M N_i \quad when \quad N_i = kT_o B$$

$$\therefore F_M = \frac{(Si/Ni)}{(So/No)} = F_1 + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_1 G_2}$$

$$IP2_M = (IP2_1 \cdot G_2 \cdot G_3) // (IP2_2 G_3) // (IP2_3)$$

$$\therefore IP2_M = \frac{1}{\frac{1}{IP2_1 \cdot G_2 \cdot G_3} + \frac{1}{IP2_2 G_3} + \frac{1}{IP2_3}}$$

$$I_2 = \frac{G_{CONVERSION} P_{RF}}{IMD_2} \approx \frac{(G_{CONVERSION} P_{IN})^2}{IP_2} \equiv 2(G_{CONVERSION} P_{IN}) - IP_2$$

Assuming linear operation for each stage, calculate the following where appropriate:

i) Carrier power levels and overall power gain.

Node

A -17 dBm

B -3 dBm

C +5 dBm

D +10 dBm

Overall power gain is 501.2 or 27 dB

[2]

ii) Second-order intermodulation component power levels.

Node

B -26 dBm

C -5 dBm

D +10 dBm

[3]

iii) Suppression of second-order intermodulation components.

$$IMD_2 = \frac{\left(G_{conversion} P_{RF\_IN}\right)}{I_2} \quad and \quad IMD_2 \approx (IP_2 - G_M P_{RF\_IN})[dBc] \rightarrow IMD_2 = \frac{IP_2}{G_{conversion} P_{RF\_IN}}$$

Node

B +23 dBc

C +10 dBc

D 0 dBc

[3]

iv) Noise figure.

Noise factor calculated is 1.873, giving a noise figure of 2.73 dB

[3]

v) Noise temperature, given a room temperature of 20 °C.

Noise temperature, $Tm = To\ (Fm-1)$ = 255.8 K

[2]

vi) Input noise power.

Ni = 36.4 pW, giving -74 dBm

[2]

vii) Input signal-to-noise ratio.

Si/Ni = 57.4 dB

[1]

viii) Output noise power.

$No = Gm\ Fm\ Ni = 34.1\ pW$ = -44.66 dBm

[2]

ix) Output signal-to-noise ratio.

So/No = 54.66 dB

[1]

x) Show that the value from 3(iv) can be calculated using the values from 3(vii) and 3(ix).

Si/Ni / *So/No* gives 117.39 dB - 114.66 dB = 2.73 dB Q.E.D.

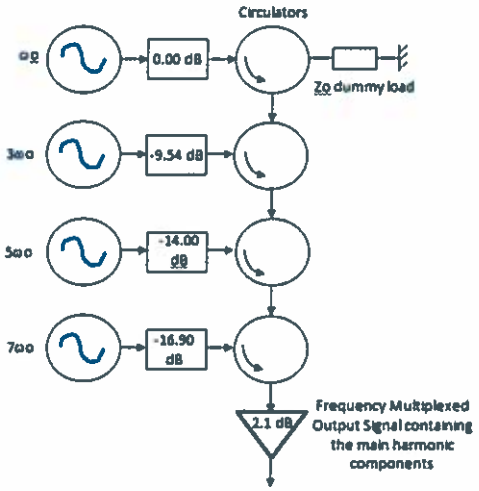
[1]

Model answer to Q 4(a): New Design

a) Using some of the above, design a system that will best synthesize the waveform defined by the following general mathematical expression (clearly identify all values of power attenuation, power gain and any assumptions about appropriate operating frequencies and impedance matching conditions):

$$f(x) = \frac{4}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \sin\left(\frac{n\pi x}{L}\right) \qquad (4.1)$$

To best synthesize the waveform harmonics 1, 3, 5 and 7 need to be included by the four oscillators, attenuators and circulators. The choice of the first harmonic frequency is between 1 and 1.42857 GHz. Also, all blocks operate within an impedance-matched environment, represented by the match load.

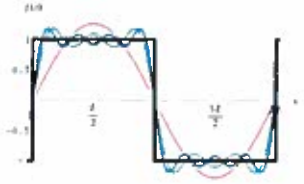


[10]

Model answer to Q 4(b): Bookwork Example

What waveform does the series in (4.1) represent? Also, sketch the output voltage waveform from the approximating implementation design given in 4(a).

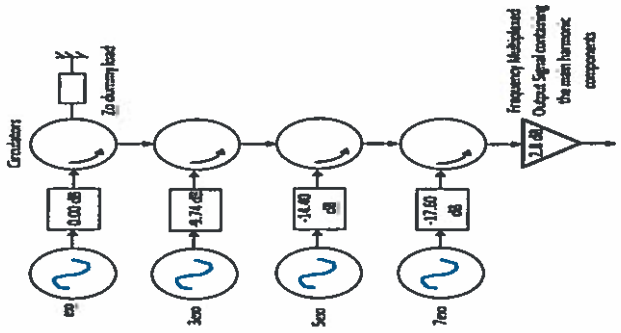
Equation (4.1) represents the Fourier series for an ideal square wave.



[2]

Model answer to Q 4(c): New Design

If the original circulators now have a 0.1 dB insertion loss, re-tune the design given in 4(a) to restore operation.



[2]

Model answer to Q 4(d): Calculated Example

If the original circulators now have ideal transmission line interconnects that introduce a combined insertion phase delay of 45 degrees at the first harmonic frequency, calculated the differential-phase group delay as a fraction of the period of the first harmonic. Similarly, for each harmonic, calculate the overall differential-phase group delay at the output of the waveform generator. Briefly explain the effect of the interconnect delays on the output waveform generated.

Differential-phase group delay is given by:

$$\tau = -\frac{\partial Phase}{\partial \omega} \rightarrow -\frac{\Delta Phase}{\Delta \omega} = \frac{45}{360 fo} = \frac{To}{8}$$

Where *To* is the period of the first harmonic.

For an ideal transmission line interconnect, the third harmonic will have 3 x 45 degrees for a period of To/3. Therefore, this leads to the conclusion that there will be an identical differential-phase group delay at all harmonics for a single interconnect.

However, the total differential-phase group delays at the output of the waveform generator will be 11To/8, 8To/8, 5To/8 and 2To/8 for the first, third, fifth and seventh harmonics, respectively. As a result, the different delays means that the Fourier components will not arrive at the same time and so the rectangular pulse approximation cannot be constructed.

[4]

Model answer to Q 4(e): Thought Experiment

If there is an impedance mismatch at the input of the original circulators, attenuators or amplifier, what could be the effects on the performance of the waveform generator?

Any impedance mismatch reflections from the circulators will affect the amplitude of the Fourier components through the following stages, since less power it transmitted if some of the power is reflected, causing a distortion in the construction of the square wave. The reflected power will make its way back up the chain and into the dummy load.

An impedance mismatch reflection at the amplifier will have a similar affect as that for the circulators, except that all the Fourier components will be affected by the same amount and so the rectangular approximation will not change, but the amplitude will decrease.

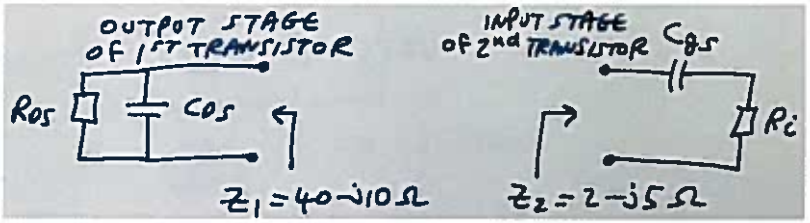
Any impedance mismatch reflections from the attenuators may cause frequency detuning of the carrier oscillator, which will require frequency re-tuning.

[2]

Model answer to Q 5(a): Calculated Example

A MESFET has input and output impedances of 2 – j 5 Ω and 40 – j 10 Ω, respectively. You are required to design the inter-stage impedance matching network for a two-stage 1 GHz amplifier. Assume that the MESFET input and output impedances are fixed and ignore DC biasing networks.

Draw the *RC* lumped-element models for the output of the first-stage transistor and the input for the second-stage transistor. Identify the dominant intrinsic parasitic resistive and capacitive elements of the MESFET.



[2]

Model answer to Q 5(b): Calculated Example

From the *RC* lumped-element models drawn in 5(a), calculate:

i) Parasitic values for both resistances and both capacitances.

$$Y_1 = \frac{1}{Z_1} = \frac{1}{R_1 + jX_1} \equiv G_1 + jB_1$$

$$\therefore R_{OS} = \frac{1}{G_1} = \frac{R_1^2 + X_1^2}{R_1} = 42.5\,\Omega$$

$$\text{and } C_{OS} = \frac{B_1}{\omega_0} = \frac{-X_1}{R_1^2 + X_1^2} = 0.936\,pF$$

$$Z_2 = R_2 + jX_2$$

$$\therefore R_i = R_2 = 2\,\Omega$$

$$\text{and } C_{GS} = \frac{-1}{\omega_0 X_2} = 31.831\,pF$$

[4]

ii) Using the values in 5(b)(i), calculate the loaded quality factors for the input and output of the MESFET. State if it is the input or output that limits the bandwidth of operation.

$$Q_1 = \omega_0 C_{OS} R_{OS} = 0.25$$

$$Q_2 = \frac{1}{\omega_0 C_{GS} R_i} = 2.5$$

SINCE $Q = \frac{f_0}{BW}$ AND $Q_1 < Q_2$

$\therefore$ INPUT LIMITS THE BANDWIDTH TO 0.4 GHz

[4]

Model answer to Q 5(c): Calculated Example

Using discrete lumped-element matching, calculate the:

i) lumped-element component values and state their orientation needed to resonate out the intrinsic parasitic capacitances of the MESFET at the output of the first MESFET and input of the second MESFET.

PUT A { $\frac{1}{C_{DS}\omega_0^2} = 27.06\,nH$ INDUCTOR IN PARALLEL WITH C_{DS} ; $\frac{1}{C_{GS}\omega_0^2} = 0.796\,nH$ INDUCTOR IN SERIES WITH C_{GS}

[2]

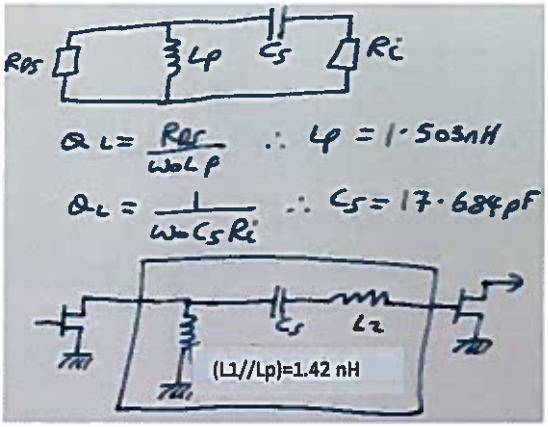
ii) loaded quality factor of the inter-stage impedance matching network and its bandwidth. State if it is the input of the first MESFET, inter-stage impedance matching network or output of the second MESFET that limits the bandwidth of operation.

$Q_L = \sqrt{\frac{R_{DS}}{R_i} - 1} = 4.5$

THIS NETWORK LIMITS THE BANDWIDTH TO 0.2 GHz

[2]

iii) lumped-element component values needed to implement a one-stage resistive L-matching network. Draw the complete impedance matching network having the minimal number of lumped-element components.



[4]

Model answer to Q 5(d): Calculated Example

With a two-stage resistive L-matching network calculate the new loaded quality factor. State if it is the input of the first MESFET, new inter-stage impedance matching network or output of the second MESFET that limits the bandwidth of operation.

$R_{INTERSTAGE} = \sqrt{R_{DS} \times R_i} = 9.22\,\Omega$

$Q_L|_{NEW} = \sqrt{\frac{R_{DS}}{R_{INTERSTAGE}} - 1} = 1.90$

∴ INPUT OF THE FIRST-STAGE MESFET LIMITS THE BANDWIDTH AGAIN TO 0.4 GHz.

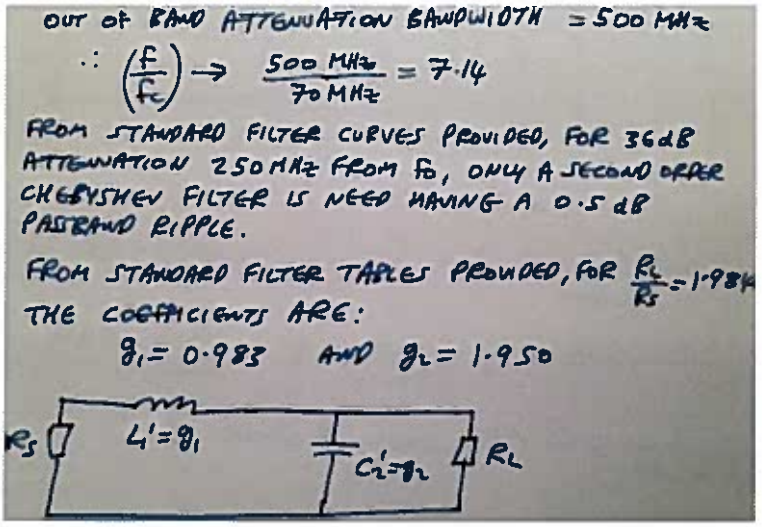
[2]

Model answer to Q 6(a): New Synthesis Example

Using the standard filter curves and tables provided, you are required to design a BPF that meets the following specifications:

- Pass band attenuation ripple = 0.5 dB
- Centre frequency, *fo* = 1.0 GHz
- -3 dB bandwidth = 70 MHz
- Attenuation ±250 MHz from centre frequency = 36 dB
- Source impedance, Z_S = 0.504 Ω
- Load impedance, Z_L = 1.000 Ω

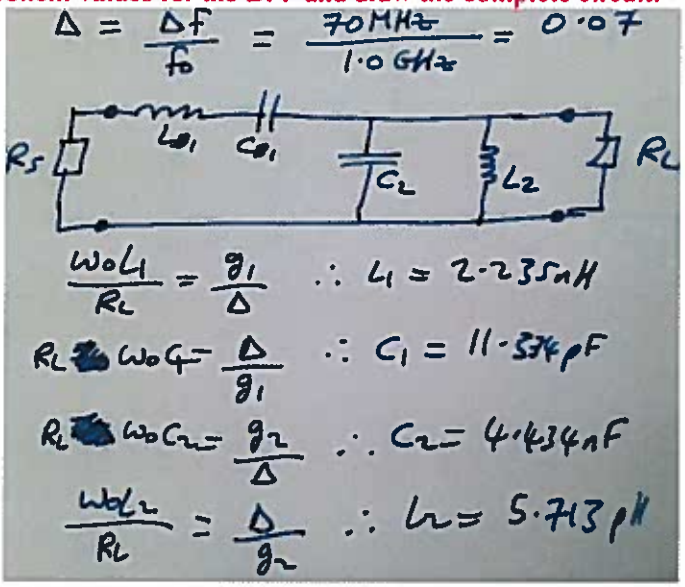
Identify the minimum theoretical order of the filter and draw the LPF prototype circuit, quoting the coefficients for each element.

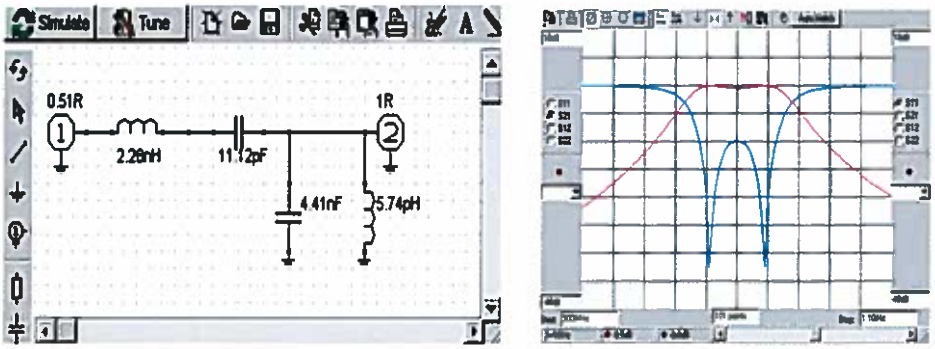


[5]

Model answer to Q 6(b): Calculated Example

Calculate all the component values for the BPF and draw the complete circuit.



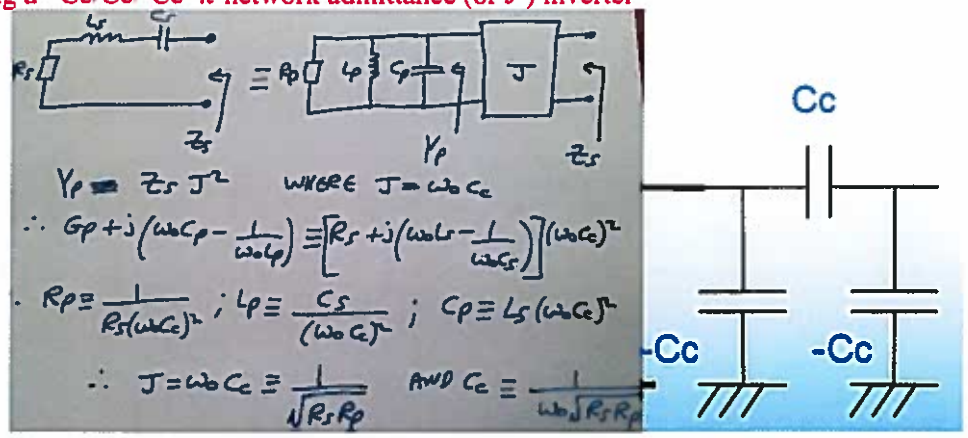


[5]

Model answer to Q 6(c): New Derivation

Given a series $R_SL_SC_S$ circuit, with the aid of a diagram, show how an admittance inverter employing lumped-element capacitors can be used to synthesise the $R_SL_SC_S$ circuit using a shunt $R_PL_PC_P$ circuit. Derive expressions for all the $R_PL_PC_P$ components.

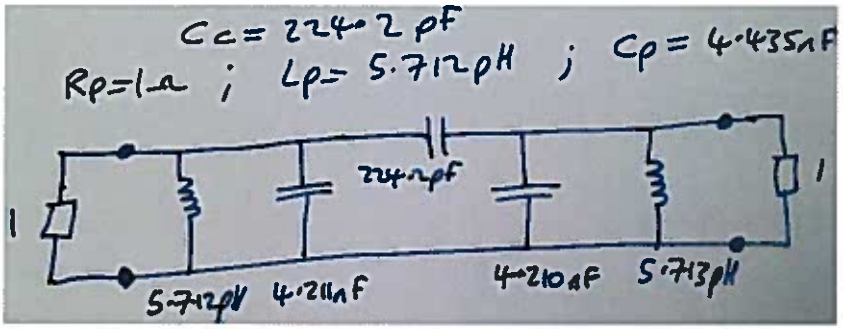
Employing a –Cc/Cc/-Cc π-network admittance (or J-) inverter

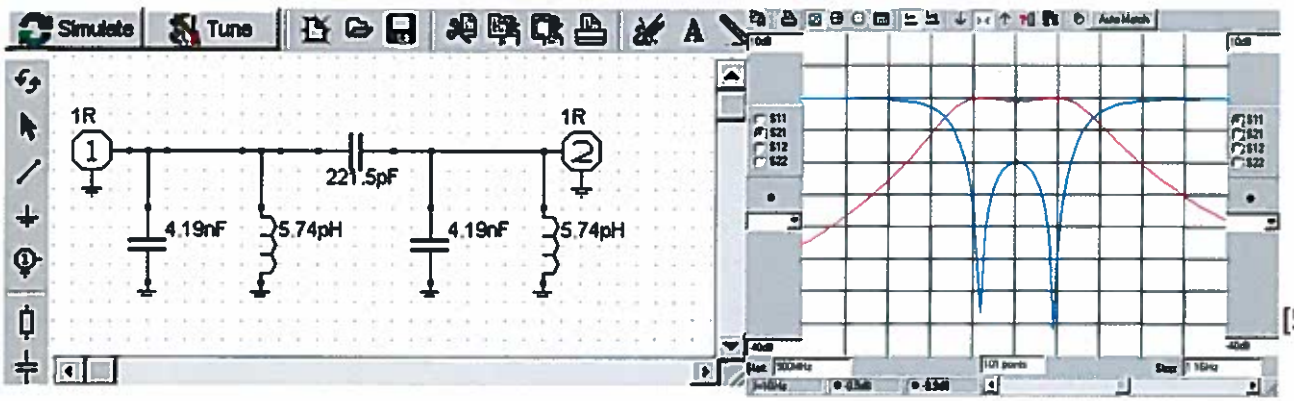


[5]

Model answer to Q 6(d): Calculated Example

Use the technique in 6(c) to impedance match the source impedance of the circuit in 6(b) to ZL. Calculate all the new component values for the BPF and draw the complete circuit.





[5]