Digital Electronics 1 EE1-02

Solutions

Question 1

1. a) (i)

$$\overline{\left(A+\overline{B}\right)\left(\overline{AC\overline{D}}\right)}$$
$$=\left(\overline{A+\overline{B}}\right)+A\overline{C\overline{D}}$$
$$=\left(\overline{A+\overline{B}}\right)+A\left(\overline{C}+D\right)$$
$$=\overline{A}+B+A\overline{C}+AD$$
$$=\overline{A}+\overline{C}+B+AD$$
$$=\overline{A}+\overline{C}+B+D$$

[3]

(ii)

$$\left(\overline{\overline{A}\oplus\overline{BC}}\right)\left(\overline{A+B+\overline{C}}\right)$$
$$=\left(\overline{A}\,\overline{BC}+ABC\right)\left(\overline{A}\overline{B}C\right)$$
$$=\left(\overline{A}\left(\overline{B}+\overline{C}\right)+ABC\right)\left(\overline{A}\overline{B}C\right)$$
$$=\overline{A}\overline{B}C$$

[3]

b)

$$f\left(A,B,C,D\right)=\Sigma\left(0,2,4,5,6,7,8,10,15\right)$$

AB \ CD	00	01	11	10
00	1	0	0	1
01	1	1	1	1
11	0	0	1	0
10	1	0	0	1

$$\Rightarrow f=\overline{B}\overline{D}+\overline{A}\overline{D}+\overline{A}B+BCD$$

Here, 1 mark for drawing the Karnaugh map, 1 for filling it out correctly, 1 for the correct grouping, and 1 for the final expression.

[4]

c)

$$f = A\overline{B}\overline{C} + B\overline{C}\overline{D} + \overline{A}\overline{B}C + \overline{B}C\overline{D} + \overline{A}\overline{B}\overline{C}D$$

AB \ CD	00	01	11	10
00	0	1	1	1
01	1	0	0	0
11	1	0	0	0
10	1	1	0	1

$$\Rightarrow f = \left(A+B+C+D\right)\left(\overline{B}+\overline{D}\right)\left(\overline{B}+\overline{C}\right)\left(\overline{A}+\overline{C}+\overline{D}\right)$$

Here, 1 mark for drawing the Karnaugh map, 1 for filling it out correctly, 1 for the correct grouping, and 1 for the final expression.

[4]

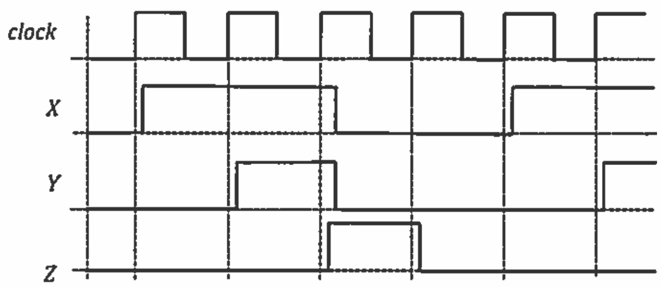
d)

Hexadecimal	Octal	Signed binary	Signed Decimal
97		1001 0111	-105
BD	275		-67

Give 2 marks per answer.

[8]

e)



Give 2 marks per waveform X, Y and Z.

[6]

f) (i) The truth table for the full-adder is as follows:

A	B	C_{in}	Σ	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Give 1 mark for correctly showing the possible values of A, B and C_{in}, and 1 mark each for Σ and C_{out}.

[3]

(ii) Using a Karnaugh map, simplified Boolean expressions for Σ and C_{out} are as follows:

Σ: A \ BC_{in}	00	01	11	10
0	0	1	0	1
1	1	0	1	0

C_{out}: A \ BC_{in}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$\Sigma = \overline{A}.\overline{B}.C_i + \overline{A}.B.\overline{C_i} + A.\overline{B}.\overline{C_i} + A.B.C_i$$

$$= A \oplus B \oplus C_i$$

$$C_{out} = AB + AC_i + BC_i$$

Give 1 mark for using Karnaugh maps or Boolean algebra for simplification, and 1 mark each for the correct final expressions for for Σ and C_{out}.

[3]

g) (i) Initially, write the truth table for f and g as follows:

X	Y	Z	f	g
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

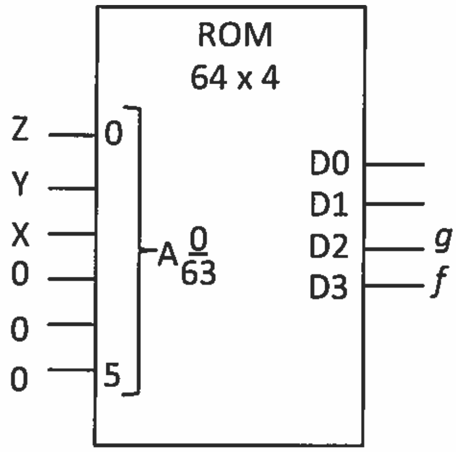
Comparison with the hexadecimal data given in Fig. 1.3(b) shows that if D3 = f, D2 = g, and D1 = D0 = 0 for the first eight data locations, then the correct sequence is obtained in Fig. 1.3(b). Furthermore, if address line A2 = X, A1 = Y and A0 = Z, then these data locations are accessed correctly. This gives the following complete table:

A[5:0]	D[3:0]
00	0
01	C
02	8
03	0
04	C
05	4
06	0
07	C

Give 1 mark for each correct entry.

[4]

(ii) The connections to address and data lines are shown below. Note that A5 = A4 = A3 = 0, to allow the first eight data locations to be addressed.

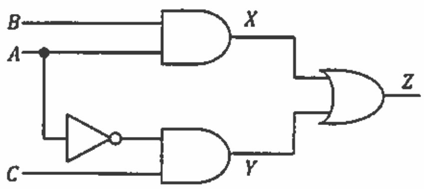


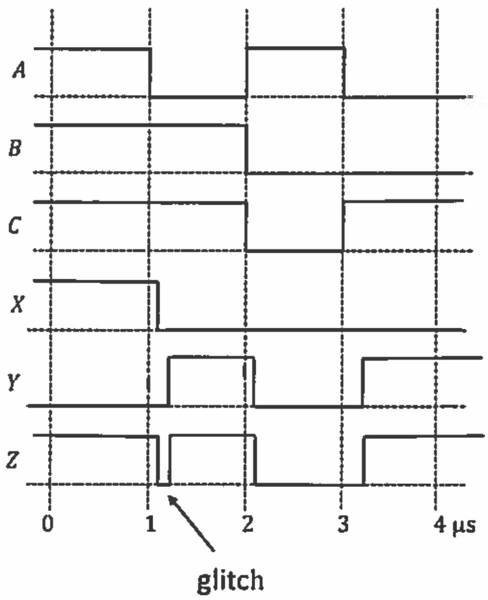
Give 1 mark for correct address line connections and 1 mark for correct data line connections.

[2]

Question 2

2. a) (i)





2 marks each for the waveforms for X, Y and Z. These should show the switching delay, and the glitch in *Z*.

[6]

(ii) To prevent a static 1 hazard, i.e. a glitch which transitions from 1 – 0 – 1, we require covering '1's in the Karnaugh map which are adjacent but in different groups. For the function in the circuit:

$$Z = AB + \bar{A}C$$

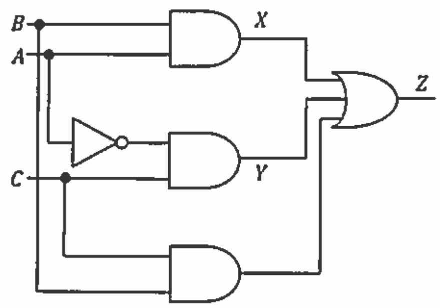
The Karnaugh map is as follows:

Z

A \ BC	00	01	11	10
0	0	1	1	0
1	0	0	1	1

Here the grouping BC will eliminate the hazard, giving the Boolean expression and circuit as follows:

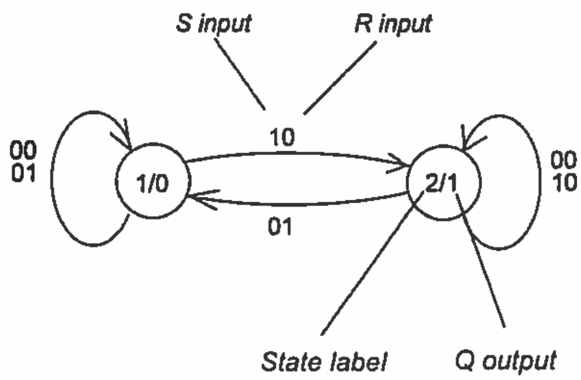
$Z = AB + \bar{A}C + BC$



2 marks for Karnaugh map, 1 mark for the introduction of the correct extra term or Boolean expression, and 1 for the redesigned circuit diagram.

[4]

(b) (i) The state diagram for the SR flip-flop is as follows:



1 mark for states, 1 mark for interconnections, and 2 for labelling.

[4]

(ii) To find the characteristic Boolean equations for the flip-flop, we first draw the assigned state table from the state diagram:

Present Output	Next output inputs: SR			
	00	01	11	10
0	0	0	X	1
1	1	0	X	1

Re-drawing this as a Karnaugh map for next state output Q^+, with inputs Q (the present state), S and R:

Q\SR	00	01	11	10
0	0	0	X	1
1	1	0	X	1

The Karnaugh map gives the following Boolean equations:

$$Q^+ = Q\overline{R} + S \qquad \overline{Q^+} = \overline{Q}\,\overline{S} + R$$

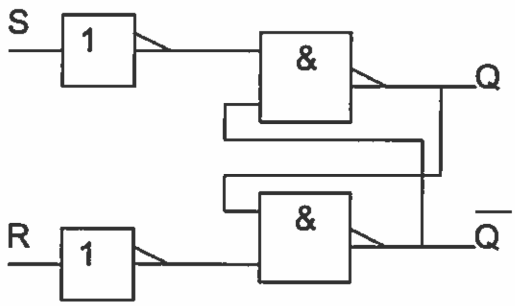
1 mark each for the assigned state table and Karnaugh map, and 1 mark each for the Boolean equation.

[4]

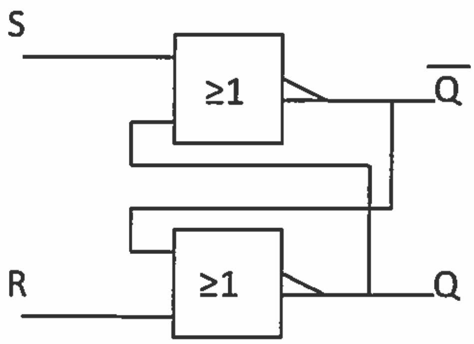
(iii) Rewrite the Boolean equations using NAND gates only, and draw the circuit diagram:

$$Q^+ = \overline{\overline{(Q\overline{R})}.\overline{S}}$$

$$\overline{Q^+} = \overline{\overline{(\overline{Q}\,\overline{S})}R}$$



By replacing the NAND gates by their alternative symbols (NOR with inverted inputs), and cancelling inversion bubbles where required, we obtain the NOR version of the circuit:



1 mark for NAND implementation, 1 mark for the NAND circuit, and 2 for the NOR circuit.

[4]

(c) (i) The MUXs may be used to directly write give the following Boolean equations. This requires understanding the MUX IEEE symbol and operation.

$$X = A\bar{B}\bar{C} + A\bar{B}C = A\bar{B}$$
$$Y = \bar{A}B + A\bar{B}$$

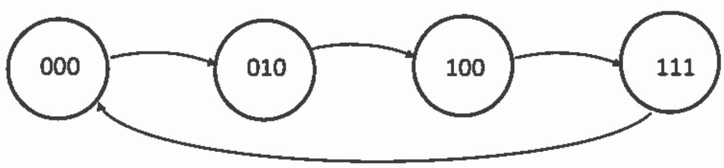
2 marks each for the Boolean equation.

[4]

(ii) Initially, draw the state transition table for the FSM:

Present state	Next state
Q2Q1Q0 A B C	$Q2^+Q1^+Q0^+$
0 0 0	0 1 0
0 0 1	0 1 0
0 1 0	1 0 0
0 1 1	1 0 0
1 0 0	1 1 1
1 0 1	1 1 1
1 1 0	0 0 0
1 1 1	0 0 0

If the initial state for the FSM is 000, then the Moore diagram is the following. Note that not all states in the table above are used here:

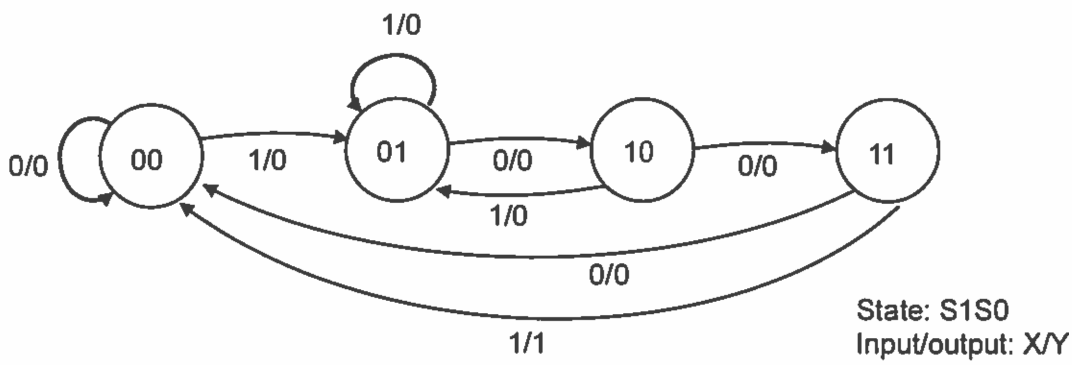


2 marks for the state transition table and 2 marks for the Moore diagram.

[4]

Question 3

(a) Mealy diagram for the FSM:



Give 2 marks for correct number of states, 4 marks for correct interconnections, and 2 marks correct labelling of the interconnections.

[8]

b)

State transition table for the FSM:

Current state		Input	Next state		Output
S1	S0	X	S1+	S0+	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	0	0
1	1	1	0	0	1

Give 1 mark for each correct row of the table.

[8]

c)

The transition table for the J-K flip-flop is the following:

Transition	*J*	*K*
$0 \rightarrow 0$	0	X
$0 \rightarrow 1$	1	X
$1 \rightarrow 0$	X	1
$1 \rightarrow 1$	X	0

Give 1 mark for the table.

Using this table, it is possible to draw Karnaugh maps for J1, K1 and J0, K0, as a function of S1, S0 and X, to give the next states S1+ and S0+. Y may be obtained directly from S1, S0 and X.

<u>For S1+:</u>

K-map for J1:

X \ $S1S0$	00	01	11	10
0	0	1	X	X
1	0	0	X	X

K-map for K1:

X \ $S1S0$	00	01	11	10
0	X	X	1	0
1	X	X	1	1

$J1 = \bar{X}S0$

$K1 = X + S0$

<u>For S0+:</u>

K-map for J0:

X \ $S1S0$	00	01	11	10
0	0	X	X	1
1	1	X	X	1

K-map for K0:

X \ $S1S0$	00	01	11	10
0	X	1	1	X
1	X	0	1	X

$J0 = X + S1$

$K0 = \bar{X} + S0$

Give 2 marks for each K-map with its associated equation.

<u>For Y:</u>

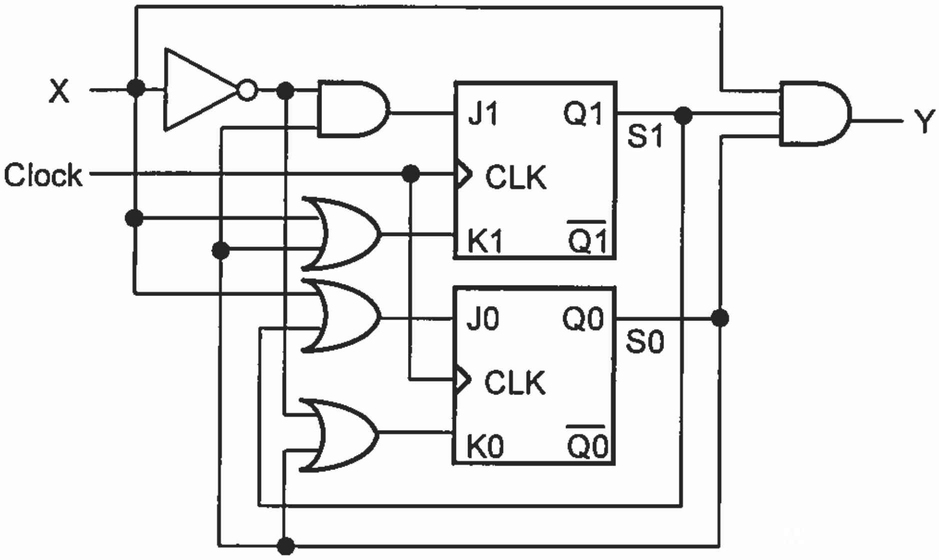
Y can be found directly from the state transition table:

$Y = S1S0X$

Give 1 mark for this.

[10]

d)



Give 1 mark for correct number of flip-flops, 2 marks for correct gates and 1 for correct interconnections.

[4]