E3.05
ISE3.19

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2009

EEE/ISE PART III/IV: MEng, BEng and ACGI

Q6, a1.

DIGITAL SYSTEM DESIGN

Corrected Copy

Wednesday, 29 April 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	P.Y.K. Cheung
	Second Marker(s) :	T.J.W. Clarke

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X[7:0] is an eight bit bus with X7 being the MSB and X0 the LSB.

Hexadecimal numbers are prefixed with '$'. For example the decimal number 10 is written as $A.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

1. Figure 1.1 shows a channel in a vending machine through which coins are rolled down and detected by three light sensitive detectors. The timing diagram for the signals X, Y, Z from the three detectors Dx, Dy and Dz when 5p, 10p and 50p coins are respectively fed into the machine in that order are given in Figure 1.2. The detectors are so positioned that only waveforms X, Y, Z as shown are possible. A synchronous finite state machine (FSM) is used to generate the three output signals p5, p10 and p50 as shown in Figure 1.2 to indicate the type of coin being detected.

   You may assume that a clock signal of suitably high frequency is available. In addition, the detectors are arranged in such a way that the rising edge of Z is at least one clock cycle before Y, and the rising edge of Y is at least one clock cycle before X. When a coin is detected, one of the three outputs goes high shortly after the falling edge of Z for one clock period. Also assume that these are the only three types of coins ever used, and that only one coin can roll down the channel at any one time.

   a) Design a Moore FSM in the form of a state diagram using 7 states.

   [6 marks]

   b) Draw a state transition table for your FSM design. (Hint: use don't care conditions where possible).

   [6 marks]

   c) Using one-hot encoding, implement your design using an Altera Cyclone II FPGA in the form of Boolean equations. A Logic Element (LE) in Altera's Cyclone II device consists of a 4-input lookup table and a flip-flop. Estimate the number of Logic Elements (LEs) required to implement your design.

   [8 marks]

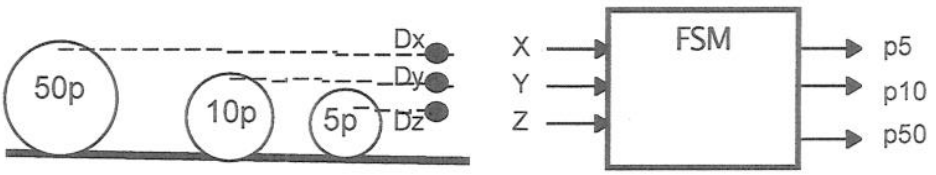

Figure 1.1

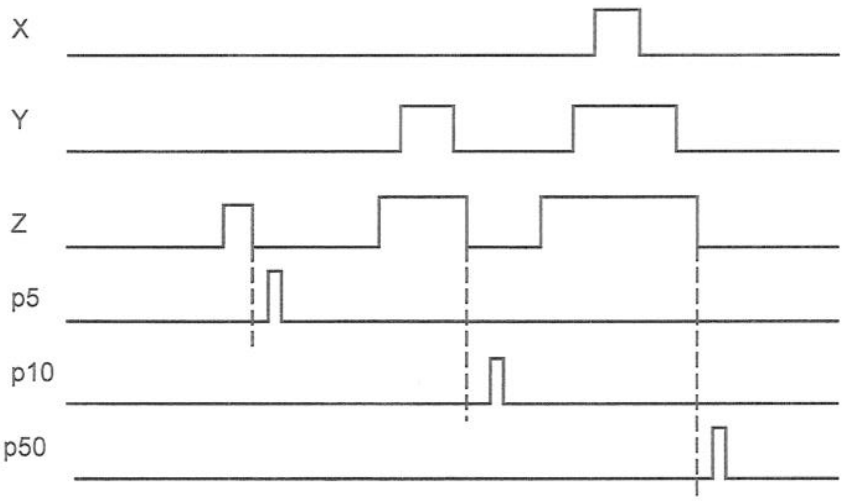

Figure 1.2

2. a) Explain the cause of ground bounce found in digital circuits. How may ground bounce be reduced?

[4 marks]

b) With the help of a schematic, explain what is a bus-hold circuit. What is the use of such a circuit?

[4 marks]

c) What happens to the output of a digital signal when it goes into metastable state? What are the circumstances under which metastability arises?

[4 marks]

d) Figure 2.1 shows a circuit to synchronise an asynchronous input A to a synchronous system G. The synchronous system G can operate with a maximum clock frequency of 400 MHz and the input setup time is 2ns. Flip-flops FF1 and FF2 have a setup time of 1ns, a hold time of 0ns, and a clock-to-output delay of 2ns. Ignoring the possibility of metastability, what is the maximum clock frequency of this circuit?

[2 marks]

e) The mean time between failures (MTBF) of a synchronising flip-flop is given by Equation 2.1:

$$MTBF = \frac{e^{t/\tau}}{T_a \times f \times a} \qquad (2.1)$$

where t is the maximum duration over which metastability may persist from the time of the clock edge without causing errors, f is the frequency of the clock signal to the synchronizing flip-flop, a is the transition rate of the asynchronous input, and $T_a = 2\times10^{-11}$ s and $\tau = 0.05$ns for these flip-flops.

Using the maximum clock frequency determined in d), and assuming that the asynchronous transition rate is 50MHz, determine the MTBF of FF1.

[6 marks]

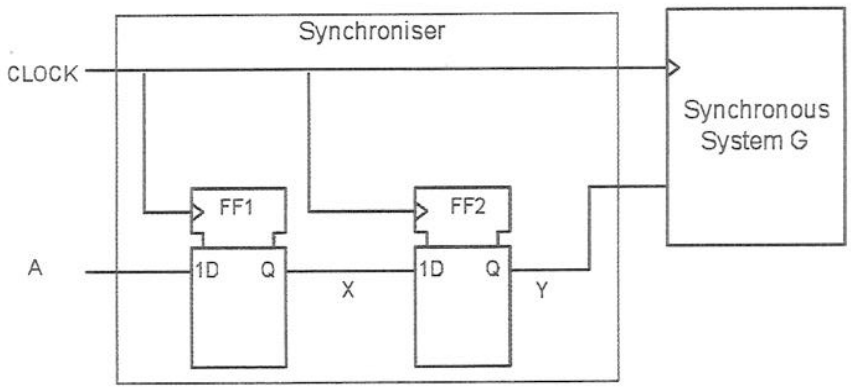

Figure 2.1

3. Figure 3.1 shows the schematic of a 5-input, 4-output finite state machine (FSM) implemented using a 4k bit memory block (M4K) in Altera's Cyclone II FPGA. The input `IN4:0` to the FSM is one-hot encoded. The M4K is configured as a 512 x 8 ROM with registered address inputs. The contents of some of the ROM locations are shown in Figure 3.2. All the other locations contain the value 0.

   a) Draw a state transition diagram for this FSM.

   [8 marks]

   b) A Logic Element (LE) in Altera's Cyclone II device consists of a 4-input lookup table and a flip-flop. Re-implement the FSM with logic elements (LEs) instead of a memory block using one-hot state encoding. How many LEs are required to implement your FSM?

   [12 marks]

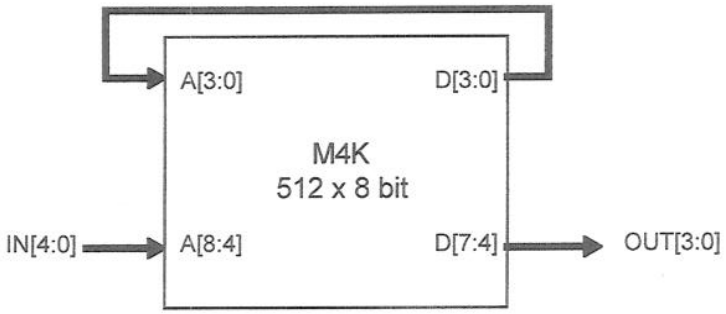

Figure 3.1

FSM inputs A[8:4]	A[3:0]	FSM outputs D[7:4] (hex)	D[3:0]
1	0	3	1
2	0	3	2
4	0	3	3
8	1	5	0
4	1	5	5
1	2	A	1
4	2	A	5
1	3	C	1
8	3	C	4
1	4	F	5
4	4	F	3
1	5	4	3
2	5	4	0
16	5	4	1

Figure 3.2

4. a) Figure 4.1 shows a parallel implementation of an n-stage CORDIC processor. Hence or otherwise, derive the iterative equations of the rotation mode CORDIC algorithm implemented by the circuit shown.

[6 marks]

b) Rotation of a 2-dimensional vector with coordinate (x,y) counter-clockwise by $\theta°$ to (x',y') is achieved by applying equation 4.1:

$$\begin{bmatrix} x' \\ y' \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix} \qquad (4.1)$$

Explain how the CORDIC algorithm can be used to perform such rotation operation.

[8 marks]

c) The CORDIC processor shown in Figure 4.1 is implemented on an Altera Cyclone II FPGA with estimated worst-case delay through the LUT of 0.5ns, a flip-flop setup time of 0.5ns and a clock-to-Q output delay of 1ns. Estimate with reasons the highest frequency at which this processor will operate correctly if all datapaths are 16 bit wide and the CORDIC processor performs 10 iterations. How can this design be speeded up? Estimate the highest operating frequency possible after the speedup.

[6 marks]

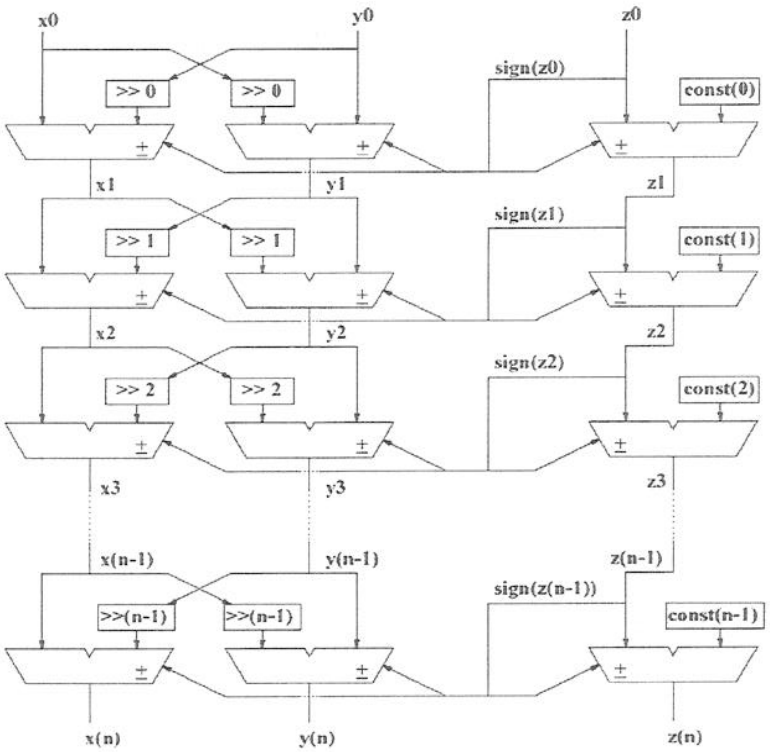

Figure 4.1

5. For this question, assume that the following timing specification applies:

Propagation delay of all combinatorial gates	t_p	2 ns
Setup time for D flipflop	t_{su}	1 ns
Hold time for D flipflop	t_h	0 ns
Clock to output delay for D flipflop	t_{cq}	3.5 ns

a) Figure 5.1 shows a simple clocked circuit. Draw the waveforms for the signals P, Q, X and Y over 5 clock cycles indicating the time at all signal transitions.

[7 marks]

b) What function does this circuit perform? What is the maximum clock frequency below which the circuit operates correctly?

[5 marks]

c) Figure 5.2 shows a clock generation circuit. Assuming that CIN is a symmetric clock signal, draw the timing waveform for the output signals A and B. What is the relationship between B and CIN? What is the maximum frequency of CIN for this circuit to work correctly?

[8 marks]

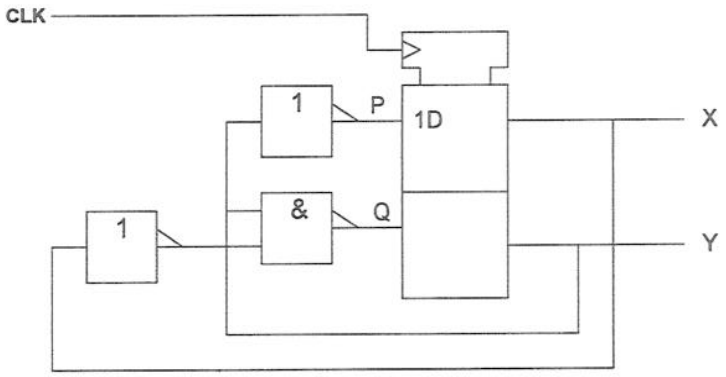

Figure 5.1

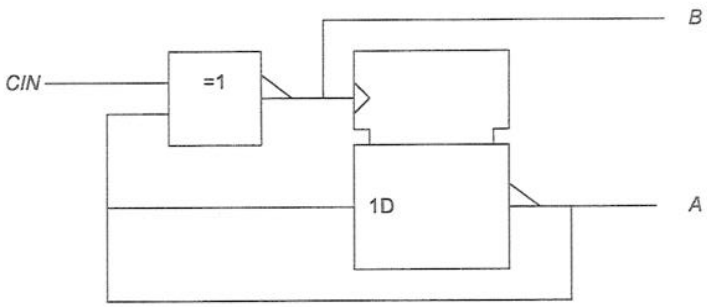

Figure 5.2

6. The correlation between two 64 × 64 pixel images X and Y can be estimated using sum-of-square differences as defined by the following equation:

$$C = \sum_{j=0}^{63} \sum_{i=0}^{63} \left(x_{ij} - y_{ij}\right)^2 \tag{6.1}$$

where x_{ij} and y_{ij} are the 8-bit unsigned intensity value of the pixel at row i and column j of X and Y respectively.

The correlator is to be implemented on an Altera Cyclone II FPGA which contains Logic Elements (LEs), each consisting of a 4-input Lookup Table (LUT) and a register. The FPGA also contains 4k-bit block RAMs (M4K) which can be configured according to Figure 6.1. Furthermore, the M4K blocks are synchronous dual-port memories.

a) Assuming that X and Y are already stored in memory, design a digital circuit to evaluate the correlation as defined by *Equation 6.1*. The circuit should perform the computation one pixel at a time. Your design should show all the building blocks such as memories, adders, counters and multiplexers relating to the datapath. There is no need to show any control circuitry. Do not show the detailed gate level circuit.

[12 marks]

b) Estimate the number of LEs and block RAMs needed to implement your design and the number of clock cycles required to complete the computation for each image frame.

[4 marks]

c) A parallel implementation using 64 computation units is to be employed so that one entire row can be processed in a single clock cycle. Explain how you may use the block RAM ~~efficient~~ to implement such as design.

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[4 marks]

Feature	M4K Blocks
Maximum performance *(1)*	250 MHz
Total RAM bits (including parity bits)	4,608
Configurations	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36

Figure 6.1

[END]

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IMPERIAL COLLEGE OF SCIENCE TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

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M.Eng., B.Eng., B.Sc(Eng.) and A.C.G.I. EXAMINATIONS 2009

PART III and PART IV

DIGITAL SYSTEM DESIGN

SOLUTIONS 2009

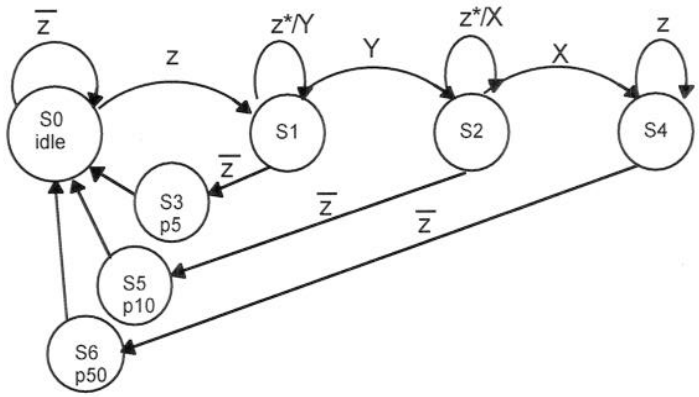
First Marker: *Peter Y. K. Cheung*

Second Marker: *Thomas Clarke*

Answer to Question 1

This question tests students' ability to design a reasonably complex FSM.

(a)



[6 marks]

(b)

Current State	X	Y	Z	Next State	p50	p10	p5
0	x	x	0	0	0	0	0
0	x	x	1	1	0	0	0
1	x	x	0	3	0	0	0
1	x	1	x	2	0	0	0
1	x	0	1	1	0	0	0
2	x	x	0	5	0	0	0
2	1	x	x	4	0	0	0
2	0	x	1	2	0	0	0
3	x	x	x	0	0	0	1
4	x	x	0	6	0	0	0
4	x	x	1	4	0	0	0
5	x	x	x	0	0	1	0
6	x	x	x	0	1	0	0

[6 marks]

(c)

N0 = S0*/Z + S3 + S5 + S6
N1 = S0*Z + S1*/Y*Z
N2 = S1*Y + S2*/X*Z
N3 = S1*/Z
N4 = S2*X + S4*Z
N5 = S2*/Z
N6 = N4*/Z
p5 = S3
p10 = S5
p50 = S6

Total 9 LEs (N0 and N2 require 2 LEs, N1, N3-N6 require 1 LE each, p5-p50 are free!)

[8 marks]

Answer to Question 2

This question tests students on a variety of issues relating to practical digital system design.

a) (Book work)

Cause of ground bounce:

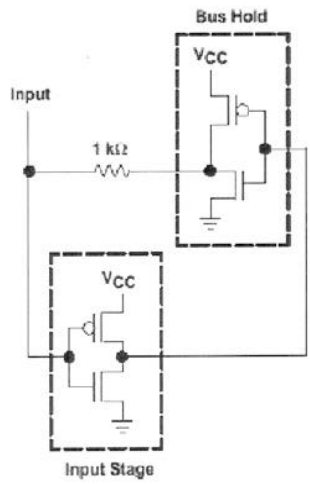
- Ground Bounce is a voltage oscillation between the ground pin on a component package and the ground reference level on the component die.
- Ground Bounce is one of the primary causes of false switching in high speed components and is a major cause of poor signal quality.
- It is caused by a current surge passing through the lead inductance of the package.
- The effect is most pronounced when all outputs switch simultaneously, (hence the alternate name, Simultaneous Switching Noise).
- While the inductance is the combined effect of the package lead, the package lead frame, the bond wire and the inductance in the die pad, most of the inductance is caused by the bond wire.

Ground Bounce effect can be reduced by:

1. Using all Vcc/Gnd pins available
2. Avoid pullup/pulldown resistors (i.e. use bus hold circuit)
3. Possibly use series damping resistors
4. Control output slew rate
5. Extra care in holding clock signals to solid voltage level (Vh) and fast clock transistions

[4 marks]

b) (Book work)
The schematic for a bus-hold circuit is:



- Bus-hold circuits are used to help solve the floating-input problem and eliminate the need for pullup and pulldown resistors.
- Bus-hold circuits consist of two back-to-back inverters with the output fed back to the input through a resistor.
- To understand how the bus-hold circuit operates, assume that an active driver has switched the line to a high level. This results in no current flowing through the feedback circuit.
- Now, the driver goes to the high-impedance state and the bus-hold circuit holds the high level through the feedback resistor.
- The current requirement of the bus-hold circuit is determined only by the leakage current of the circuit.
- The same condition applies when the bus is in the low state and then goes inactive.

c) When an output of digital circuit is in metastable state, the logic level in undefined and the time for this signal to exit metastable state and acquire either a logic '0' or '1' level is also not known.

Metastability can occur whenever a signal is sampled in a clock domain that is asynchronous to it. It occurs when the transition of this asynchronous signal violate the setup and/or hold time of the flip-flop in the new clock domain.

[4 marks]

d) Synchroniser imposes a maximum of clock period of (2 + 1) ns. Therefore maximum clock frequency is 333MHz, which is lower than maximum frequency that G can operate in.

[2 marks]

e) Since the synchronizer is operating at 250MHz, the available time for metastability to settle is (tperiod - tsetup) ns = 2 ns. For FF1:

$$\text{MTBF (2ns)} = \exp(2/0.05) / (2\text{x}10^{-11} \text{ x } 250 \text{ x } 10^{6} \text{ x } 5 \text{ x } 10^{7})$$
$$= 0.94 \text{ x } 10^{12} \text{ sec.}$$

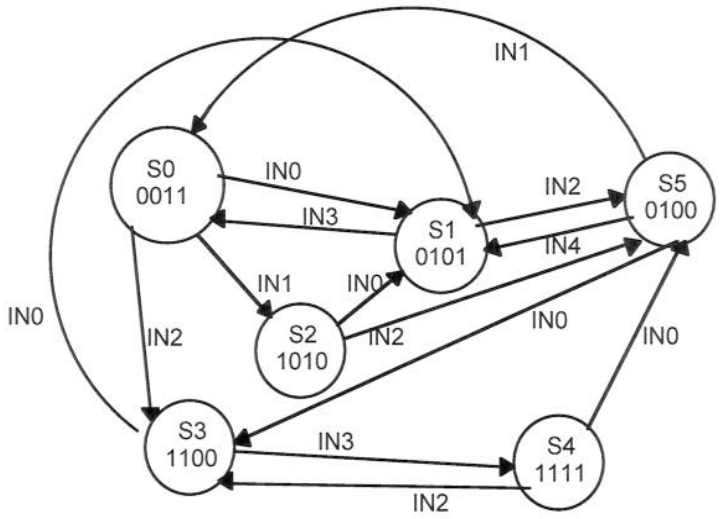
[4 marks]

Adding FF2 provides an additional window over which the signal has a chance to settle. However, the probability of FF2 going into metastability is much harder to calculate because its input X is no longer asynchronous. If the MTBF of FF2 is MTBF2, the overall probability of failure is the product of the two.

[2 marks]

Answer to Question 3

a) This tests student's ability to understand a FSM implemented using block RAM on an FPGA.



[8 marks]

b)

N0 = S1*IN3+S5*IN1	(1 LE)
N1 = S0*IN1 + S2*IN0 + S5*IN4 + S3*IN0	(2 LEs)
N2 = S0*IN1	(1 LE)
N3 = S0*IN2 + S3*IN2 + S5*IN0	(2 LEs)
N4 = S3*IN3	(1 LE)
N5 = S1*IN2 + S4*IN0	(1 LE)
OUT0 = S0 +S1 + S4	(1 LE)
OUT1 = S0 + S2 + S4	(1 LE)
OUT2 = S1 +S3 + S4 +S5	(1 LE)
OUT3 = S2 + S3 + S4	(1 LE)

[12 marks]

Therefore 12 LEs required in total.

Answer to Question 4

Students have designed a CORDIC processor as the course work for this course. This question tests their ability to apply what they have learned in this course work under examination conditions.

(a) From the circuit diagram, and from book work,

Given:
$$x_{i+1} = x_i - y_i \tan\alpha_i$$
$$y_{i+1} = y_i + x_i \tan\alpha_i$$
$$z_{i+1} = z_i - \alpha_i$$

Let:
$$\alpha_i = \tan^{-1} 2^{-i}$$
$$\tan\alpha_i = 2^{-i}$$

This the iterative equation:
$$x_{i+1} = x_i - d_i\, y_i 2^{-i}$$
$$y_{i+1} = y_i + d_i\, x_i 2^{-i}$$
$$z_{i+1} = z_i - d_i\, \alpha_i$$

where
$$d_i \in \{-1, 1\}$$
as determined by some criterion

[6 marks]

(b) In order to implement this affine transformation, we need to compute sin θ and cos θ, and then perform 4 sum of products.

For rotation mode to compute sin θ and cos θ, we need to perform the following using CORDIC:

1. Set $z = \alpha$
2. $x = 1/K = 0.607252935$ (or some scaling constant)
3. $y = 0$
4. Iterate with $d_i = \text{sign}(z_i)$

After m rotations, we get

$$x_m \approx \cos(z)$$
$$y_m \approx \sin(z)$$
$$z_m \approx 0$$
$$y / x \approx \tan(z)$$

[8 marks]

(c)

Figure 4.1 shows a non-pipelined version. Delay through each stage is 16 x 0.5ns = 8ns. Note that the shifters is by a fixed amount and therefore incurs no delay (except wiring delay). Therefore 10 stages will incur 80ns delay. Assuming that the input is supplied through a synchronous register, and the output is also registered, the worst-case timing will be
(80 ns + setup + clock-to-Q) = 81.5ns. Therefore the operating frequency is 12.27MHz.

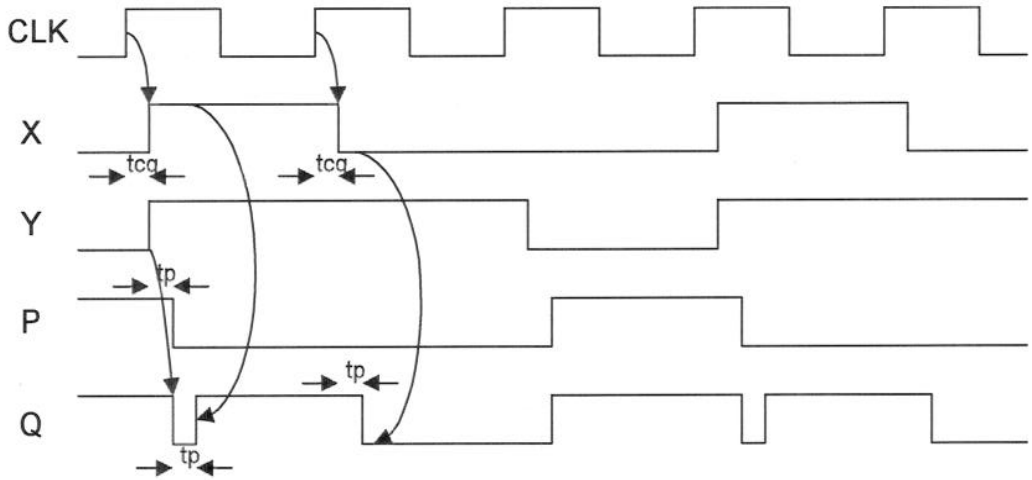
Pipeline registers can be added at outputs of all adders/subtractors. In which case, the worst-case delay is 8 + 0.5 + 1 = 9.5ns. The operating frequency is now 105.3MHz.

[6 marks]

Answer to Question 5

This question tests students' ability to handle timing in digital circuits.

a)



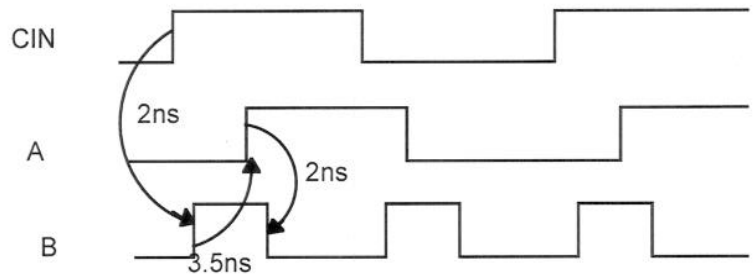
[7 marks]

b) This is a 1/3 and 2/3 divider circuit.

Tperiod ≥ Tcq + Tsu + 2* Tp ≥ 8.5 ns.

[5 marks]

c)



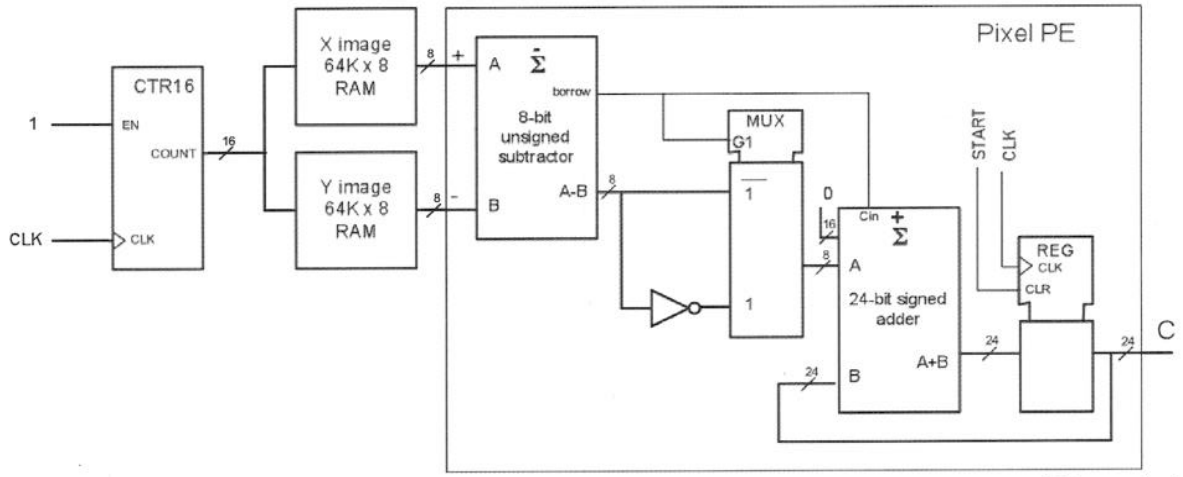
This is a clock frequency doubler. Maximum period of CIN is

2*(2*tp + tcq) = 2*7.5 = 15ns. Therefore maximum frequency is 66.7MHz.

[8 marks]

Answer to Question 6

a)



[12 marks]

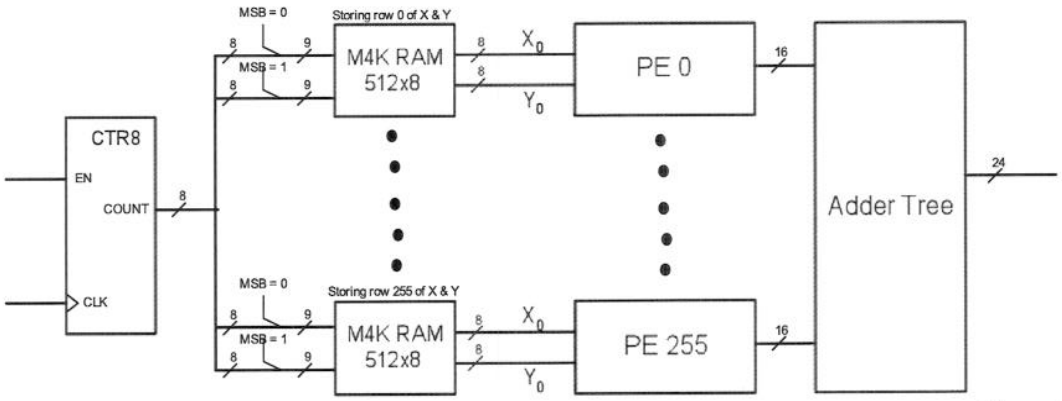
b)

Block	LE	Block
Counter	16	-
Image memory	-	2 x M-RAM
Subtractor	8	-
MUX + inv	8	-
Adder + Reg	24	-
Total	56	2 x M-RAM

Requires 64^2 clock cycles.

[4 marks]

c) Best solution is to use 256 M4K RAM organised as 256 x 16 , each storing one row of X and Y. Using the dual-port feature of M4K Block RAM, and by setting MSB of X and Y addresses to be 0 and 1 respectively, both images can be accessed simultaneously without conflict. Design is now (not required for full marks).



[4 marks]

[END]