IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2009

Corrected Copy

**FACTS AND POWER ELECTRONICS**

Wednesday, 6 May 10:00 am

Time allowed: 3:00 hours

**There are SIX questions on this paper.**

**Answer FOUR questions.**

*All questions carry equal marks.*

*Please use a separate answer book for Sections A and B.*

**Any special instructions for invigilators and information for candidates are on page 1.**

| | | |
|---|---|---|
| Examiners responsible | First Marker(s) : | T.C. Green, B.C. Pal |
| | Second Marker(s) : | P.D. Mitcheson, T.C. Green |

# The Questions

## PART A

1.

(a) Describe Optimal PWM and explain why it is useful when the switching frequency of an inverter is relatively low. [5]

(b) Explain how multi-level converters achieve low distortion AC voltages without high switching frequency. Choose one example of a multi-level circuit and explain its operation. [10]

(c) Multi-pulse circuits are an alternative to multi-level circuits. Compare and contrast the two approaches. [5]

2.

(a)

(i) Draw a diagram of a thyristor structure and with the use of a suitable equivalent circuit model explain why, under certain circumstances, the device is able to latch into an *on state* when the gate current is removed.

[5]

(ii) Derive a simple expression for the condition that ensures that the device latches on once the gate current is removed.

[3]

(b)

(i) Explain the problems associated with connecting thyristors in series to construct a valve capable of blocking a higher voltage than an individual device.

[2]

(ii) Explain the problems associated with paralleling thyristors in order to make a valve with a greater current rating than an individual device.

[2]

(iii) You are required to design a thyristor valve for use in a power converter connected to a distribution network. The application requires that the valve must be capable of blocking 11 kV peak and conducting 100 A.

You should use a thyristor with the following specification:

120 A max cathode current,

Maximum blocking voltage of 1010 V,

Leakage current of between 1 mA and 3 mA when in the off-state,

Reverse recovery charge guaranteed between 10 nC and 30 nC.

Design a suitable valve capable of working in both DC and transient conditions using the minimum number of devices possible. Draw a circuit diagram and show calculations for the component values.

[5]

(iv) If the valve is over-rated by adding 1 additional device, by what fraction does the power consumption of the valve decrease in the blocking state?

[3]

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3.

(a) The transform matrices in equations Q3.1 and Q3.2 are used to transform three-phase variables to the αβγ form and then to dqγ form. Explain the properties of the matrices and the usefulness of the transformations obtained.

[4]

$$[T]=\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad \text{(Equation Q3.1)}$$

$$[T_R]=\begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 0 \\ -\sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad \text{(Equation Q3.2)}$$

(b) For the circuit in Figure Q3.1 (overleaf),

(i) write the circuit equations in matrix form,

[4]

(ii) write the circuit equations once transformed into *dqγ* form,

[4]

(iii) sketch the equivalent circuit of the transformed system.

[4]

(c) Figure Q3.2 (overleaf) shows a PV array and DC/DC power converter feeding a DC-link and a DC/AC converter interfaced to a grid. Briefly describe the elements of the control system for the grid-side converter in terms of the reference signals, feedback signals and the format of the control loops.

[4]

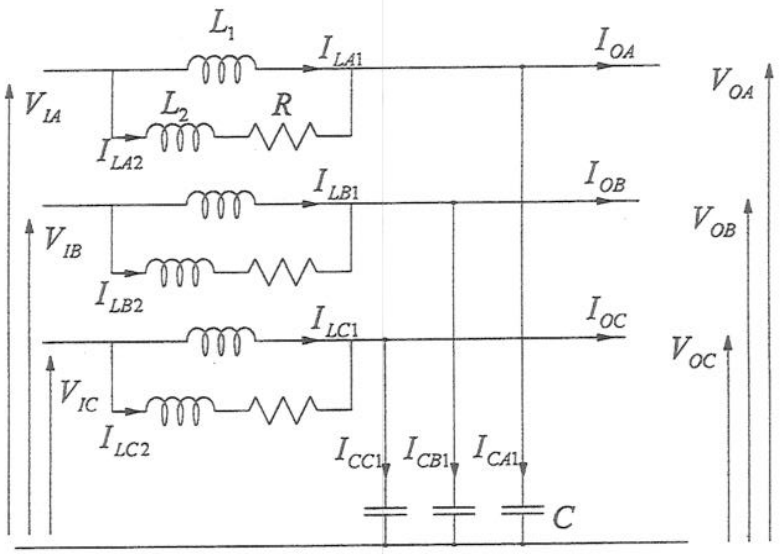


Figure Q3.1

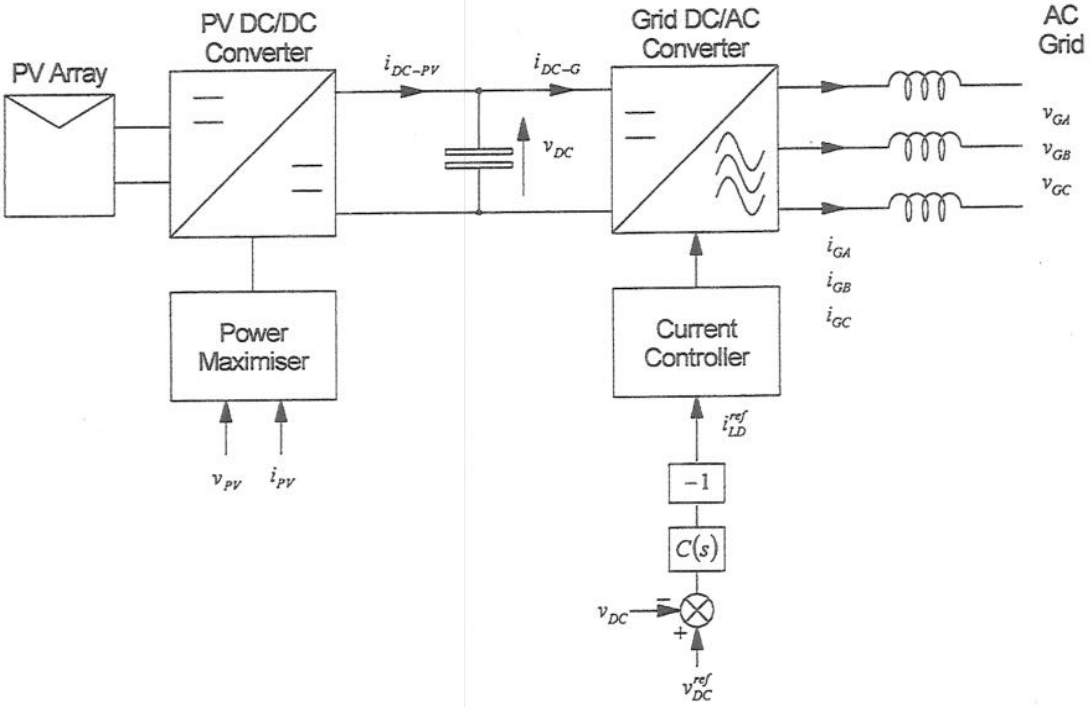


Figure Q3.2

## PART B

4.

a) Discuss the factors that may limit power transmission in AC networks.

[5]

b)

i) What is surge impedance loading (SIL) of a lossless line?

[5]

ii) Explain how it is possible to load a very long line, for instance a 500 mile long, 400 kV line, beyond its surge impedance loading.

[2]

c) What are the structural and functional differences between a Thyristor Control Series Capacitor (TCSC) and a Static Series Synchronous Compensator (SSSC)?

[5]

d) List the various technical benefits of converter-based FACTS controllers over thyristor-based FACTS controllers.

[3]

5

a) What are the operational benefits of series compensation? [4]

b) Figure Q5.1 shows a simple model of an interconnected power system. The voltages at the two end are $V_s\angle\delta$ and $V_r\angle 0$ p.u. The line is modelled by a series inductance expressed as $X_L$ p.u.

i) Derive expressions for real and reactive power flow in the line. [6]

ii) The line is now equipped with a series capacitor of variable capacitive reactance $X_c = kX_L$ where $k$ is controllable. Sketch the variation of power with $\delta$ for k = 0.0, 0.2 and 0.4. With the help of the sketch justify the influence of the series capacitor in transmission power flow control. [10]

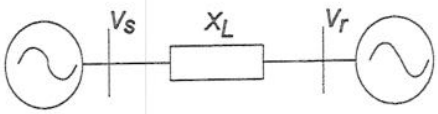


Figure Q5.1: A simple interconnected power system model

6.

a)

i) Discuss the operating principle of a Static VAr Compensator (SVC) employing a thyristor switched capacitor (TSC) topology and an SVC employing a thyristor controlled reactor (TCR) topology.

[5]

ii) Plot the V-I characteristic of a combined TSC and TCR topology.

[3]

b)

i) Sketch the basic scheme of a unified power flow controller (UPFC) and label the major building blocks.

[5]

ii) Show how the functionalities of series, shunt and phase compensation are realised by this device.

[7]

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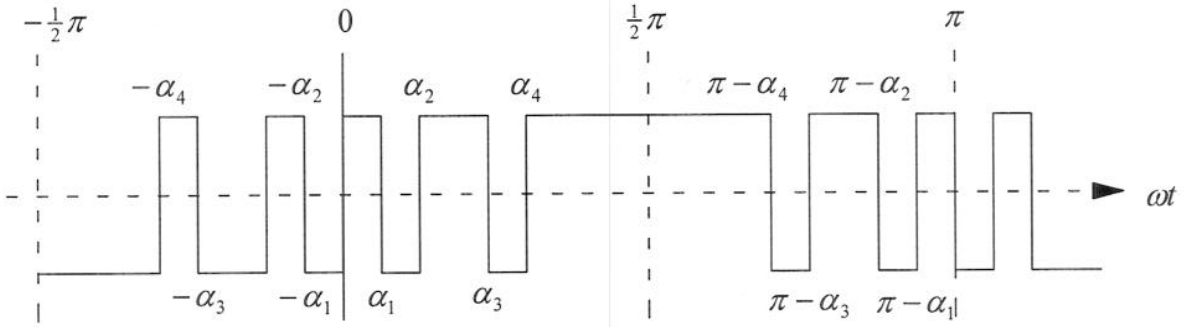
1.

(a) Describe Optimal PWM and explain why it is useful when the switching frequency of an inverter is relatively low. [5]

*[Bookwork]*
*In cases where the switching frequency is limit, the number of on- and off-commutations per cycle of the modulating wave is low. A problem with this is that without synchronisation, sub-harmonics may be generated. An opportunity is that (once synchronised) the small number of commutation times can be chosen (optimised) to improve the spectrum. Assuming we have a three-wire three-phase system, triplen harmonics do not contributed to distortion in the load and can be left uncontrolled while attempts are made to reduce non-triplen harmonics. The figure shows the angles available for optimisation assuming quarter-wave symmetry (which sets all even harmonics to zero)*



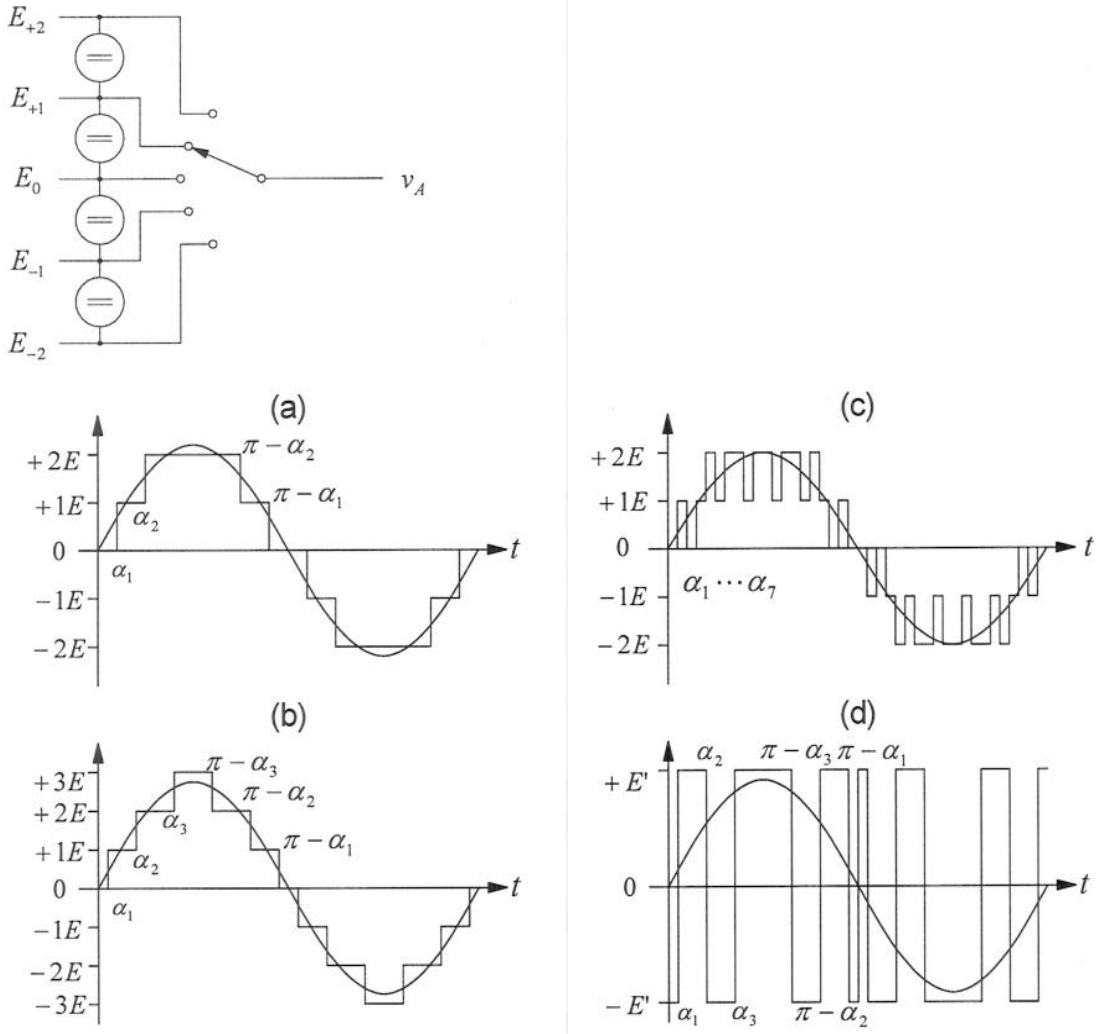

*The objective is to chose the angles to set terms in the Fourier series to zero. This has to be done through numerical optimisation off-line and stored for use in real-time.*

$$V_{n=odd}=\frac{4}{\pi}\left\{\begin{array}{l}\int_0^{\alpha_1}\frac{1}{2}V_{DC}\sin(n\omega t).d(\omega t)+\int_{\alpha_1}^{\alpha_2}\frac{-1}{2}V_{DC}\sin(n\omega t).d(\omega t)+\int_{\alpha_2}^{\alpha_3}\frac{1}{2}V_{DC}\sin(n\omega t).d(\omega t)\\ +\int_{\alpha_3}^{\alpha_4}\frac{-1}{2}V_{DC}\sin(n\omega t).d(\omega t)+\int_{\alpha_4}^{\pi}\frac{1}{2}V_{DC}\sin(n\omega t).d(\omega t)\end{array}\right\}$$

$$V_{n=odd}=\frac{4}{\pi}V_{DC}\left\{1-\cos(n\alpha_1)+\cos(n\alpha_2)-\cos(n\alpha_3)+\cos(n\alpha_4)\right\}$$

(b) Explain how multi-level converters achieve low distortion AC voltages without high switching frequency. Chose one example multi-level circuit and explain its operation. [10]

*[Bookwork]*
*Multi-level converters use a switch array to connect the output terminal to a series of different voltage sources such that a staircase waveform is created.*




*It is possible to add pulse-width modulation between adjacent voltage levels to achieve a further improvement in output voltage spectrum.*

*Three main classes of multi-level circuit exist any can be chosen to illustrate the detail. For the chosen circuit the question requires:*

- *A sketch of the circuit*
- *An illustration of one or more switch states for achieving a given output voltage level.*
- *A discussion of whether redundant states exist*
- *A discussion of any constraints on operation or additional control challenges such as a need to balance capacitor charge flows.*

(c) Multi-pulse circuits are an alternative to multi-level circuits. Compare and contrast the two approaches. [5]

*[Bookwork: interpretation of material]*
*Discussion should include the following points:*

- *In essence, there is no difference between the two approaches in terms of the converter power rating achieved as a function of number of switch devices employed. With a large number of*

*devices there is a small advantage for the multi-pulse type in allowing a slightly higher voltage magnitude from the quasi-square-wave employed in each 6-pulse element.*

- *Multi-pulse inverters based on 2-level 6-pulse units do not give voltage magnitude control so some additional commutation or a 3-level base unit is needed.*
- *Multi-pulse converters eliminate pairs of harmonics around certain multiples $6^{th}$ harmonic throughout the spectrum. The multi-level converters eliminate only low order harmonics. In terms of total harmonic distortion, the multi-pulse system has some advantage. Because the advantage is in terms of high order harmonics, a relatively small filter can achieve similar results for multi-level converters.*
- *Multi-pulse circuits need line-frequency transformers to isolate the converters and to provide phase shifting. The phase-shift transformers get increasing complex as the number of pulses rises.*
- *Multi-level converters also scale poorly (n2 diodes for diode-clamped or n2 capacitors flying capacitor). The cascade cell converter does scale well but requires transformer isolated DC-links for real power transfer.*

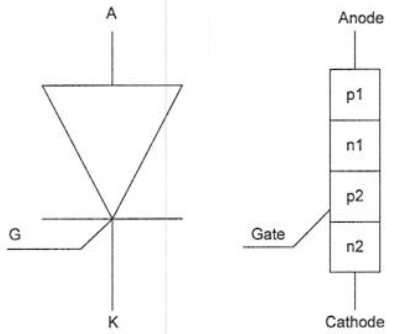
2.

(a)

(i) Draw a diagram of a thyristor structure and with the use of a suitable equivalent circuit model explain why, under certain circumstances, the device is able to latch into an on state when gate current is removed.

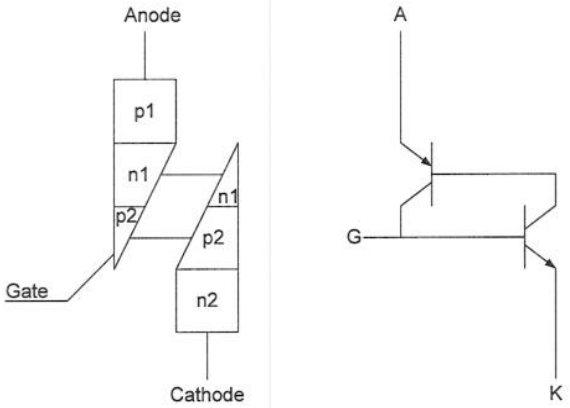
[5]

*[bookwork]*
*The thyristor is a 4 layer pnpn structure as shown below:*




*[1]*

*For analysis, the thyristor can be thought of as two cross connected BJTs, as shown below.*




*[2]*

*The circuit is able to latch into an on-state because the when both BJTs are turned on, the collector current of the pnp device supplies the base of the npn device and the collector current of the npn supplies base current for the pnp.*

*[2]*

(ii) Derive a simple expression for the condition that, on removal of gate current, the device latches on.

[3]

*[mostly bookwork, but easy enough to derive from scratch]*
*Naming the npn transistor as Q1 and the pnp as Q2, we require that there is enough gain in the loop that the base current in 1 transistor can cause enough collector current in the other, so that that collector current can sustain the original base current. More specifically we require:that the*

*base current in Q1 causes enough current to flow in the collector of Q2 to drive the base current in Q1.*

*Mathematically, we can write this as:*

$$\beta_1 I_{B1} \beta_2 > I_{B1}$$

*Thus for latching) we require the product of the betas to be greater than 1, i.e.:*

$$\beta_1 \beta_2 > 1$$

*(Also allow the answer that the sum of the alphas must be 1 or more)*

*[3]*

(b)

(i) Explain the problems associated with stacking thyristors in series to construct a valve capable of blocking more voltage than an individual device.

[2]

*[bookwork]*
*When thyristors are placed in series, they are forced to share the same current. Any mismatch between the reverse saturation currents (due to manufacturing, or differences in operating temp) will cause the device with the smallest leakage current to take more than its share of the blocked voltage. This can cause it to latch into the on state, at which point it supports no voltage. This leads to a cascading failure of the valve.[2]*

(ii) Explain the problems associated with paralleling thyristors in order to make a valve with a greater current rating than an individual device

[2]

*[bookwork]*
*When devices are placed in parallel, they are forced to share the same voltage. Thus, the device with the lowest resistance will conduce the most current and thermal runaway may occur, resulting in a cascade failure of the valve. [2]*

(iii) You are required to design a thyristor valve for use in a multilevel converter connected to the distribution system. The application requires that the valve must be capable of blocking 11 kV peak and conducting 100 A.

You should use a thyristor with the following specification:

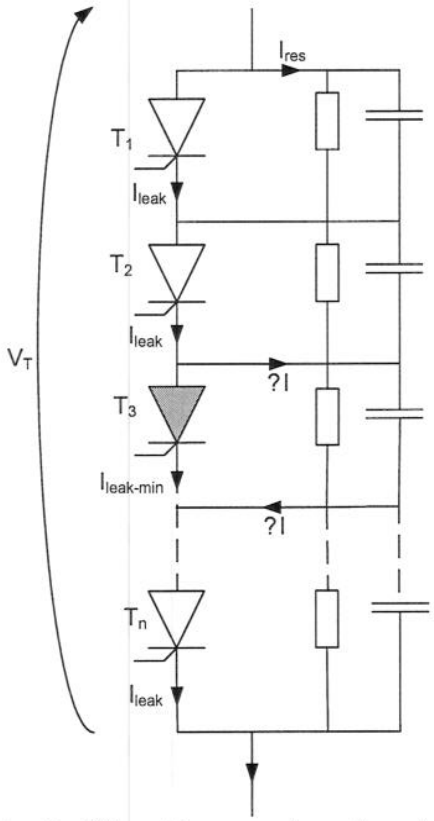
120 A max cathode current,
Maximum blocking voltage of 1010 V,
Leakage current of between 1 mA and 3 mA when in the off-state,
Reverse recovery charge guaranteed between 10 nC and 30 nC

Design a suitable valve capable of working in both DC and transient conditions using the minimum number of devices possible. Draw a circuit diagram and show calculations for the component values.

[5]

*[calculation]*
*The valve must be capable of blocking 11000 V, which requires a minimum of 10.8, i.e. 11 devices.*

*The circuit should look this:*




*The resistors ensure good voltage sharing for DC and the capacitors allow sharing for transients.*

*the resistor value can be calculated as the worst case (10 devices with the largest leakage and 1 with the lowest leakage) as:*

$$\therefore R = \frac{nV_{BD} - V_T}{(n-1)\Delta I}$$

*Which gives R=(11*1010-11000)/(10*2m)=5.5 kΩ*

*The capacitor can be sized in a similar way as:*

$$C = \frac{(n-1)\Delta Q}{nV_{BD} - V_S}$$

*Which gives C=10*20e-9/(11*1010 - 11000) =98nF*

(iv) If the valve is overrated by adding 1 additional device, by what faction does the static power consumption of the valve decrease in the blocking state?

[3]

*[calculation]*
*The new value of parallel resistor is:*

*$R=(12*1010-11000)/(11*2m)=50.9\ k\Omega$ [2]*

*Therefore the power consumption decreases to 5.5/50.9 = 0.108 of the original value [1]*

3.

(a) The transform matrices in equations Q3.1 and Q3.2 are used to transform three-phase variables to the αβγ form and then to the dqγ. Explain the properties of the matrices and the usefulness of the transformations obtained. [4]

$$[T]=\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad \text{(Equation Q3.1)}$$

$$[T_R]=\begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 0 \\ -\sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad \text{(Equation Q3.2)}$$

*[bookwork: interpretation of notes]*
*T separates zero-sequence components into the γ-term leaving only positive and negative sequence components in the αβ-terms. Balanced three phase sets are transformed into an equivalent two-phase set in αβ. The transform is produces orthogonal terms in order that power can be separately calculated for each term and the transform is power invariant since $T^T = T^{-1}$*

*$T_R$ does not transform the γ-term. A reverse rotation is applied to the the αβ-terms that transforms a positive sequence set to a station set in dq. The dq terms represent the amplitude and phase of the original three-phase set.*

(b) For the circuit in figure Q3.1 (overleaf),
(i) write the circuit equations in matrix form [4]
(ii) transform the equations to *dqγ* form [4]
(iii) sketch the circuit of the transformed system [4]

*[Application of analysis technique]*
*(i) First use Kirchoff's laws to write equations for each phase then assemble into matrix form with the parameter matrices defined as shown.*

$$v_{1abc} = \mathbf{L_1}\frac{di_{1abc}}{dt} + v_{Oabc}$$

$$\text{where } \mathbf{L_1} = \begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_1 & 0 \\ 0 & 0 & L_1 \end{bmatrix}$$

$$v_{1abc} = \mathbf{L_2}\frac{di_{2abc}}{dt} + \mathbf{R}i_{2abc} + v_{Oabc}$$

$$\text{where } \mathbf{L_2} = \begin{bmatrix} L_2 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & L_2 \end{bmatrix} \text{ and } \mathbf{R} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix}$$

$$i_{1abc} + i_{2abc} = \mathbf{C}\frac{dv_{2abc}}{dt} + i_{Oabc}$$

$$\text{where } \mathbf{C} = \begin{bmatrix} C & 0 & 0 \\ 0 & C & 0 \\ 0 & 0 & C \end{bmatrix}$$

*(ii) The two transforms leave the parameter matrices untouched (because they are scaled identity matrices) but transformation of derivative terms yields two terms in the normal way for reactive components. (Product rule applies since both currents and the transform matrix are time dependent where one term is the normal sinusoidal voltage term of an inductor which occurs in quadrature to the current (off diagonal terms cause d-axis voltage from q-axis current).)*

$$vI_{dq\gamma} = \mathbf{L_1}\frac{di_{1dq\gamma}}{dt} + \mathbf{X_{L1}}\,i_{1dq\gamma} + v_{Odq\gamma}$$

$$\text{where } \mathbf{X_{L1}} = \begin{bmatrix} 0 & -\omega L_1 & 0 \\ \omega L_1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix},$$

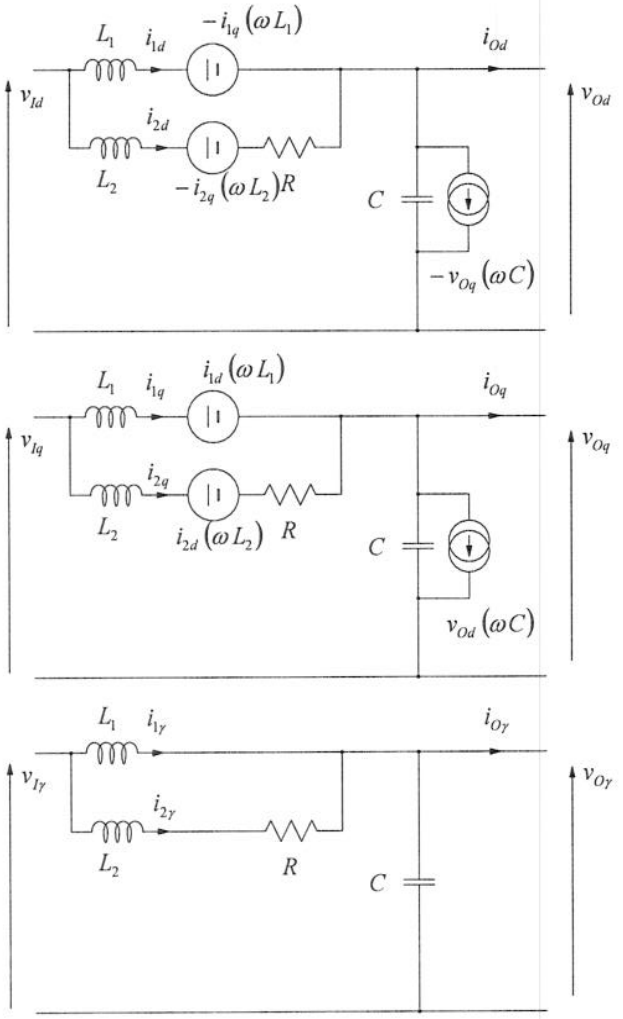
$$v_{1dq\gamma} = \mathbf{L_2}\frac{di_{2dq\gamma}}{dt} + \mathbf{X_{L2}}\,i_{2dq\gamma} + \mathbf{R}i_{2dq\gamma} + v_{Odq\gamma}$$

$$\text{where } \mathbf{X_{L2}} = \begin{bmatrix} 0 & -\omega L_2 & 0 \\ \omega L_2 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$i_{1dq\gamma} + i_{2dq\gamma} = \mathbf{C}\frac{dv_{2dq\gamma}}{dt} + \mathbf{B_C}\,v_{2dq\gamma} + i_{Odq\gamma}$$

$$\text{where } \mathbf{B_C} = \begin{bmatrix} 0 & -\omega C & 0 \\ \omega C & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

*(ii) The three rows of these equations can be separated out and equivalent circuits drawn. The D and Q axis circuit are coupled through the reactance terms.*




(c) Figure Q3.2 (overleaf) shows a PV array and DC/DC power converter feeding a DC-link and DC/AC converter interfaced to a grid. Briefly describe the elements of the control system for the gird-side converter in terms of the reference signals, feedback signals and the format of the control loops. [4]

*[Bookwork: summarising notes and interpretation]*
*The following points should be included in the discussion:*

- *The primary task is to export to the grid the power produced by the PV array. A convenient way to arrange this is to set a reference for the DC-link voltage and form a voltage error signal. A rise in DC-link voltage indicates a need to export more real power. A feed-forward term from the power point tracker of the DC/DC converter could be included.*
- *The voltage error (multiplied by a controller transfer function) will indicate the power set point for the grid-side converter. Dividing the power by the AC voltage magnitude will give a magnitude for the AC-side current.*
- *The exported current must be phase-aligned to the grid voltage and so a phase-locked loop is employed to find instantaneous the phase-angle of the grid voltage.*

- *For a three-phase system 9as illustrated), it would be convenient to establish current control loops in a DQ reference frame and use the angle from the PLL to perform ABC/DQ transformations.*

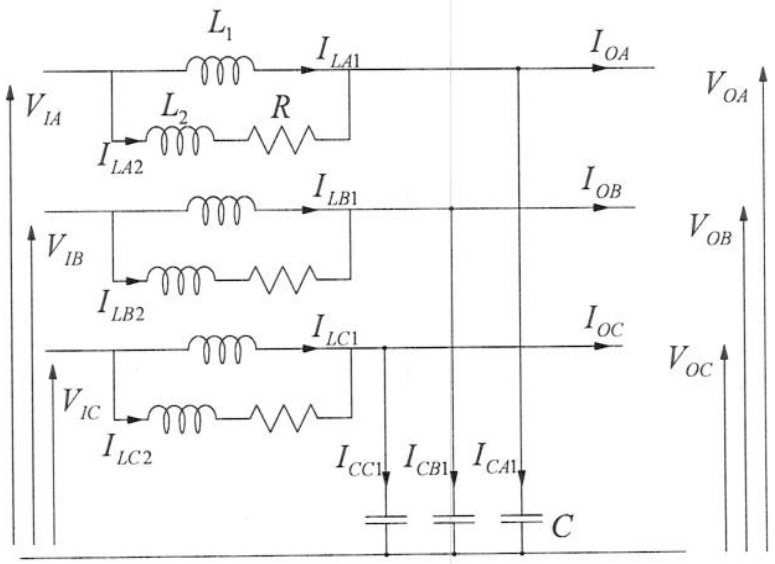



Figure Q3.1

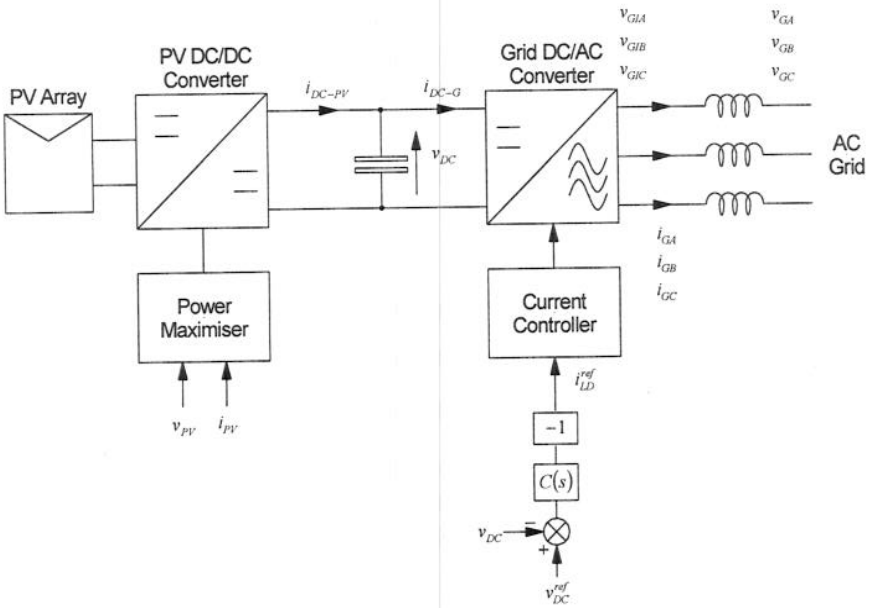



Figure Q3.2

## PART B

4.

*a)* *Discuss the basic limitations of AC power transmission*

[5]

The students are expected to highlight

- increased losses
- lower power transfer capacity because of voltage and angle stability reason
- loop flows in meshed network
- absence of control
- under and over voltage problems

b)

i) *What is surge impedance loading (SIL) of a lossless line?*

[5]

When a loss less line is terminated by its surge impedance, the loading is known as *surge* or *natural loading* and is expressed as:

$SIL = \frac{V_0^2}{Z_0}, V_s = V_r = V_0$ is the nominal or rated voltage of the line.

At the surge impedance loading:

Voltage and current remain constant in amplitude along the line

Voltage and current are in phase throughout the length of the line

The phase angle between the sending and the receiving end voltage is $\beta l$

This means the transmitted power is independent of the length of the line. At SIL, the reactive power absorbed by the series inductance is equal to the reactive power generated by the shunt capacitance of the line per unit length.

ii) *Explain how is it possible to load a 500 mile long, 400 kV line beyond its surge impedance loading?*

[2]

Reactive power compensation either in series or in shunt will be required. The function of the reactive power compensation is to match the balance of reactive power generation and absorption in line which is dependent on loading level.

c) *What are the structural and functional differences between a Thyristor Control Series Capacitor (TCSC) and a Static Series Synchronous Compensator (SSSC)?*

[5]

Structurally both of them are series devices but TCSC acts as a dependent current source or variable series reactance. The current through the line is controlled by the voltage impressed across it. The turn on time can be controlled not turn off time. This makes TCSC a slowly acting device. The amount of voltage to compensate drop in line reactance is dependent on current. The reactive power generated is proportional to the square of the current.

The SSSC on the other hand, employs voltage source converter where switching on and off are controlled. The response is faster than TCSC. The device behaves as an independent voltage source with a phase angle difference of 90 degree with line current. The amount of voltage across it is not dependant on loading. So from line drop compensation point of view this is good, but from reactive power generation point of view it is linearly proportional to current.

d) List various technical benefits of converter based FACTS controllers over thyristor based FACTS controllers.

[3]

The students must mention the following

- faster response
- better control range and control speed
- operational suitability at low voltage condition

5

a) *What are the operational benefits of series compensation?*

[4]

- Series compensation enhances the power transfer limit of the line
- This enables higher utilisation of line capacity, towards thermal limit
- Reduce transmission reinforcement
- Offers controllability to AC power transmission

b) Figure 5.1 shows a simple model of an interconnected power system. The voltages at the two end are $V_s\angle\delta$ and $V_r\angle 0$ p.u. The line is modelled by a series inductance and expressed as $X_L$ p.u.

i) Derive the expressions for real and reactive power flow in the line.

[6]

The sending and receiving end voltage are defined as:

$V_s = Ve^{j\delta}, V_r = Ve^{-j0}$

The current through the line is given by $I = \frac{V_s - V_r}{jX_L}$

The power is: $V_r I^* = P_r + jQ_r$

The expression for power

$$P_r = \frac{V_s V_r}{X_L} sin\delta;\ Q_r = \frac{{V_r}^2}{X_L} - \frac{V_s V_r}{X_L} cos\delta$$

It is interesting to note that real power flow cannot be changed without changing the demand on the reactive power in sending and receiving ends. The power flow can be controlled, by controlling voltage (V), reactance (X) and angle (δ). However, there are some operating restrictions on these variables beyond which, the power flow can not be controlled through these variables. We discuss these limitations later.

*ii) The line is now equipped with a series capacitor of variable capacitive reactance $X_c = kX_L$ where k is controllable. Sketch the variation of power with δ for k = 0.0, 0.2 and 0.4. With the help of the sketch justify the influence of the series capacitor in transmission power flow control*

*[10]*

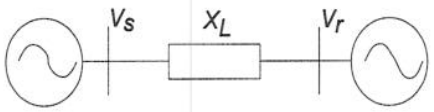



*Fig 5.1: A simple interconnected power system model*

The percentage of compensation is defined as $k$*100%, where $k$ is degree of compensation. The effective transmission reactance is given by

$$X_{eff} = X_L - X_c \; ; \; k = \frac{X_c}{X_L}$$

'$k$' is known as the degree of series compensation. The expression for power are given as:

$$P = \frac{V_s V_r}{(1-k)X_L} \sin\delta \, , Q_c = -\frac{V_r^2}{X_L}\frac{k}{(1-k)^2} + \frac{V_s V_r}{X_L}\frac{k}{(1-k)^2}\cos\delta$$

Consider a two machine power system as shown in Fig .1 with magnitude of volatge at both end equal The power angle equation is as follows:

$$P = \frac{V^2}{X_L(1-k)} Sin\delta; \; Q = \frac{2V^2}{X_L(1-k)^2}(1-cos\delta)$$

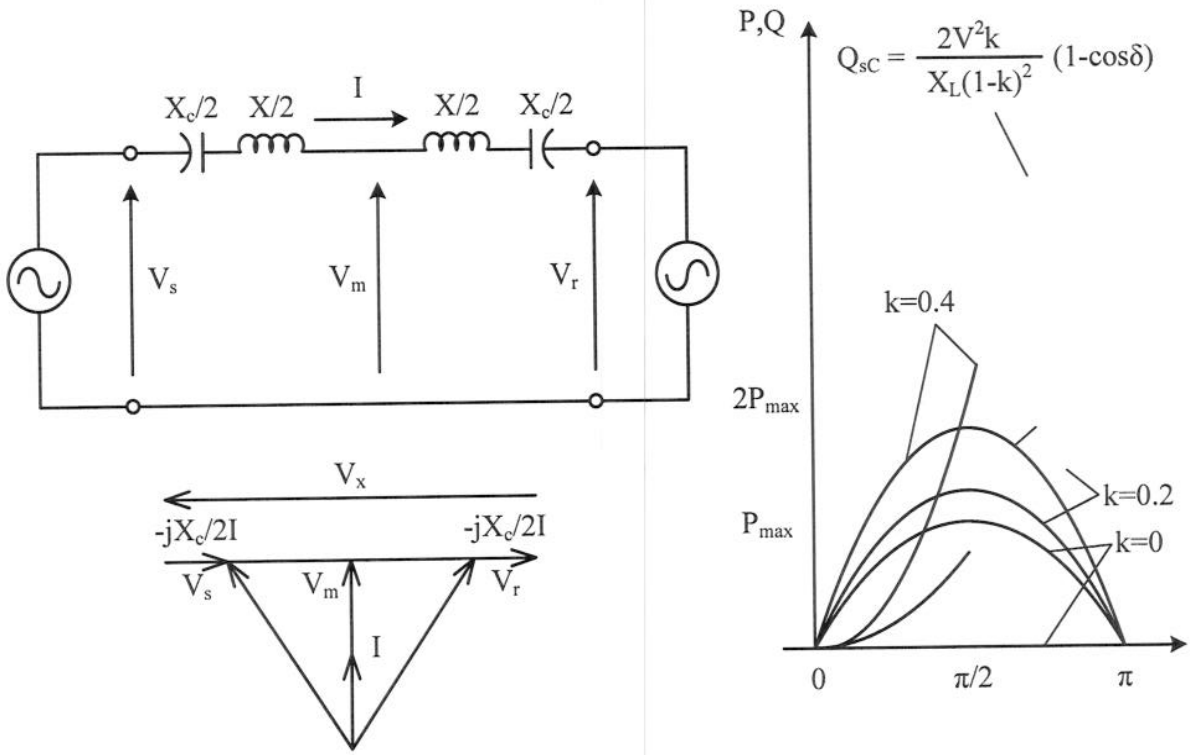



Fig .1 Power flow control through fixed capacitor

It is seen that the power transfer capacity is enhanced because of reduction effective line impedance. The power transfer capability increases with degree of compensation. The reactive power supplied by the capacitor to the system also rapidly increases with degree of compensation.

6.

a)

i) *Discuss the operating principle of an SVC employing a thyristor switched capacitor (TSC) topology and thyristor controlled reactor (TCR) topology.*

[5]

A basic single-phase TSC-TCR arrangement is shown in Fig. B.14. For a given capacitive output range, it typically consists of n TSC branches and one TCR. The number of branches, n, is determined by practical considerations that include the operating voltage level, maximum var output, current rating of thyristor valves etc. The inductive range can also be extended to any maximum rating by including more TCR branches. The operation of the basic TSC-TCR var generator can be described as follows:

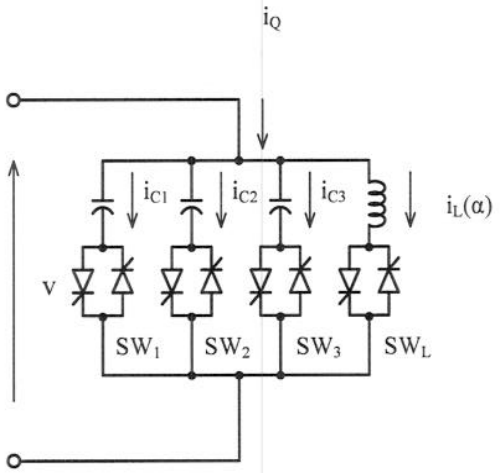



Fig A6.1:TSC+TCR topology

The total capacitive output range is divided into n intervals. In the first interval, the output of the var generator is controllable in the zero to $Q_{cmax}/n$ range, where $Q_{cmax}$ is the total rating provided by all TSC branches. In this interval, one capacitor bank is switched in by firing associated thyristor, and, simultaneously the current in the TCR is set by appropriate firing angle delay angle so that the sum of the var output of the TSC (negative) and that of the TCR (positive) equals the capacitive output required. In the subsequent intervals the output is controllable in the range $Q_{cmax}/n$ to $2Q_{cmax}/n$ , $2Q_{cmax}/n$ to $3Q_{cmax}/n$ and so on and using the TCR to absorb the surplus capacitive vars.

By being able to switch the capacitor banks in and out within one cycle of the applied ac voltage, the maximum surplus capacitive var in the total output range can be restricted to that produced by one capacitor bank, and, thus, theoretically, the TCR should have the same var rating as the TSC. However, to ensure that the switching conditions at the endpoints of the intervals are not indeterminate, the var rating of the TCR has to be somewhat larger than one TSC unit in order to have enough overlap between 'switching in' and 'switching out'.

From the black box view point both FC+TCR and TSC+TCR can be considered as controllable reactive admittance. The time response between the var demand to var output is mainly decided by the firing delay angle. The response time naturally varies with two topologies with TSC+TCR response taking bit longer. For power system studies, it is fairly reasonable to take a value of T/3 to T/6 where T is the time period of fundamental power frequency.

*ii) Plot the associated V-I characteristic of TSC+TCR topologies.*

[3]