IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2008

EEE PART II: MEng, BEng and ACGI

Corrected Copy

ANALOGUE ELECTRONICS 2

Thursday, 19 June 2:00 pm

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	C. Papavassiliou, C. Papavassiliou
	Second Marker(s) :	E. Rodriguez-Villegas, E. Rodriguez-Villegas

E2.2 ANALOGUE ELECTRONICS

The first question is mandatory.

1. This question consists of 10 brief items. Each item can be answered in a few words or a short paragraph. Please answer all sub-questions, which carry equal marks.

   a) A unilateral voltage amplifier has an input admittance of 0.1 S, an output impedance of 10 Ω and a voltage gain of 100. Calculate the input impedance of this amplifier when it drives a 10 Ω load. [4]

   b) Write equations which define the small signal hybrid ("h") parameters of a transistor. State the units of each one of the hybrid parameters. [4]

   c) Define the "Quality factor" of a second order filter. Explain the practical significance of a large quality factor. [4]

   d) Write an expression for the transfer function of a second order high pass filter. Explain the meaning of all constants that appear in this equation. [4]

   e) Explain the difference between an ideal voltage amplifier and an op-amp. [4]

   f) With the aid of a circuit diagram describe the common collector amplifier. Comment on the magnitude of the input and output impedance of the common collector amplifier. What is the function of the common collector amplifier, what is its alternative name and which of the 4 small signal parameter representations is in your opinion the best one to use when analysing a common collector amplifier? [4]

   g) With the aid of a diagram state the series form of the Miller theorem. [4]

   h) With the aid of a circuit diagram describe the bipolar transistor Darlington pair. Explain how the Darlington pair can be considered to be a sequence of two single transistor amplifiers. State the type (common emitter, common base or common collector) of amplifier of each of the two stages. [4]

   i) A commercial op-amp has a gain bandwidth product of $GB = 10$ MHz. What is the open loop gain of this amplifier at a frequency of 1 MHz? What is the phase of the gain at 1MHz? Explain your answer. [4]

   j) A bipolar transistor has a transit frequency $f_T = 318.3$MHz when its collector current is $I_C = 5mA$. Calculate the base-emitter capacitance of this transistor. Assume that the base-collector capacitance is negligibly small. The thermal voltage at room temperature is approximately $V_{th} = kT/q = 25mV$. [4]

[Total: 40]

2. a) Calculate the frequency dependence of the voltage gain of the circuit in figure 2.1. Assume that the op-amp is ideal. [5]

b) Calculate the frequency dependence of the voltage gain of the circuit in figure 2.1, if the op-amp is a dominant pole op-amp with infinite input impedance. The DC gain of the op-amp is equal to $G_{DC} = 10^5$ and its gain bandwidth product is $GB = 10^6$ Hz. [10]

c) Observe that the transfer function is the sum of two elementary 2nd order transfer functions. Identify these two transfer functions, and calculate the natural frequency, quality factor and gain for each one. [5]

d) Use the voltage transfer function you calculated in part b) to calculate the frequency response of the input and output impedance of the circuit in figure 2.1, if the op-amp input impedance is $1M\Omega$ and the op-amp output impedance is 100Ω. What are the limits for the input and output impedance of the circuit at low and high frequencies? [10]

[Total: 30]

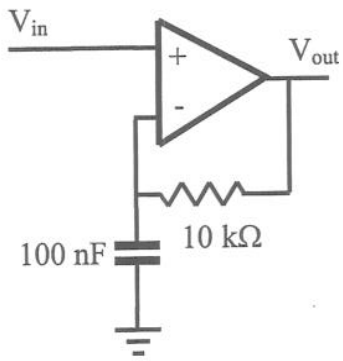

Figure 2.1 Circuit for question 2.

3. In this question you will analyse the amplifier in figure 3.1.

The NPN transistor has the following characteristics: Current gain $\beta = 200$, Early voltage $V_A = 100V$, Transit frequency $f_T = 500$ MHz. The NPN transistor is biased at a quiescent current of $I_C = 0.1mA$, and has negligible base-collector and collector-emitter capacitances. The DC base-emitter voltage at $I_C = 0.1mA$ is $V_{BE} = 0.5V$.

The PNP transistor has the following characteristics: Current gain $\beta = 50$, Early voltage $V_A = 50V$, Transit frequency $f_T = 100$ MHz. The PNP transistor is biased at a quiescent current of $I_C = 0.2mA$, and has negligible base-collector and collector-emitter capacitances. The DC base-emitter voltage at $I_C = 0.2mA$ is $V_{BE} = 0.5V$.

The components have the following values: $R_1 = 25k\Omega$, $R_2 = 45k\Omega$, $C = 100nF$. The power supply is $V_{CC} = 10V$.

The thermal voltage at room temperature is $V_{th} = kT/q = 25mV$.

a) Draw a small signal equivalent circuit for each transistor. Calculate numerical values for all components appearing in the equivalent circuits at the operating point stated above for each transistor. [10]

b) Calculate the low frequency small signal voltage gain of the amplifier in figure 3.1.
HINT: Show that the input impedance of the second stage is extremely large. Explain why the two stages can be considered independently. [5]

c) Use the voltage gain from part b) and the parallel form of the Miller theorem to calculate the small signal input impedance of the amplifier in figure 3.1. [5]

d) Calculate the small signal output impedance of the amplifier in figure 3.1. [5]

e) Explain how the frequency of the dominant pole of this amplifier depends on the signal source impedance. Calculate the dominant pole frequency when the amplifier is driven by an ideal voltage source. [5]

[Total: 30]

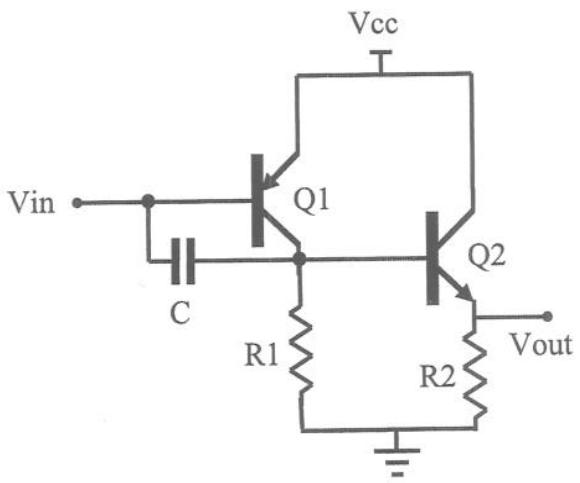

Figure 3.1 The amplifier for question 3.

4. The schematic of an active filter is shown in figure 4.1. The op-amp has zero output impedance. The rest of the assumptions on the op-amp are stated in each question.

'HPF' refers to the circuit within the dashed box in figure 4.1.

a) Draw a signal flow graph (block diagram) for HPF. The op-amp has a finite gain G and infinite input impedance. Write expressions for the block gains in terms of the circuit elements. [5]

b) Calculate the transfer function of HPF. The op-amp has a finite gain G and infinite input impedance. Calculate the input impedance of HPF. [5]

c) Evaluate the transfer function and input impedance of the circuit in figure 4.2 in terms of Z_1, Z_2, Z_3 and $G(s)$. Model this circuit with the same signal flow graph you used for the HPF. Define the values of the gain blocks of the graph in terms of Z_1, Z_2, Z_3 and $G(s)$. [10]

d) Assign values to Z_1, Z_2, Z_3 and $G(s)$ so that HPF is equivalent to the circuit in figure 4.2. The op-amp has a finite gain $G(s)$ and a finite input impedance Z_{amp}. [5]

e) Assign values to Z_1, Z_2, Z_3 and $G(s)$ so that the filter of figure 4.1 is equivalent to the circuit in figure 4.2.
HINT: In figure 4.1 HPF plays the role of a non-ideal op-amp. [5]

[Total: 30]

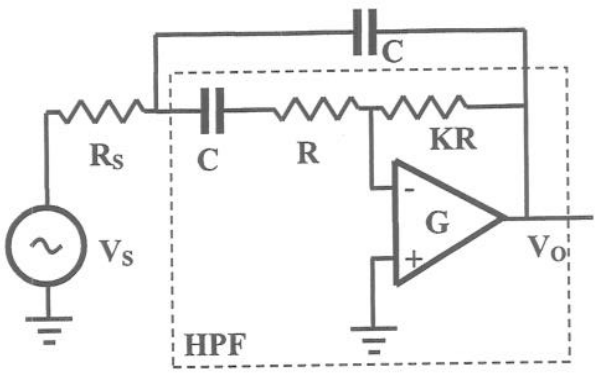

Figure 4.1 The filter for question 4.

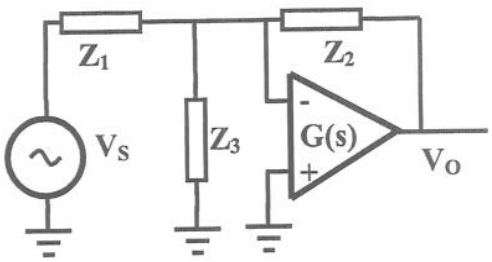

Figure 4.2 Equivalent circuit for a non-ideal inverting amplifier.