IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2008

MSc and EEE/ISE PART IV: MEng and ACGI

Corrected copy

INTRODUCTION TO DIGITAL INTEGRATED CIRCUIT DESIGN

Tuesday, 6 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible   First Marker(s) :   P.Y.K. Cheung

                          Second Marker(s) :   C. Bouganis

Information for Invigilators:

Students may bring any written or printed aids into the examination.

Information for Candidates:

Students may need red, green, blue, yellow and black coloured pens.

1. a) *Figure 1.1* (see the colour supplementary sheet) shows the layout of an n-well CMOS circuit *P* with four terminals: M, W, B and BB. Extract and draw the transistor-level schematic diagram of this circuit. Note that the supply signals are labelled as vdd, gnd_1 and gnd_2.

   Giving that the transistor labelled T5 is of size $4\lambda \times 2\lambda$, label all transistors in this circuit with their sizes.

   [8 marks]

   b) What function does this circuit perform? Provide a brief description on how this circuit works.

   [3 marks]

   c) Explain why if this cell is manufactured, it may fail in the field. What should be done to ensure that such failure is to be avoided?

   [3 marks]

   d) For the layout shown in *Figure 1.1*, draw the vertical cross section along the lines PP' and QQ'. Label your diagram indicating the n-well region and the different types and levels of doping (e.g. p^-, n^+ etc).

   [6 marks]

2. a) Provide a brief description (200-500 words) of your design project and your personal contribution.

   [9 marks]

   b) Full custom or cell-based semi-custom design style was adapted in your design group project. Discuss whether your design would have been better suited for other design implementation such as gate array or FPGA. Provide reasons for your opinion.

   [5 marks]

   c) Answer one of the following:

      (i) Explain the test strategy adopted for your chip.
      (ii) If you were to repeat the design exercise again, what would you have done differently and why?

   [6 marks]

3. *Figure 3.1* shows the circuit of a semi-dynamic D flip-flop.

a) With the help of timing diagrams showing the signals C, D, S, X and Q, explain how this circuit works.

[8 marks]

b) What constraints must inverters G5-8 satisfy in order for this circuit to work properly? What are the consequences if inverts G5-8 are removed?

[3 marks]

c) Modify this circuit in order to embed the following Boolean function with the D flip-flop.

$$D = P \bullet N + M \bullet \overline{N}$$

[3 marks]

d) Design the layout of the circuit shown in *Figure 3.1* in the form of a symbolic layout or a stick diagram.

[6 marks]
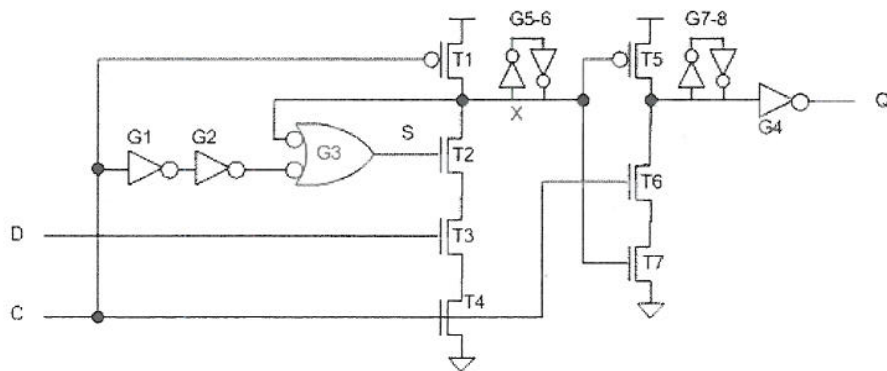
Figure 3.1

4. *Figure 4.1* shows a bit-serial comparator circuit that compares two m-bit unsigned numbers A and B supplied to the circuit bit-serially with the least significant bit first. The output is high only if A>B, and is low otherwise. The LSB signal is high when the least significant bit is supplied. The circuit is driven by non-overlapping two phase clock signals $\Phi 1$ and $\Phi 2$.

The latches are clocked by the signals indicated in *Figure 3.1*, and all have inverting outputs. The bit compare logic module BCL together with the latch L1 implements the logic function:

$$\overline{L_{n+1}} = \overline{A \bullet \overline{B} + L_n \bullet (A + \overline{B})}$$

where n is the bit number being processed.

a) Draw the timing diagram for the circuit for m=4, and for two sets of input numbers (A=0011, B=0110) and (A=1100, B=0010). Your diagram should include signals $\Phi 1$, $\Phi 2$, A, B, LSB, L_{n+1} and MIN.

[10 marks]

b) Design a transistor level circuit to implement the bit comparator logic module BCL. Marks may be deducted for unnecessarily large circuit.
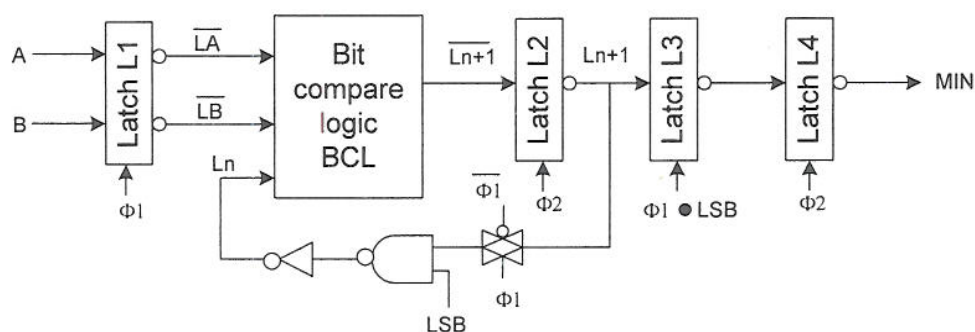
[10 marks]

Figure 4.1

5. a)   By applying the method of Logical Effort, explain why the oscillation frequency of an n-stage ring oscillator is (approximately) independent of the sizes of the transistors used. Furthermore, explain how a ring oscillator can be used to calibrate the speed of a fabrication process.

[6 marks]

    b)   *Figure 5.1* shows the circuit of a static XOR gate. All transistors are of length 2λ. The number adjacent to each transistor indicates its width in λ units. Using the method of Logical Effort estimate, in terms of the number of unit inverter delays, the delay from A or B input to the XOR output. Assume that the loading on the output is equivalent to 10 standard inverter loads where a standard inverter is assumed to have pull-up and pull-down transistor widths of 4λ and 2λ respectively. You may ignore the effect of parasitic capacitances.

[6 marks]

    c)   Calculate the transistor sizes for stages 2 and 3 of the circuit in order to minimize the delay through the circuit, assuming that the loading is equivalent to 10 standard inverters of size 4λ ×2λ, Estimate the new delay from either input to the output. You may again ignore the effect of parasitic capacitances.
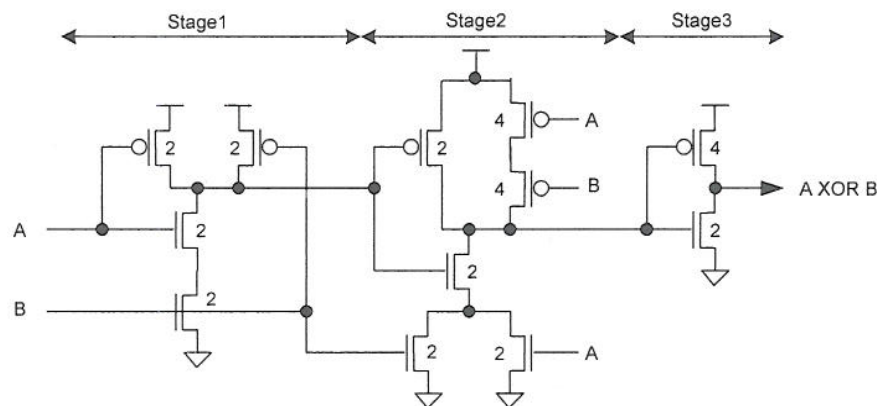
[8 marks]

Figure 5.1

6. a) Describe briefly how scan-path registers can be used to improve the testability of digital circuits. What are the disadvantages of using scan-path registers?

   Figure 6.1 shows a simplified block diagram of a processor chip. Suggest where you might add scan-path latches in order to improve the testability of this chip.

   [8 marks]

   b) Design in schematic form the circuit of a scan-path register and explain the different modes of operation when it is used in testing and normal environment.

   [6 marks]

   c) Consider the circuit shown *in Figure 6.2*. Explain why a stuck-at-0 fault at node X is undetectable.
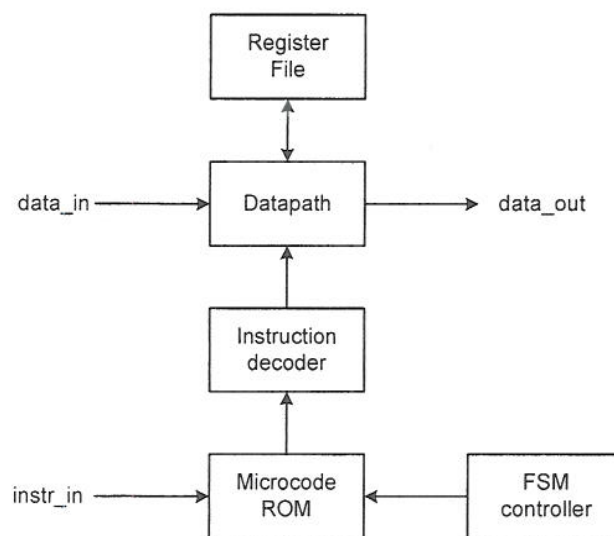
   [6 marks]
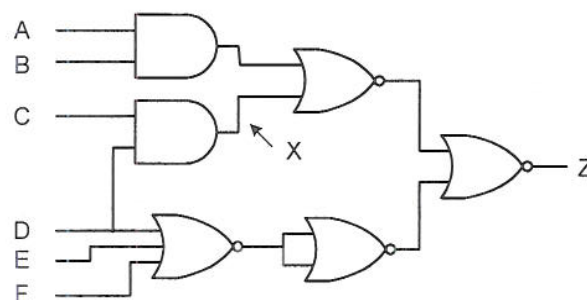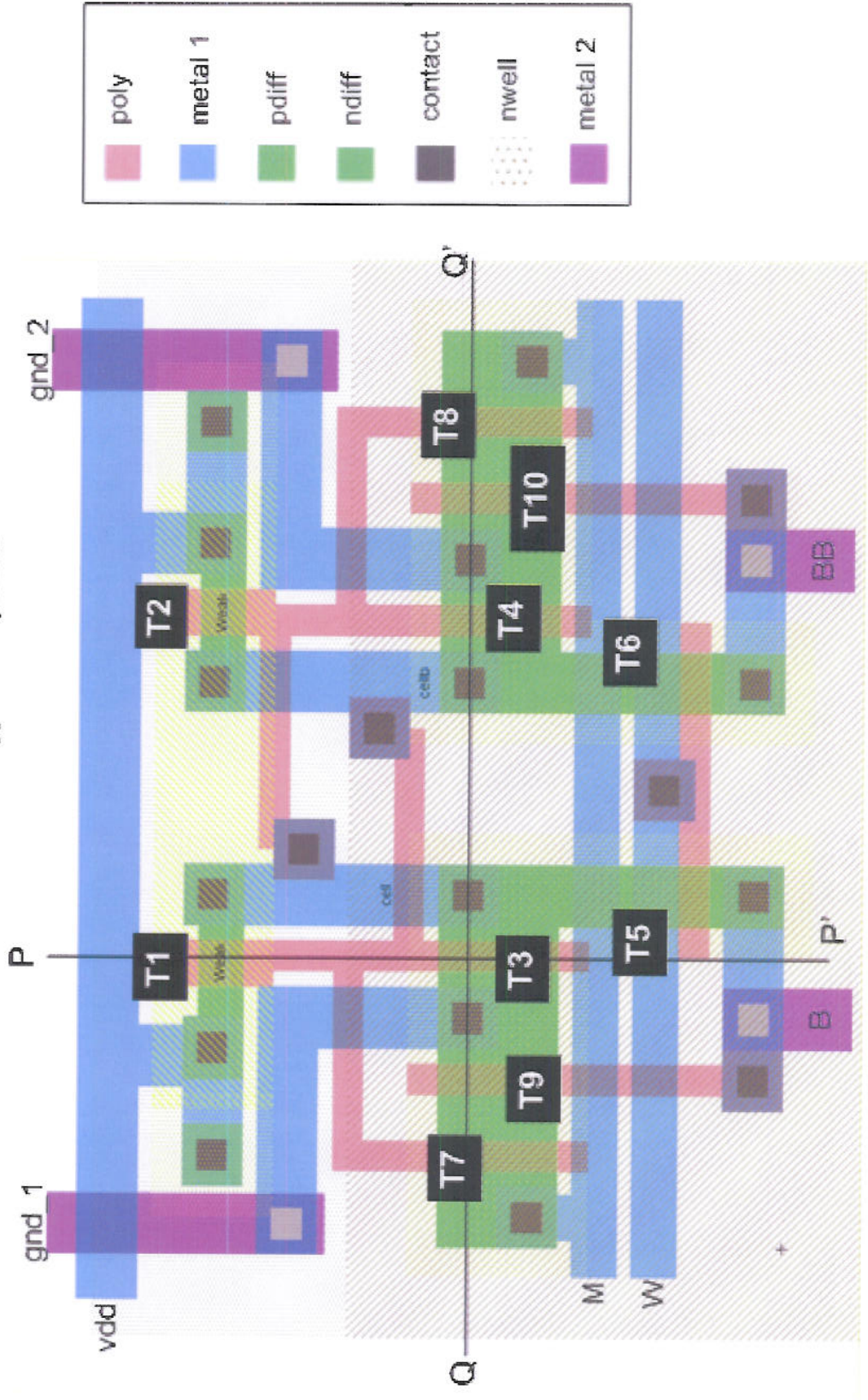

Figure 6.1

Figure 6.2

Colour Supplementary Sheet

Figure 1.1 Layout of full-custom cell for Question 1