IC设计-HW3

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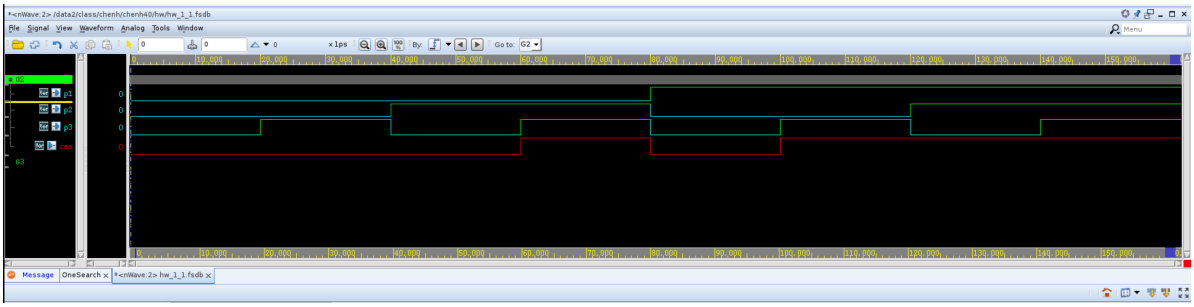
hw_1_1_tb

代码：

```
module hw_1_1_tb();
    reg     p1,p2,p3;   //input
    wire    res;        //output

    hw_1_1 hw_1_1_test(
        .p1(p1),
        .p2(p2),
        .p3(p3),
        .res(res)
    );

        //generate input
        initial begin
            p1 = 0;
            #(CYCLE*4);
            p1 = 1;
        end

        initial begin
        repeat(2) begin
            p2 = 0;
            #(CYCLE*2);
            p2 = 1;
            #(CYCLE*2);
            end
        end

        initial begin
        repeat(4) begin
            p3 = 0;
            #(CYCLE*1);
            p3 = 1;
            #(CYCLE*1);
            end
        end

        //dump fsdb
        initial begin
            $fsdbDumpfile("hw_1_1.fsdb");
            $fsdbDumpvars(0,hw_1_1_test);
            $fsdbDumpon;
            end
endmodule
```

仿真波形：



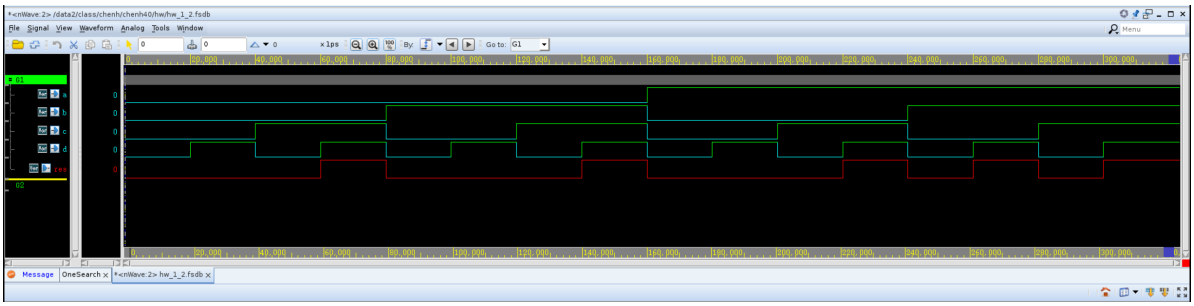
hw_1_2_tb

代码

```
module hw_1_2_tb();
    reg     a,b,c,d;
    wire    res;

    hw_1_2 hw_1_2_test(
        .a(a),
        .b(b),
        .c(c),
        .d(d),
        .res(res)
    );

        //generate input
        initial begin
            a = 0;
            #(CYCLE*8);
            a = 1;
        end

        initial begin
        repeat(2) begin
            b = 0;
            #(CYCLE*4);
            b = 1;
            #(CYCLE*4);
            end
        end

        initial begin
        repeat(4) begin
            c = 0;
            #(CYCLE*2);
            c = 1;
            #(CYCLE*2);
            end
        end

        initial begin
        repeat(8) begin
            d = 0;
            #(CYCLE*1);
            d = 1;
            #(CYCLE*1);
            end
```

```
        end

        //dump fsdb
        initial begin
            $fsdbDumpfile("hw_1_2.fsdb");
            $fsdbDumpvars(0,hw_1_2_test);
            $fsdbDumpon;
            end
endmodule
```

仿真波形：



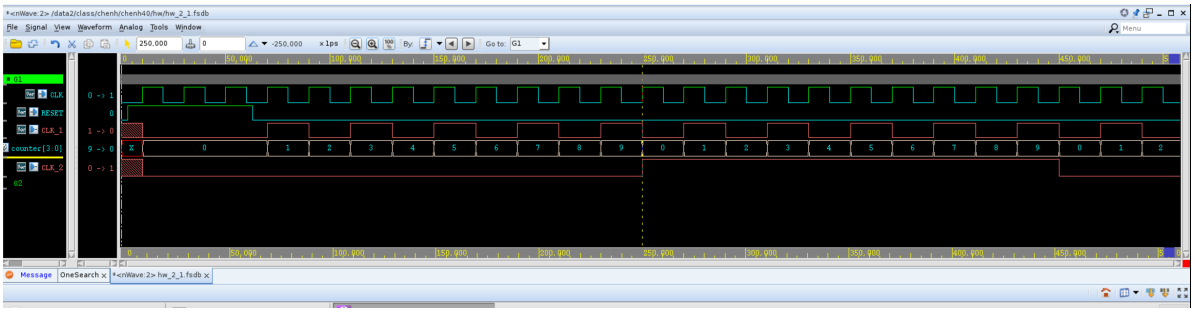
hw_2_1_tb

代码：

```
module hw_2_1_tb();
    reg clk;
    reg rst;

    wire clk_1,clk_2;

    parameter CYCLE = 20;
    parameter RESET_TIME = 3;

    hw_2_1 hw_2_1_test(
        .CLK    (clk),
        .RESET  (rst),
        .CLK_1  (clk_1),
        .CLK_2  (clk_2)
    );

        //CLK
        initial begin
            clk = 0;
            forever
            #(CYCLE/2)
            clk = ~clk;
        end

        //RESET
        initial begin
            rst = 0;
            #3;
            rst = 1;
            #(CYCLE * RESET_TIME)
            rst = 0;
            #(CYCLE*22);
            $finish;
```

```
34          end
35
36      //dump fsdb
37      initial begin
38      $fsdbDumpfile("hw_2_1.fsdb");
39      $fsdbDumpvars(0,hw_2_1_test);
40      $fsdbDumpon;
41      end
42
43  endmodule
```

仿真波形：



hw_2_2_tb

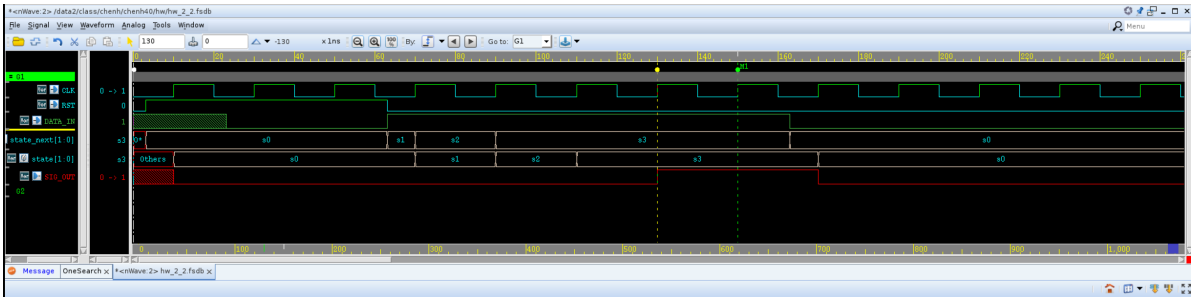
代码：

```
1   module hw_2_2_tb();
2       reg CLK,RST;
3       reg DATA_IN;
4       wire SIG_OUT;
5
6       parameter CYCLE = 20;
7       parameter RESET_TIME = 3;
8
9       hw_2_2 hw_2_2_test(
10          .CLK     (CLK),
11          .RST   (RST),
12          .DATA_IN   (DATA_IN),
13          .SIG_OUT   (SIG_OUT)
14      );
15
16          //CLK
17          initial begin
18              CLK = 0;
19              forever
20              #(CYCLE/2)
21              CLK = ~CLK;
22          end
23
24          //RESET
25          initial begin
26              RST = 0;
27              #3;
28              RST = 1;
29              #(CYCLE * RESET_TIME)
30              RST = 0;
31              #(CYCLE*50);
```

```
            $finish;
        end


        initial begin
        #3;
        repeat (2) begin
            #CYCLE ;
            DATA_IN = 0;
        end
        repeat(5) begin
          #CYCLE;
          DATA_IN = 1;
          end
          #CYCLE;
          DATA_IN = 0;
        end

    //dump fsdb
    initial begin
    $fsdbDumpfile("hw_2_2.fsdb");
    $fsdbDumpvars(0,hw_2_2_test);
    $fsdbDumpon;
    end
endmodule
```

仿真波形：

定义了在第3个时钟后开始连续输入5个1，可以看到state和state_next均正确翻转，sig_out识别到三个1111序列并正确输出持续三个周期的高电平，符合预期。



hw_2_3_tb

代码：

```
module hw_2_3_tb();
    reg CLK,RST;
    wire SEQ_OUT;

    parameter CYCLE = 20;
    parameter RESET_TIME = 3;

    hw_2_3 hw_2_3_test(
        .CLK    (CLK),
        .RST  (RST),
        .SEQ_OUT  (SEQ_OUT)
    );

        //CLK
```

```
        initial begin
            CLK = 0;
            forever
            #(CYCLE/2)
            CLK = ~CLK;
        end

        //RESET
        initial begin
            RST = 0;
            #3;
            RST = 1;
            #(CYCLE * RESET_TIME)
            RST = 0;
            #(CYCLE*33);
            $finish;
        end

    //dump fsdb
    initial begin
    $fsdbDumpfile("hw_2_3.fsdb");
    $fsdbDumpvars(0,hw_2_3_test);
    $fsdbDumpon;
    end
endmodule
```

仿真波形：

如图展示了完整的三个周期能完整的循环输出0100_1011_001的序列