

# IC设计-HW3

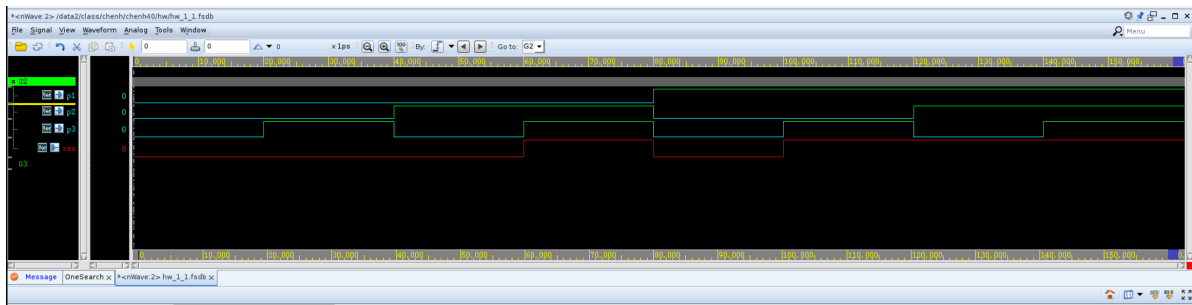
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## hw\_1\_1\_tb

代码:

```
1 module hw_1_1_tb();
2     reg    p1,p2,p3;    //input
3     wire    res;        //output
4
5     hw_1_1 hw_1_1_test(
6         .p1(p1),
7         .p2(p2),
8         .p3(p3),
9         .res(res)
10    );
11
12    //generate input
13    initial begin
14        p1 = 0;
15        #(CYCLE*4);
16        p1 = 1;
17    end
18
19    initial begin
20        repeat(2) begin
21            p2 = 0;
22            #(CYCLE*2);
23            p2 = 1;
24            #(CYCLE*2);
25        end
26    end
27
28    initial begin
29        repeat(4) begin
30            p3 = 0;
31            #(CYCLE*1);
32            p3 = 1;
33            #(CYCLE*1);
34        end
35    end
36
37    //dump fsdb
38    initial begin
39        $fsdbDumpfile("hw_1_1.fsdb");
40        $fsdbDumpvars(0,hw_1_1_test);
41        $fsdbDumpon;
42    end
43 endmodule
```

仿真波形:



## hw\_1\_2\_tb

### 代码

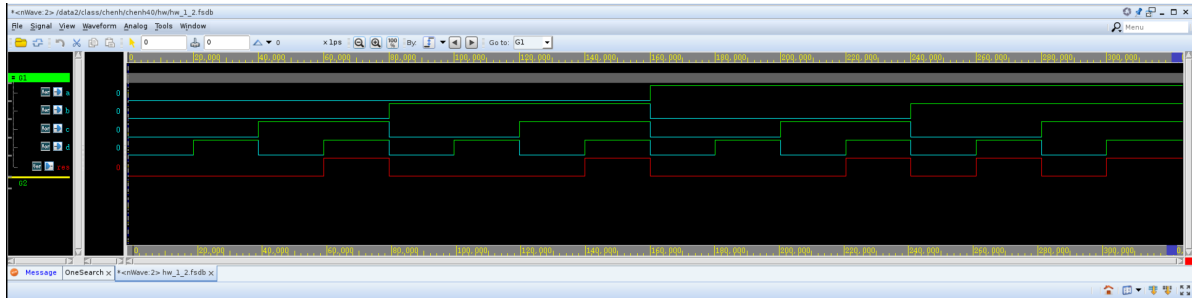
```
1 module hw_1_2_tb();
2     reg    a,b,c,d;
3     wire    res;
4
5     hw_1_2 hw_1_2_test(
6         .a(a),
7         .b(b),
8         .c(c),
9         .d(d),
10        .res(res)
11    );
12
13    //generate input
14    initial begin
15        a = 0;
16        #(CYCLE*8);
17        a = 1;
18    end
19
20    initial begin
21        repeat(2) begin
22            b = 0;
23            #(CYCLE*4);
24            b = 1;
25            #(CYCLE*4);
26        end
27    end
28
29    initial begin
30        repeat(4) begin
31            c = 0;
32            #(CYCLE*2);
33            c = 1;
34            #(CYCLE*2);
35        end
36    end
37
38    initial begin
39        repeat(8) begin
40            d = 0;
41            #(CYCLE*1);
42            d = 1;
43            #(CYCLE*1);
44        end
45    end
```

```

45         end
46
47         //dump fsdb
48         initial begin
49             $fsdbDumpfile("hw_1_2.fsdb");
50             $fsdbDumpvars(0,hw_1_2_test);
51             $fsdbDumpon;
52         end
53     endmodule

```

仿真波形：



hw\_2\_1\_tb

代码：

```

1  module hw_2_1_tb();
2      reg clk;
3      reg rst;
4
5      wire clk_1,clk_2;
6
7      parameter CYCLE = 20;
8      parameter RESET_TIME = 3;
9
10     hw_2_1 hw_2_1_test(
11         .CLK    (clk),
12         .RESET  (rst),
13         .CLK_1  (clk_1),
14         .CLK_2  (clk_2)
15     );
16
17     //CLK
18     initial begin
19         clk = 0;
20         forever
21             #(CYCLE/2)
22                 clk = ~clk;
23     end
24
25     //RESET
26     initial begin
27         rst = 0;
28         #3;
29         rst = 1;
30         #(CYCLE * RESET_TIME)
31         rst = 0;
32         #(CYCLE*22);
33         $finish;

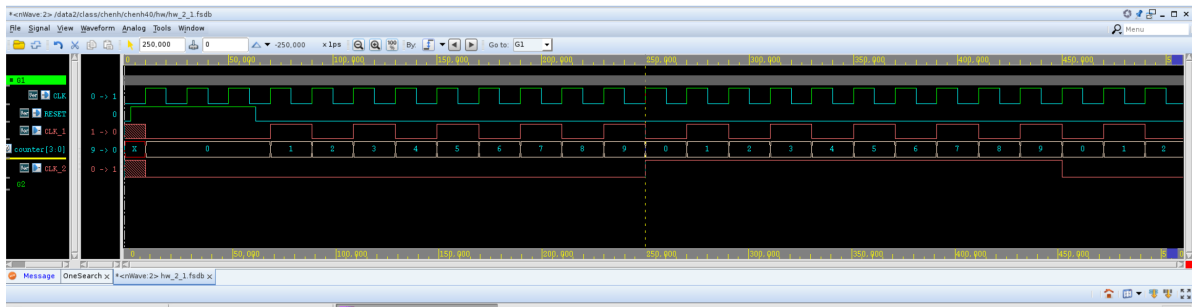
```

```

34         end
35
36         //dump fsdb
37         initial begin
38             $fsdbDumpfile("hw_2_1.fsdb");
39             $fsdbDumpvars(0,hw_2_1_test);
40             $fsdbDumpon;
41         end
42
43     endmodule

```

仿真波形：



hw\_2\_2\_tb

代码：

```

1  module hw_2_2_tb();
2      reg CLK,RST;
3      reg DATA_IN;
4      wire SIG_OUT;
5
6      parameter CYCLE = 20;
7      parameter RESET_TIME = 3;
8
9      hw_2_2 hw_2_2_test(
10         .CLK      (CLK),
11         .RST      (RST),
12         .DATA_IN   (DATA_IN),
13         .SIG_OUT    (SIG_OUT)
14     );
15
16     //CLK
17     initial begin
18         CLK = 0;
19         forever
20             #(CYCLE/2)
21             CLK = ~CLK;
22     end
23
24     //RESET
25     initial begin
26         RST = 0;
27         #3;
28         RST = 1;
29         #(CYCLE * RESET_TIME)
30         RST = 0;
31         #(CYCLE*50);

```

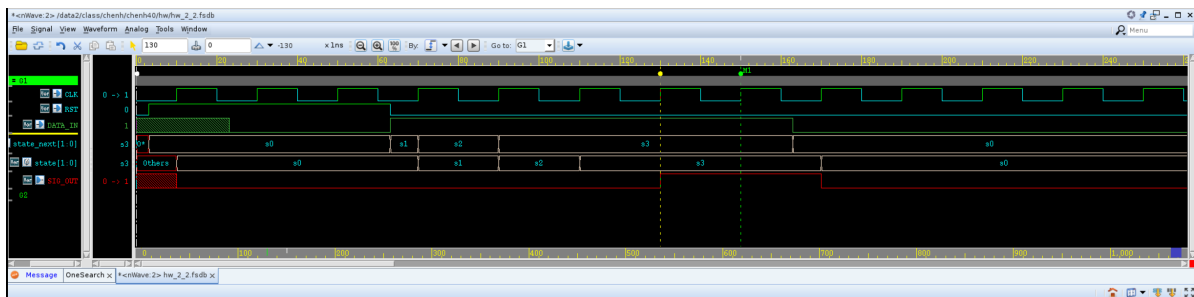
```

32         $finish;
33     end
34
35
36     initial begin
37     #3;
38     repeat (2) begin
39         #CYCLE ;
40         DATA_IN = 0;
41     end
42     repeat(5) begin
43         #CYCLE;
44         DATA_IN = 1;
45     end
46     #CYCLE;
47     DATA_IN = 0;
48     end
49
50     //dump fsdb
51     initial begin
52     $fsdbDumpfile("hw_2_2.fsdb");
53     $fsdbDumpvars(0,hw_2_2_test);
54     $fsdbDumpon;
55     end
56 endmodule

```

仿真波形：

定义了在第3个时钟后开始连续输入5个1，可以看到state和state\_next均正确翻转，sig\_out识别到三个1111序列并正确输出持续三个周期的高电平，符合预期。



hw\_2\_3\_tb

代码：

```

1  module hw_2_3_tb();
2      reg CLK,RST;
3      wire SEQ_OUT;
4
5      parameter CYCLE = 20;
6      parameter RESET_TIME = 3;
7
8      hw_2_3 hw_2_3_test(
9          .CLK      (CLK),
10         .RST      (RST),
11         .SEQ_OUT   (SEQ_OUT)
12     );
13
14     //CLK

```

```

15     initial begin
16         CLK = 0;
17         forever
18             #(CYCLE/2)
19             CLK = ~CLK;
20     end
21
22     //RESET
23     initial begin
24         RST = 0;
25         #3;
26         RST = 1;
27         #(CYCLE * RESET_TIME)
28         RST = 0;
29         #(CYCLE*33);
30         $finish;
31     end
32
33     //dump fsdb
34     initial begin
35         $fsdbDumpfile("hw_2_3.fsdb");
36         $fsdbDumpvars(0,hw_2_3_test);
37         $fsdbDumpon;
38     end
39 endmodule

```

仿真波形：

如图展示了完整的三个周期能完整的循环输出0100\_1011\_001的序列

