Bandgap Voltage Reference Project

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***Abstract*—Voltage references are crucial to biasing analog and digital circuits. In this paper, four different voltage reference designs were analyzed and iterated for optimization in terms of the temperature coefficient, V_{DD} sensitivity, and the total power consumption. The approach was to develop equations and calculate each design parameter and then simulate and verify the handwritten calculations to LTspice. Based on the results, the circuit was either modified for improved performance or stored as the final result. Overall, the methodology and approach led to the design goals being mostly met.**

I. Introduction

Voltage references play a critical role in analog and digital circuits. Fig. 1 illustrates the relationships between each module found in analog circuits.

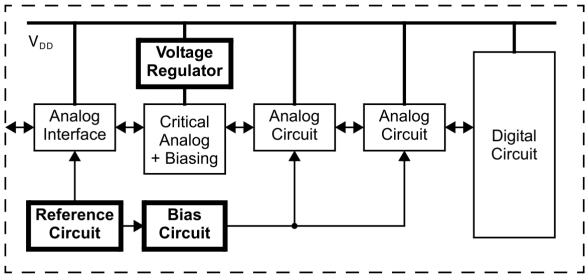

Fig. 1. Overview of modules found in analog circuits.[1]

Ideally, voltage references provide a constant voltage regardless of changes in temperature, supply voltage, or load. This is important for subsystems which depend on a fixed voltage where the environmental conditions are not constant. Examples include ADC/DAC, voltage regulators, measurement, and control systems.

A. Design Tools, Set Up and Assumptions

The following tools, settings, and assumptions were used.

- LTspice IV
- Electric VLSI Design System
- MATLAB
- 0.18μm CMOS technology based off the Analog Integrated Circuit Design 2nd Ed. course website[2] website
- Temperature range between -50 to 100 °C
- Ideal voltage/current source
- Ideal operational amplifier

[1]Image taken from Analog Integrated Circuit Design 2nd Ed. by Carusone
[2]Analog Integrated Circuit Design 2nd Ed. Model Files

B. Design Objectives

The main objectives for the voltage reference design are

1) Minimize $TC(V_{ref})$ (temperature coefficient)
2) Minimize V_{DD} sensitivity
3) Minimize P consumption

These design objectives are achieved using an iterative approach. The layout is done only for the MOSFET-Only Voltage Divider.

C. Design Methodology

Our design methodology is outlined in the flowchart show in Figure 2. For each circuit topology, we will: develop the necessary design equations/assumptions, size the circuit components, simulate the circuits in LTSpice, and evaluate the simulation results. If the results do not meet our design objectives, then we will examine our design equations/assumptions, resize the circuit components, and re-run the simulations. If the results meet our design objectives, then we move onto the next circuit.

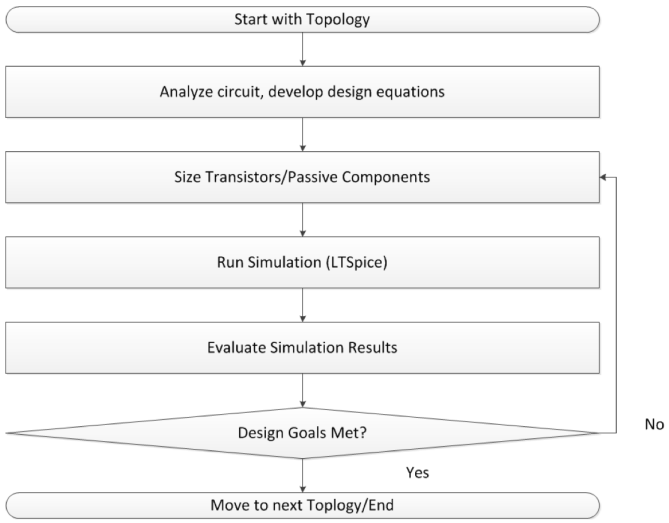

Fig. 2. Design Methodology

For the MOSFET-Only circuit topology, we will also layout and simulate the design in Electric. If the simulation results meet our design requirements, we will move on to the next topology. Otherwise, we will iterate the design as is done for the rest of the circuit topologies.

D. Design Topologies

Four different voltage reference topologies are investigated.

1) Design 1. Resistor-MOSFET Voltage Divider: The most basic design. This design should be good for first-order effects but simulation performance may suffer when higher-order parameters are included.

2) Design 2. MOSFET-Only Voltage Divider: Improved design. This design should have a better temperature coefficient than the Resistor-MOSFET design since the P-channel MOSFET load adds an additonal degree of freedom.

3) Design 3. Current-Diode Voltage Reference: Improved design. This topology should perform well in simulation, however this circuit is difficult to realize due to the reliance on an absolute, ideal current source which is nearly impossible to design and impliment.

Note: Designs 1-3 will be designed and tested without consideration of next-stage loading effects. Section V discusses how to minimize these effects on the reference voltage.

4) Design 4. CMOS Bandgap Voltage Reference: Advanced design; based on the Brokaw Bandgap Reference. This design is implemented using vertical CMOS diode-connected PNP BJTs and an ideal operational amplifier; it will be verified that the ideal op amp is performing within a reasonable approximation of a real op amp.

E. Global Design Parameters

The following parameters are used in the calculations for each circuit topology.

- $V_{DD} = 1.8$ V *(except in Design 4 where* $V_{DD} = 3.3$ V*)*
- $TC_R = 2,000$ ppm (0.002)
- $T_0 = 20\ ^\circ C$

TABLE I
PARAMETERS FOR CALCULATIONS

Parameter	NMOS	PMOS	PNP Diode
V_{to} (V)	0.45	-0.45	-
K_n (μA/V^2)	270	70	-
$\lambda \cdot L$ (μm/V)	0.08	0.08	-
I_S (A)	-	-	1e$-$18
$TC(V_{TP,TN})$	3,000 *ppm*	3,000 *ppm*	-

II. Resistor-MOSFET Voltage Divider

Design 1 consists of a diode connected N-channel MOSFET with a resistive load. The resistive load has a positive temperature coefficient while the N-channel MOSFET has a negative temperature coefficient. This relationship allows for close-to-constant output voltage based on proper sizing of the devices.

Figure 3 shows the basic circuit topology. This is a simple resistor-MOSEFT voltage divider without consideration for loading effects. Figure 4 shows the small signal circuit equivalent for the resistor-MOSFET divider.

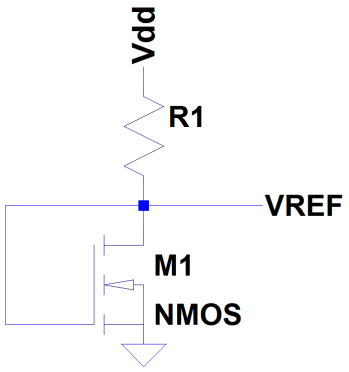

Fig. 3. Resistor-MOSFET Circuit

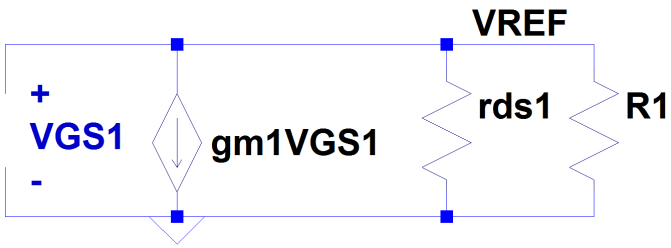

Fig. 4. Resistor-MOSFET Small Signal Circuit

A. Resistor-MOSFET Design Approach

Table II gives the design equations used throughout the design of the Resistor-MOSFET Voltage Divider. The original design goals call for minimizing TC but setting Eq. **??** does not provide a reasonable approach. Instead, the main goal for the resistor-MOSFET circuit was to keep the total power at or below 500 mW. Another constraint included was to was to obtain a voltage reference of 1.24 V, which is close to the Silicon bandgap voltage. From here, the current can be calculated. This allows for the W/L ratio to be solved using the drain current equation. The result leads to a load resistor of 2 kΩ.

B. Iteration 1

1) Device Sizes: Table III gives the device sizes for iteration 1 of the Resistor-MOSFET circuit topology.

2) Design Discussion: Analyzing the simulation results showed the power consumption, voltage reference, Z_{out} matched well with the hand calculations. The temperature coefficient was high and should be compensated in the next iteration if possible. This can be done by setting V_{REF} close to V_{TN}. When these two are close to equal, the drain current is minimized, thereby reducing power consumption. In addition, we can see from Equation 4 that the temperature will be reduced and still positive.

C. Iteration 2

1) Device Sizes: Table IV gives the device sizes for iteration 2 of the Resistor-MOSFET circuit topology.

TABLE II
RESISTOR-MOSFET DESIGN EQUATIONS

Voltage Reference	$V_{REF} = V_{TN} - \sqrt{\frac{2(V_{DD}-V_{REF})}{RK_n}}$	(1)
Transconductance Parameter	$KP(T) = KP(T_0)(\frac{T}{T_0})^{-1.5}$	(2)
V_{DD} Sensitivity	$S_{VDD}^{VREF} = \frac{V_{DD}}{V_{REF}} \frac{\partial V_{REF}}{\partial V_{DD}} \approx \frac{1}{V_{TN}\sqrt{\frac{2RK_n}{V_{DD}}}+2}$	(3)
Temperature Coefficient	$TC_{REF} = \frac{1}{V_{REF}} \frac{\partial V_{REF}}{\partial T} = \frac{1}{V_{REF}} \left[V_{TN} TC_{V_{TN}} - \frac{1}{2}\sqrt{\frac{2L}{W}\frac{V_{DD}}{RKP(T)}} \cdot \left[\frac{1}{R} \cdot \frac{\partial R}{\partial T} - \frac{1.5}{T} \right] \right]$	(4)
Power Consumption	$P = IV$	(5)

TABLE III
RESISTOR-MOSFET DEVICE SIZES, ITERATION 1

Parameter	NMOS	R1
W (μm)	3	-
L (μm)	1	-
R (Ω)	-	2k

TABLE IV
RESISTOR-MOSFET DEVICE SIZES, ITERATION 2

Parameter	NMOS	R1
W (μm)	3	-
L (μm)	1	-
R (Ω)	-	823k

2) Design Discussion: Analyzing the results showed significant improvement on the power consumption, temperature coefficient and sensitivity to V_{DD}.

III. MOSFET-ONLY VOLTAGE DIVIDER

The MOSFET-Only Voltage Divider topology is shown in Figure 5. This topology similar to the Resistor-MOSFET topolgy, but R1 is replaced with a diode connected PMOS transistor as an active load. Figure 6 shows the small signal circuit equivalent for the MOSFET-Only Voltage Divider.

A. MOSFET-Only Design Approach

Table V gives the design equations used throughout the design of the MOSFET-Only Voltage Divider. The design approach for the MOSFET-Only voltage divider is as follows:

1) Develop the equations for the V_{ref} and $TC(V_{ref})$.
2) Set the addition argument in (10) $= 0$.

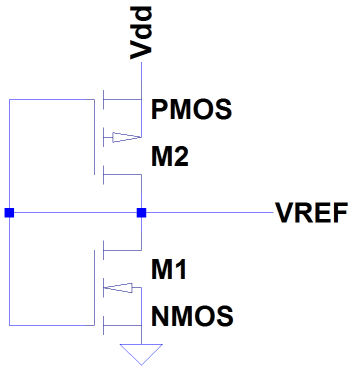

Fig. 5. MOSFET-Only Circuit

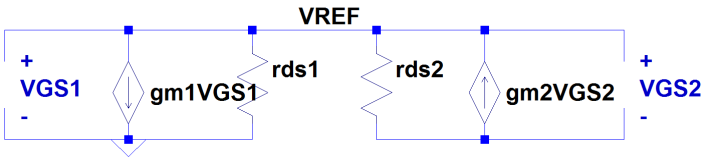

Fig. 6. MOSFET-Only Small Signal Circuit

3) Solve for the ratio $\sqrt{\frac{K_n}{K_p}}$.

Equation 10 is developed under the design constraints give in 6 and the assumption that $\frac{\partial V_{TP,TN}}{\partial T} >> \frac{\partial K_{n,p}}{\partial T}$. Since $TC(V_{TP}) = TC(V_{TN})$ and $|V_{TN}| = |V_{TP}|$, the ratio $\frac{K_n}{K_p} = 1$. This also implies that $gm_1 = gm_2$; thus, the output impedance is given by (7).

B. Iteration 1

1) Device Sizes: Table VI gives the device sizes for iteration 1 of the MOSFET-Only circuit topology.

2) Design Discussion: Analyzing the simulation results showed the power consumption and reference voltage matched well with the hand calculations, but our measured temperature coefficient was far higher than expected. This is because we simplified the design equations to first order terms and set the temperature coefficient to zero to find our device sizes. The temperature coefficient is minimized in the second iteration of the design.

C. Iteration 2

1) Optimization Approach: To optimize this circuit with a second iteration, we decided increase K_n while keeping K_p constant in order to increase the current draw of the NMOS transistor. This will cause the PMOS transistor to have a greater voltage drop across it and lower the V_{DS} of the NMOS transitor. This brings V_{GS} closer to V_{TN} and will reduce the temperature coeffcient down in a similar manner as is performed in the Optimization of Design 1.

2) Device Sizes: Table VII gives the device sizes for iteration 2 of the MOSFET-Only circuit topology design.

TABLE V
MOSFET-ONLY DESIGN EQUATIONS

Design Constraints	$V_{GS1} = V_{GS2} = V_{ref}$ $I_{D1} = I_{D2}$ (6)
Output Resistance	$I_T = gm_1 V_{GS1} + \frac{V_T}{r_{ds1}} + \frac{V_T}{r_{ds2}} + -gm_2 V_{GS2}$ $\therefore R_{out} = r_{ds1} // r_{ds2}$ (7)
MOSFET Drain Current	$I_{DN} = K_n (V_{REF} - V_{TN})^2$ (8a) $I_{DP} = K_p (V_{REF} - V_{TP})^2$ (8b)
Voltage Reference	$V_{REF} = \frac{-V_{TP} + V_{DD} + \sqrt{\frac{K_n}{K_p}} V_{TN}}{\sqrt{\frac{K_n}{K_p}} + 1}$ (9)
Temperature Coefficient	$TC_{REF} = \frac{1}{V_{REF}} \frac{\partial V_{REF}}{\partial T}$ $= \frac{1}{V_{REF}} \frac{1}{\sqrt{\frac{K_n}{K_p}} + 1} \left(\frac{\partial -V_{TP}}{\partial T} + \sqrt{\frac{K_n}{K_p}} \frac{\partial V_{TN}}{\partial T} \right)$ (10)

TABLE VI
MOSFET-ONLY DEVICE SIZES, ITERATION 1

Parameter	NMOS	PMOS
W (μm)	2	8
L (μm)	1	1

TABLE VII
MOSFET-ONLY DEVICE SIZES, ITERATION 2

Parameter	NMOS	PMOS
W (μm)	32	8
L (μm)	1	1

3) Design Discussion: Analyzing simulation of iteration two of the MOSFET-Only Voltage Divider, we see that we have traded power consumption and size for performance. We will not optimize this design any further.

4) Layout: Figure 7 displays the layout of iteration two the MOSFET-Only Voltage Divider. Figure 24 displays the simulations of iteration two the MOSFET-Only Voltage Divider.

IV. CURRENT-DIODE VOLTAGE REFERENCE

The Current-Diode Voltage Divider topology is shown in Figure 8. This consists of an absolute, ideal current source in series with a diode. This diode is a vertical CMOS diode conected PNP BJT. The output of the circuit is taken at the node between the current source and the anode of the diode.

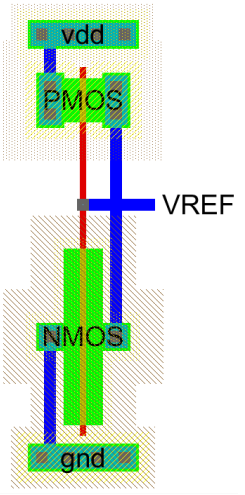

Fig. 7. MOSFET-Only Layout

Figure 9 shows the small signal circuit equivalent for the Current-Diode Voltage Reference.

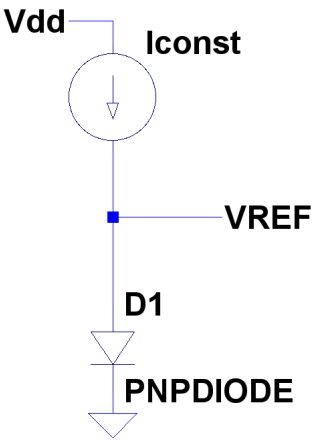

Fig. 8. Current-Diode Circuit

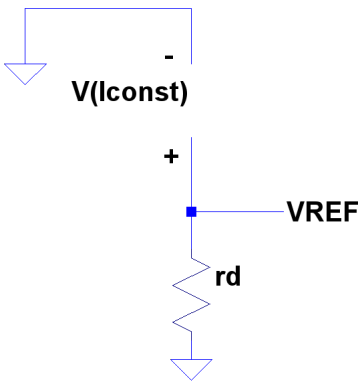

Fig. 9. Current-Diode Circuit LFSSM

A. Current-Diode Design Approach

Table XI gives the relevant design equations for the Current Diode Voltage Reference design. Equation 15 gives the diode voltage for a given diode current at the given reference temperature (20 °C). To achieve a low power design, we set $I_{const} = 1\mu$A; this sets the reference voltage to V_{BE0} at T_0. To find the temperature coefficient of V_{ref} near our reference temperature, we take $\frac{\partial V_{BE}}{\partial T}$ with $J_C = J_{C0}$ due to the constant current source and divide by V_{BE0}. This gives Equation 17 where k is Boltzman's Constant, $m = 2.3$ and $V_{G0} = 1.206$ (V).

TABLE VIII
CURRENT-DIODE DESIGN EQUATIONS

SS Diode Impedance	$r_d = \frac{V_T}{I_D} = \frac{kT}{qI_D}$ (11)
Input Resistance	$R_{in} = \frac{V_T}{I_T} = \infty$ (12)
Output Resistance	$R_{out} = \frac{V_T}{I_T} = r_d$ (13)
Diode Current	$I_D = I_s e^{V_D/V_T} = I_s e^{qV_D/kT}$ (14)
V_{BE0}	$V_{BE0} = \frac{kT_0 ln(I_D/I_s)}{q}$ (15)
V_{BE}	$V_{BE} = V_{G0}(1 - \frac{T}{T_0}) + V_{BE0}\frac{T}{T_0} + \frac{mkT}{q} ln(\frac{T_0}{T}) + \frac{kT}{q} ln(\frac{J_c}{J_{c0}})$ (16)
$TC(V_{BE})$	$TC(V_{BE}) = \frac{1}{V_{BE0}}[\frac{1}{T_0}(V_{BE0} - V_{G0}) + \frac{mk}{q}(\ln\frac{T_o}{T} - 1)]$ (17)

B. Iteration 1

1) Device Parameters: Table IX shows the design parameters for the first iteration of the Current Diode Voltage Reference.

TABLE IX
CURRENT DIODE VOLTAGE REFERENCE, ITERATION 1

Parameter	PNPDIODE	Iconst	R1
R (Ω)	-	-	-
I_S (A)	1e-18	-	-
I (μA)	-	1	-

2) Design Discussion: The results of the Current Diode Voltage Reference iteration 1 simulations closely match the handcalculations. This lack of percent error is mainly due to the fact that we had complete control over I_S and I_D. This V_{ref} of this design has the expected negative temperature coefficient of a diode. This temperature coefficeint is reduced in the second design iteration.

C. Iteration 2

1) Optimization Approach: To reduce the temperature coefficient of the Current Diode Voltage Reference, we connected a resistor between the anode of the diode and the output node. We set the temperature coefficient of the resistor to be the opposite of that of the diode at T_0. This way, the temperature coefficeints of the diode and resistor cancel and reduce the temperature coefficent of the reference voltage without increasing power consumpiton. The size of the resistor was chosen such that $V_{ref} = 1.24$ V.

2) Device Parameters: Table X shows the design parameters for the second iteration of the Current Diode Voltage Reference.

TABLE X
CURRENT DIODE VOLTAGE REFERENCE, ITERATION 2

Parameter	PNPDIODE	Iconst	R1
R (Ω)	-	-	500k
I_S (A)	1e-18	-	-
I (μA)	-	1	-

3) Design Discussion: The simulation results of iteration 2 of the Current Diode Voltage Reference are not idea; however, the temperature coeffcient of the reference voltage is greatly reduced. The nonzero temperature coefficeint is due to the nonlinear temperature coefficient of the diode. No further iteration of this circuit is desired.

V. DESIGN 1-3 LOAD BUFFERING

Designs 1-3 were improved until their output parameters would be sufficient for most reference voltage needs. However, if these designs are to be implimented, they must be buffered from next stage loading effects. Each circuit's operating integrity is heavily dependent on the operating current of the of the bottom half of a divider. Additionally, these circuits have too high of output impedances to serve as reliable voltage sources. In order to actaully impliment these circuits, one would need to connected a buffer between the reference voltage and desired input stage as shown in Figure **??**.

VI. CMOS BANDGAP VOLTAGE REFERENCE

The CMOS Bandgap Voltage Reference is the most advanced voltage reference topology covered in this paper. Figure 11 shows the generic CMOS Bandgap Voltage Reference circuit.

The basic theory of operation behind this bandgap reference is as follows:

1) The ratio of I_1 and I_2 is set by the ratio of $R1$ and $R3$.

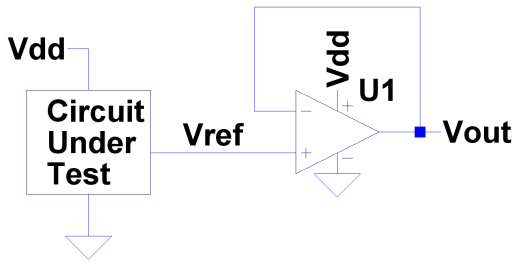

Fig. 10. Next Stage Load Buffering Circuit

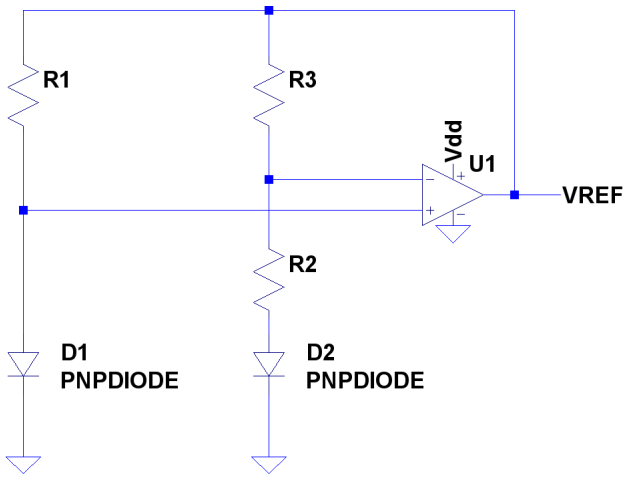

Fig. 11. CMOS Bandgap Voltage Reference Circuit

2) This generates a voltage of $-\Delta V_{BE}$ at the V_- node of the opamp.
3) The ΔV_{BE} voltage is scaled by the ratio of $R3$ and $R2$.
4) The op amp adds V_{BE} with the scaled version of ΔV_{BE} to create the output voltage.

ΔV_{BE} has a positive temperature coefficient (PTAT) and V_{BE} negative temparture coefficient (CTAT); thus, their sum has a near zero temperature coefficient. This circuit provides very low V_{DD} sensitivity as the only connection to V_{DD} is the power supply to the op amp. However, the circuit shown in 11 cannot run on a low voltage supply because the summation of ΔV_{BE} and V_{BE} may be larger than V_{DD} and cause the circuit to fail. Therefore, we raised the V_{DD} to 3.3 V for the Bandgap Voltage Referene Circuit Design.

Note: In implementation, the topology shown in **??** *requires a start-up circuit to reach the desired reference voltage steady-state. However, we did not find it necessary to include the start-up circuit in our simulations.*

A. Design Equations

B. Design Approach

The design approach taken in the first iteration of the sizing the components in the Bandgap Voltage Reference Circuit was to set the total power consumption, ratio of I_1 and I_2 currents, and desired V_{ref}. This produced the necessesary resistor values to realize this design.

TABLE XI
BANDGAP VOLTAGE REFERENCE DESIGN EQUATIONS

ΔV_{BE}	$\Delta V_{BE} = V_2 - V_1 = \frac{kT}{q} ln\left(\frac{J_2}{J_1}\right)$ (18)
V_{ref}	$V_{REF} = V_{EB1} + \frac{R_3}{R_2}\frac{kT}{q} ln\left(\frac{R_3}{R_1}\right)$ (19)

C. Iteration 1

1) Device Parameters: Table XII gives the design parameters for iteration 1 of the Bandgab Voltage Reference Circuit.

TABLE XII
BANDGAP REFERENCE DEVICE PARAMETERS, ITERATION 1

Parameter	PNPDIODE	R1	R2	R3
R (Ω)	-	1.69k	2.13k	16.9k
I_S (A)	1e-18	-	-	-

2) Design Discussion: The simulation results for iteration one of the Bandgap Voltage Reference closely match the hand calculations. However, the temperature coefficient was larger than we had anticipated. The temperature coeffeicient is reduced in iteration 2.

D. Iteration 2

1) Optimization Approach: There are multiple paths to reducing the Bandgap Voltage Reference. We noticed that the PTAT slope was overly prominent in our output voltage reference; thus, we set out to reduce the slope of the PTAT component of the reference voltage. The most direct way to reduce this slope was to raise R2. To find the new value of R2, we found our maximum error in our output voltage then set R2 such that

$$R2 = R2 + \beta R2 max(error_{V_{ref}}) \quad (20)$$

We then experimentaly determined that β = 4 gave the desired reduction in temperature coeffcient.

2) Device Parameters: Table XIII gives the design parameter for the second iteration of the Bandgap Voltage Reference Circuit.

TABLE XIII
BANDGAP REFERENCE DEVICE PARAMETERS, ITERATION 2

Parameter	PNPDIODE	R1	R2	R3
R (Ω)	-	1.69k	3.02k	16.9k
I_S (A)	1e-18	-	-	-

3) Design Discussion: The design parameters were met for the CMOS Bandgap Voltage Reference. No further iteration is desired.

VII. Simulation and Results/Comparisons

Figure 12 in the Appendix shows the circuit for testing the input impedance of each circuit topology. Figure 13 in the Appendix shows the circuit for testing the output impedance of each circuit topology. Figure 15 in the Appendix shows the circuit for testing the frequency response of each circuit topology.

Note: The frequency response of each circuit was not tested because we ran out of time and the frequency response measurement was not crucial to operation of the voltage references.

TABLE XIV
RESISTOR-MOSFET VOLTAGE DIVIDER RESULTS

Parameter	Hand-calc	Iteration 1	Iteration 2	Comments
# Passive Elements	1	1	1	
# Active Elements	1	1	1	
$\sum$Width (μm)	3	3	3	
$\sum$Area (μm)^2	3	3	3	
$\sum P$ (mW)	0.500	0.442	0.003	
V_{ref} (V)	1.24	1.314	0.466	
TC(Vref) (ppm)	2,171	616	3.5	
V_{DD} Sens.	0.267	0.514	0.035	
Z_{out} (Ω)	1.06k	1.03k	30k	
Z_{in} (Ω)	2k	4.12k	854k	
$V_{out,max}$ (V)	1.24	1.37	0.468	
$V_{out,min}$ (V)	1.24	1.25	0.467	
Gain (dBV)				
BW (Hz)				
GBW (dBVHz)				

TABLE XV
MOSFET-ONLY VOLTAGE DIVIDER RESULTS

Parameter	Hand-calc	Iteration 1	Iteration 2	Comments
# Passive Elements	0	0	0	0
# Active Elements	2	2	2	2
$\sum$Width (μm)	10	10	40	
$\sum$Area (μm)^2	10	10	40	
$\sum P$ (mW)	0.1	0.094	0.225	
V_{ref} (V)	0.904	.894	0.596	
TC(Vref) (ppm)	13.6	120.4	3.06	
V_{DD} Sens.	1.0045	0.5	0.175	
Z_{out} (Ω)	101.25k	2.3k	626	
Z_{in} (Ω)	-165	10.4k	4.33k	
$V_{out,max}$ (V)	0.904	.903	0.597	
$V_{out,min}$ (V)	0.904	.887	0.594	
Gain (dBV)				
BW (Hz)				
GBW (dBVHz)				

TABLE XVI
CURRENT DIODE VOLTAGE DIVIDER RESULTS

Parameter	Hand-calc	Iteration 1	Iteration 2	Comments
# Passive Elements	0	0	1	
# Active Elements	1	1	1	
$\sum$Width (μm)	-	-	-	-
$\sum$Area (μm)^2	-	-	-	-
$\sum P$ (mW)	0.0018	0.0018	0.0018	P is set by Id
V_{ref} (V)	0.698	0.725	1.216	
TC(Vref) (ppm)	-2,800	-2,160	-137	
V_{DD} Sens.	0	0	0	
Z_{out} (Ω)	25.3k	25.9k	525.9k	
Z_{in} (Ω)	∞	∞	∞	
$V_{out,max}$ (V)	0.698	0.833	1.23	
$V_{out,min}$ (V)	0.698	0.597	1.20	
Gain (dBV)				
BW (Hz)				
GBW (dBVHz)				

TABLE XVII
CMOS BANDGAP VOLTAGE REFERENCE RESULTS

Parameter	Hand-calc	Iteration 1	Iteration 2	Comments
# Passive Elements	3	3	3	
# Active Elements	3	3	3	
$\sum$Width (μm)	-	-	-	
$\sum$Area (μm)^2	-	-	-	
$\sum P$ (mW)	1	1.26	0.985	
V_{ref} (V)	1.24	1.33	1.184	
TC(Vref) (ppm)	0	396	27.2	
V_{DD} Sens.	0	0.068	0.032	
Z_{out} (Ω)	0	72.7	72.7	
Z_{in} (Ω)	∞	∞	∞	
$V_{out,max}$ (V)	1.24	1.37	1.184	
$V_{out,min}$ (V)	1.24	1.29	1.180	
Gain (dBV)	-			
BW (Hz)	-			
GBW (dBVHz)	-			

VIII. Conclusion

The analyses of all four topologies proved to fit the design parameters. The mosfet only topology alone showed some variation for the input (Zin) and output (Zin) impedance. They differed quite a bit from the hand calculations. The two iterations for each topology gave a concrete picture on the analysis.

APPENDIX

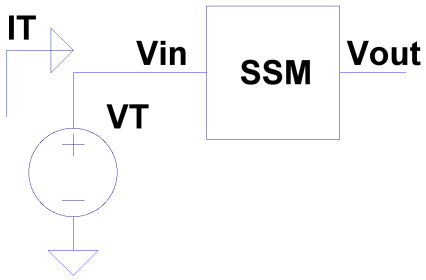

Fig. 12. Input Impedance Measurement Circuit

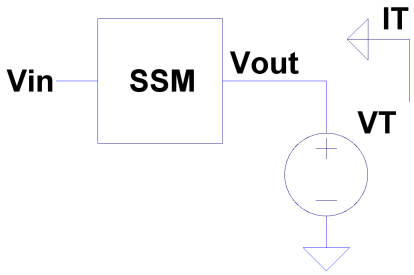

Fig. 13. Output Impedance Measurement Circuit

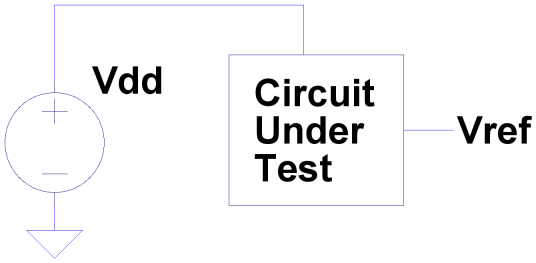

Fig. 14. V_{DD} Sensitivity Measurement Circuit

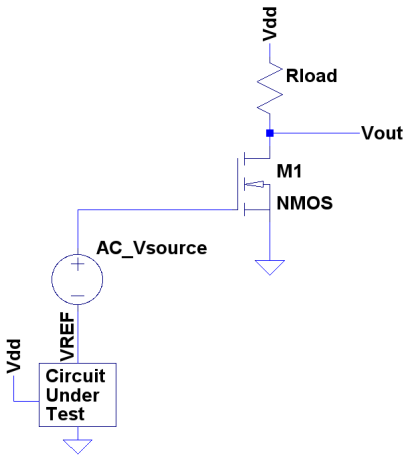

Fig. 15. Frequency Response Measurement Circuit

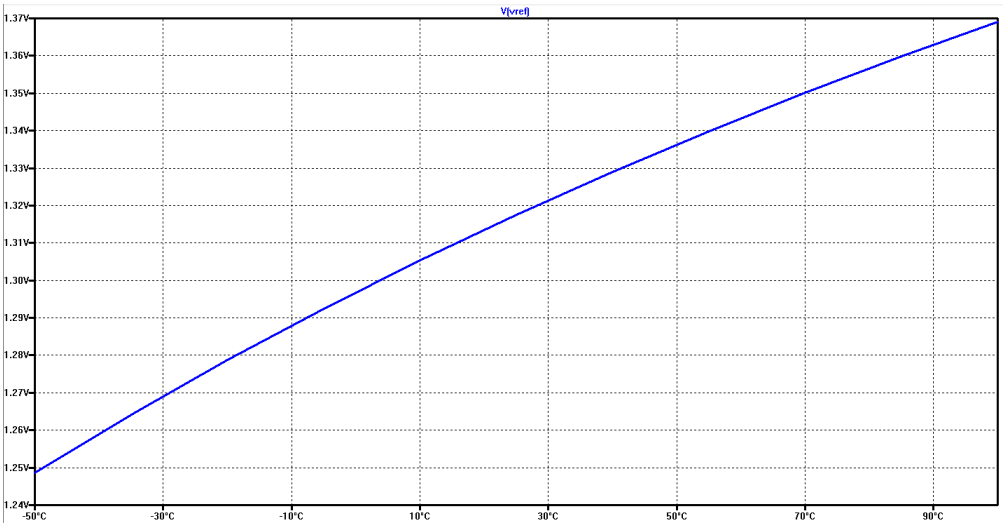

Fig. 16. Resistor-MOSFET Output Voltage @ 20°C-Iteration 1

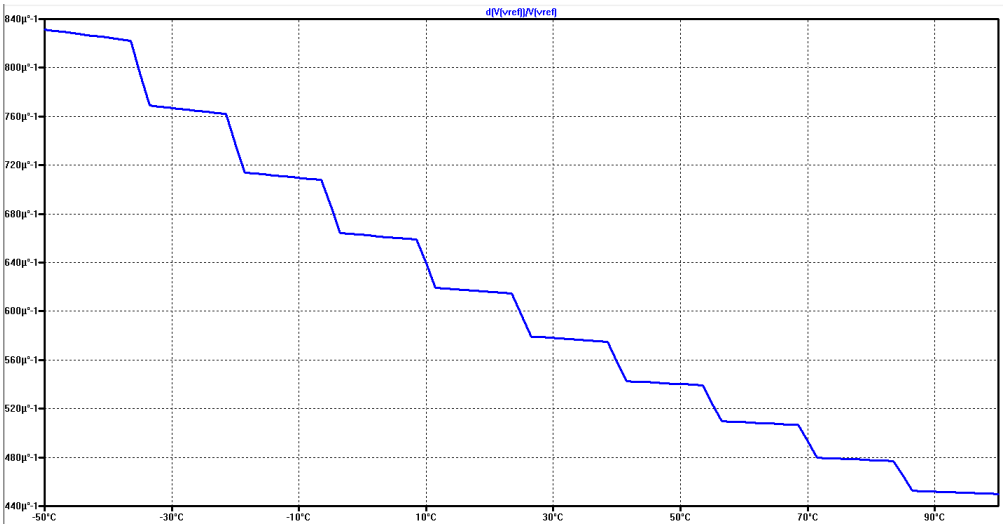

Fig. 17. Resistor-MOSFET Temperature Coefficient @ 20°C-Iteration 1

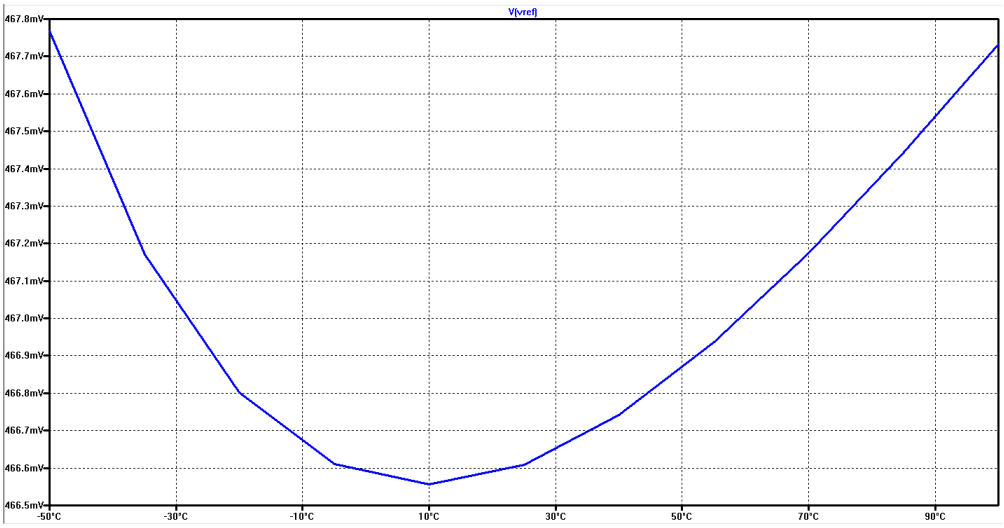

Fig. 18. Resistor-MOSFET Output Voltage @ 20°C-Iteration 2

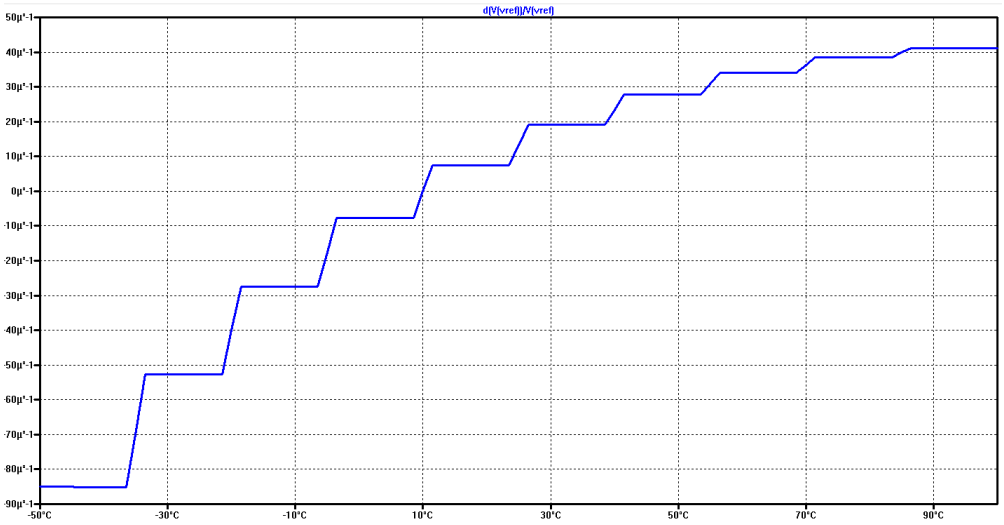

Fig. 19. Resistor-MOSFET Temperature Coefficient @ 20°C-Iteration 2

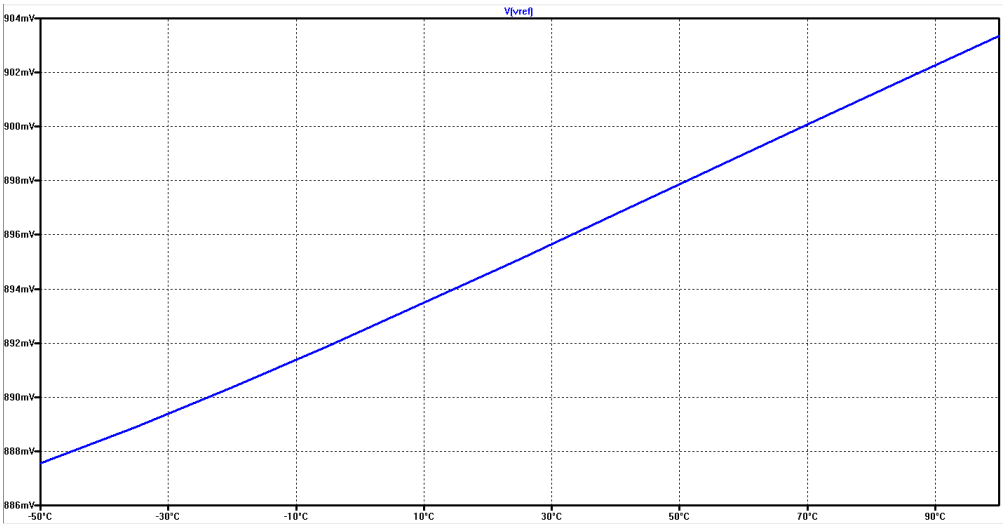

Fig. 20. MOSFET-Only Output Voltage @ 20°C-Iteration 1

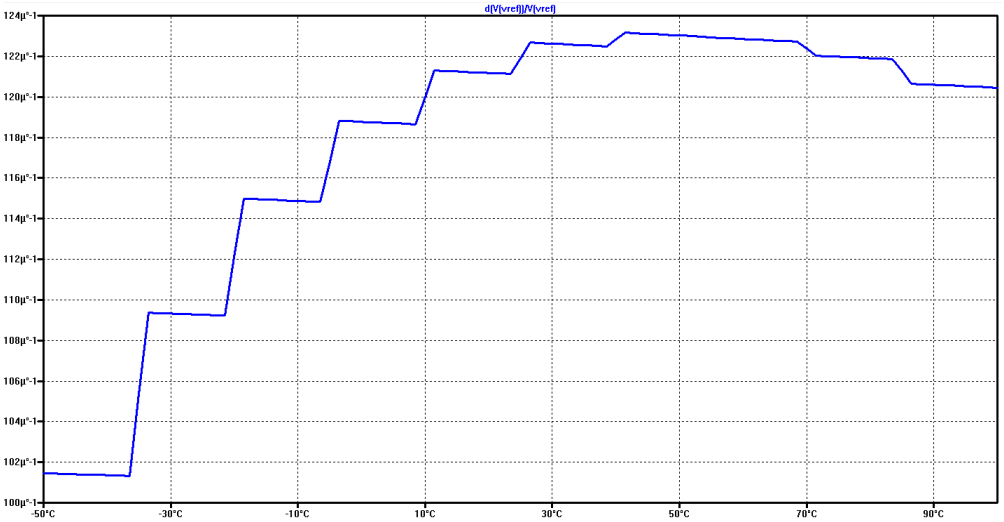

Fig. 21. MOSFET-Only Temperature Coefficient @ 20°C-Iteration 1

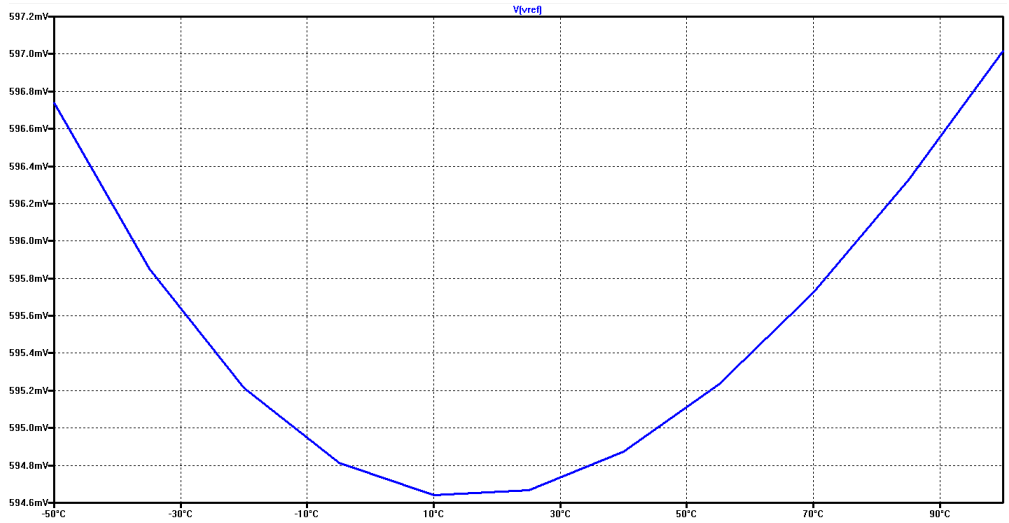

Fig. 22. MOSFET-Only Output Voltage @ 20°C-Iteration 2

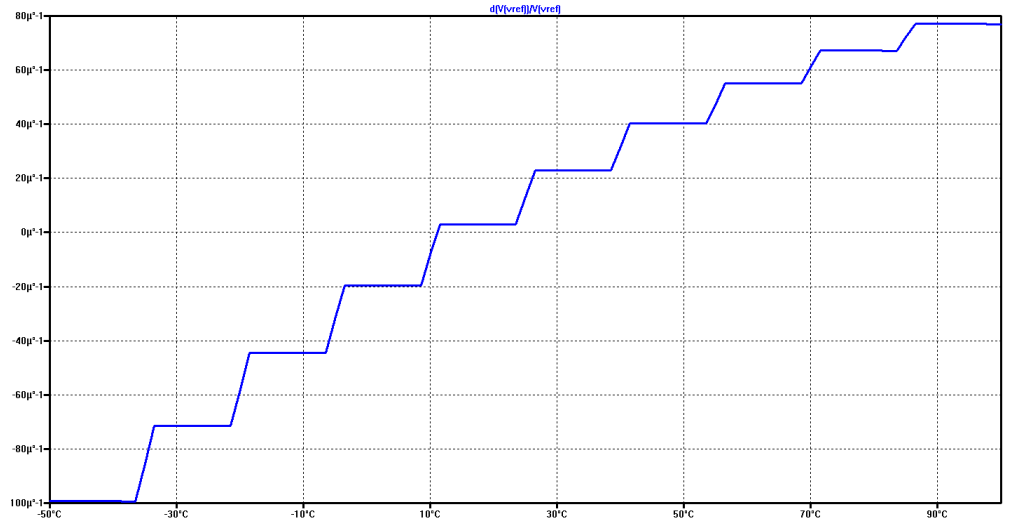

Fig. 23. MOSFET-Only Temperature Coefficient @ 20°C-Iteration 2

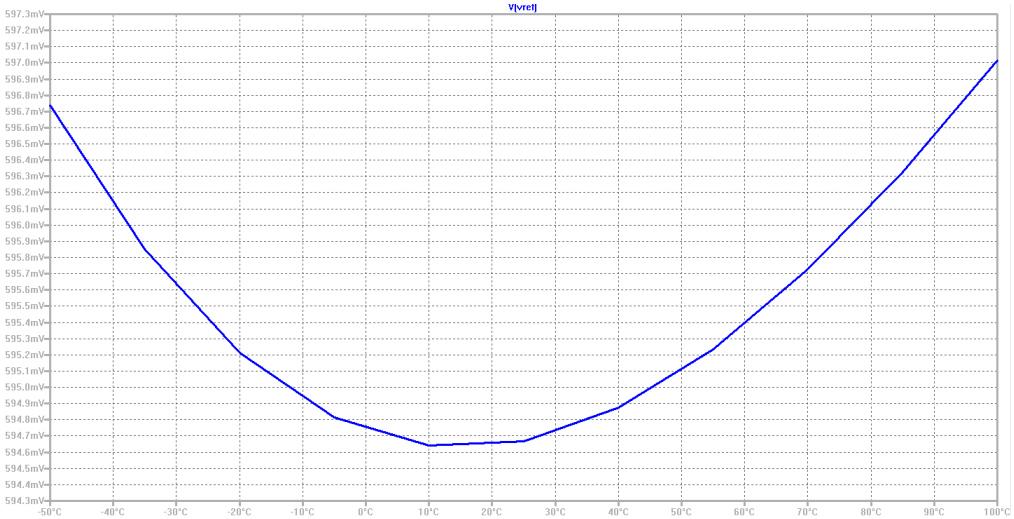

Fig. 24. MOSFET-Only Layout Output

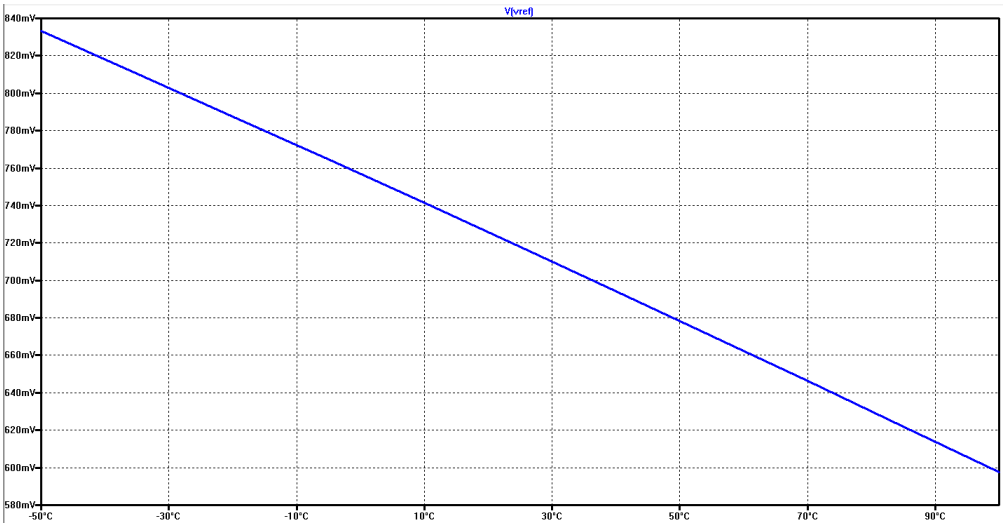

Fig. 25. Current Diode Output Voltage @ 20°C-Iteration 1

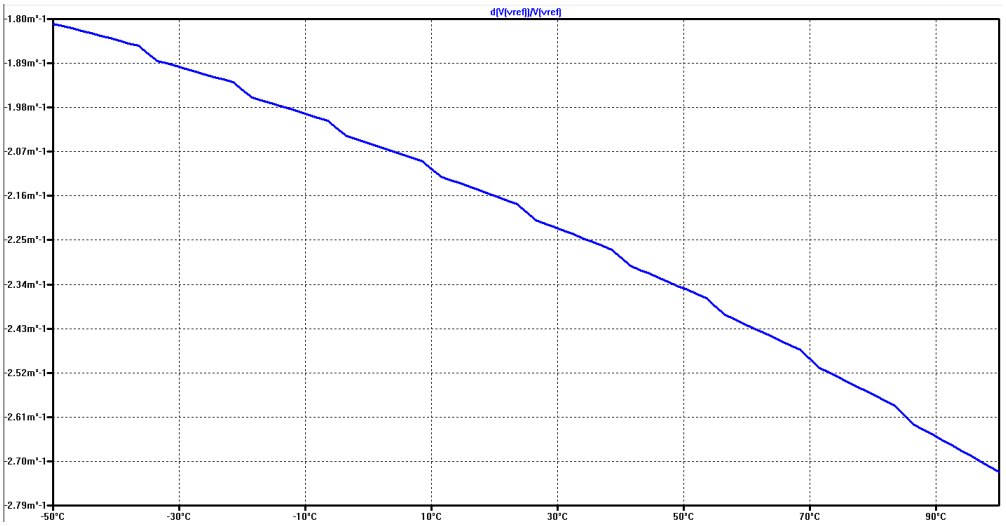

Fig. 26. Current Diode Temperature Coefficient @ 20°C-Iteration 1

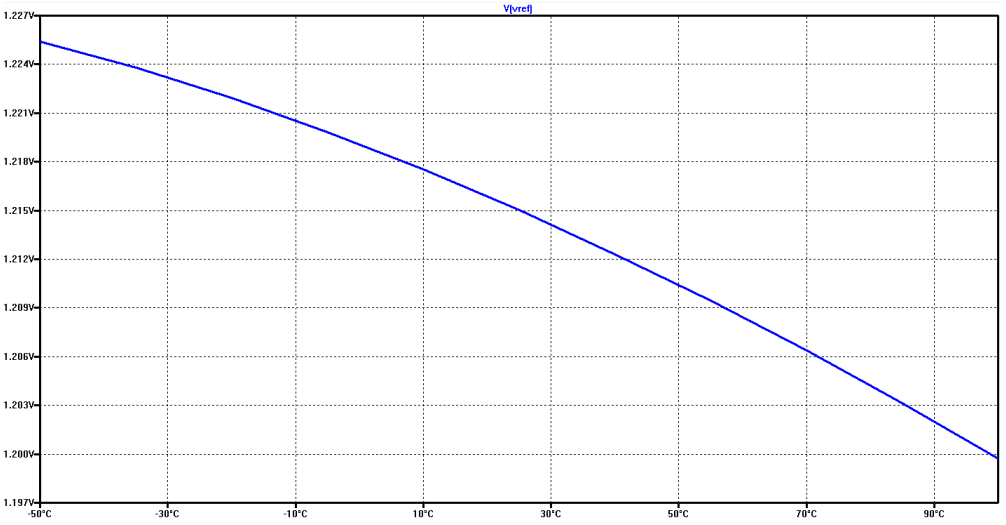

Fig. 27. Current Diode Output Voltage @ 20°C-Iteration 2

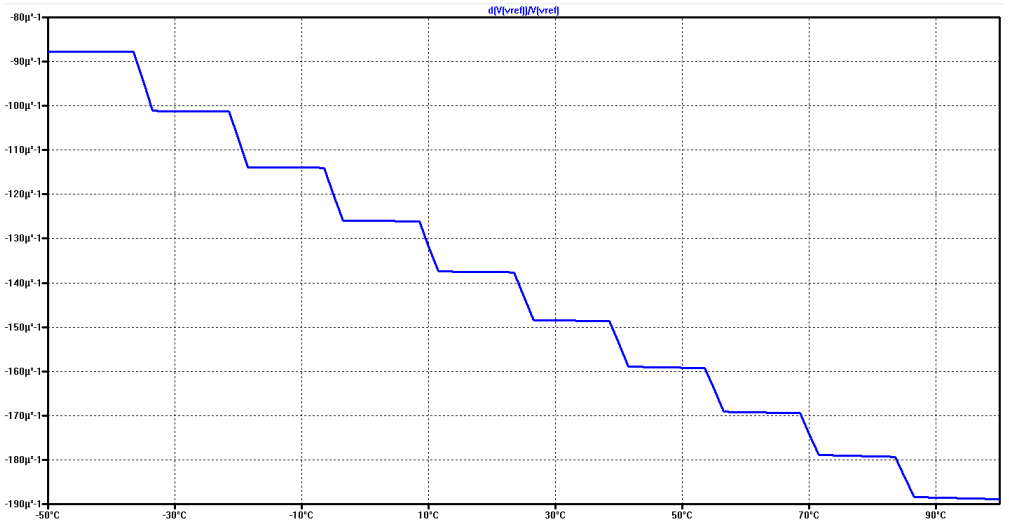

Fig. 28. Current Diode Temperature Coefficient @ 20°C-Iteration 2

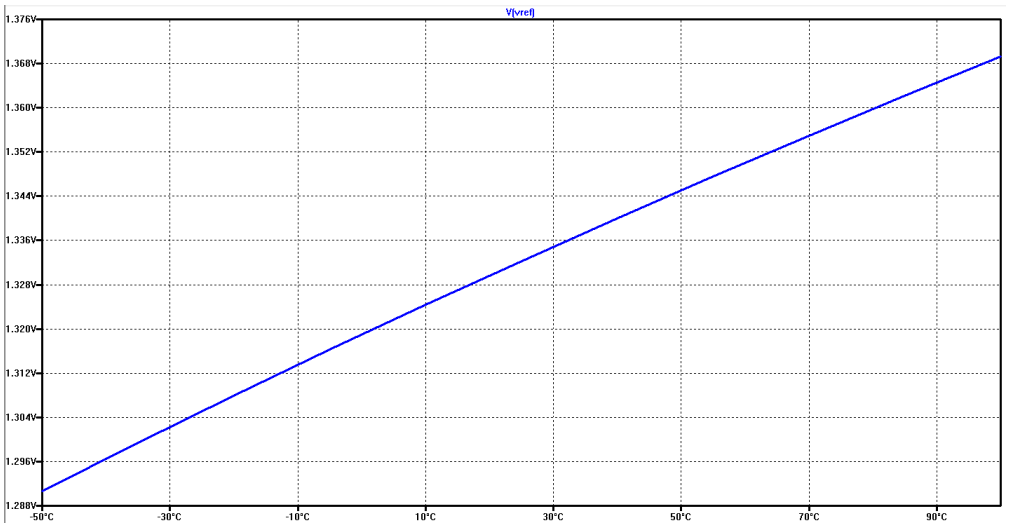

Fig. 29. Bandgap Voltage Reference Output Voltage @ 20°C-Iteration 1

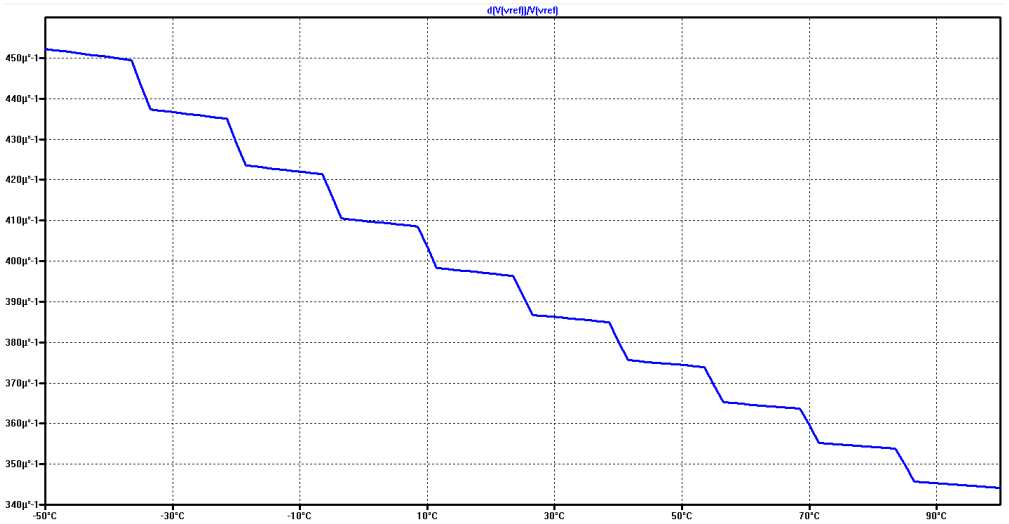

Fig. 30. Bandgap Voltage Reference Temperature Coefficient @ 20°C-Iteration 1

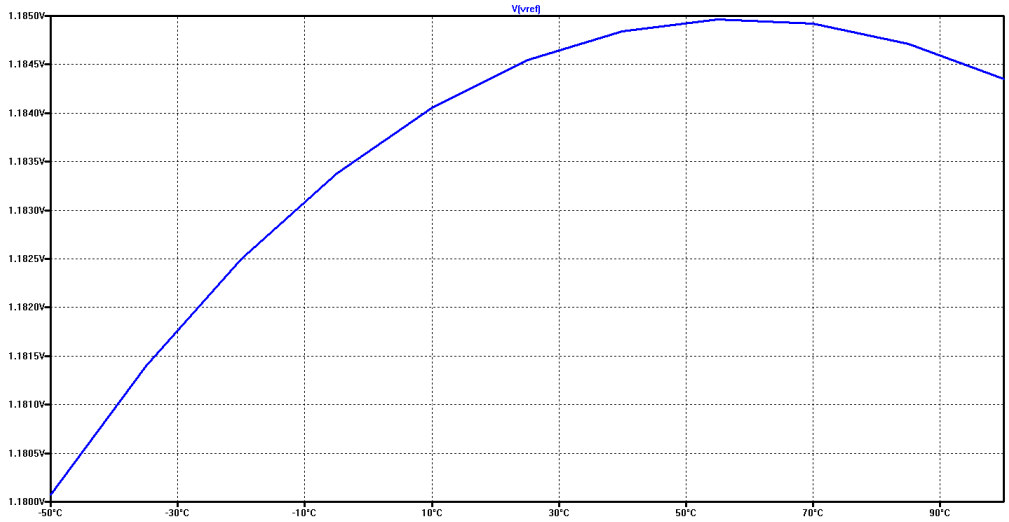

Fig. 31. Bandgap Voltage Reference Output Voltage @ 20°C-Iteration 2

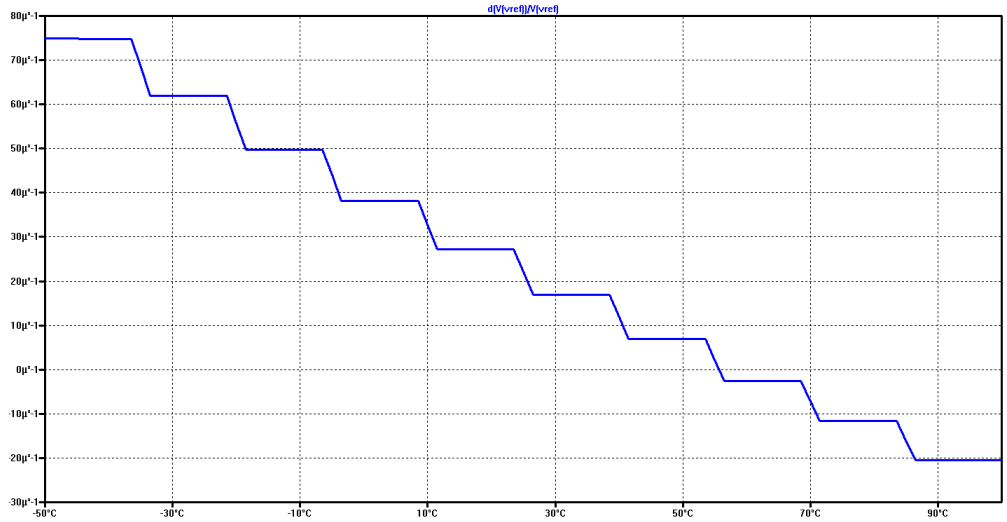

Fig. 32. Bandgap Voltage Reference Temperature Coefficient @ 20°C-Iteraton 2

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[1] R. Jacob Baker, "CMOS: Circuit Design, Layout, and Simulation", 3rd edition, Wiley-IEEE Press, 2010
[2] T. Chan Carusone, D. Johns, and K. Martin, "Analog Integrated Circuit Design," 2nd edition, J. Wiley & Sons, 2011.