Electronic Circuits
Chapter 3: Multistage Amplifier and Differential Amplifier

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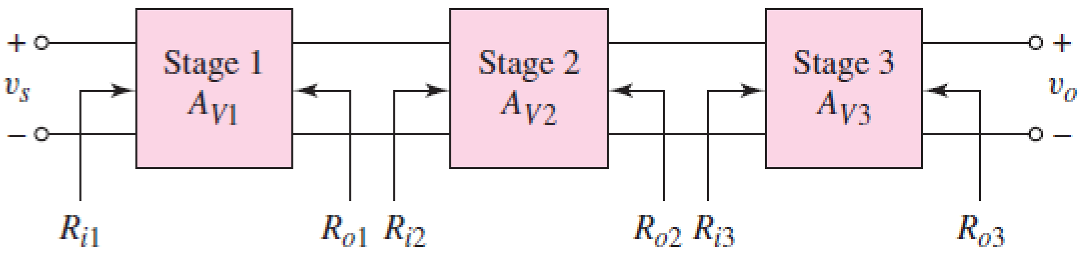
Content

Introduction

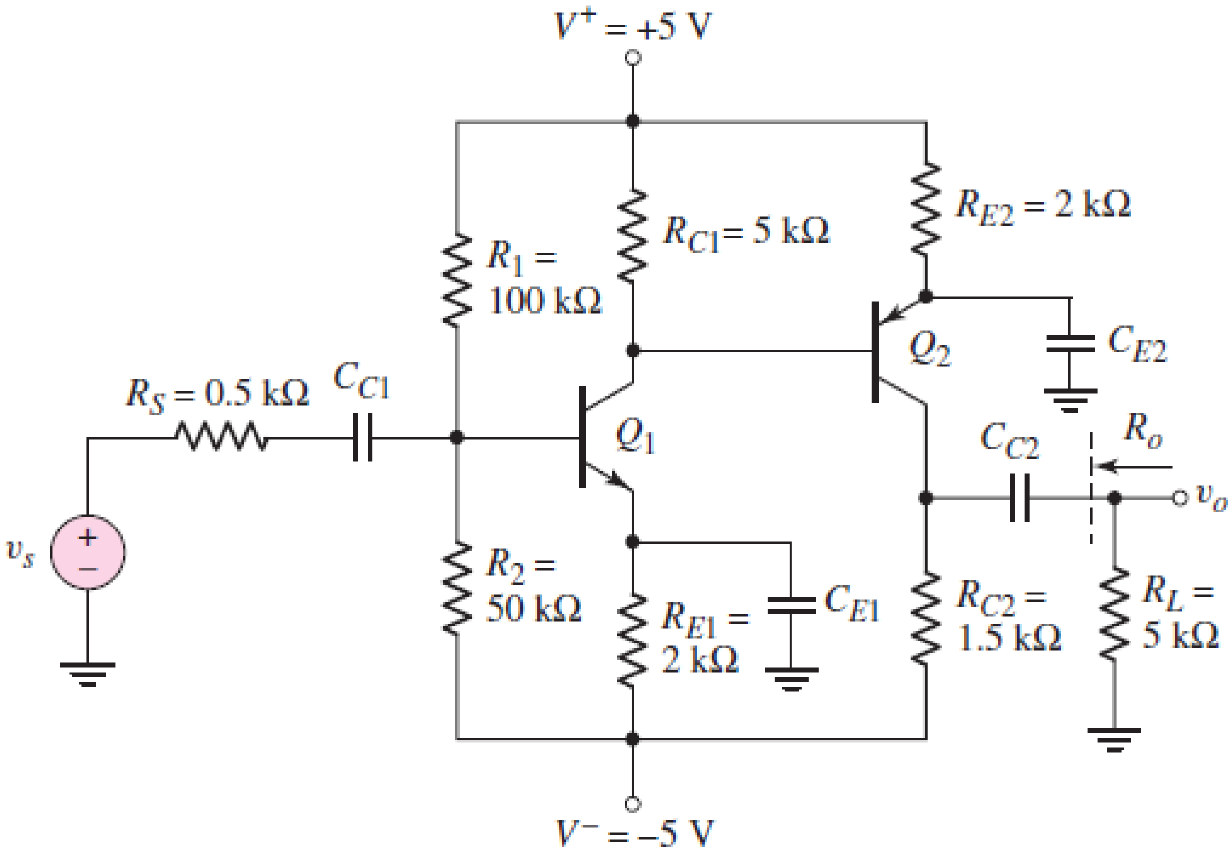
In most applications, a single transistor amplifier will not be able to meet the combined specifications of a given amplification factor, input resistance, and output resistance.



A generalized three-stage amplifier

Name	BJT		Comments
	1st stage	2nd stage	
Voltage Amp	CE	CE	High Voltage Gain
Cascode	CE	CB	High bandwidth
Op-Amp	CE	CC	High Zin low Zout
Current buffer	CB	CC	Higher Zout than CB/CG
Current buffer	CB	CE	
Not common	CB	CB	
Not common	CC	CE	
Differential Amp	CC	CB	High voltage gain and BW.
Darlington	CC	CC	High current gain

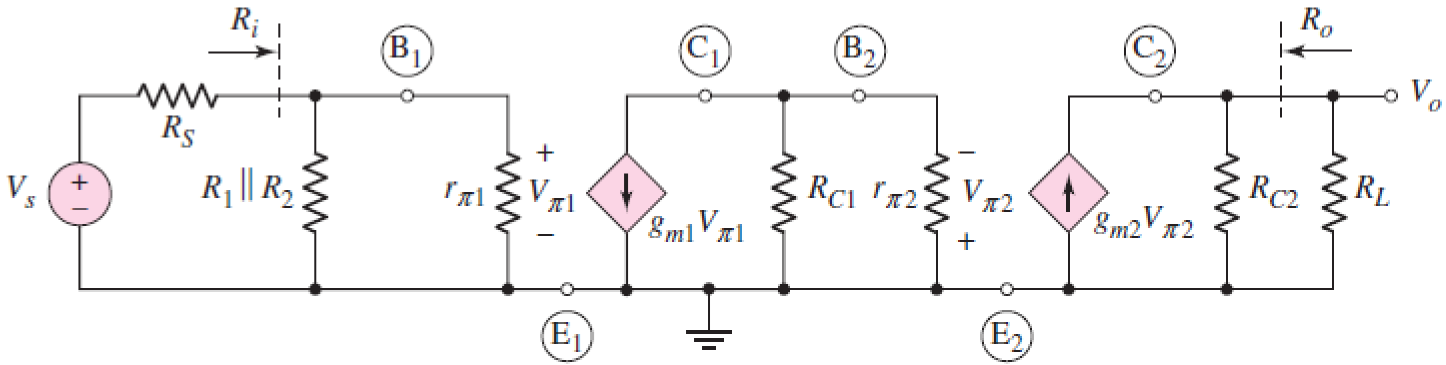
Cascade Configuration



A two-stage common-emitter amplifier in a cascade configuration with npn and pnp transistors

Cascade Configuration

❖ Two stage common-emitter amplifier in a cascade configuration: small signal equivalent circuit.



❖ Input resistance: $R_{in} = R_1 \parallel R_2 \parallel r_{\pi 1}$

❖ Small signal voltage gain:

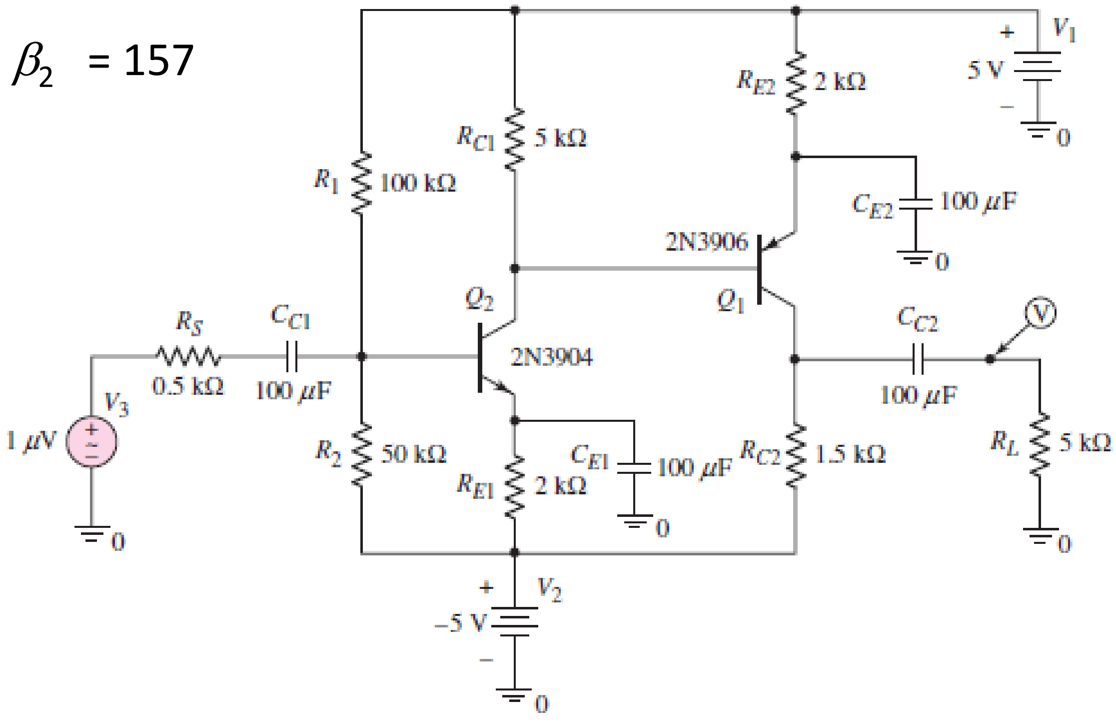
$$A_v = g_{m2}(R_2 \parallel R_L) g_{m1}(R_{C1} \parallel r_{\pi 2}) \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_s}$$

Cascade Configuration

Example 1: Determine the small-signal voltage gain of the following multi-transistor circuit:

$\beta_1 = 173$

$\beta_2 = 157$



$I_{CQ1} = 2.54$ mA

$I_{CQ2} = 1.18$ mA

$V_{C1} = -0.82$ V

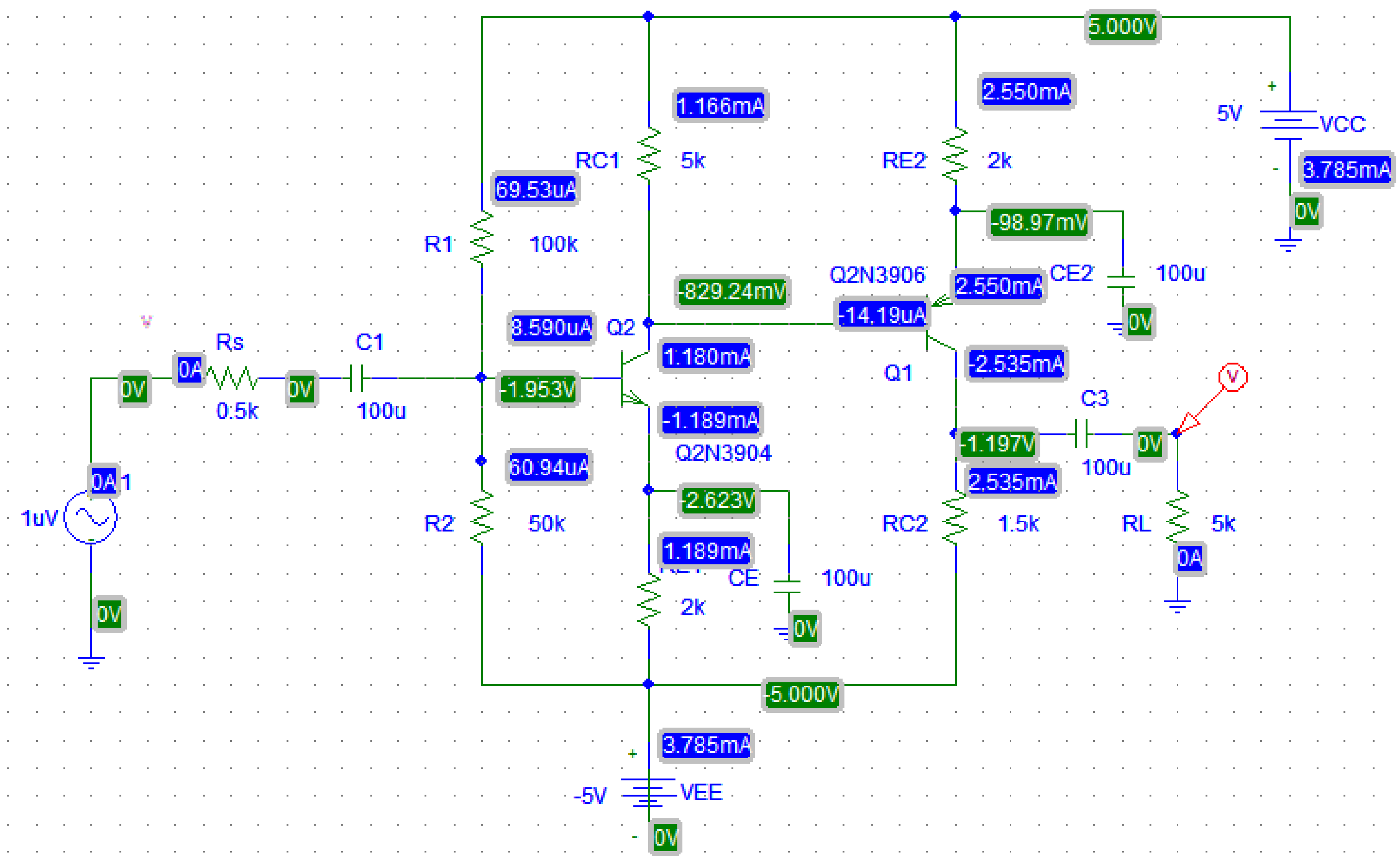
$V_{ECQ1} = 1.10$ V

$V_{CEQ2} = 1.79$ V

$G_V = 4790$

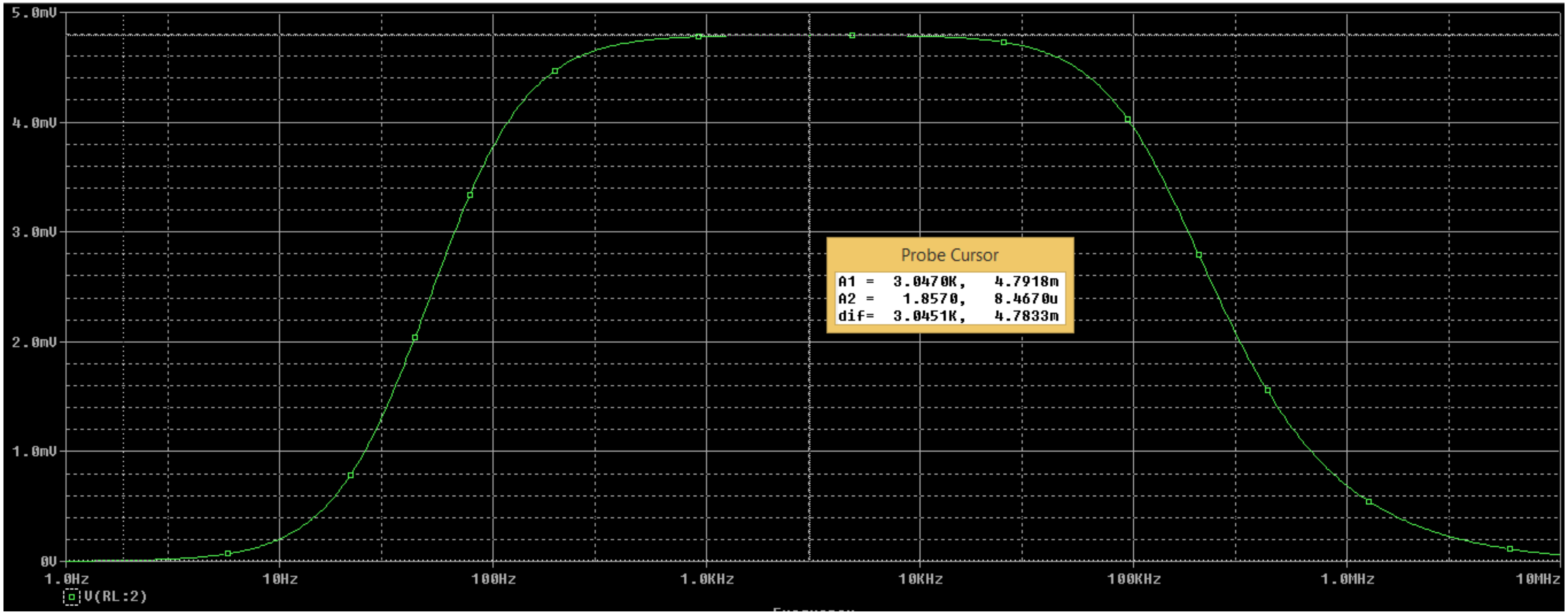
Cascade Configuration

Example 1: Determine the small-signal voltage gain of the following multi-transistor circuit:



Cascade Configuration

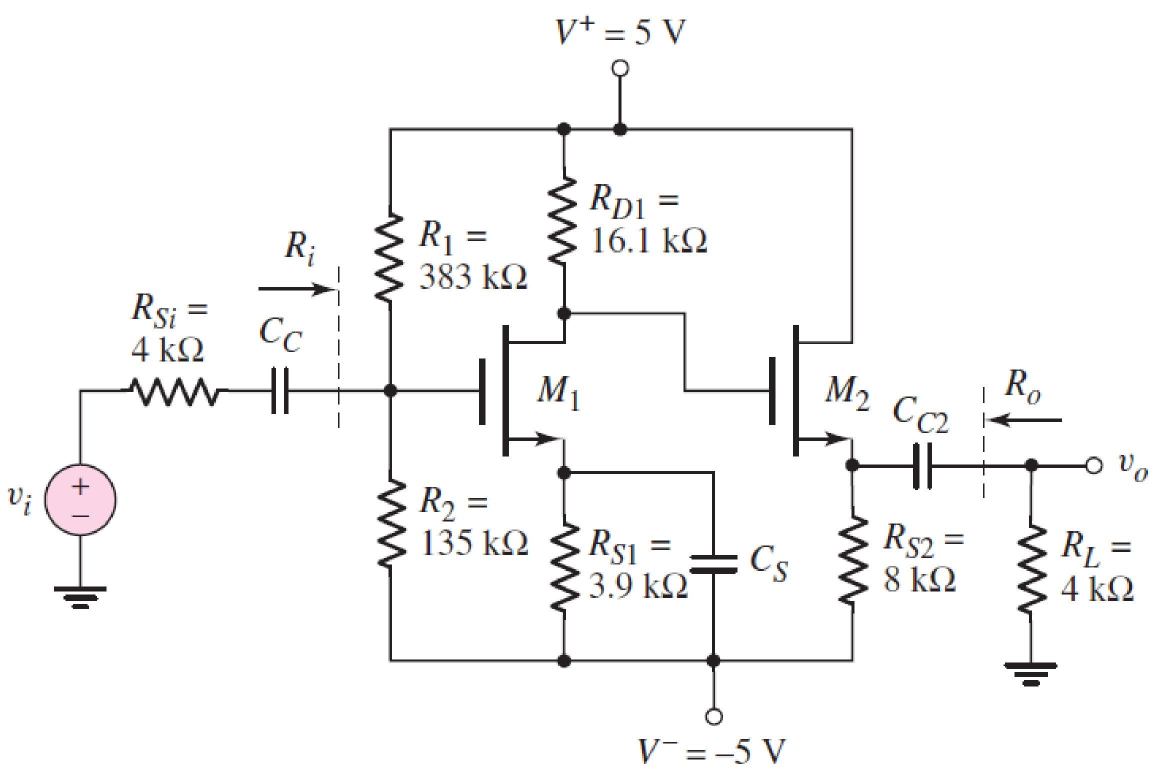
Example 1: Determine the small-signal voltage gain of the following multi-transistor circuit:



Cascade Configuration

Example 2: Consider the circuit shown in the following figure. The transistor parameters are $k_{n1} = 0.5mA/V^2$, $k_{n2} = 0.2mA/V^2$ and $V_{TN1} = V_{TN2} = 1.2V$. The Q point is: $I_{D1} = 0.2mA$, $I_{D2} = 0.5mA$.

Determine the small-signal voltage gain of a multistage cascade circuit.



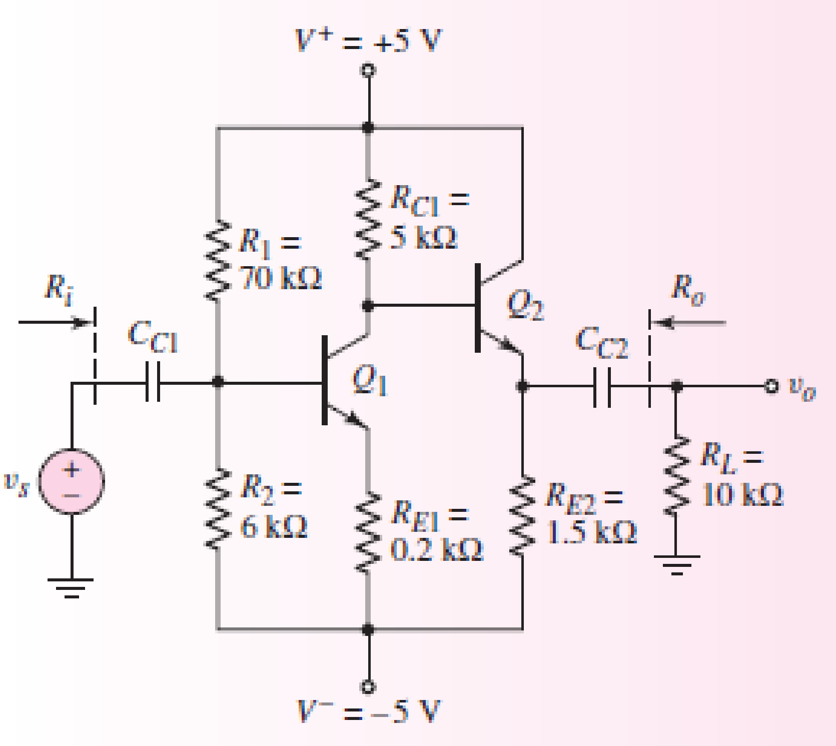
$G_v = -6.14$

Cascade Configuration

Exercise 1: Consider the circuit shown in the following figure. The transistor parameters are $\beta = 125$, $V_{BE}(on) = 0.7V$

a. Determine the small-signal voltage gain of the multistage cascade circuit.

b. Determine the input resistance and output resistance.

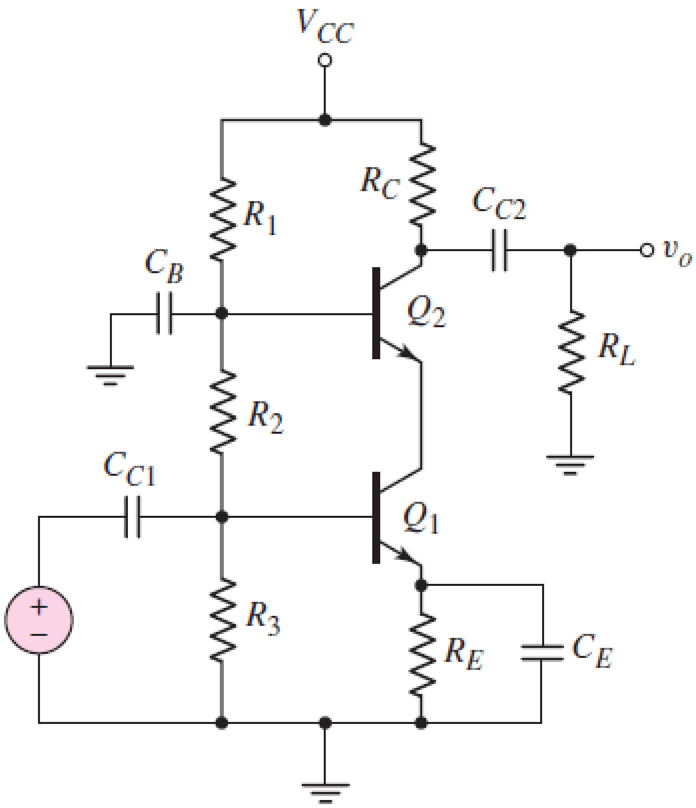


G_v = -17.7

R_{in} = 4.76 kΩ

R_o = 43.7 Ω

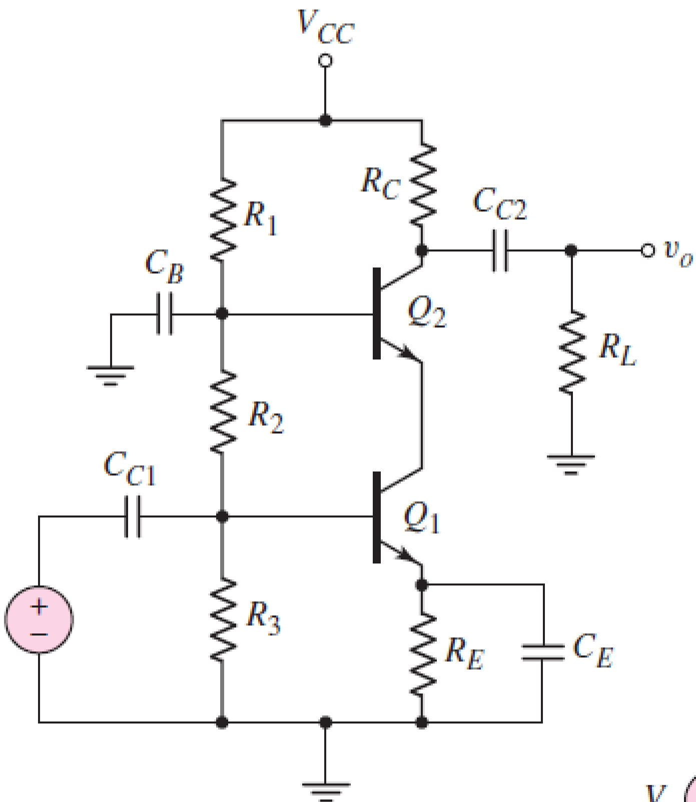
Cascode Configuration



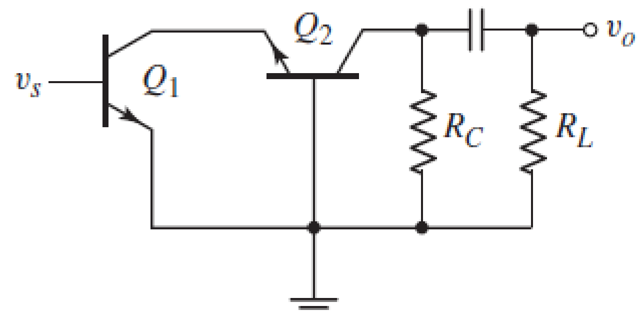
Cascode Amplifier

- In cascode configuration, a ***Common-Emitter (or Common-Source)*** amplifier drives a ***Common-Base (or Common-Gate)*** amplifier.
- The input capacitance of CE amplifier is small because the voltage gain of Q1 is small (near unity) which means the Miller capacitance is minimized.
- The CE stage increases the input impedance of the CB stage.
- The voltage gain is achieve in the Common-Base stage.

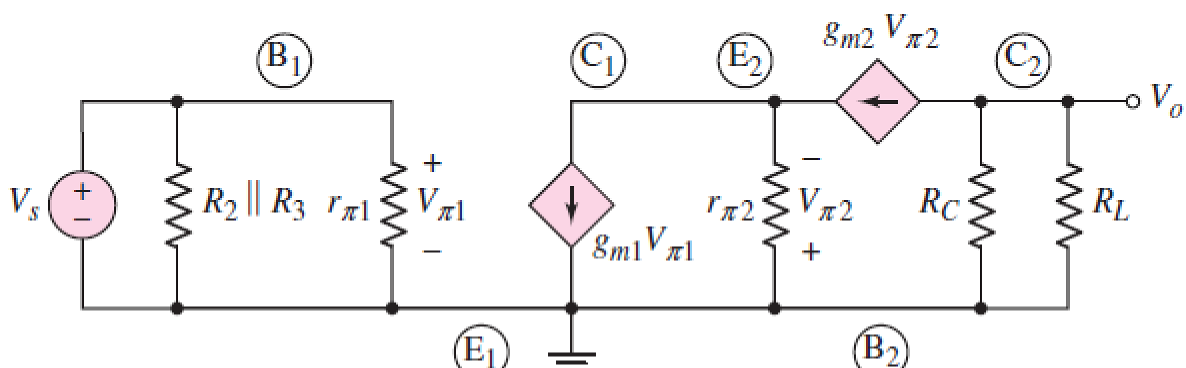
Cascode Configuration



Cascode Amplifier

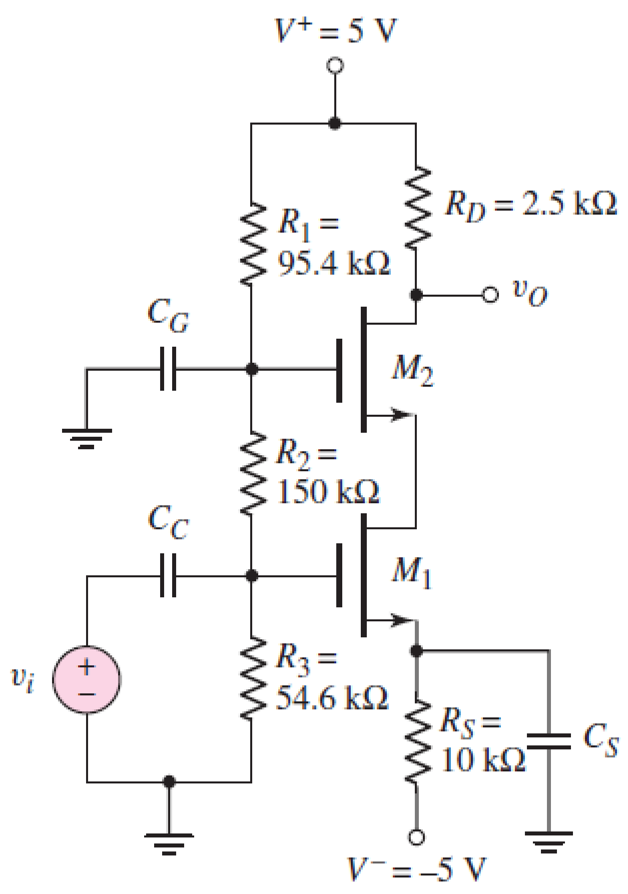


The ac equivalent circuit



The small-signal equivalent circuit

Cascode Configuration

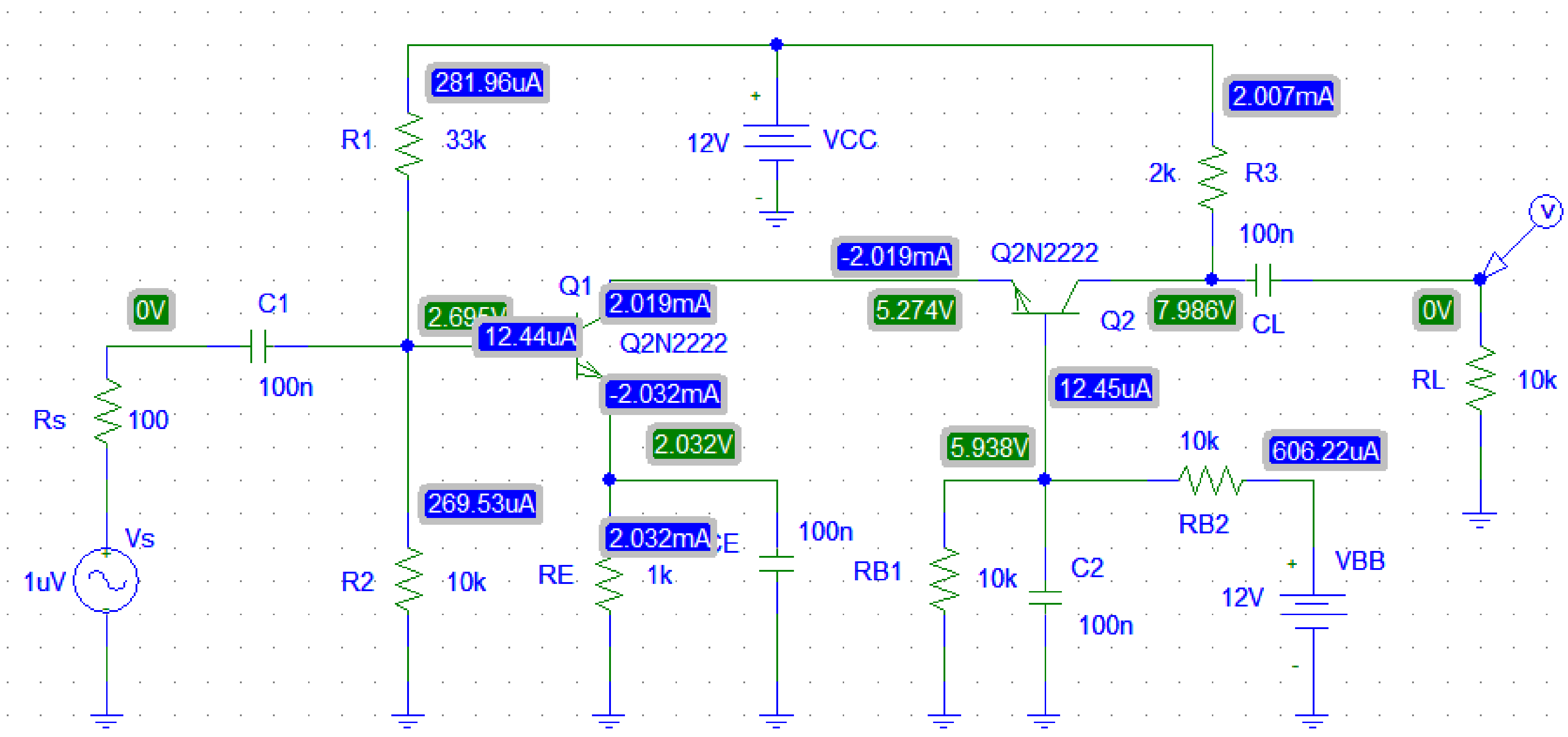


Example 2: Consider the circuit shown in the following figure. The transistor parameters are $k_{n1} = 0.8mA/V^2$, $k_{n2} = 0.8mA/V^2$ and $V_{TN1} = V_{TN2} = 1.2V$. The Q point is: $I_{D1} = 0.4mA$, $I_{D2} = 0.4mA$.

Determine the small-signal voltage gain of the cascode circuit.

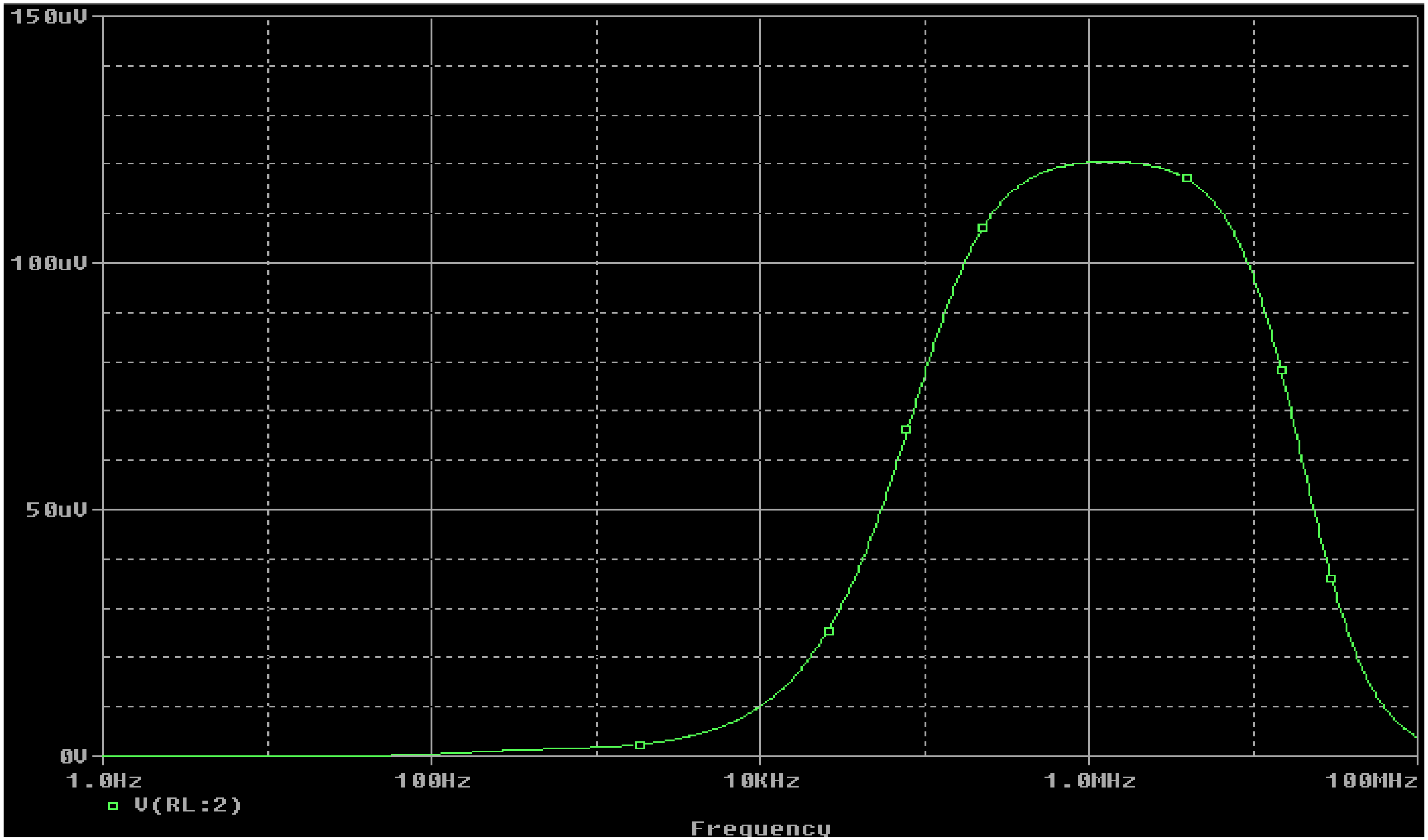
Cascode Configuration

PSPICE Simulation: Use PSPICE to run simulation for the following CE-CB (cascode) amplifier. The Beta DC of Q1,Q2 are 162 and 161 respectively. The mid-band gain of the amplifier from PSPICE is 120. Validate the DC and AC analysis of the amplifier using circuit analysis? Note that Beta AC gain of Q1, Q2 are 177 and 176 respectively.



Cascode Configuration

PSPICE Simulation: It is clear that the high-frequency (HF) 3dB cut-off frequency of the Cascode amplifier is much higher than that of the circuit in Example 1 (CE-CE Amplifier).



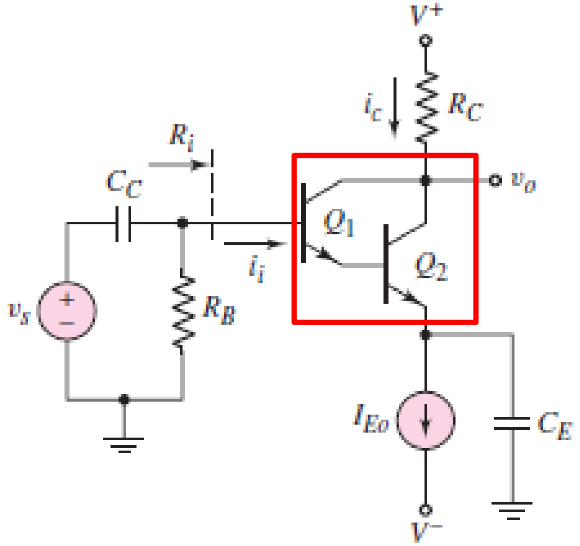
Darlington Pair

- In some applications, it would be desirable to have a bipolar transistor with a much larger current gain than can normally be obtained.
- A **Darlington configuration** provides increased current gain.
- The effective β of the Darlington pair is:

$$\beta_{DP} = \beta_1\beta_2 + \beta_1 + \beta_2$$

- Darlington pairs are often fabricated on a single chip to achieve matched Q_1 and Q_2 characteristics. Then:

$$\beta_{DP} = \beta^2 + 2\beta$$



A Darlington pair configuration

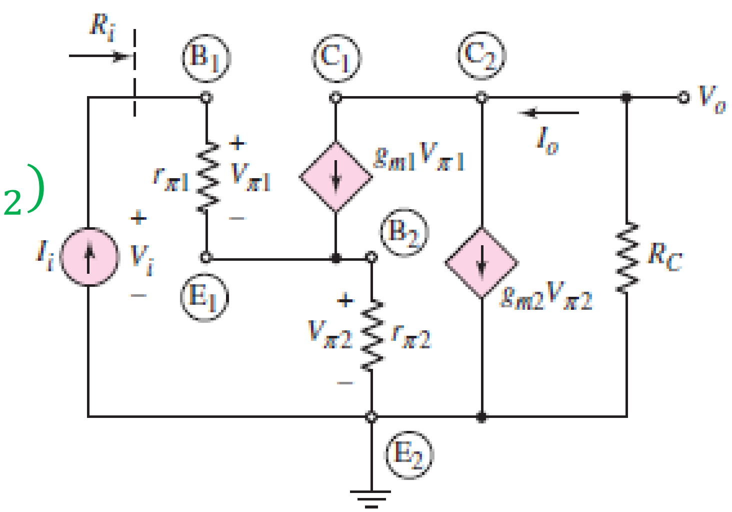
Darlington Pair

❖ The effective small-signal input resistance of the Darlington pair is:

$$r_{in(DP)} = \beta_1\left(r_{e1} + r_{in(base)2}\right) \simeq \beta_1(r_{e1} + \beta_2 r_{e2})$$

where:

$$r_{e1} = \frac{25mV}{I_{C1}} \qquad r_{e2} = \frac{25mV}{I_{C2}}$$



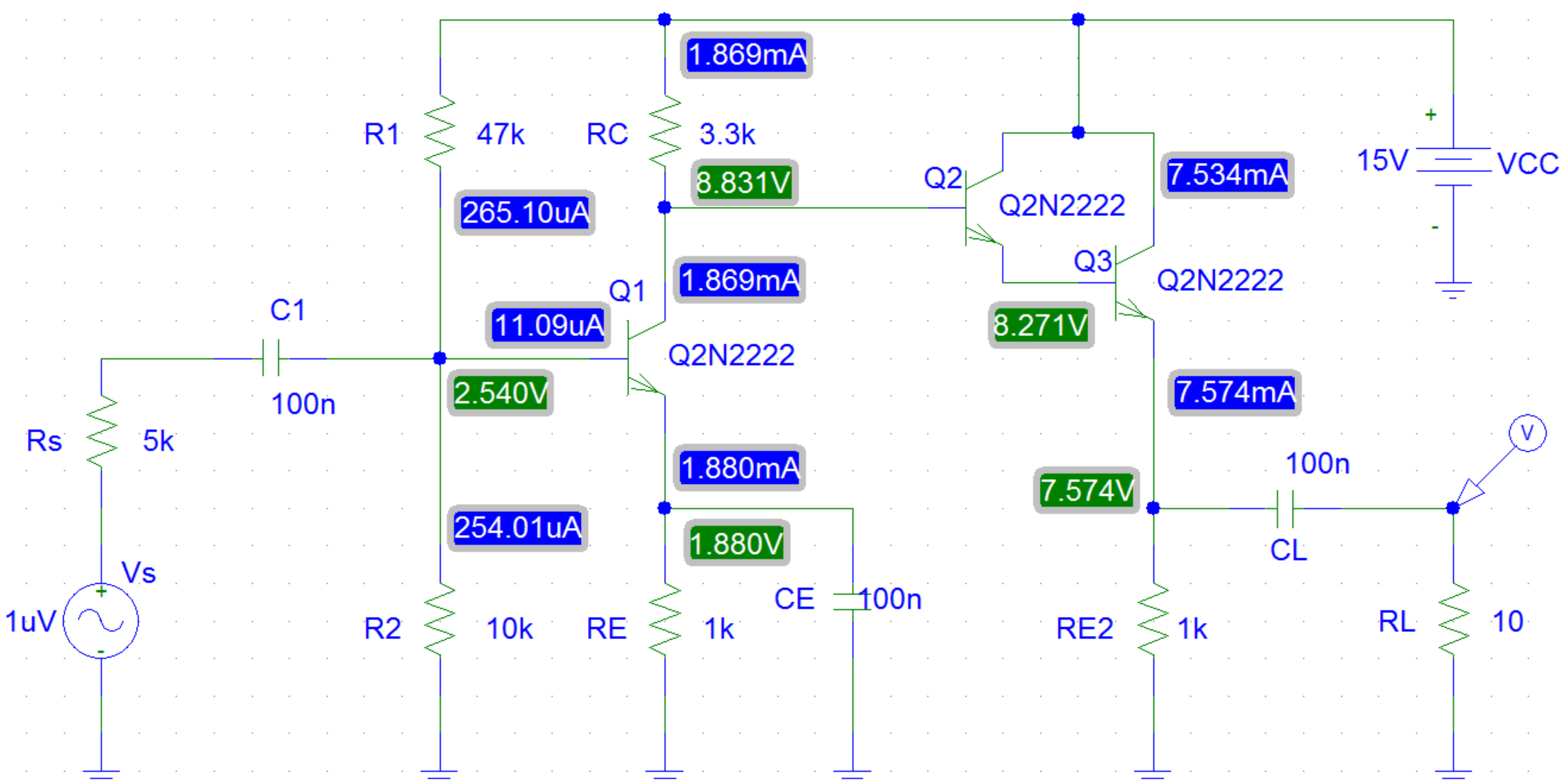
Small-signal equivalent circuit

❖ Note that: $I_{E2} \simeq \beta_2 I_{E1}$. Then: $r_{e1} \simeq \beta_2 r_{e2}$

❖ And: $r_{in(DP)} \simeq \beta_1(r_{e1} + \beta_2 r_{e2}) = 2r_{e2}$

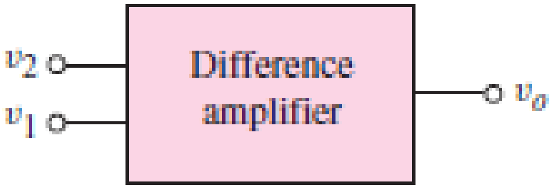
Darlington Pair

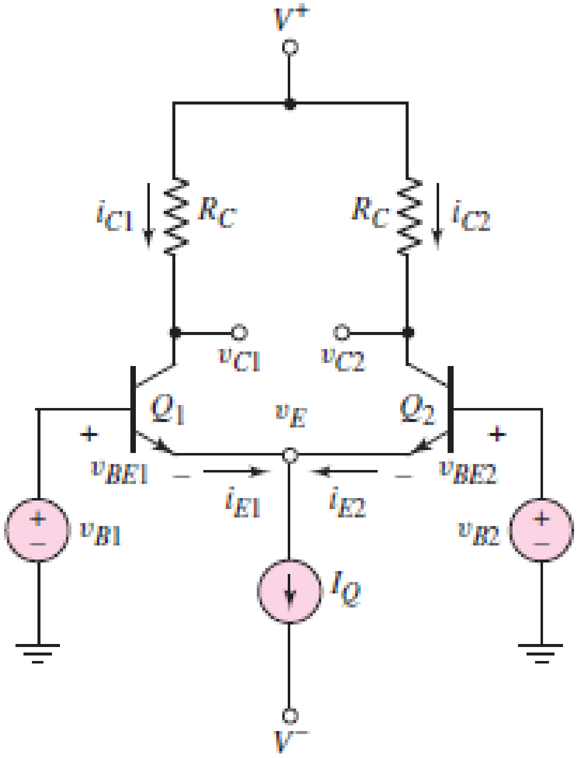
PSPICE Simulation: Use PSPICE to run simulation for the following CE-CC amplifier. The Beta DC gain of Q1,Q2 and Q3 are 168, 187 and 108 respectively. The mid-band gain of the amplifier from PSPICE is 26. Validate the DC and AC analysis of the amplifier using circuit analysis? Note that Beta AC gain of Q1, Q2 and Q3 are 184, 197 and 126 respectively.



Differential Amplifier

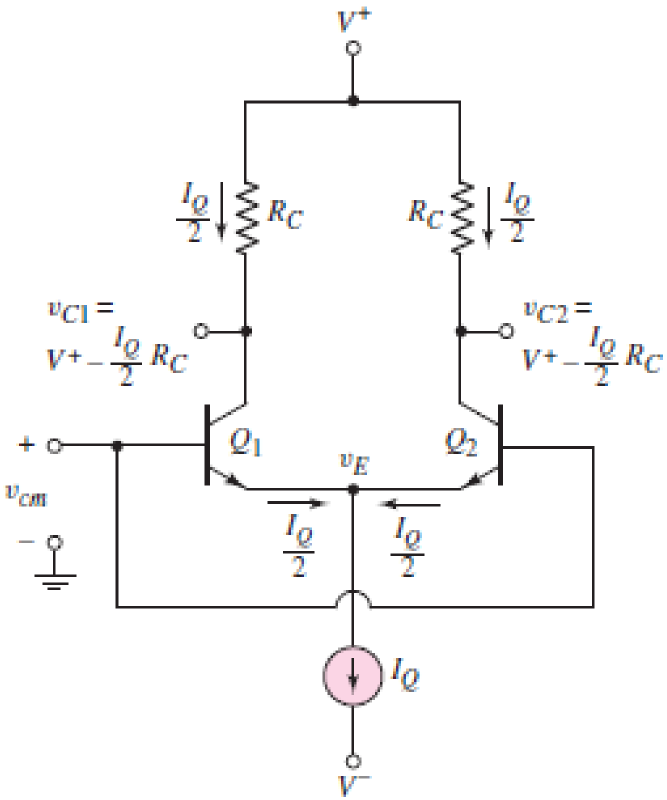
- The input stage of every op amp is a differential amplifier.
- Less sensitive to noise and interference.
- Enable to bias amplifier and connect to other stage without the use of coupling capacitors.





Differential Amplifier – DC Analysis

❖ Assume Q_1 and Q_2 are matched.

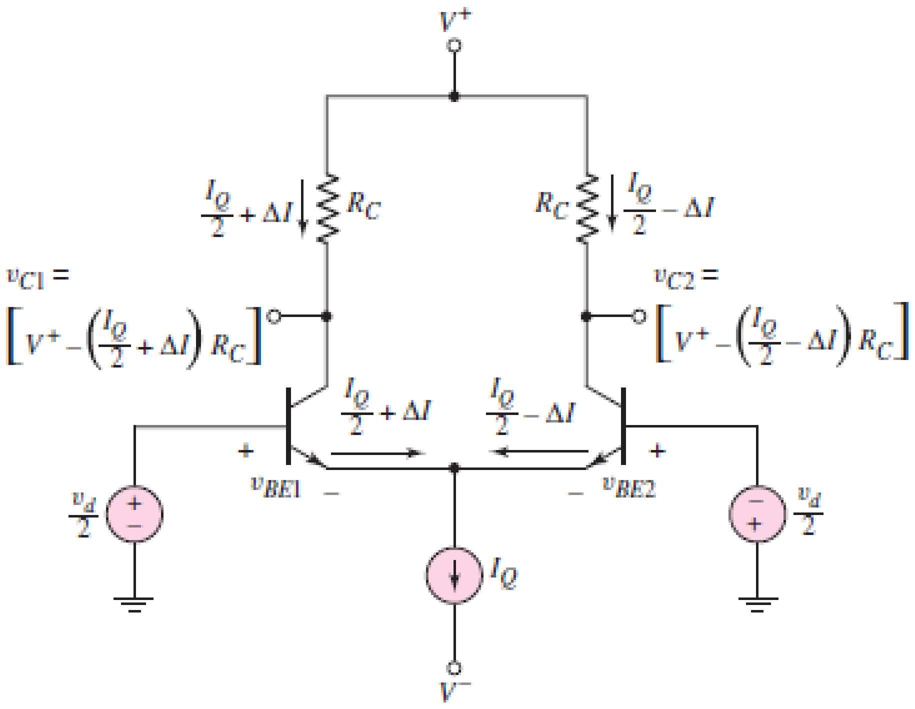


$$I_{E1} = I_{E2} = \frac{I_Q}{2}$$

$$v_{C1} = v_{C2} = V^+ - \frac{I_Q}{2} R_C$$

Diffrential Amp – Small Signal Operation

❖ If $v_{id} \neq 0$:



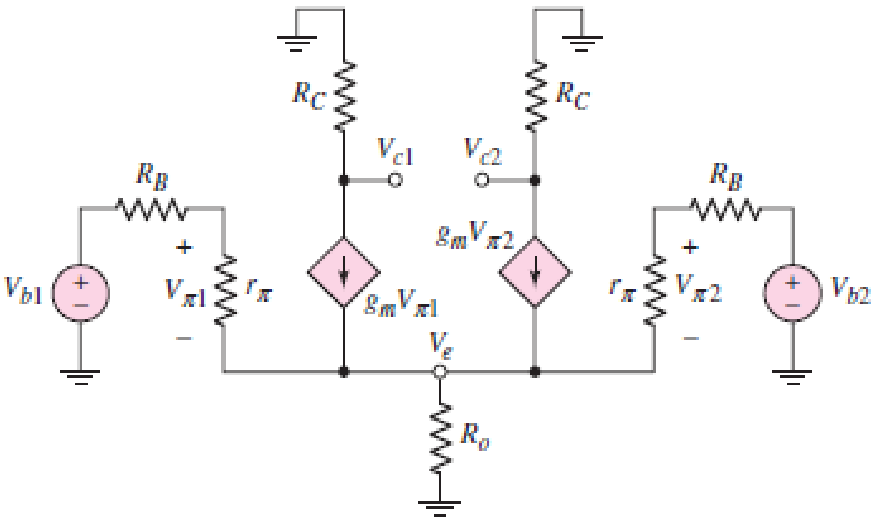
$$v_{C1} = \left[V^+ - \left(\frac{I_{CQ}}{2} + \Delta I\right) R_C\right]$$

$$v_{C2} = \left[V^+ - \left(\frac{I_{CQ}}{2} - \Delta I\right) R_C\right]$$

$$v_{C1} - v_{C2} = 2\Delta I R_C$$

Diffrential Amp – Small Signal Operation

❖ If $v_{id} \neq 0$:



❖ Since the two transistors are biased at the same quiescent current:

$$r_{\pi 1} = r_{\pi 2} = r_\pi \qquad g_{m1} = g_{m2} = g_m$$

❖ At node V_e:

$$\frac{V_{\pi 1}}{r_\pi} + g_m V_{\pi 1} + g_m V_{\pi 2} + \frac{V_{\pi 2}}{r_\pi} = \frac{V_e}{R_o}$$

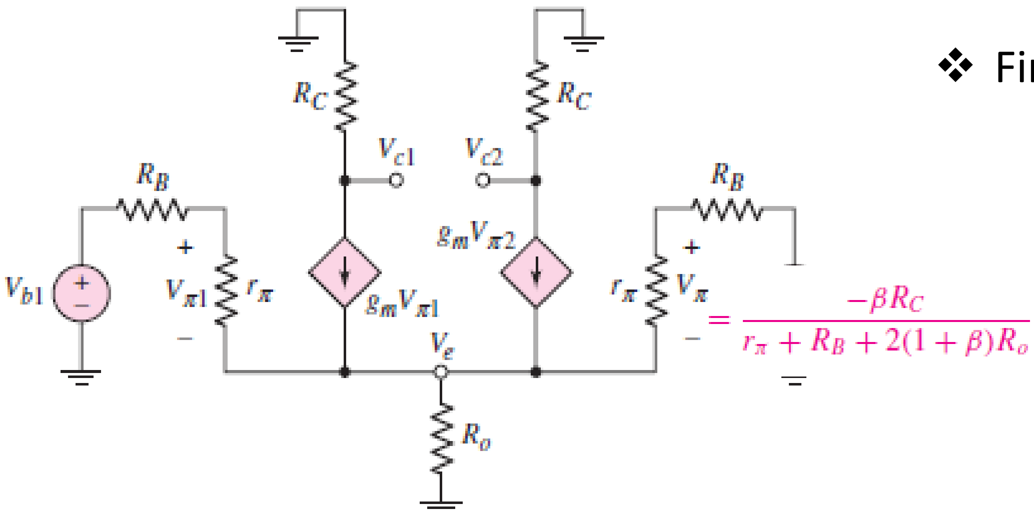
or: $$V_{\pi 1}\left(\frac{1+\beta}{r_\pi}\right) + V_{\pi 2}\left(\frac{1+\beta}{r_\pi}\right) = \frac{V_e}{R_o}$$

❖ From the circuit we see that:

$$\frac{V_{\pi 1}}{r_\pi} = \frac{V_{b1} - V_e}{R_B + r_\pi} \quad \text{and} \quad \frac{V_{\pi 2}}{r_\pi} = \frac{V_{b2} - V_e}{R_B + r_\pi}$$

Diffrential Amp – Small Signal Operation

❖ If $v_{id} \neq 0$:



❖ Finally we have:

$$(V_{b1} + V_{b2} - 2V_e)\left(\frac{1+\beta}{r_\pi + R_B}\right) = \frac{V_e}{R_o}$$

$$V_e = \frac{V_{b1} + V_{b2}}{2 + \frac{r_\pi + R_B}{(1+\beta)R_o}}$$

❖ One-sided output:

$$v_{b1} = v_{cm} + \frac{v_d}{2} \qquad v_{b2} = v_{cm} - \frac{v_d}{2} \qquad V_o = V_{c1} - V_{c2}$$

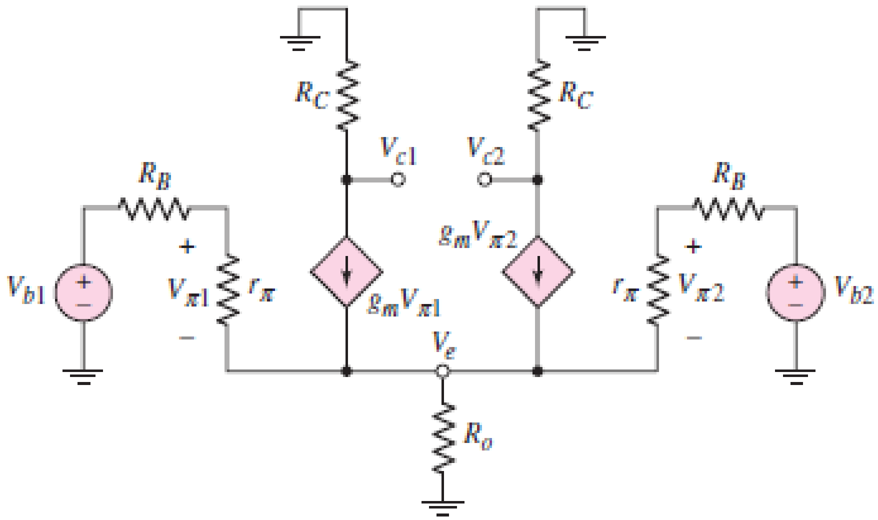
$$A_d = \frac{\beta R_C}{2(r_\pi + R_B)} \qquad A_{cm} = \frac{-\beta R_C}{r_\pi + R_B + 2(1+\beta)R_o}$$

❖ Two-sided output:

$$A_d = \frac{\beta R_C}{r_\pi + R_B} \qquad A_{cm} = 0$$

Diffrential Amp – Small Signal Operation

❖ *Two-sided output: Effect of R_C mismatch*



$$V_o = V_{c1} - V_{c2}$$

$$= -g_m V_{\pi 2} R_{C2} + g_m V_{\pi 1} R_{C1}$$

$$A_d = g_m R_C$$

$$A_{cm} = g_m(2\Delta R_C)\frac{1}{1 + \dfrac{2(1+\beta)R_o}{r_\pi}} \approx \frac{\Delta R_C}{R_o}$$

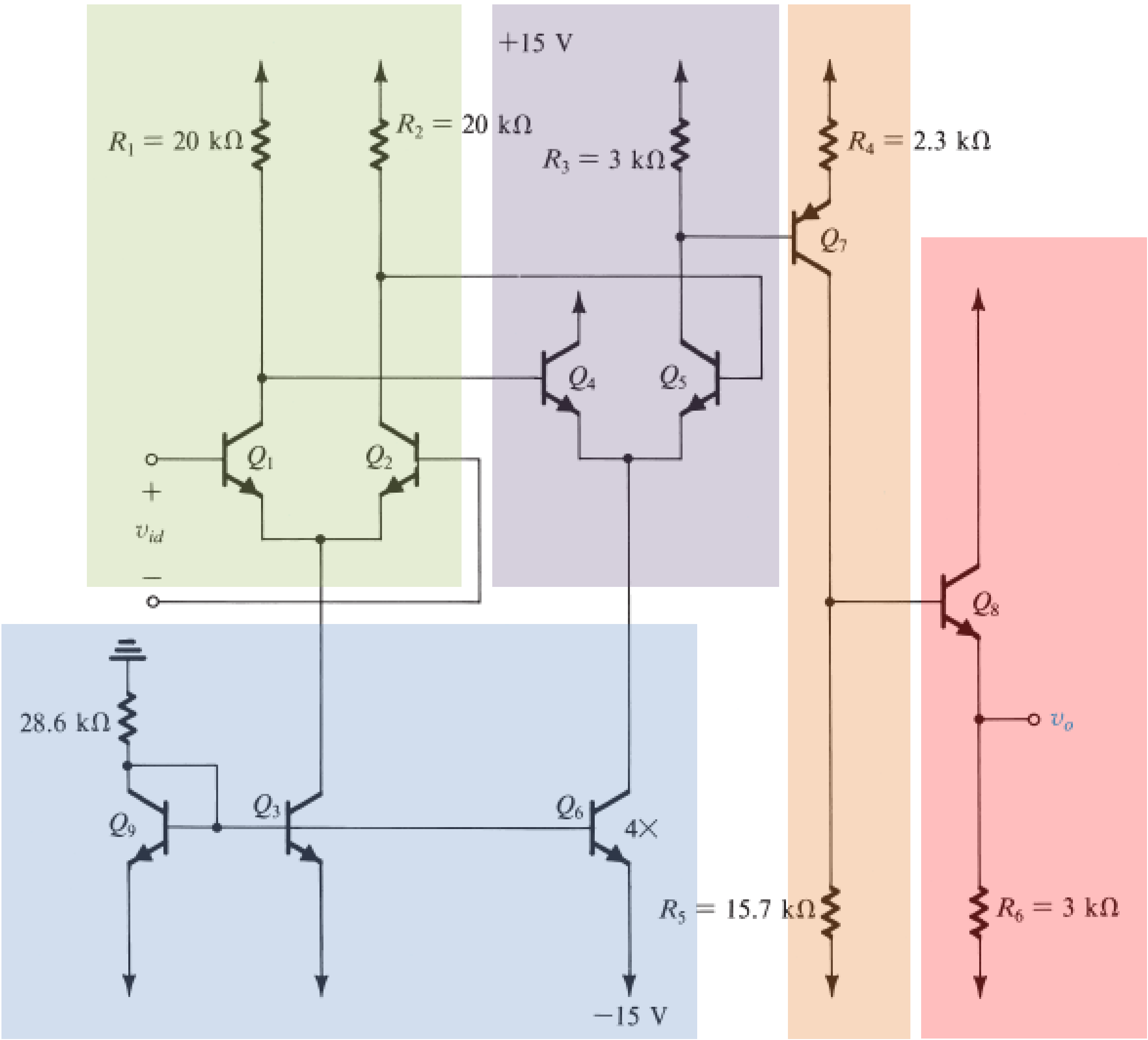
❖ The Common Mode Rejection Ratio (CMRR) is:

$$CMRR = \left|\frac{A_d}{A_{cm}}\right| = \frac{g_m R_o}{\Delta R_C / R_C}$$

Operational Amplifiers

- Practical transistor amplifiers *consist of a number of stages* connected in cascade.
- In addition to providing gain, the first (or input) stage is usually required to:
  - Provide a high input resistance.
  - In a differential amplifier the input stage must also provide large CMRR.
  - The middle stages of an amplifier cascade is to provide the bulk of the voltage gain.
  - The middle stages convert the signal from differential mode to single-ended mode.
  - The middle stages also shift the DC level of the signal in order to allow the output signal to swing both positive and negative .
  - The last (or output) stage of an amplifier is to provide a low output resistance.
- In order to illustrate the circuit structure an method of analysis, two examples: a CMOS Op-Amp and a bipolar Op-Amp will be investigated.

A Bipolar OpAmp



Current Source

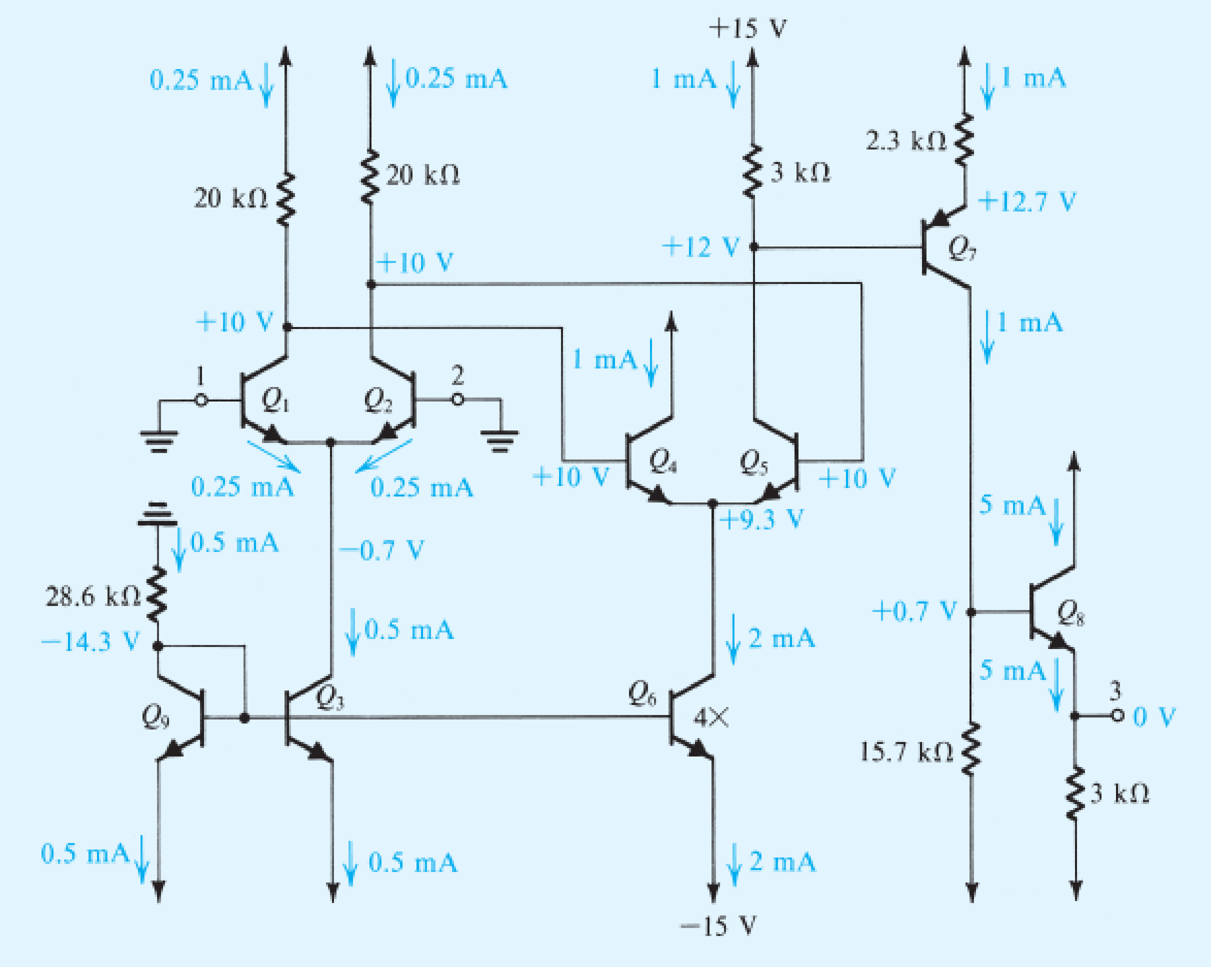
Differential Amplifier

Conversion from differential to single-ended

Shifting DC level

Emitter Follower (CC) Amplifier: Voltage Buffer

A Bipolar OpAmp – DC Analysis



Example 2:

a. Perform DC Analysis of the bipolar Op-Amp.

b. Determine the small-signal voltage gain, input resistance and output resistance of the circuit.

$R_{id} = 20.2k\Omega$

$R_o = 152\Omega$

$G_V = 8513$

Q&A