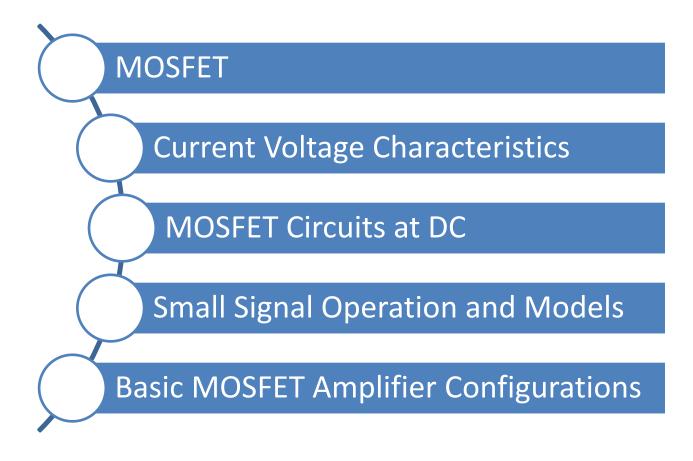
Electronic Circuits Chapter 3: FET

Dr. Dung Trinh

Content

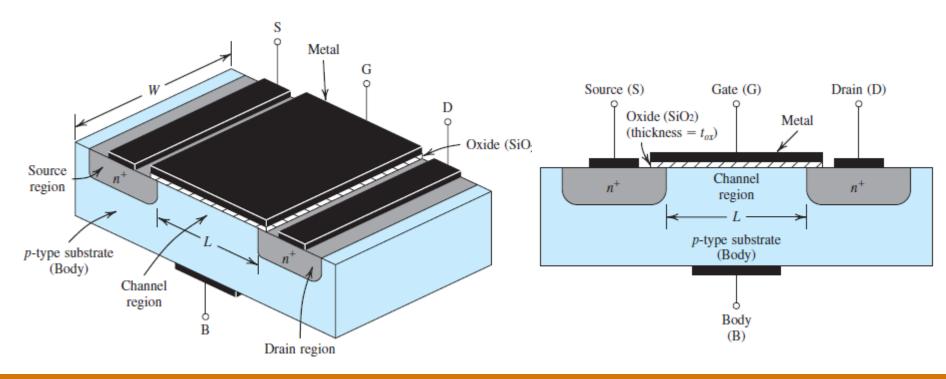


MOSFET

- * MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor.
- According to the physics of the device, we can classify transistors into two main classes:
 - Field Effect Transistors (FET): Conduction is controlled by electric field which is produced by voltage applied to the control terminals. So, the control draws no current and FET is a voltage- controlled device.
 - ➤ Bipolar Junction Transistors (BJT): Diode-based device which is usually blocked unless the control terminals are forward- biased. So, the control is a current, and BJT is a current amplifier by nature.

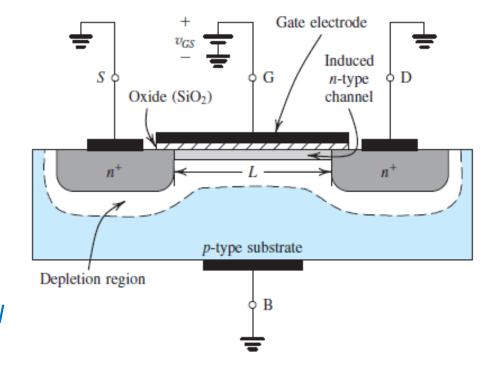
MOSFET

- **❖ MOSFET** is a four-terminal device: gate (G), source (S), drain (D) and body (B).
- * Two kinds of MOSFETs: n-channel (NMOS) and p-channel (PMOS) devices.
- ❖ The device structure is basically symmetric in terms of drain and source.
- ❖ Source and drain terminals are specified by the operation voltage.



MOSFET

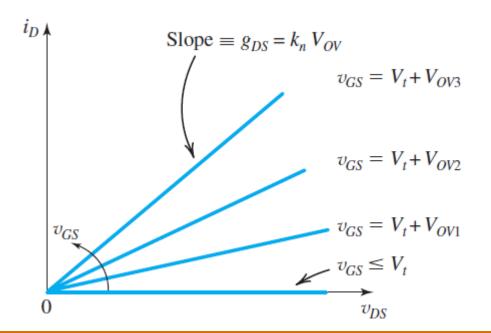
- ❖ Gate voltage exceeds a threshold voltage $v_{GS} > V_t$: electrons start to accumulate on the substrate surface. $V_t = 0.3 \div 1$ (V)
- The positive $v_{GS} > V_t$ is used to induce the channel and it is called n-channel enhancement type MOSFET.
- The induced n region forms a channel for current flow from drain to source.

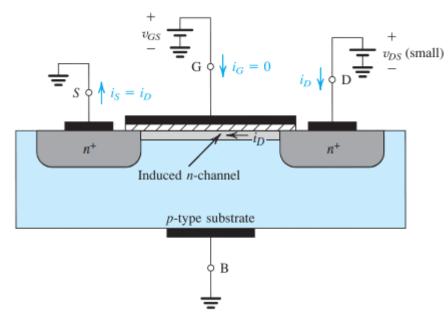


The field controls the amount of charge in the channel and determines the channel conductivity.

$\mathsf{MOSFET}-\mathsf{Small}\ v_{DS}$

- $ightharpoonup Small v_{DS}$ is applied: free electrons travel from source to drain through the induced n-channel.
- \bullet The resulting current i_D flows from drain to source (opposite to the direction of the flow of negative charge).



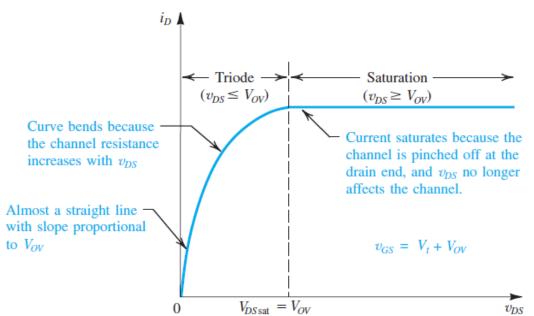


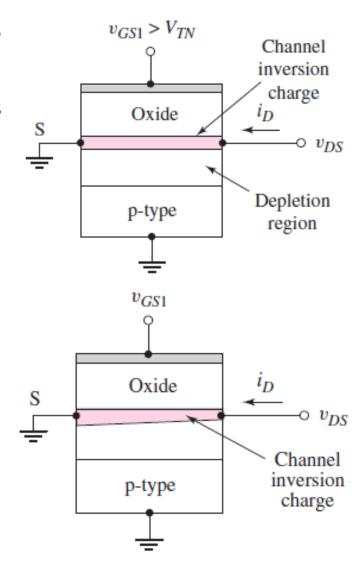
- ightharpoonup The resulting current i_D flows from drain to source (opposite to the direction of the flow of negative charge).
- The channel is controlled by the effective voltage or overdrive voltage:

$$V_{OV} = V_{GS} - V_t$$

MOSFET – Increasing v_{DS}

- \diamond As v_{DS} is increased, the channel becomes more tapered and its resistance increases correspondingly.
- \diamond At the point $v_{DSsat} = v_{GS} V_t$, the channel is pinched off at the drain side.
- \diamond Triode region: $v_{DS} < v_{DSsat}$
- ❖ Saturation region: $v_{DS} ≥ v_{DSsat}$





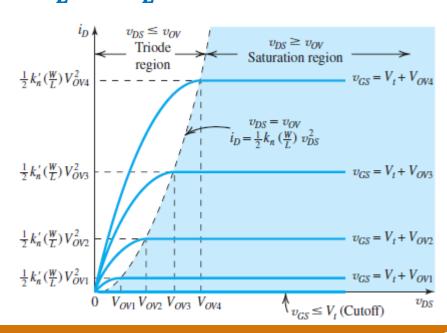
MOSFET – IV Relationship

- ❖ Triode region: $i_D = k_n \left[(v_{GS} V_t) v_{DS} \frac{1}{2} v_{DS}^2 \right]$
- Saturation region: $i_{Dsat} = \frac{1}{2} k_n (v_{GS} V_t)^2$
- Arr Channel resistance: $r_{DS} = \frac{1}{k_n(v_{GS} V_t)}$
- Transconductance parameter: $k_n = \mu_n C_{ox} \frac{W}{L} = k_n' \frac{W}{L}$ where:

 C_{ox} : oxide capacitance per unit area.

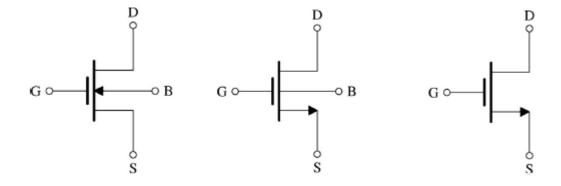
 μ_n : mobility of electron in the inversion layer.

W and L: channel width and length.

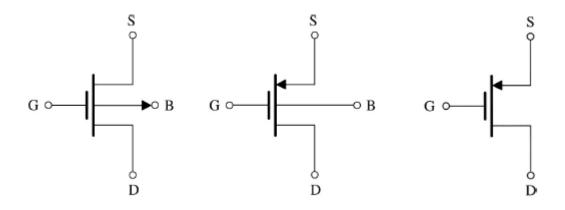


MOSFET – Circuit Symbols

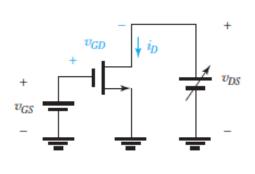
❖ n-channel enhancement-mode MOSFET:

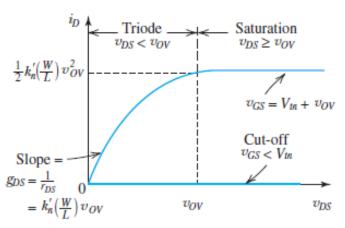


***** p-channel enhancement-mode MOSFET:

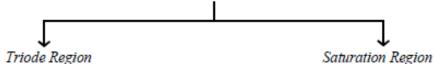


NMOS – Current Voltage Characteristics





- v_{GS} < V_{tn}: no channel; transistor in cut-off; i_D = 0
- v_{GS} = V_{tn} + v_{OV}: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched-off at the drain end;



Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then.

$$i_D = k'_n \left(\frac{\vec{W}}{I}\right) \left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2 \right]$$

or equivalently,

$$i_D = k'_n \left(\frac{W}{L}\right) \left(v_{OV} - \frac{1}{2}v_{DS}\right) v_{DS}$$

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \ge v_{OV}$$

Then

$$i_D = \frac{1}{2}k'_n \left(\frac{W}{L}\right) (v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2} k'_n \left(\frac{\overline{W}}{L} \right) v_{OV}^2$$

MOSFET - Current Voltage Characteristics

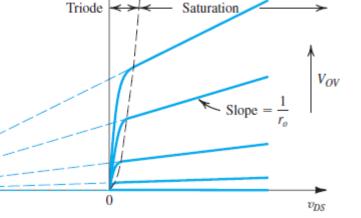
Example 1: Consider an NMOS transistor fabricated in a L = $0.18\mu m$ process with L = $0.18\mu m$ and W = $2\mu m$. The process technology is specified to have $C_{ox} = 8.6 \text{ fF}/\mu m^2$, $\mu_n = 450 \text{ cm}^2/Vs$ and $V_{tn} = 0.5V$.

- a. Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D=100\mu A$.
- b. If V_{GS} is kept constant, find V_{DS} that results in $I_D = 50 \mu A$.
- c. To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS}=0.3V$. Find the change in i_D resulting from V_{GS} changing from 0.7V by +0.01V and by -0.01V.

MOSFET – Finite Output Resistance

- $ightharpoonup In practice, increasing <math>v_{DS}$ beyond v_{OV} does affect the channel somewhat.
- This effect can be accounted for i_D in the expression for by including a factor $(1 + \lambda v_{DS})$:

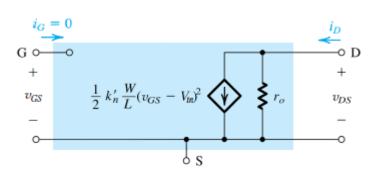
$$i_{Dsat} = \frac{1}{2}k_n(v_{GS} - V_t)^2(1 + \lambda v_{DS})$$



 \diamond Defining the output resistance r_o as

$$r_o \equiv \left[\frac{\partial v_{DS}}{\partial i_D} \right]_{v_{GS=const}} = \frac{V_A}{I_D}$$

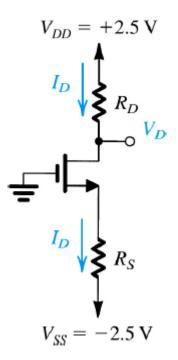
$$V_A = \frac{1}{\lambda}$$



MOSFET Circuits at DC

- DC analysis for MOSFET circuits:
 - Assume the operation mode and solve the dc bias utilizing the corresponding current equation.
 - Verify the assumption with terminal voltages (cutoff, triode and saturation).
 - If the solution is invalid, change the assumption of operation mode and analyze again.

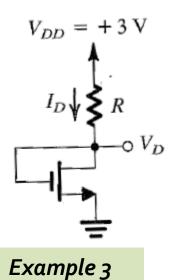
Example 2: The NMOS transistor in the following circuit has $V_t=0.7V$, $\mu_n C_{ox}=100\mu \text{A}/V^2$, $L=1\mu m$ and $W=32\mu m$. Design the circuit so that the transistor operates at $I_D=0.4mA$ and $V_D=0.5V$.



MOSFET Circuits at DC

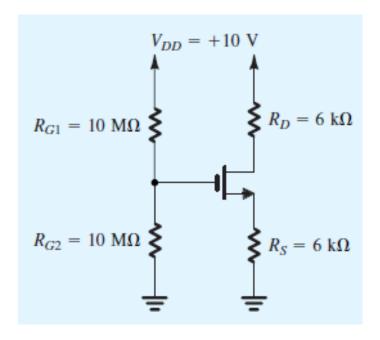
Example 3: The NMOS transistor in the following circuit has $V_t = 0.6V$, $\mu_n C_{ox} = 200 \mu A/V^2$, $L = 0.8 \mu m$ and $W = 4 \mu m$. Design the circuit so that the transistor operates at $I_D = 80 \ \mu A$. Find the DC voltage V_D .

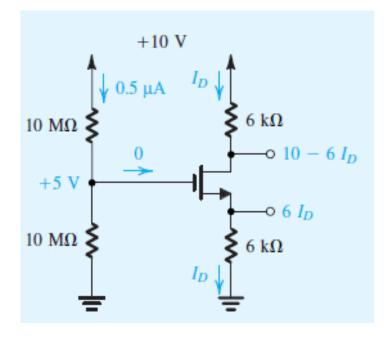
Example 4: Design the circuit so that the transistor operates at $V_D = 0.1V$. Let $V_t = 1V$, $k_n = 1 \text{mA}/V^2$. Find the effective resistance between drain and source at this operating point.



MOSFET Circuits at DC

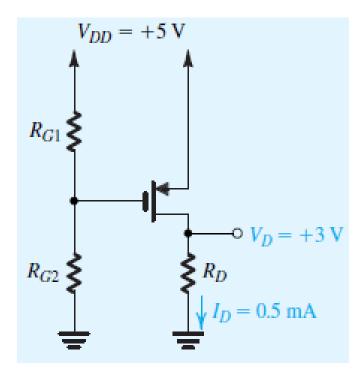
Example 5: Determine the voltage and the current of all nodes and branches? $V_t = 1V$, $k_n = 1mA/V^2$





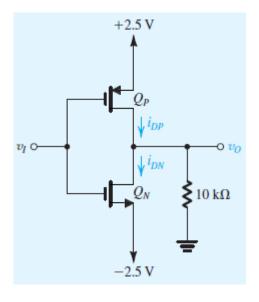
MOSFET Circuits at DC

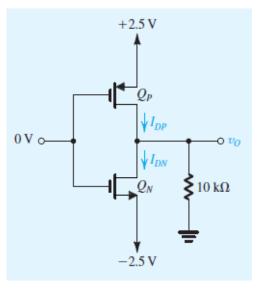
Example 6: Design the following circuit so that the transistor operates in saturation with $I_D=0.5mA$ and $V_D=3V$. Let the enhancement-type PMOS transistor have $V_{tp}=-1V$ and $k_p'\frac{W}{L}=1mA/V^2$. Assume $\lambda=0$. What is the largest value that R_D can have while maintaining saturation-region operation?

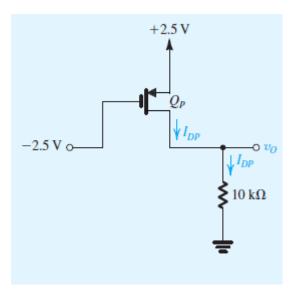


MOSFET Circuits at DC

Example 7: The NMOS and PMOS transistors in the following circuit are matched, with $k_n' \frac{W}{L} = k_p' \frac{W}{L} = 1mA/V^2$ and $V_{tn} = -V_{tp} = 1V$. Assume $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} as well as the voltage v_o for $v_I = 0V$, 2.5V and -2.5V.

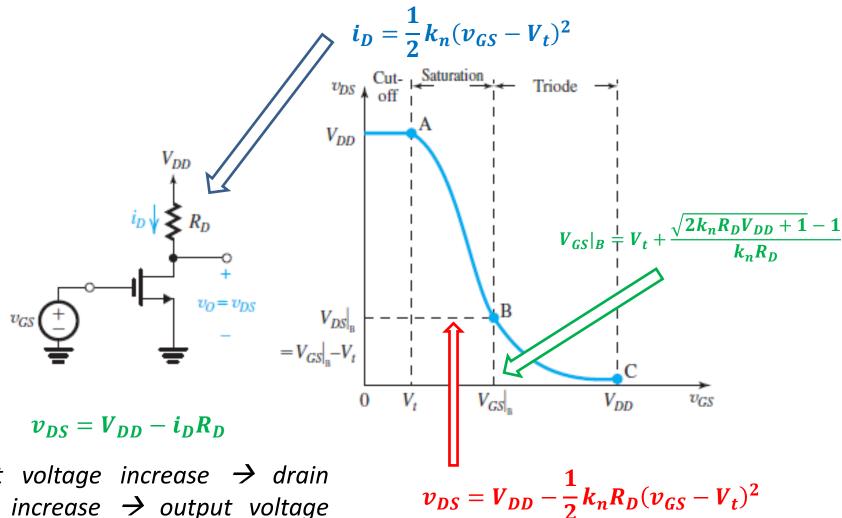






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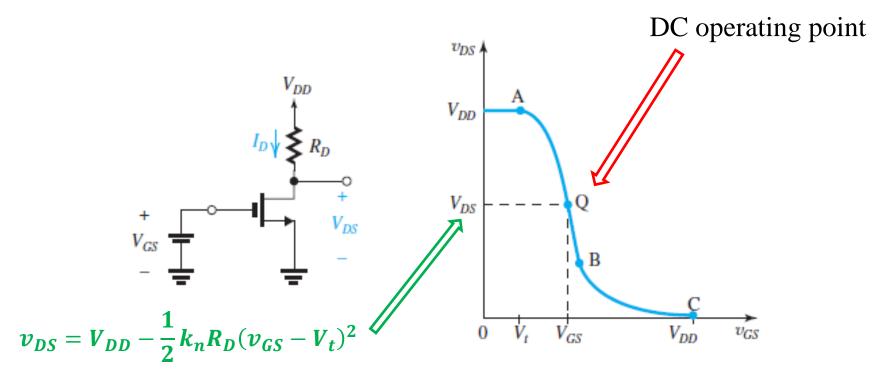
MOSFET in Amplifier Design



❖ Input voltage increase → drain current increase → output voltage decrease.

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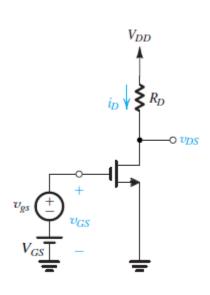
MOSFET in Amplifier Design



 \diamond The signal to be amplified, $v_{gs}(t)$, a function of time t, is superimposed on the bias voltage. Thus the total instantaneous value of becomes:

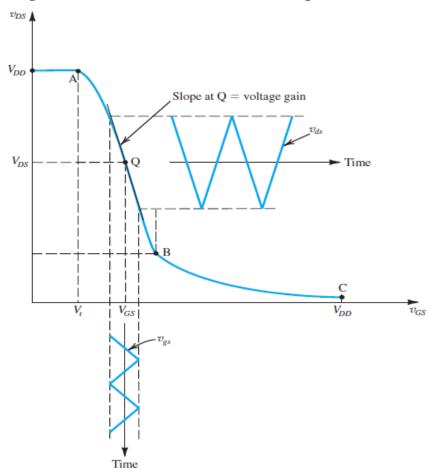
$$v_{GS}(t) = V_{GS} + v_{gs}(t)$$

MOSFET in Amplifier Design



 \bullet The signal to be amplified, $v_{gs}(t)$, a function of time t, is superimposed on the bias voltage. Thus the total instantaneous value of becomes:

$$v_{GS}(t) = V_{GS} + v_{gs}(t)$$

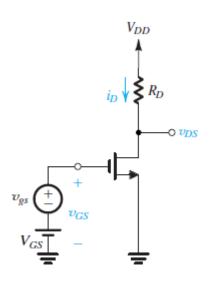


$$A_{v} \equiv \frac{\partial v_{DS}}{\partial v_{GS}}|_{v_{GS}=V_{GS}} = -k_{n}(V_{GS}-V_{t})R_{D}$$

MOSFET in Amplifier Design

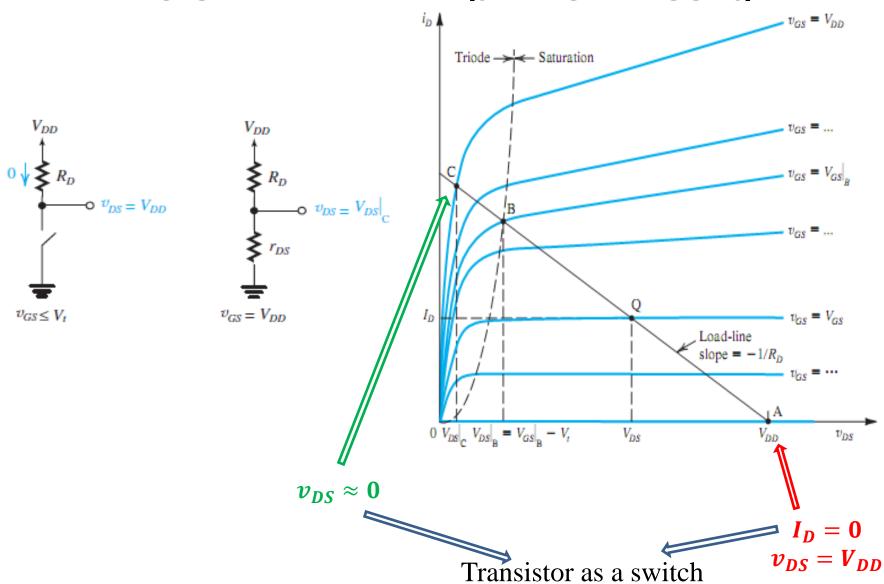
Example 8: The transistor is specified to have $V_t = 0.4V, k'_n = 0.4mA/V^2, W/L = 10, V_{DD} = 1.8V, R_D = 17.5k\Omega, V_{GS} = 0.6V.$

- a. For $v_{qs}=0$, find V_{OV} , I_{D} , V_{DS} and A_{v} .
- b. What is the maximum symmetrical signal swing allowed at the drain? Hence find the maximum allowable amplitude of a sinusoidal v_{GS} .

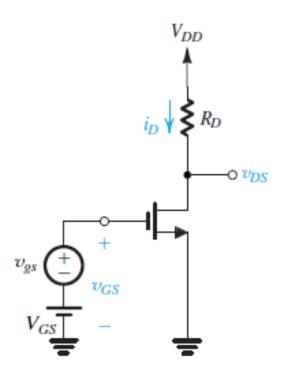


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MOSFET in Amplifier Design



Small Signal Operation and Models



The DC bias point:

$$I_D = \frac{1}{2}k_n(V_{GS} - V_t)^2 = \frac{1}{2}k_nV_{OV}^2$$

$$V_{DS} = V_{DD} - R_D I_D$$

lacktriangle When the input signal v_{gs} applied

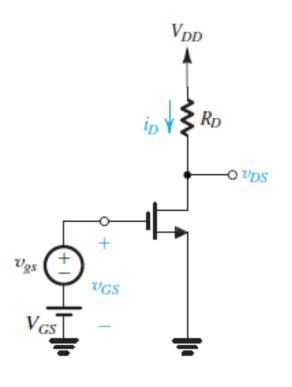
$$i_D = \frac{1}{2}k_n(V_{GS} + v_{gs} - V_t)^2$$

$$= \frac{1}{2}k_n(V_{GS} - V_t)^2 + k_n(V_{GS} - V_t)v_{gs} + \frac{1}{2}k_nv_{gs}^2$$

• In order to reduce the non-linear distortion: $\frac{1}{2}k_nv_{gs}^2 \ll k_n(V_{GS}-V_t)v_{gs}$

$$\leftrightarrow v_{qs} \ll 2(V_{GS} - V_t)$$

Small Signal Operation and Models



$$A_v \equiv \frac{v_{ds}}{v_{gs}} = -g_m R_D$$

❖ If the small signal condition is satisfied:

$$i_D = \frac{1}{2}k_n(V_{GS} - V_t)^2 + k_n(V_{GS} - V_t)v_{gS} = I_D + i_d$$

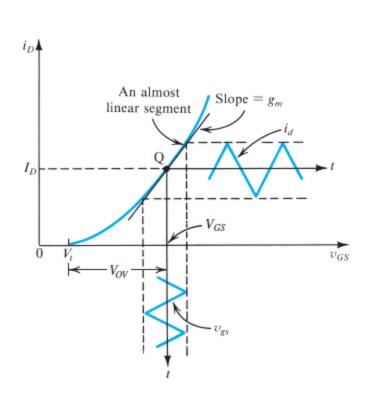
riangle The MOSFET transconductance g_m :

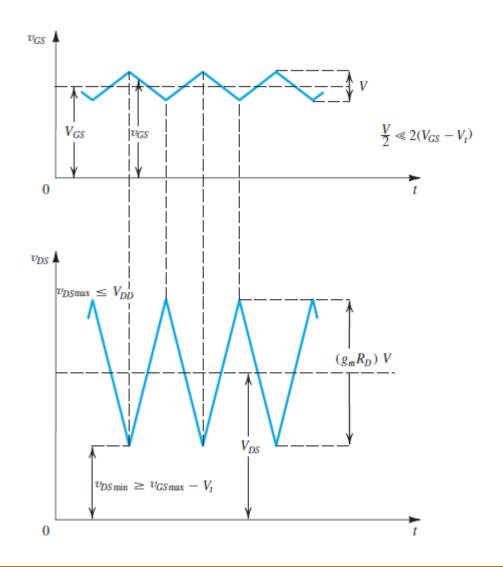
$$g_m \equiv \frac{i_d}{v_{qs}} = k_n (V_{GS} - V_t)$$

❖ Voltage gain:

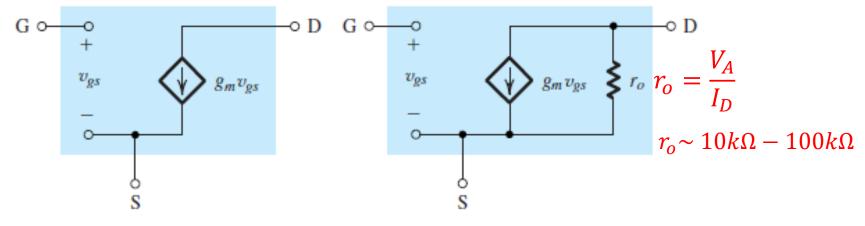
$$v_{DS} = V_{DD} - i_D R_D = V_{DD} - (I_D + i_d) R_D$$
$$= V_{DS} - i_d R_D$$

Small Signal Operation and Models





Small Signal Model

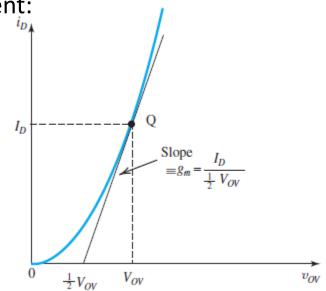


 \clubsuit The current I_D is the value of the dc drain current:

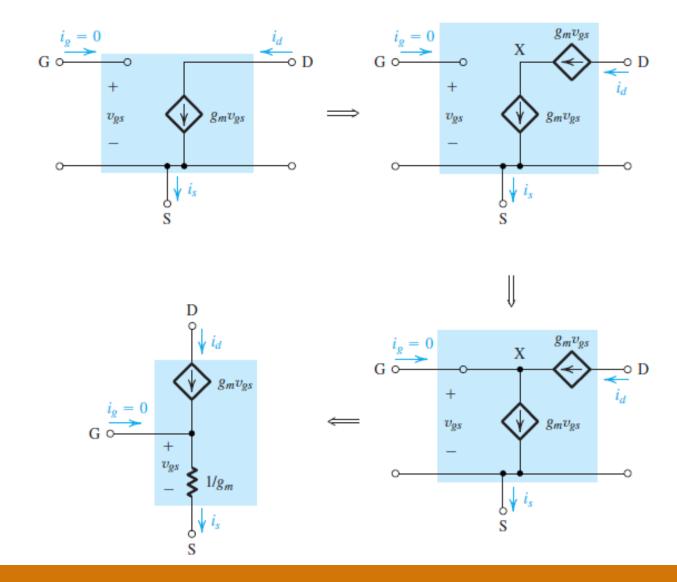
$$I_D = \frac{1}{2}k_n(V_{GS} - V_t)^2 = \frac{1}{2}k_nV_{OV}^2$$

 \clubsuit The trans-conductance g_m :

$$g_m = k_n V_{OV} = k'_n (W/L) V_{OV} = \frac{2I_D}{V_{OV}}$$

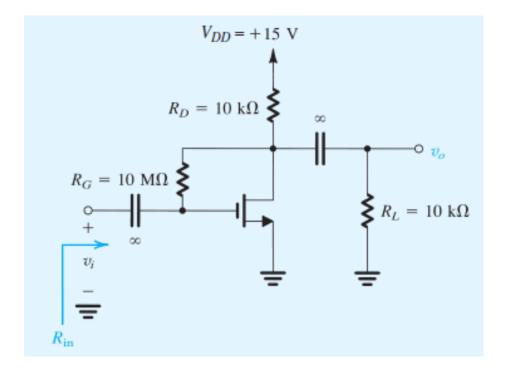


Small Signal Model – T model



Small Signal Model

Example 9: A discrete common-source MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. The transistor has $V_t = 1.5 \, V$, $k_n'W/L = 0.25 mA/V^2$ and $V_A = 50 V$. Determine its small-signal voltage gain and its input resistance.



Summary

Small-Signal Parameters

NMOS transistors

Transconductance:

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{OV}}$$

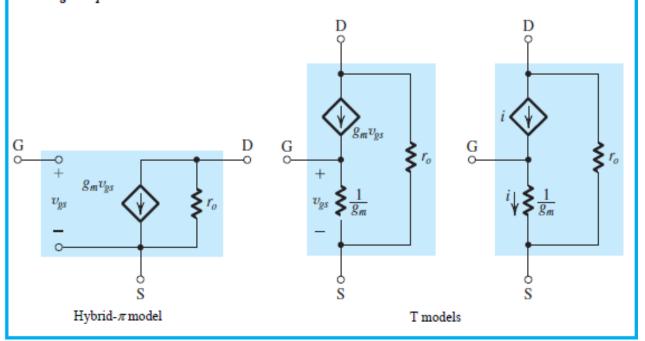
Output resistance:

$$r_o = V_A/I_D = 1/\lambda I_D$$

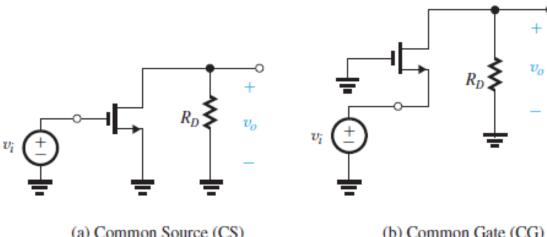
PMOS transistors

Same formulas as for NMOS except using $|V_{ov}|$, $|V_A|$, and replacing μ_n with μ_n .

Small-Signal Equivalent Circuit Models

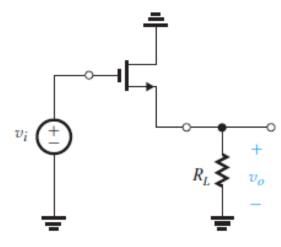


The Three Basic Configurations



(a) Common Source (CS)

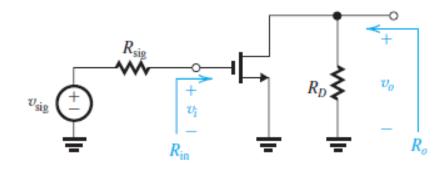
(b) Common Gate (CG)

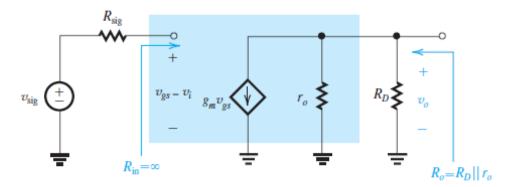


(c) Common Drain (CD)

Common Source Amplifier

- ❖ The common source is the most widely used.
- ❖ The bulk of the voltage gain is obtained by using one or more Common Source stages in the cascade.





Characteristic Parameters of the CS Amplifier:

Open circuit voltage gain:

$$A_{v0} = -g_m(R_D \parallel r_o) \approx -g_m R_D$$

Overall voltage gain:

$$G_{v} = -g_{m}(R_{D} \parallel r_{o} \parallel R_{L})$$

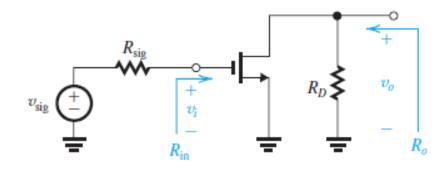
Input resistance:

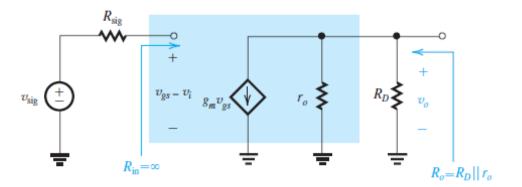
$$R_{in} = \infty$$

$$R_{out} = R_D \parallel r_o \approx R_D$$

Common Source Amplifier

- ❖ The common source is the most widely used.
- ❖ The bulk of the voltage gain is obtained by using one or more Common Source stages in the cascade.





Characteristic Parameters of the CS Amplifier:

Open circuit voltage gain:

$$A_v = -g_m(R_D \parallel r_o) \approx -g_m R_D$$

Overall voltage gain:

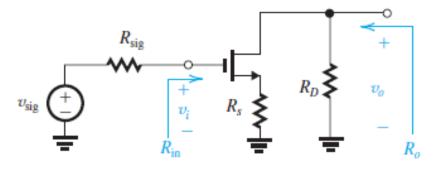
$$G_{v} = -g_{m}(R_{D} \parallel r_{o} \parallel R_{L})$$

Input resistance:

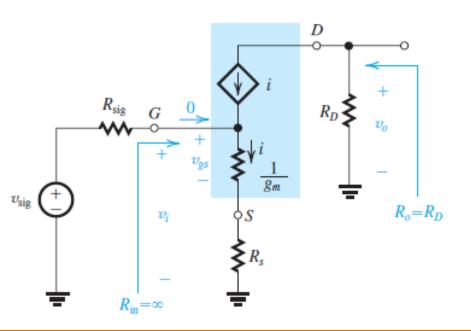
$$R_{in} = \infty$$

$$R_{out} = R_D \parallel r_o \approx R_D$$

Common Source Amplifier



CS amplifier with source resistance



Characteristic Parameters of the CS Amplifier (with source resistance):

$$i = \frac{v_i}{1/g_m + R_s} = \frac{g_m}{1 + g_m R} v_i$$
$$v_o = -iR_D$$

Open circuit voltage gain:

$$A_{v} = \frac{v_{o}}{v_{i}} = -\frac{g_{m}R_{D}}{1 + g_{m}R_{S}}$$

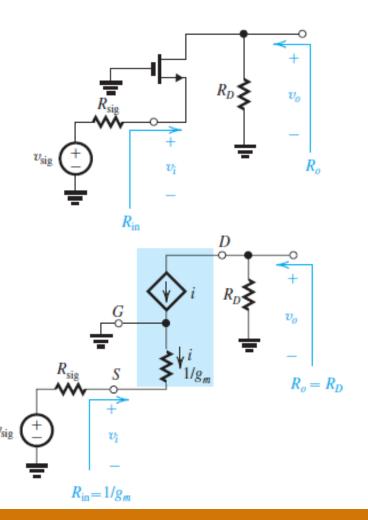
Input resistance:

$$R_{in} = \infty$$

$$R_{out} = R_D \parallel r_o \approx R_D$$

Common Gate Amplifier

Common Gate amplifier is used to obtain wide bandwidth.



Characteristic Parameters of the CS Amplifier:

Open circuit voltage gain:

$$A_{\nu} = g_m R_D$$

Overall voltage gain:

$$G_v = \frac{R_D \parallel R_L}{R_{sig} + 1/g_m}$$

Input resistance:

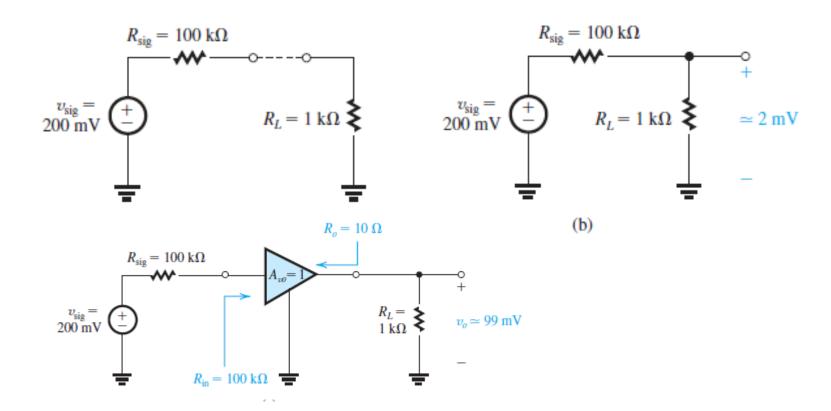
$$R_{in} = \frac{1}{g_m}$$
 Disadvantage!!!

$$R_{out} = R_D$$

Common Drain Amplifier (Source Follower)

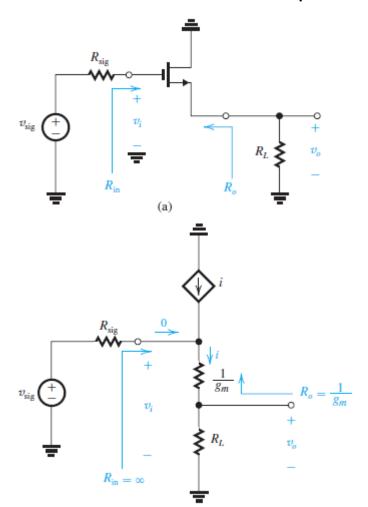
The need for voltage buffers: the amplifier has

- High input resistance.
- Low output resistance.



Common Drain Amplifier (Source Follower)

Common Drain amplifier is usually used as a voltage buffer.



Characteristic Parameters of the CS Amplifier:

Open circuit voltage gain:

$$A_v = \frac{R_L}{R_L + 1/g_m} \approx 1$$

Overall voltage gain:

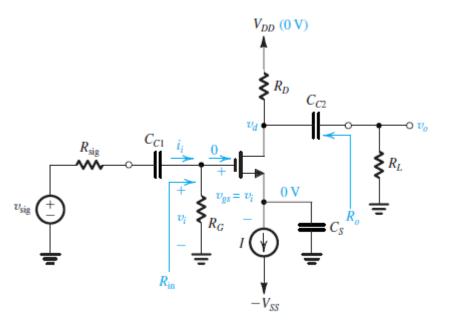
$$G_v = \frac{R_L}{R_L + 1/g_m} \approx 1$$

Input resistance:

$$R_{in} = \infty$$

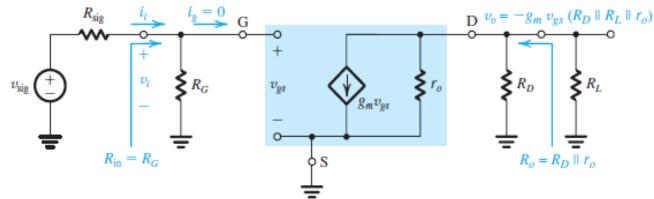
$$R_{out} = \frac{1}{g_m}$$

Discrete Circuit MOS Amplifiers

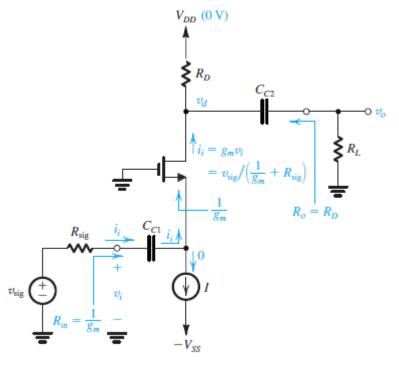


Example 9: Given $V_{DD} = V_{SS} = 10V$, $k_n = 1mA/V^2$, I = 0.5mA, $R_D = 15k\Omega$, $R_G = 4.7M\Omega$ $V_t = 1.5V$, $V_A = 75V$.

Calculate input, output resistance and overall voltage gain. $R_{sig} = 100k\Omega$, $R_L = 15k\Omega$.

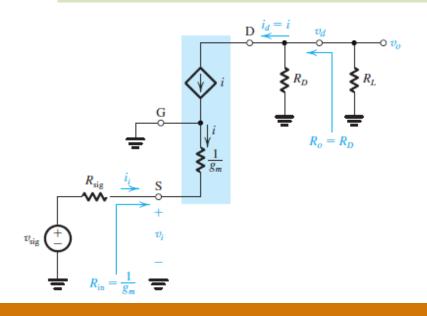


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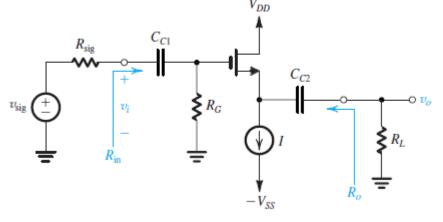


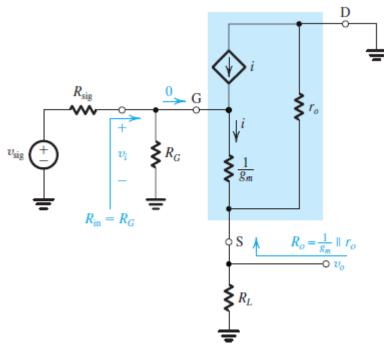
Example 10: Given $V_{DD} = V_{SS} = 10V$, $k_n = 1mA/V^2$, I = 0.5mA, $R_D = 15k\Omega$, $R_G = 4.7M\Omega$ $V_t = 1.5V$, $g_m = 1mA/V$.

Calculate input, output resistance and overall voltage gain. $R_{sig} = 50\Omega$, $R_L = 15k\Omega$.



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Example 11: Given $V_{DD} = V_{SS} = 10V$, $k_n = 1mA/V^2$, I = 0.5mA, $R_D = 15k\Omega$, $R_G = 4.7M\Omega$ $V_t = 1.5V$, $g_m = 1mA/V$.

Calculate input, output resistance and overall voltage gain. $R_{sig} = 1M\Omega$, $R_L = 15k\Omega$.

HCMUT / 2017

Summary

	Characteristics4,b				
Amplifier type	$R_{ m in}$	A_{vo}	R_o	A_v	G_v
Common source					
	00	$-g_m R_D$	R_D	$-g_m(R_D \parallel R_L)$	$-g_m(R_D \parallel R_L)$
Common source with R_s	00	$-\frac{g_m R_D}{1+g_m R_s}$	R_D	$\frac{-g_m(R_D \parallel R_L)}{1+g_m R_s}$	$-\ \frac{g_m(R_D \parallel R_L)}{1+g_mR_s}$
				$-\frac{R_D \parallel R_L}{1/g_m + R_s}$	$- \frac{R_D \parallel R_L}{1/g_m + R_s}$
Common gate	$\frac{1}{g_m}$	$g_m R_D$	R_D	$g_m(R_D \parallel R_L)$	$\frac{R_D \ R_L}{R_{\text{sig}} + 1/g_m}$
Source follower	00	1	$\frac{1}{g_m}$	$\frac{R_L}{R_L + 1/g_m}$	$\frac{R_L}{R_L + 1/g_m}$

Q&A