Abstract

In our electronic project, we are going to investigate the design and analysis of a common emitter bipolar junction transistor (BJT) amplifier Circuit. This includes key performances such as Voltage Gain, Bandwidth and input, and output impedances considering practical design constraints. Overall, this project contributes to the understanding and application of analog circuit design principles in real-world engineering contexts.

1. INTRODUCTION

1.1. Background

BJT Amplifiers are used majorly in Audio amplifiers, Radiofrequency Circuits, and many other industrial, and medical instruments. Designing a BJT amplifier involves selecting the right transistor, biasing it correctly, designing gain stages and bandwidth, implementing coupling and decoupling capacitors, determining load resistance, applying feedback networks, considering power supply decoupling, conducting simulation and testing, addressing thermal considerations and incorporating protection of the circuit.

1.2. Problem Statement

The main factor or the issue is the BJT common emitter amplifier Circuit involves optimizing parameters such as voltage gain, input/output impedance, bandwidth, and minimizing distortion while ensuring stable biasing and linear operation across varying signal frequencies and amplitudes.

1.2.1. Goals and Objectives

Goal :

The main goal is to amplify a weak input signal while maintaining linearity, low distortion, and sufficient bandwidth. This amplification should achieve a desired voltage gain with appropriate input and output impedance matching, ensuring compatibility with stability over temperature variations and manufacturing tolerances and it should operate reliably within specified voltage and current limits.

Objectives:

- Gather the information on basic BJT amplifier circuit models.
- Prepare necessary calculations on the given task.
- Simulate the Amplifier Circuit using Proteus.
- Implement the filter circuit using basic PCB circuit design methods.
- Presenting the final output.

1.2.2. Methodology

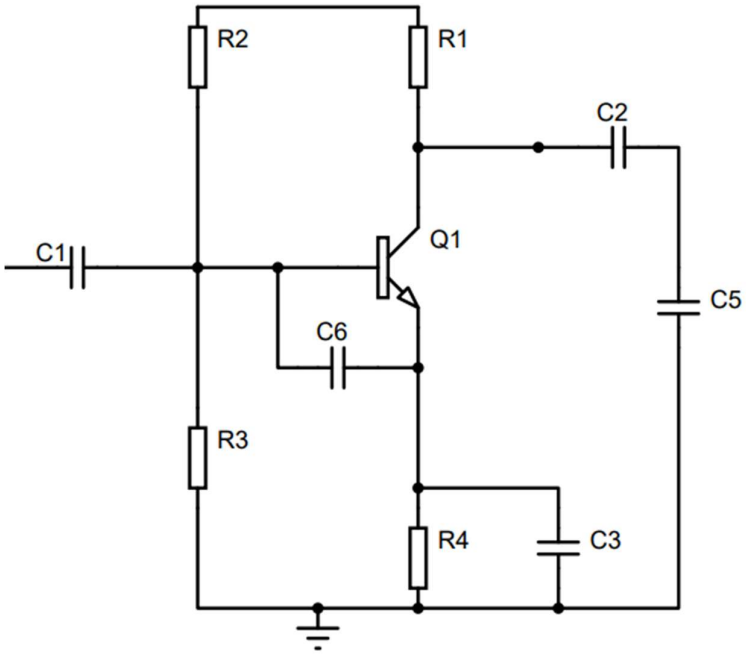

Figure 1: Methologically Designated Circuit

- Choose an appropriate BJT transistor based on voltage ratings, current ratings, and frequency response.
- All necessary values calculate according to get 170 gain and the 8MHz bandwidth
- Select capacitor values and Resistor values according to the availability

2. DESIGN & IMPLEMENTATION OF BJT AMPLIFIER CIRCUIT

2.1 Purpose

The purpose of this circuit is to amplify a signal having 170 gain and 8MHz bandwidth.

2.2 Calculations

1. Selecting a bias point

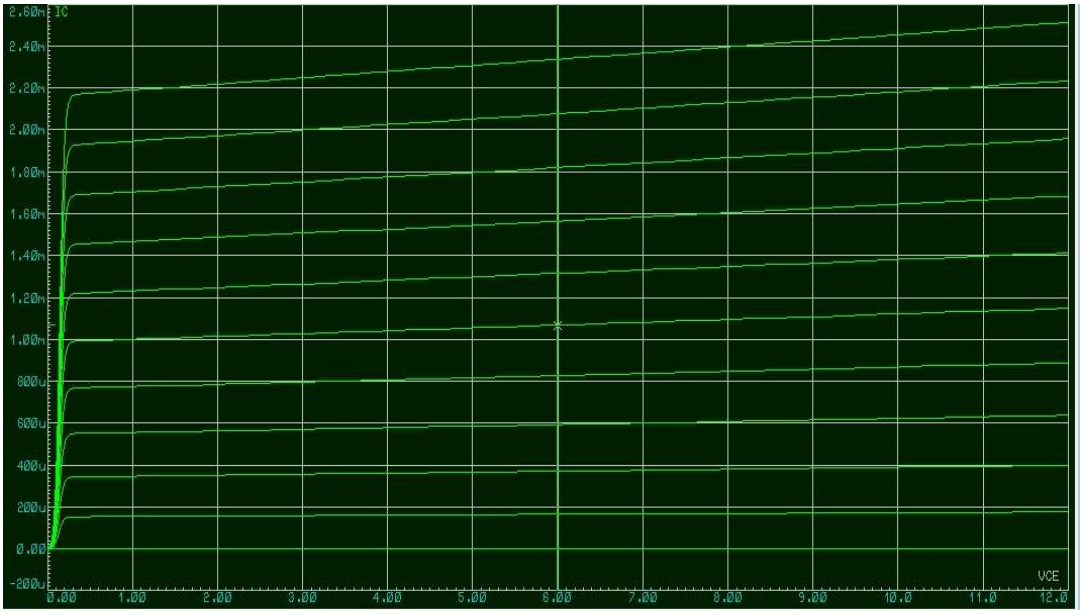

Figure 2: Output Characteristic curve of 2N3904 NPN Transistor

Using the graph Select bias point as;

V_{CE} = 6 V
I_C = 1.07 mA

Using output characteristics of 2N3904 NPN transistor,

I_B = 7.05 µA

Therefore $\beta = \frac{I_C}{I_B}$

$\beta = \frac{1.07\times10^{-3}}{7.05\times10^{-6}}$

β = 151.77

Also, $I_E = I_B + I_C$

$I_E = 7.05\mu A + 1.07\ mA$

$I_E = 1.07705 mA$

From that, we can calculate a small signal resistance of the transistor,

$$r_e = \frac{26\ mV}{I_E}$$

$$r_e = \frac{26\ mV}{1.07705 mA}$$

$$r_e = 24.14\ \Omega$$

2. Calculate resistor values

$$Gain = \frac{R_1}{r_e}$$

$$170 = \frac{R_1}{24.14}$$

$$\underline{R_1 = 4.1038\ k\Omega}$$

According to Figure 1,

$$V_{CC} = V_{CE} + I_C R_1 + I_E R_4$$

$$(V_{CC} = 12V - Supplied\ Voltage)$$

$$12 = 6 + 1.07 \times 10^{-3} \times 4.1038 \times 10^{3} + 1.07705 \times 10^{-3} \times R_4$$

$$\underline{R_4 = 1.49383\ k\Omega}$$

Emitter Voltage,

$$V_E = I_E R_4$$

$$V_E = 1.6089\ V$$

Base voltage,

$$V_B = V_E + 0.6\ V$$

$$V_B = 2.2089\ V$$

Using the Voltage divider method,

$$V_B = 12 \times \frac{R_3}{R_2+R_3}$$

$$2.2089 = 12 \times \frac{R_3}{R_2+R_3}$$

$$R_2 = 4.4325\, R_3$$

Get $R_3 = 10\Omega$ then $R_2 = 44.325\Omega$

3. Calculate capacitor values

Selecting a lower cutoff frequency of 1kHz,

Selecting C_1 Capacitor,

$$1k = \frac{1}{2\pi C_1(R_{1//}R_{2//}\beta r_c)}$$

$$= \frac{1}{2\pi C_1 \times 8.14}$$

$C_1 = 19.55\mu F$

Selecting C_3 capacitor,

$$1k = \frac{1}{2\pi C_3(R_{4//}r_c)}$$

$C_3 = 6.60\mu F$

Selecting C_2 capacitor,

$$1k = \frac{1}{2\pi C_2(R_{1)}}$$

$$1k = \frac{1}{2\pi C_2 \times 4.10 \quad \Omega}$$

$C_2 = 8.378$ nF

Selecting the upper cutoff frequency as 8.001MHz,

$C_0 = C_{M0} + C_5$

$C_0 = (1 - \frac{1}{A})\, C_{bc} + C_5$

A – Gain

C_{Mi} – Miller Input Capacitance

C_{Mo} – Miller output Capacitance

C_{bc} = 4pF using datasheet,

C_0 = 4pF + C_5

$$f = \frac{1}{2\pi \times R_c \times C_0}$$

$$8.001\text{MHz} = \frac{1}{2\pi \times 4103.8 \times C_0}$$

C_0 = 4.847 pF

C_5 = 0.847 pF

$$f = \frac{1}{2\pi (R1//R2//r\beta) C_i}$$

Ci = Cni + Cbe + C_6

Ci = Cbc(1-A) + Cbe + C_6 (A= Gain)

Ci = Cbc(171) + Cbe + C_6

= 4pF(171) + 8pF +C_6

Ci = 173×4pF + C_6

C_6 = 1751.72 pF

2.3 Required Components & Ratings

- 2N3904 silicon NPN low-power high-frequency bipolar transistor (350mW,150℃)
- Resistors (According to calculations) 10W
- Capacitors(according to calculations)

2.3 Implementation of the circuit

There are majorly two parts to the implementation process,

1. Design the Circuit for 170 Gain
2. Design the bandwidth for 8MHz

According to the calculations above scenarios can be implemented using the following circuit.

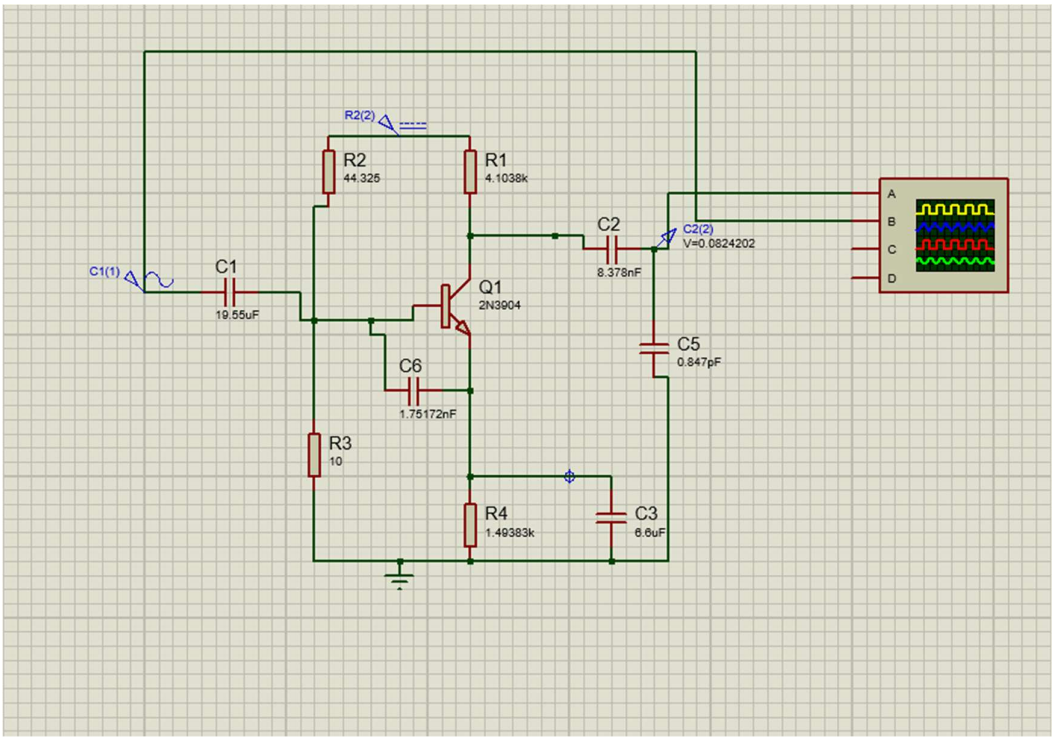

Figure 3: Schematic Layout for Designed Amplifier using proteus

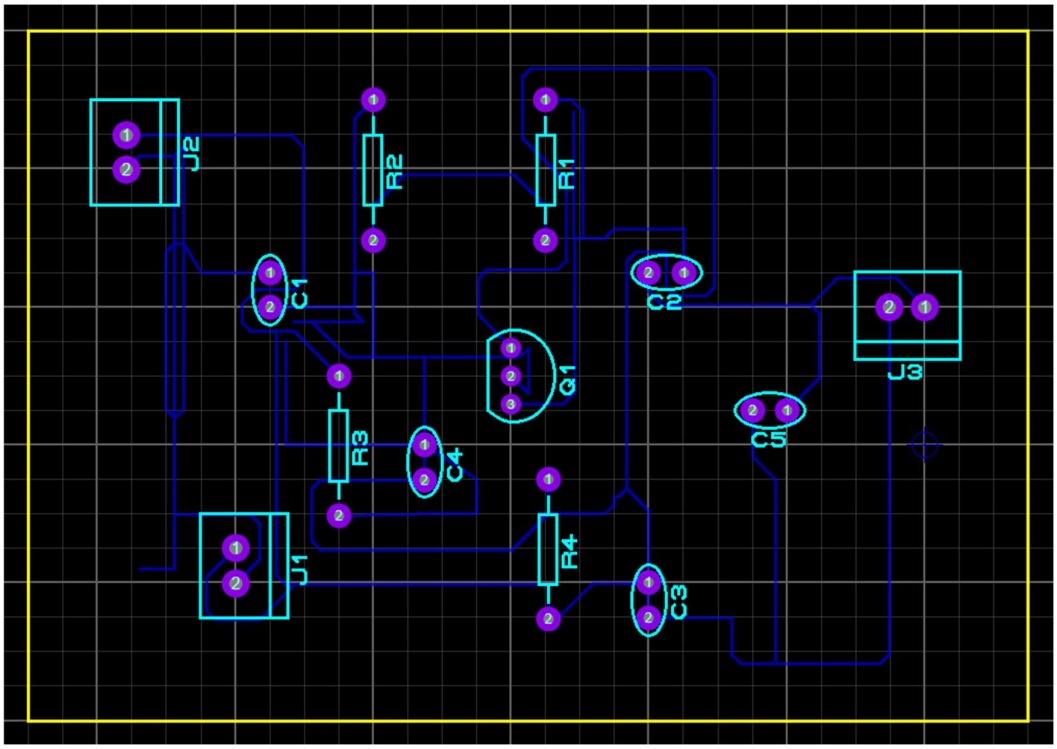

Figure 4: PCB Layout Design of the Circuit Using Proteus

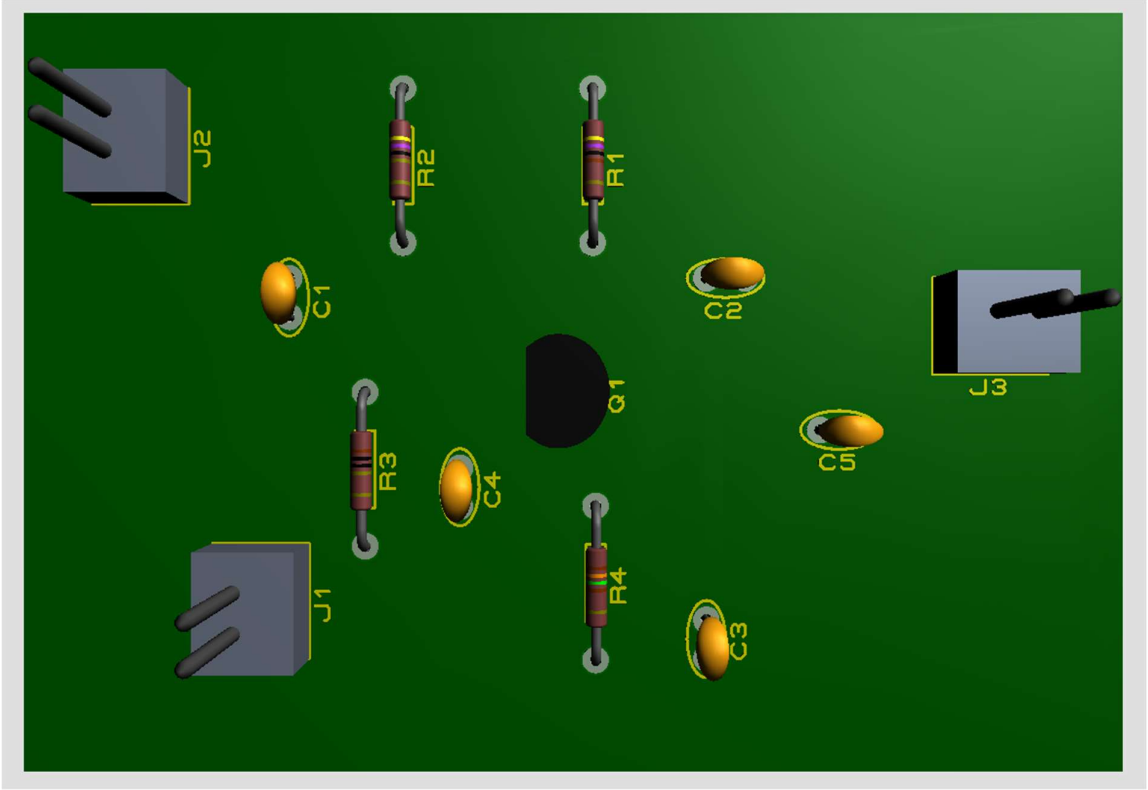

Figure 5: 3D view of the Implemented Circuit Using proteus

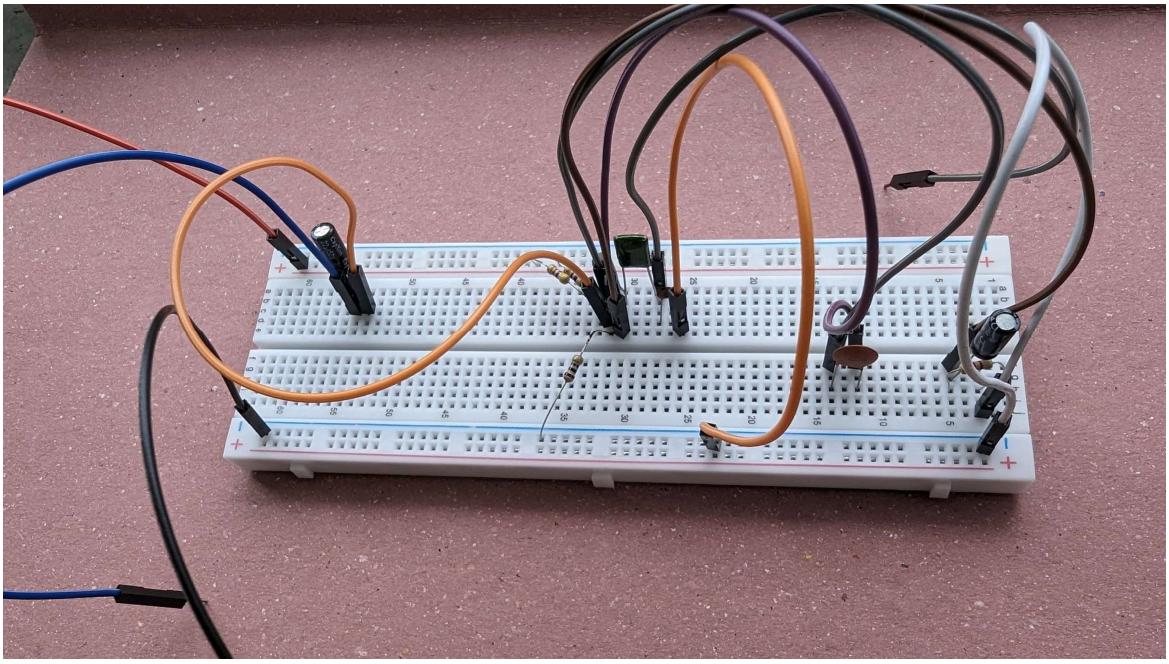

Figure 6: BJT Amplifier Implementation BreadBoard

3. RESULTS & DISCUSSION

3.1 Results Observed from the Proteus Simulation Software

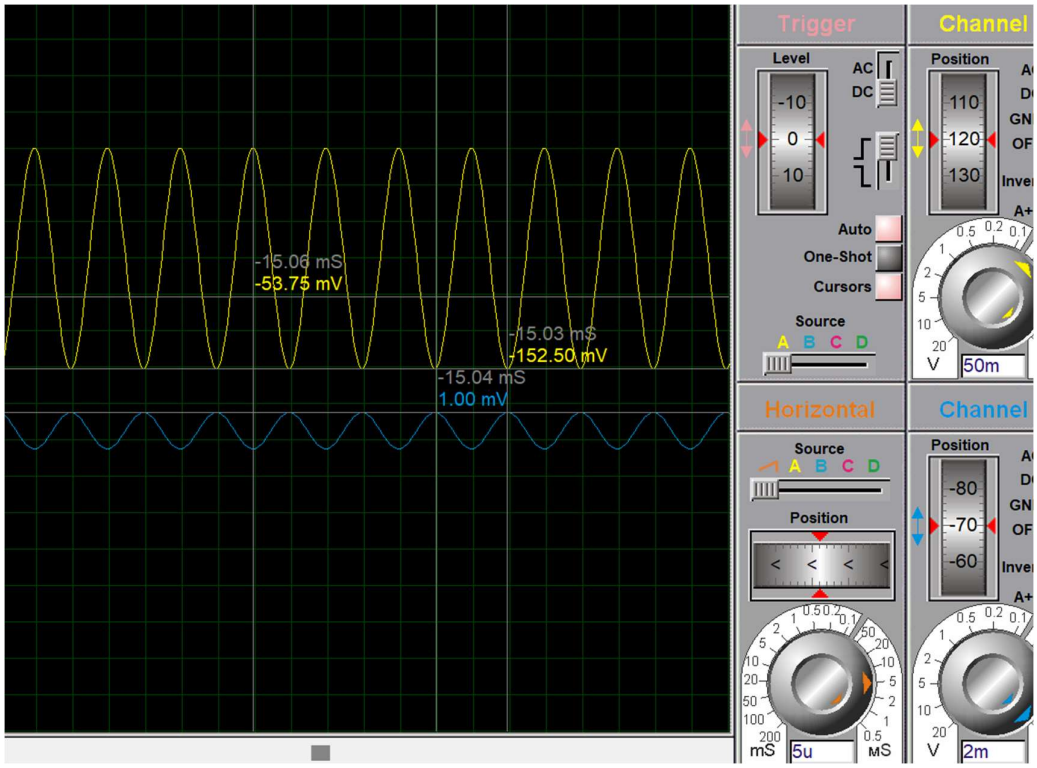

Figure 7:Observed Output Signal(yellow) for Input signal (Blue)

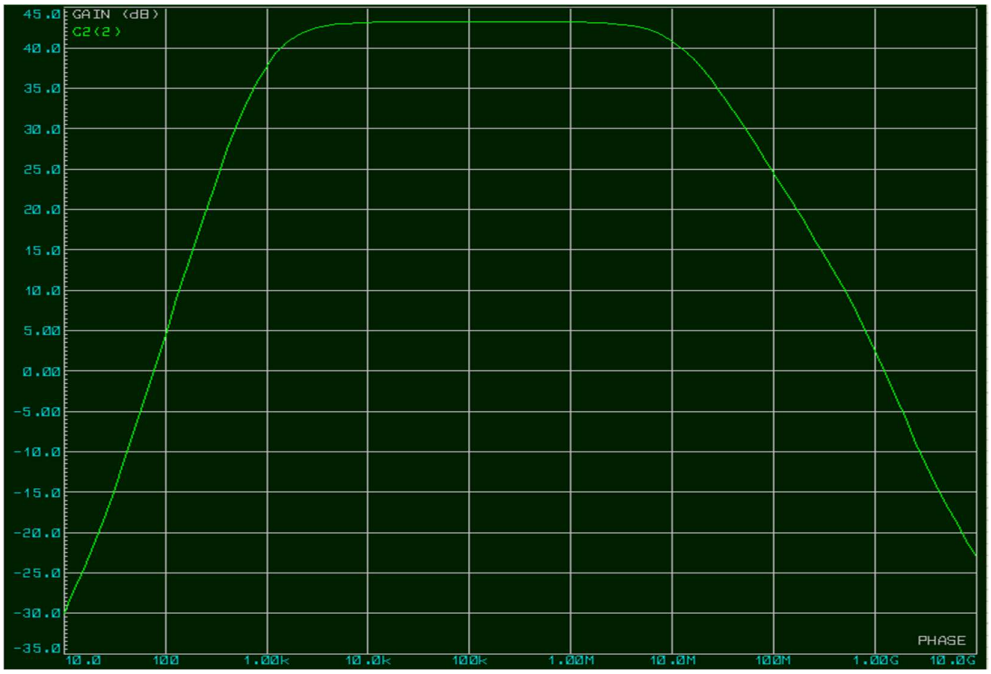

Figure 8: Observed Frequency Response for the circuit

3.2 Discussion

Table 2: Theoretical and Observed Values for Gain and Bandwidth

Parameter	Theoretical value	Observed value from simulation
Gain	170	152.5
Bandwidth	8 MHz	9.9 MHz

According to the above results, we can see there are slight variations in the implemented circuit. For Expected gain 170 only gets 152.50 Gain and For Expected Bandwidth 8MHz gets 9.9 MHz bandwidth. The main reason behind this is the calculated values cannot be perfectly placed in the simulation. Due to decimal values, it only can give some approximate values. Therefore the expected results can be changed.

For gain included resistor values and for the bandwidth included capacitance values are approximately included for several decimal places. Therefore expected output varies from the observed values. In addition to these reasons, inaccuracies in the simulation software can cause differences in these values. Inaccuracies in the models representing resistance, capacitances, and also the method of analyzing the circuit can cause these deviations between the values.

In practical scenarios for implementing 20µF,1.6pF,6.6uF, 220 nF capacitance values, and 1.35kΩ values capacitors and resistors are not commercially used. Instead of that commercially can get 22µF,2pF,10uF,,224nF capacitors, and 1.20kΩ resistors. Therefore implementing the circuit using these approximated values also can deviate expected results. Other than this temperature variation, electromagnetic interferences deviate obtained results from the expected values for the gain while layout considerations, stray capacitances, and signal degradation deviate the obtaining bandwidth from the expected bandwidth. Other than the resistance of the conductors, environmental conditions may impact the deviation of the results.