```
1 module GENERAL_PURPOSE_REGISTER
 2
       (input clk, write,
       input [15:0] data_in,
 3
 4
       output reg [15:0] data_out
 5
 6
       always @(negedge clk)
 7
           begin
               if (write) data_out <= data_in;</pre>
 8
 9
10 endmodule
```