```
1  `timescale 1ns / 1ps
2  module AC (
3      input clk,
4      input [2:0]write,
5      input [15:0] data_alu_ac,
6      output reg [15:0] data_out );
7      always @(*)
8          begin
9          if (write==3'b100) data_out = data_alu_ac;
10         end
11 endmodule
```