Module 8

Analog-to-Digital Conversion

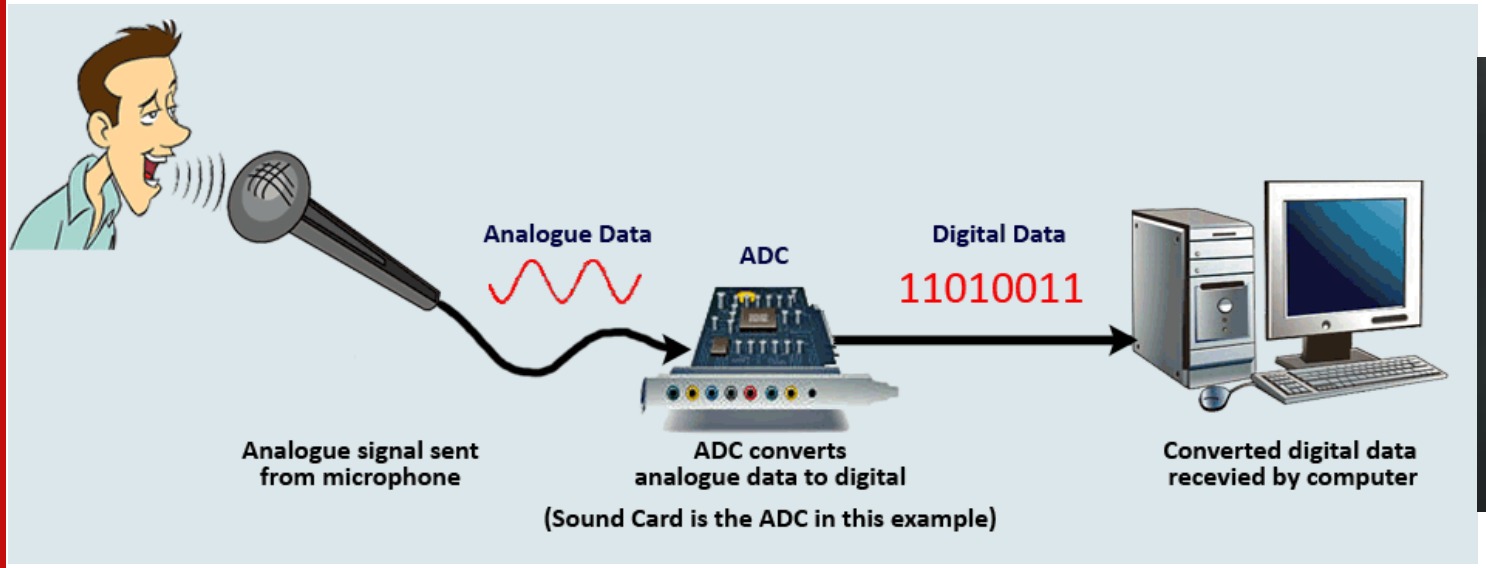
19th December 2024

ADC Architecture

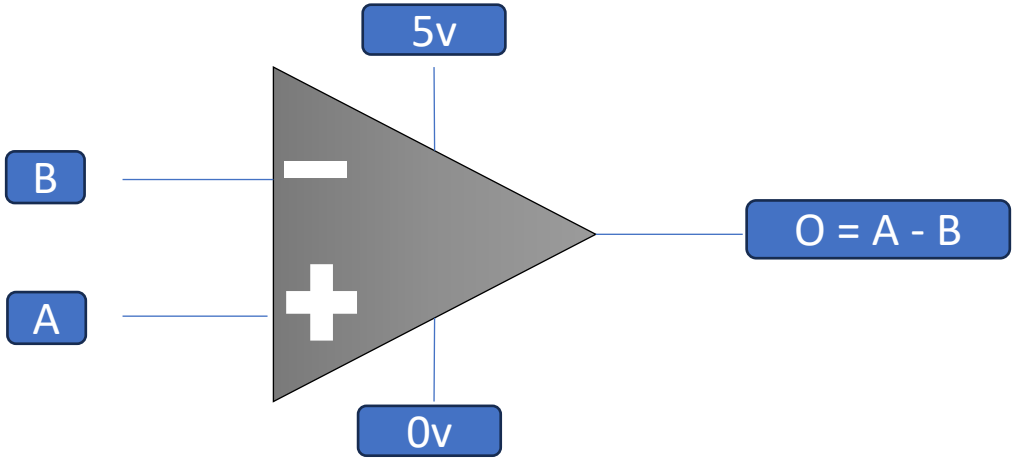
Analog-to-Digital Converters

Thynk Loop

Analog-to-digital converters (ADCs) are peripheral devices that convert continuous analog signals into discrete digital values suitable for processing by a digital system, allowing microcontrollers to interface with analog sensors and signals.

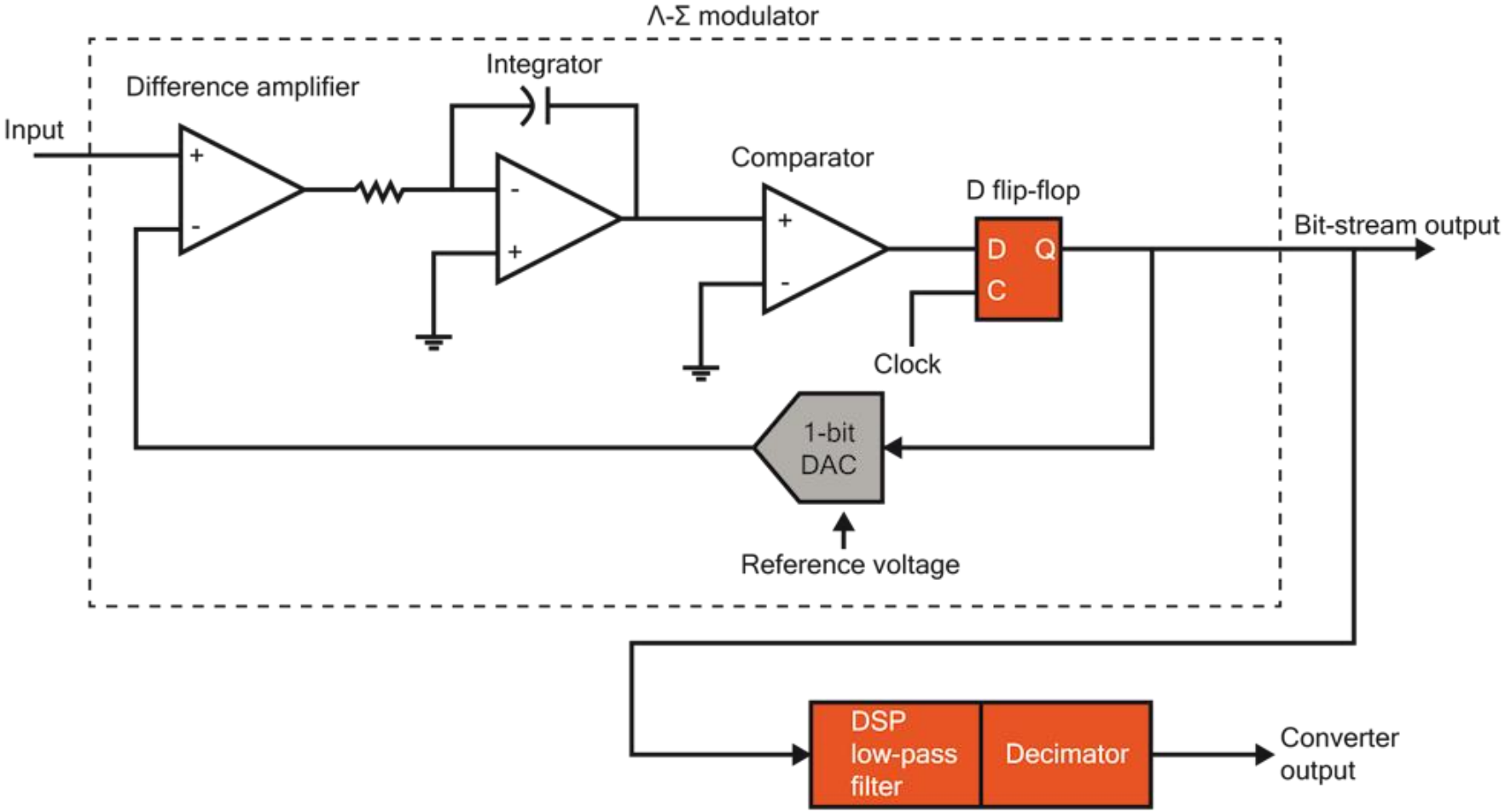


Comparator



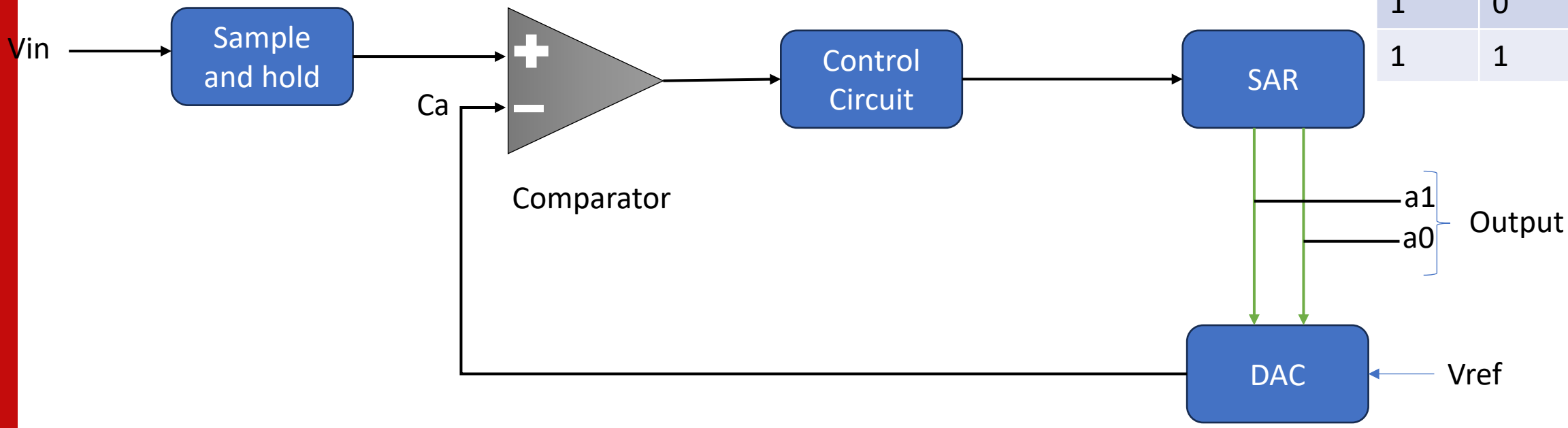
Conditions	Output (O)
A > B = +ve	5
A < B = -ve	0
A = B	X

SAR ADC


Λ-Σ modulator
Integrator
Difference amplifier
Input
Comparator
D flip-flop
Bit-stream output
D
Q
C
Clock
1-bit
DAC
Reference voltage
DSP
low-pass
filter
Decimator
Converter
output

SAR ADC

A1	A0	O/P v
0	0	0.825
0	1	1.65
1	0	2.475
1	1	3.3

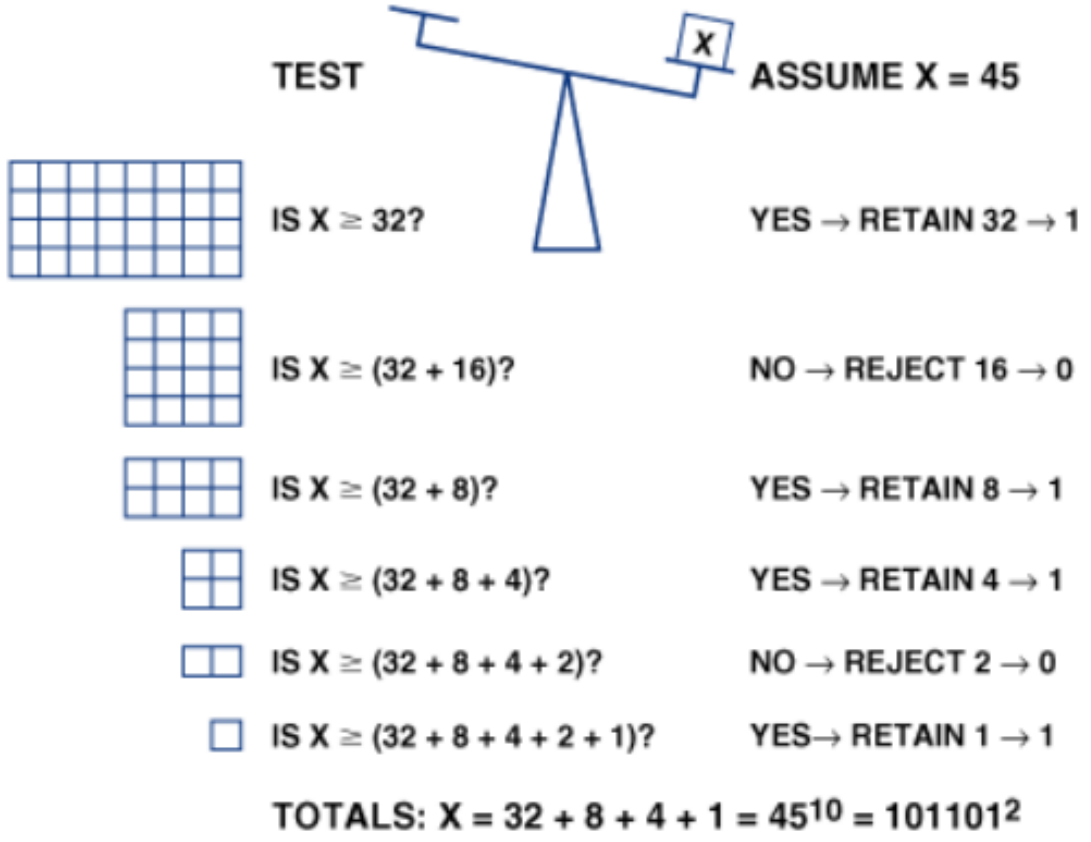


Iteration	Vin	Ca	A1 –Past	A0 - Past	A1- Curr	A0- Curr
1	1.3	2.475	1	0	0	1
2	1.3	1.65	0	1	0	0

Output codes = 2^N

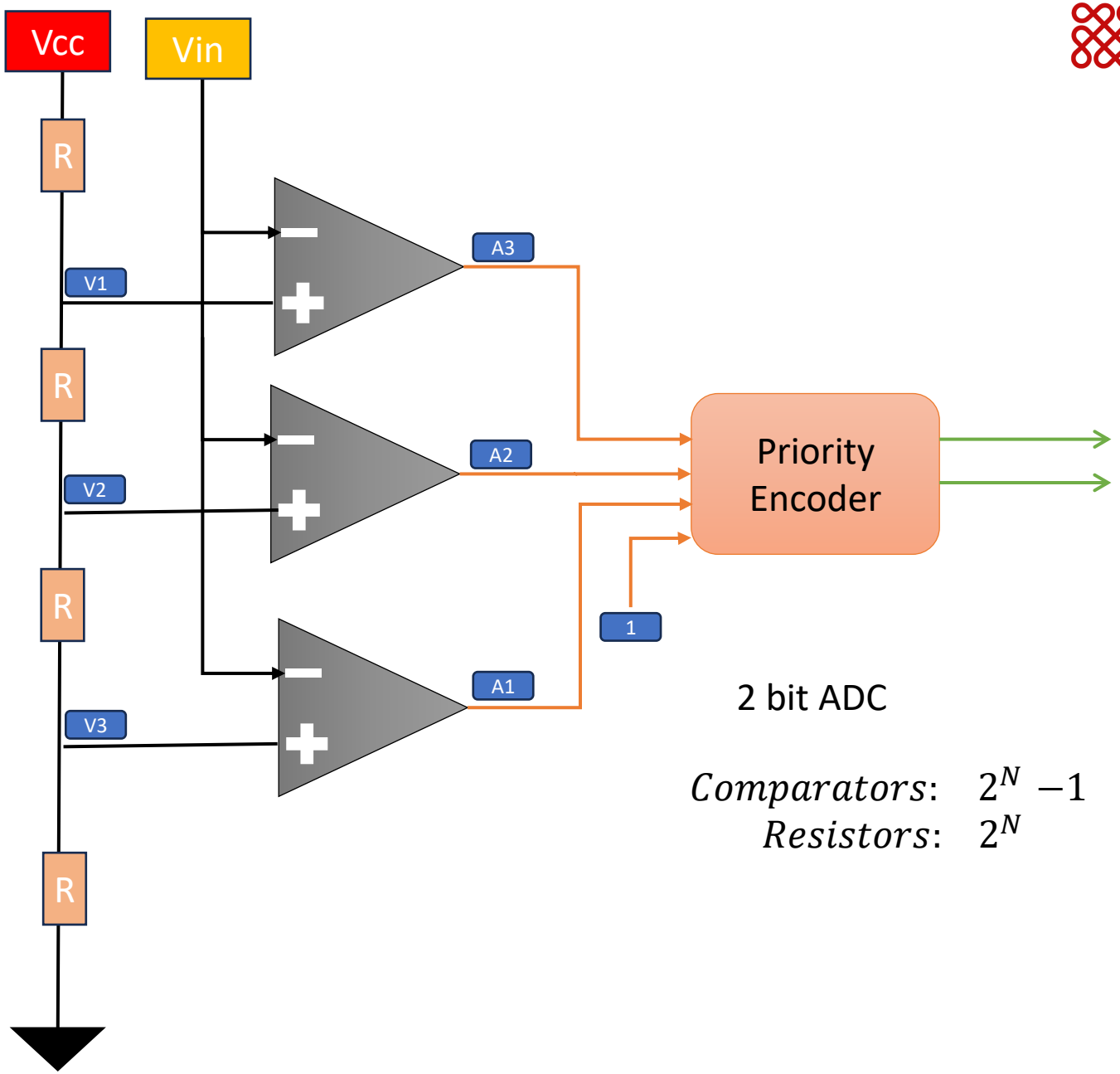
2-bit ADC:
Total output codes: 2^2 = 4
Vref = 3.3v
1 code voltage(LSB) = 3.3/4 = 0.825V

SAR ADC - Analogy



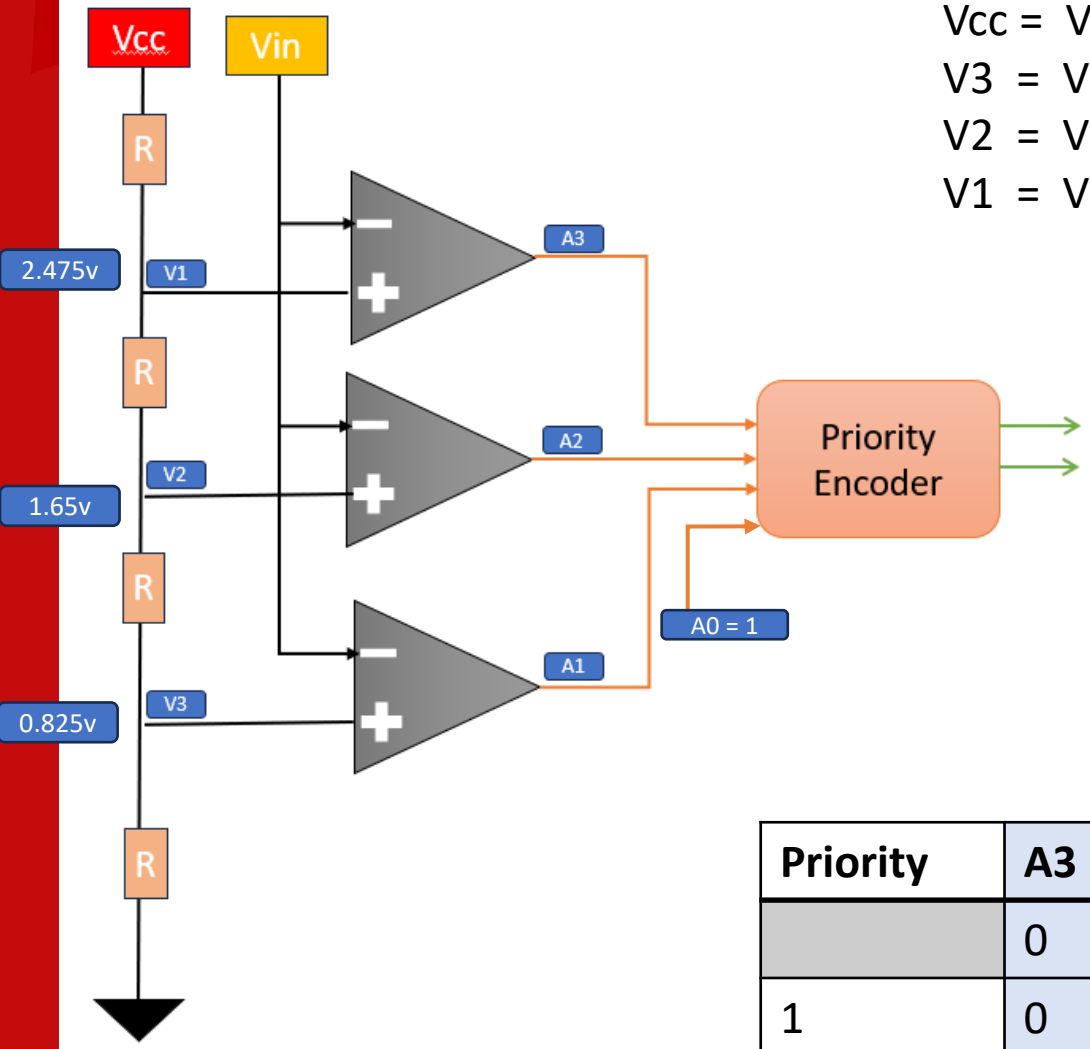
Flash ADC

- The flash ADC also known as parallel ADC is a very fast ADC.
- The application of flash ADC
  - Radar data acquisition
  - IMU measurements in missiles



2 bit ADC

$$Comparators: \quad 2^N - 1$$
$$Resistors: \quad 2^N$$



Vcc = Vref = 3.3V ,
V3 = Vref/4 = 0.825v
V2 = Vref/2 = 1.65v
V1 = Vref * (3/4) = 2.475v

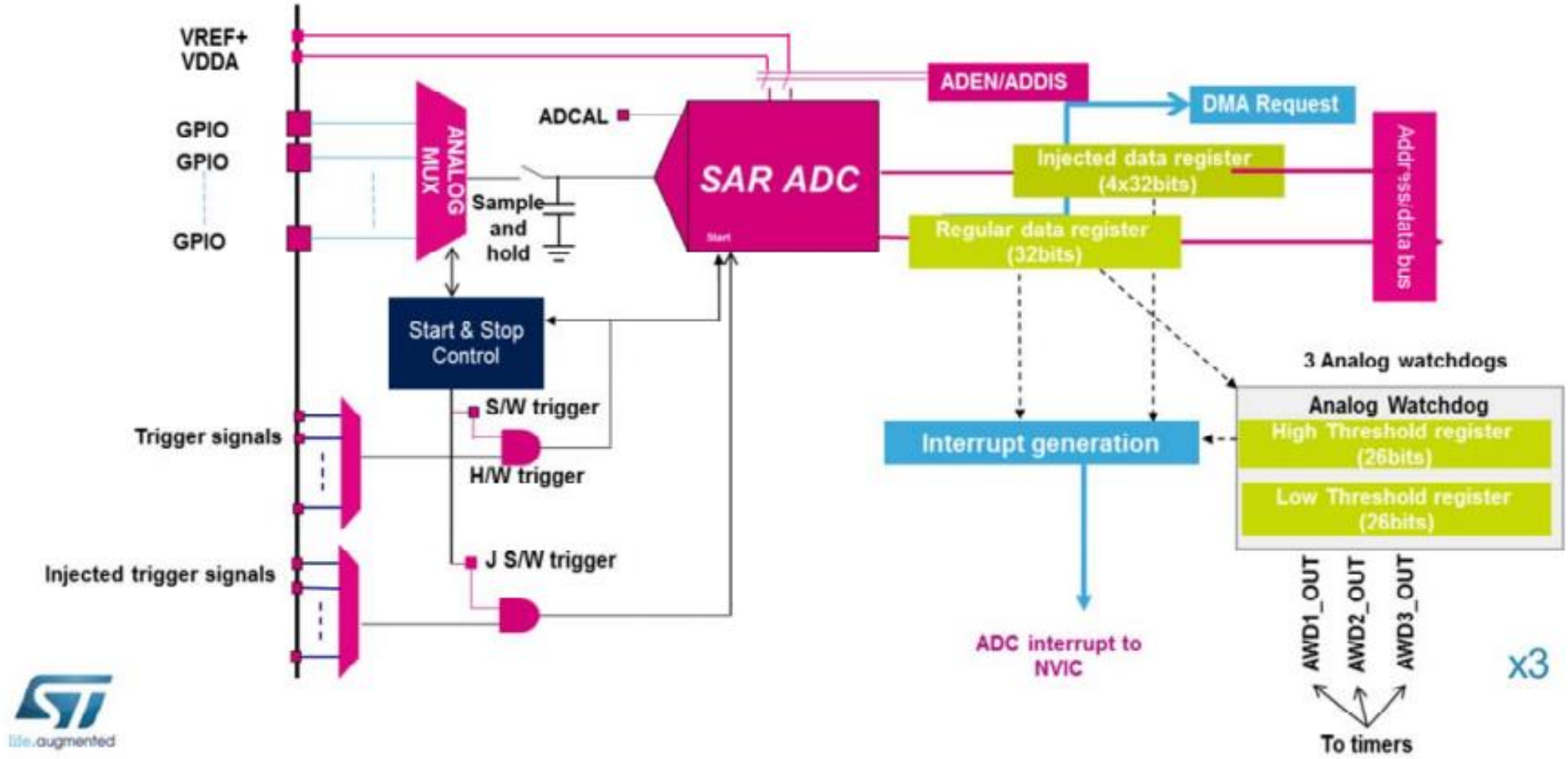
Vref = 3.3v , Vin = 1.3v	
A3 = V1 – Vin = 2.47 – 1.3 = +ve	1
A2 = V2 – Vin = 1.65 – 1.3 = +ve	1
A1 = V3 – Vin = 0.8 – 1.3 = -ve	0

Priority	A3	A2	A1	A0	B1	B0
	0	0	0	1	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	0
3	1	0	0	0	1	1

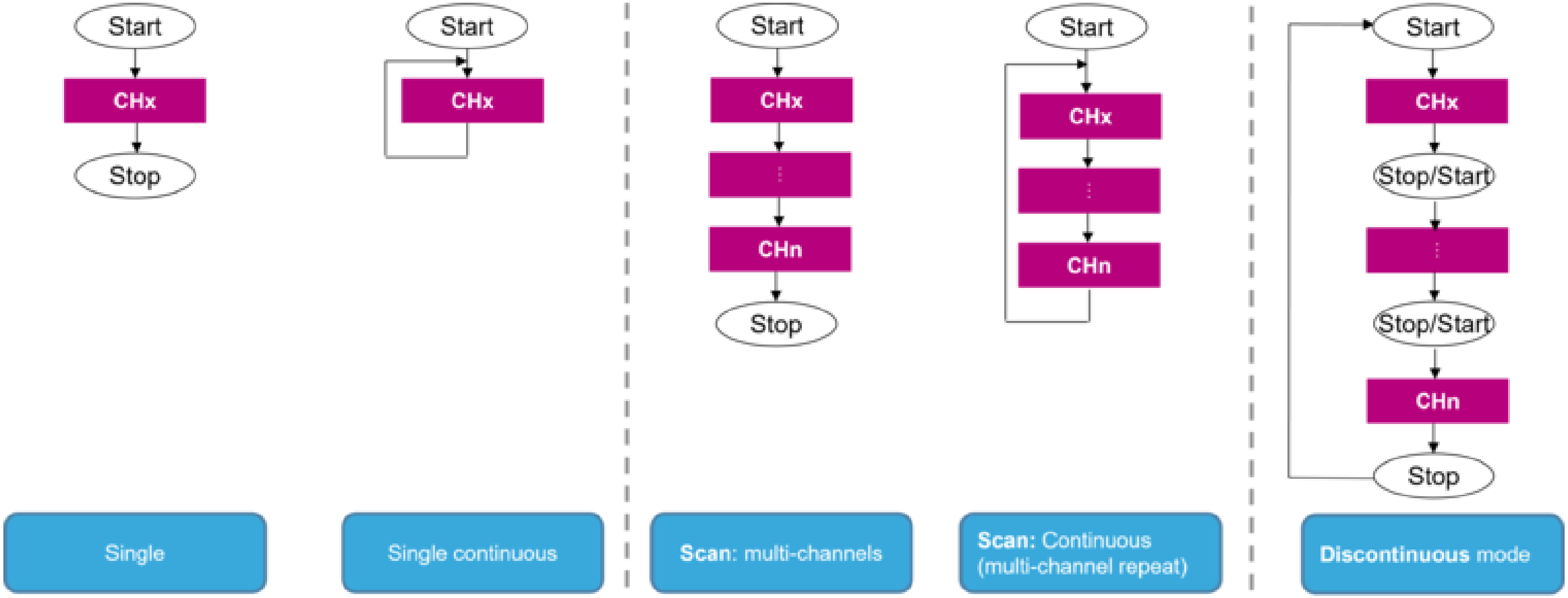
High Level Comparison

ADC TYPE	PROS	CONS	MAX RESOLUTION	MAX SAMPLE RATE	MAIN APPLICATIONS
Successive Approximation (SAR)	Good speed/resolution ratio	No inherent anti-aliasing protection	18 bits	10 MHz	Data Acquisition
Delta-sigma (ΔΣ)	High dynamic performance, inherent anti-aliasing protection	Hysteresis on unnatural signals	32 bits	1 MHz	Data Acquisition, Noise & Vibration, Audio
Dual Slope	Accurate, inexpensive	Low speed	20 bits	100 Hz	Voltmeters
Pipelined	Very fast	Limited resolution	16 bits	1 GHz	Oscilloscopes
Flash	Fastest	Low bit resolution	12 bits	10 GHz	Oscilloscopes

ADC & STM32


VREF+
VDDA
GPIO
GPIO
GPIO
ANALOG MUX
ADCAL
Sample and hold
SAR ADC
ADEN/ADDIS
DMA Request
Injected data register (4x32bits)
Regular data register (32bits)
Address/data bus
Start & Stop Control
S/W trigger
H/W trigger
Trigger signals
J S/W trigger
Injected trigger signals
3 Analog watchdogs
Analog Watchdog
High Threshold register (26bits)
Low Threshold register (26bits)
Interrupt generation
ADC interrupt to NVIC
AWD1_OUT
AWD2_OUT
AWD3_OUT
x3
To timers

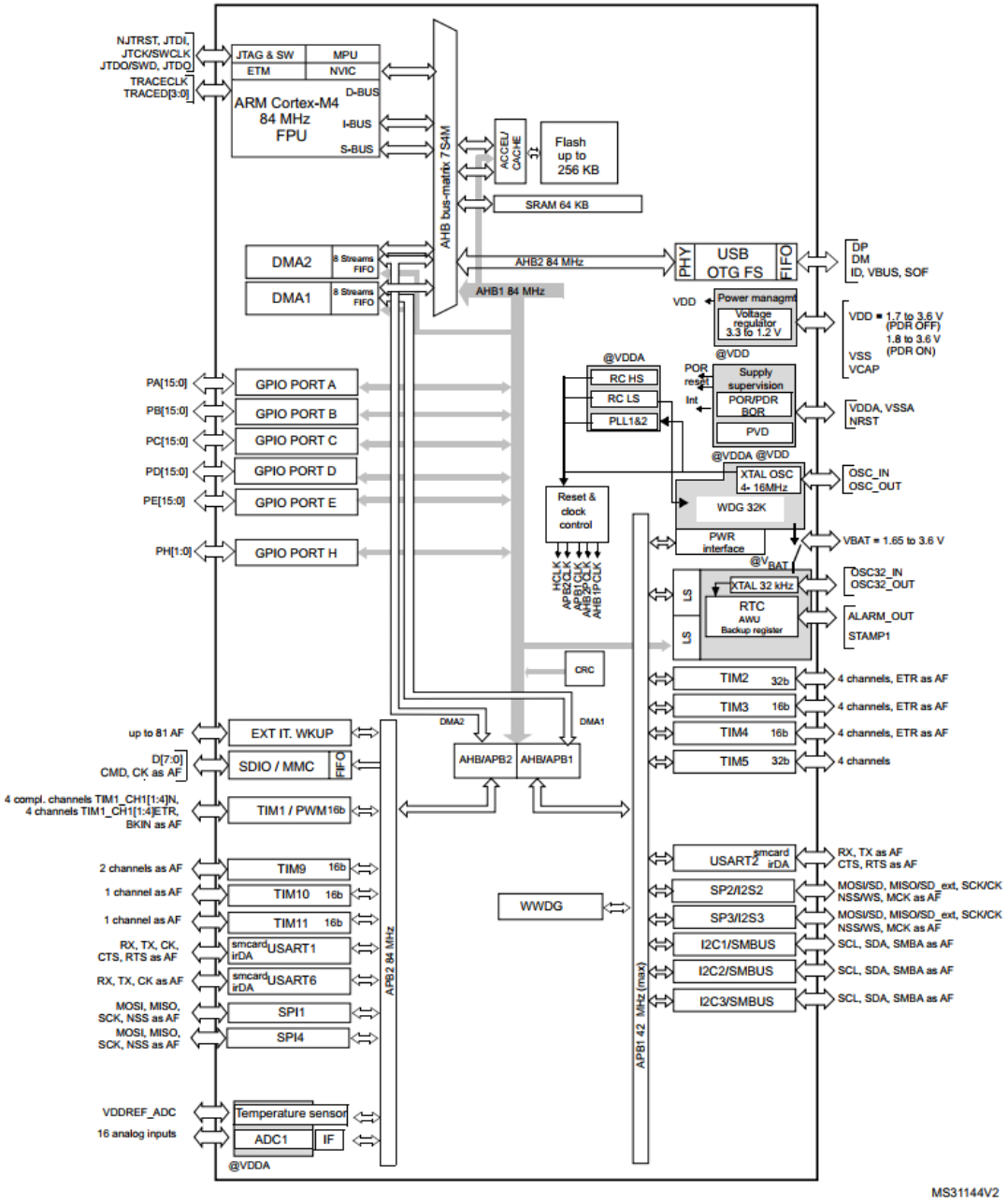
ADC & STM32



STM32 - AN3116

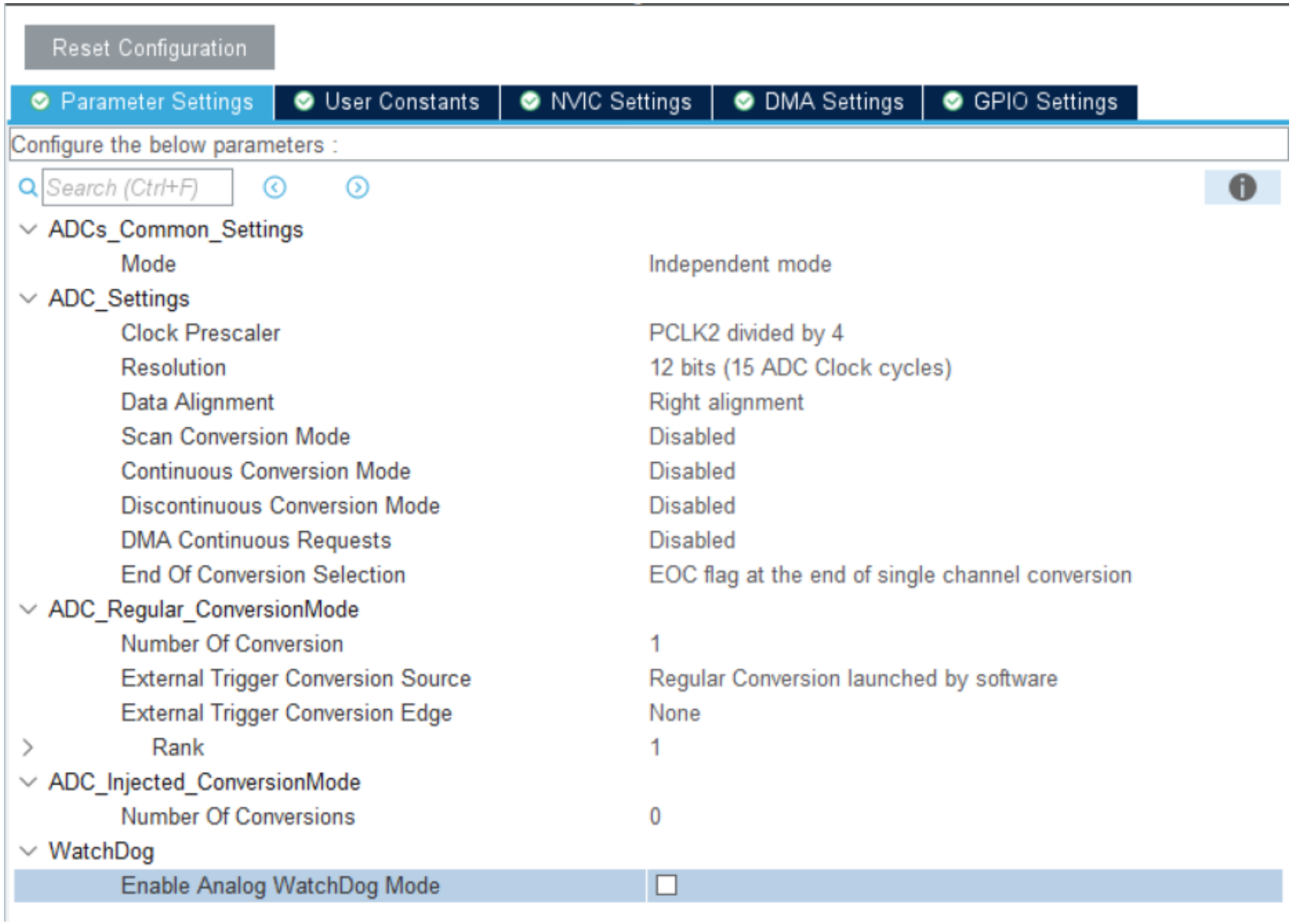
ADC in STM32F401

STM32F401 Architecture



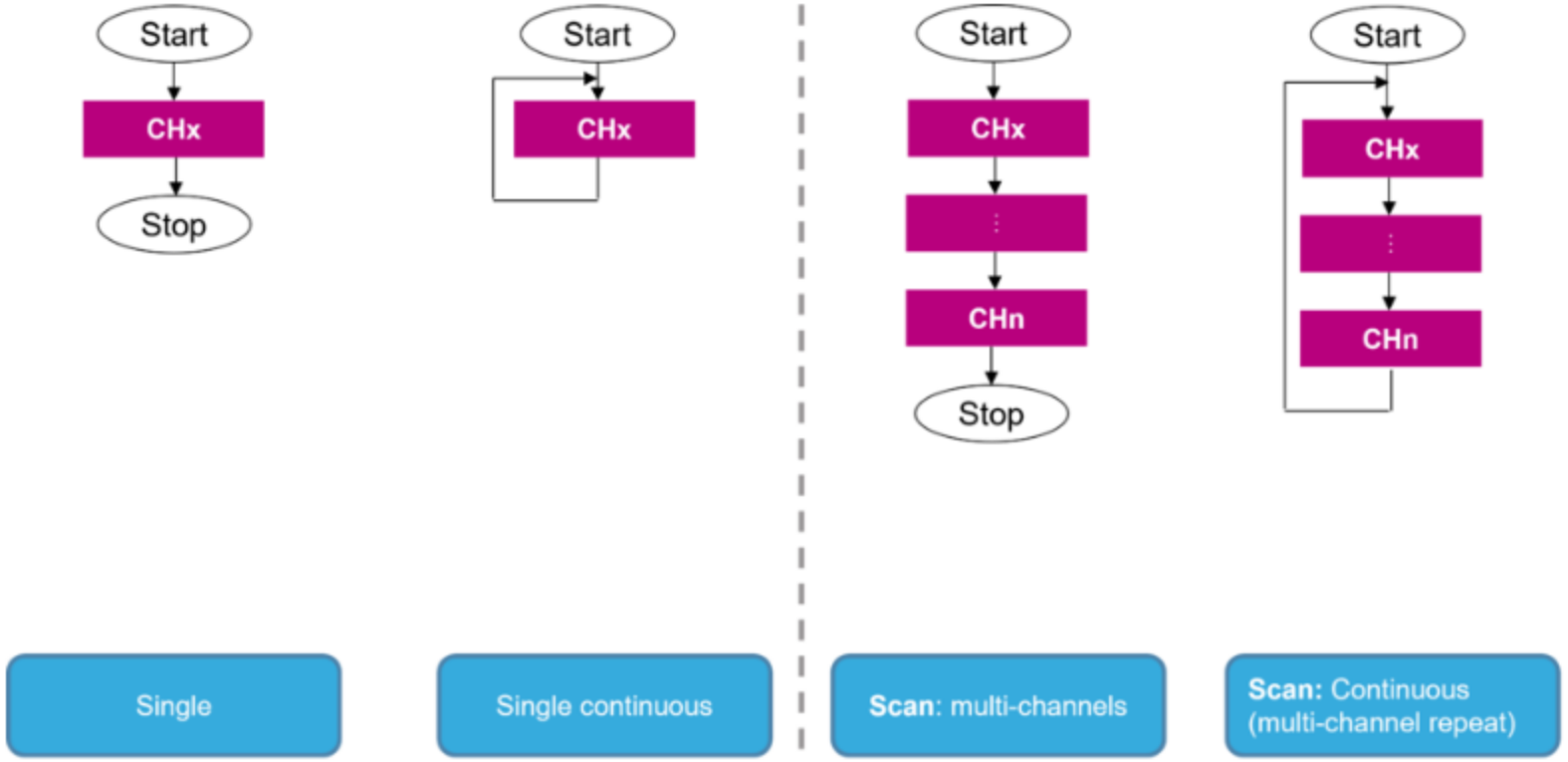
Datasheet – PG14

STM32F401 ADC Parameter Configurations



Datasheet – PG14

Conversion Modes



Source ST Website

Registers of Interest

Thynk Loop

Configuration Registers:

- SDC_SR – STRT, EOC
- ADC_CR1 – RES, SCAN
- ADC_CR2 – SWSTART, ALIGN
- ADC_SMPR1 – SMPx
- ADC_SMPR2 – SMPx
- ADC_SQR1 – L, SQ
- ADC_SQR2 - SQ
- ADC_SQR3 - SQ
- ADC_CCR - ADCPRE

Data Register:

- ADC_DR

Source ST Website

ADC_SR

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										OVR	STRT	JSTRT	JEOC	EOC	AWD
										rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bit 1 **EOC:** Regular channel end of conversion

This bit is set by hardware at the end of the conversion of a regular group of channels. It is cleared by software or by reading the ADC_DR register.

0: Conversion not complete (EOCS=0), or sequence of conversions not complete (EOCS=1)

1: Conversion complete (EOCS=0), or sequence of conversions complete (EOCS=1)

Ref Manual

ADC_CR1

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					OVRIE	RES		AWDEN	JAWDEN	Reserved					
					rw	rw	rw	rw	rw						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DISCNUM[2:0]			JDISCEN	DISCEN	JAUTO	AWDSGL	SCAN	JEOCIE	AWDIE	EOCIE	AWDCH[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 25:24 **RES[1:0]:** Resolution

These bits are written by software to select the resolution of the conversion.
00: 12-bit (15 ADCCLK cycles)
01: 10-bit (13 ADCCLK cycles)
10: 8-bit (11 ADCCLK cycles)
11: 6-bit (9 ADCCLK cycles)

Bit 8 **SCAN:** Scan mode

This bit is set and cleared by software to enable/disable the Scan mode. In Scan mode, the inputs selected through the ADC_SQRx or ADC_JSQRx registers are converted.
0: Scan mode disabled
1: Scan mode enabled

Source ST Website

ADC_CR2

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
reserved	SWSTART	EXTEN		EXTSEL[3:0]				reserved	JSWSTART	JEXTEN		JEXTSEL[3:0]			
	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved				ALIGN	EOCS	DDS	DMA	Reserved						CONT	ADON
				rw	rw	rw	rw							rw	rw

Bit 30 **SWSTART:** Start conversion of regular channels

This bit is set by software to start conversion and cleared by hardware as soon as the conversion starts.

0: Reset state

1: Starts conversion of regular channels

Note: This bit can be set only when ADON = 1 otherwise no conversion is launched.

Bit 0 **ADON:** A/D Converter ON / OFF

This bit is set and cleared by software.

Note: 0: Disable ADC conversion and go to power down mode

1: Enable ADC

Bit 10 **EOCS:** End of conversion selection

This bit is set and cleared by software.

0: The EOC bit is set at the end of each sequence of regular conversions. Overrun detection is enabled only if DMA=1.

1: The EOC bit is set at the end of each regular conversion. Overrun detection is enabled.

ADC_SMPR1

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					SMP18[2:0]			SMP17[2:0]			SMP16[2:0]			SMP15[2:1]	
					rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMP15_0	SMP14[2:0]			SMP13[2:0]			SMP12[2:0]			SMP11[2:0]			SMP10[2:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 26:0 **SMPx[2:0]:** Channel x sampling time selection

These bits are written by software to select the sampling time individually for each channel. During sampling cycles, the channel selection bits must remain unchanged.

Note: 000: 3 cycles
001: 15 cycles
010: 28 cycles
011: 56 cycles
100: 84 cycles
101: 112 cycles
110: 144 cycles
111: 480 cycles

Ref Manual - ADC

ADC_SMPR2

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SMP9[2:0]			SMP8[2:0]			SMP7[2:0]			SMP6[2:0]			SMP5[2:1]	
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMP 5_0	SMP4[2:0]			SMP3[2:0]			SMP2[2:0]			SMP1[2:0]			SMP0[2:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 26:0 **SMPx[2:0]:** Channel x sampling time selection

These bits are written by software to select the sampling time individually for each channel. During sampling cycles, the channel selection bits must remain unchanged.

Note: 000: 3 cycles
001: 15 cycles
010: 28 cycles
011: 56 cycles
100: 84 cycles
101: 112 cycles
110: 144 cycles
111: 480 cycles

Ref Manual - ADC

ADC_SQR1

Address offset: 0x2C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								L[3:0]				SQ16[4:1]			
								rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ16_0	SQ15[4:0]					SQ14[4:0]					SQ13[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw				rw	rw	rw	rw	rw

Bits 23:20 **L[3:0]:** Regular channel sequence length

These bits are written by software to define the total number of conversions in the regular channel conversion sequence.
0000: 1 conversion
0001: 2 conversions
...
1111: 16 conversions

Bits 19:15 **SQ16[4:0]:** 16th conversion in regular sequence

These bits are written by software with the channel number (0..18) assigned as the 16th in the conversion sequence.

ADC_SQR2

Address offset: 0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SQ12[4:0]					SQ11[4:0]					SQ10[4:1]			
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ10_0	SQ9[4:0]					SQ8[4:0]					SQ7[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:30 Reserved, must be kept at reset value.

Bits 29:26 **SQ12[4:0]:** 12th conversion in regular sequence
These bits are written by software with the channel number (0..18) assigned as the 12th in the sequence to be converted.

Bits 24:20 **SQ11[4:0]:** 11th conversion in regular sequence

Bits 19:15 **SQ10[4:0]:** 10th conversion in regular sequence

Bits 14:10 **SQ9[4:0]:** 9th conversion in regular sequence

Bits 9:5 **SQ8[4:0]:** 8th conversion in regular sequence

Bits 4:0 **SQ7[4:0]:** 7th conversion in regular sequence

Ref Manual - ADC

ADC_SQR3

Address offset: 0x34

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SQ6[4:0]					SQ5[4:0]					SQ4[4:1]			
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ4_0	SQ3[4:0]					SQ2[4:0]					SQ1[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:30 Reserved, must be kept at reset value.

Bits 29:25 **SQ6[4:0]:** 6th conversion in regular sequence
These bits are written by software with the channel number (0..18) assigned as the 6th in the sequence to be converted.

Bits 24:20 **SQ5[4:0]:** 5th conversion in regular sequence

Bits 19:15 **SQ4[4:0]:** 4th conversion in regular sequence

Bits 14:10 **SQ3[4:0]:** 3rd conversion in regular sequence

Bits 9:5 **SQ2[4:0]:** 2nd conversion in regular sequence

Bits 4:0 **SQ1[4:0]:** 1st conversion in regular sequence

ADC_CCR

Address offset: 0x04 (this offset address is relative to ADC1 base address + 0x300)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								TSVREFE	VBATE	Reserved				ADCPRE	
								rw	rw					rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bits 17:16 **ADCPRE:** ADC prescaler

Set and cleared by software to select the frequency of the clock to the ADC. .

Note: 00: PCLK2 divided by 2
01: PCLK2 divided by 4
10: PCLK2 divided by 6
11: PCLK2 divided by 8

Bits 15:0 Reserved, must be kept at reset value.

ADC_DR

Address offset: 0x4C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **DATA[15:0]:** Regular data

These bits are read-only. They contain the conversion result from the regular channels. The data are left- or right-aligned as shown in *Figure 35* and *Figure 36*.

ADC Configuration Sequence

ADC CONFIGURATION SEQUENCE

Thynk Loop

→Enable ADC clock bus
→Enable ADC clock

→Configure the GPIO as Analog

→Turn off the ADC
→Configure the ADC clock prescalar
→Configure the resolution, ADC Mode
→Configure the sequence
→Configure the sampling time
→Turn on the ADC

Reading Data From ADC

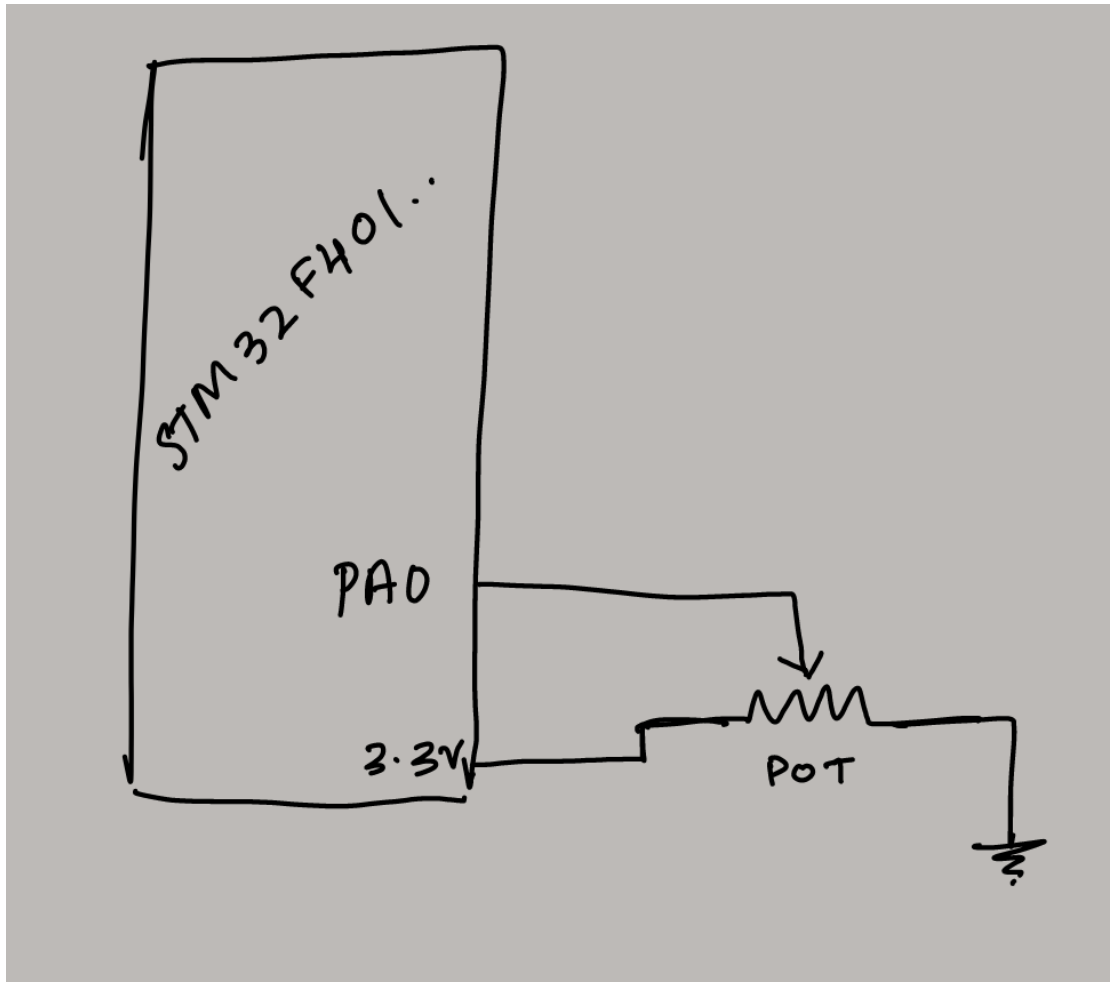
Reading Data From ADC

→Start the ADC conversion

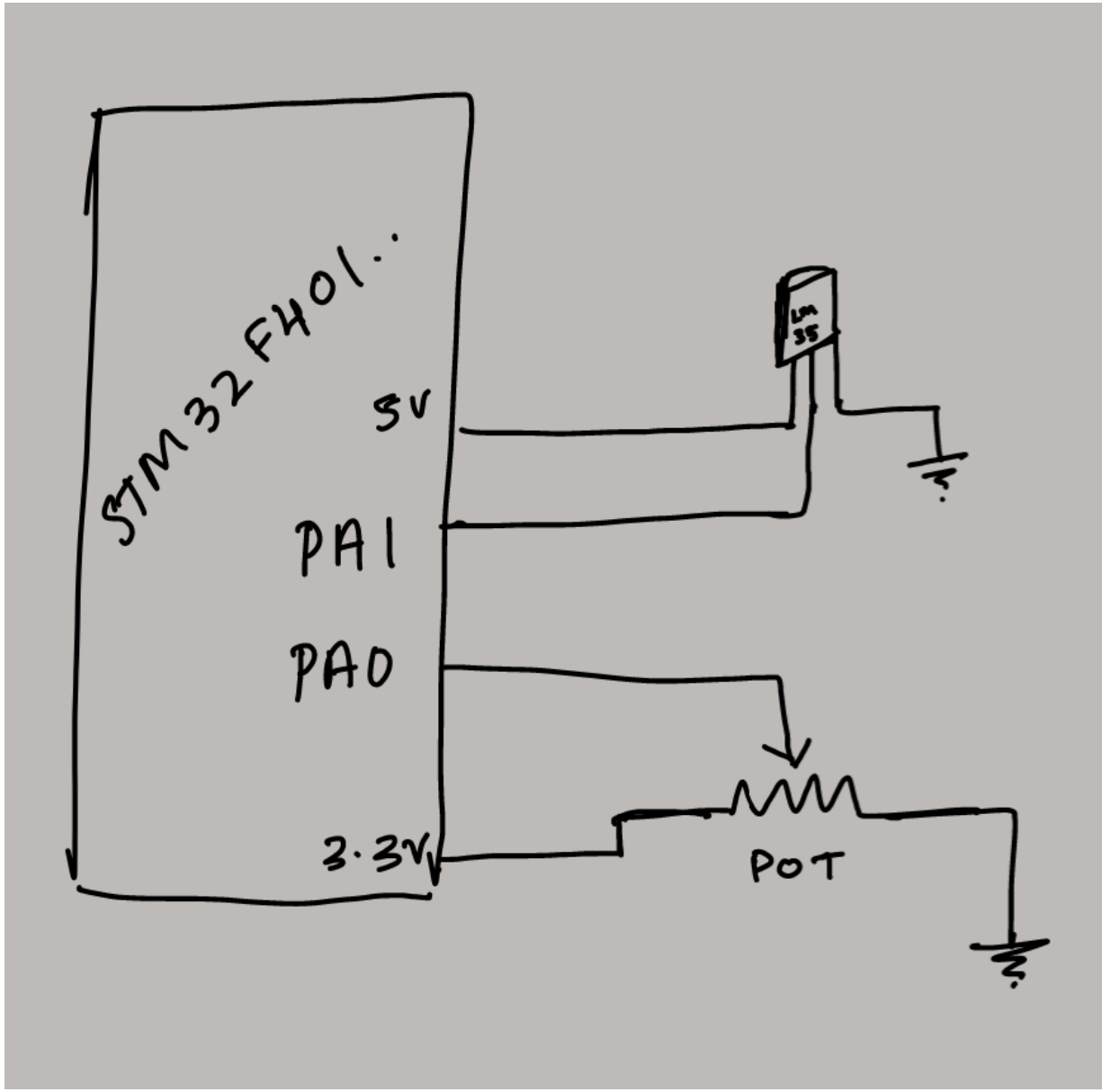
→Pol the EOC flag for conversion End

→Read the data from DR register

Circuit Connection



Circuit Connection - Multi ADC



ADC CONFIGURATION SEQUENCE – Multi Channel

Thynk Loop

→Enable ADC clock bus
→Enable ADC clock

→Configure the GPIO as Analog

→Turn off the ADC
→Configure the ADC clock pre scalar
→Configure the resolution, ADC Mode
→Configure the sampling time – CH0
→Configure the sampling time - CH1
→Turn on the ADC

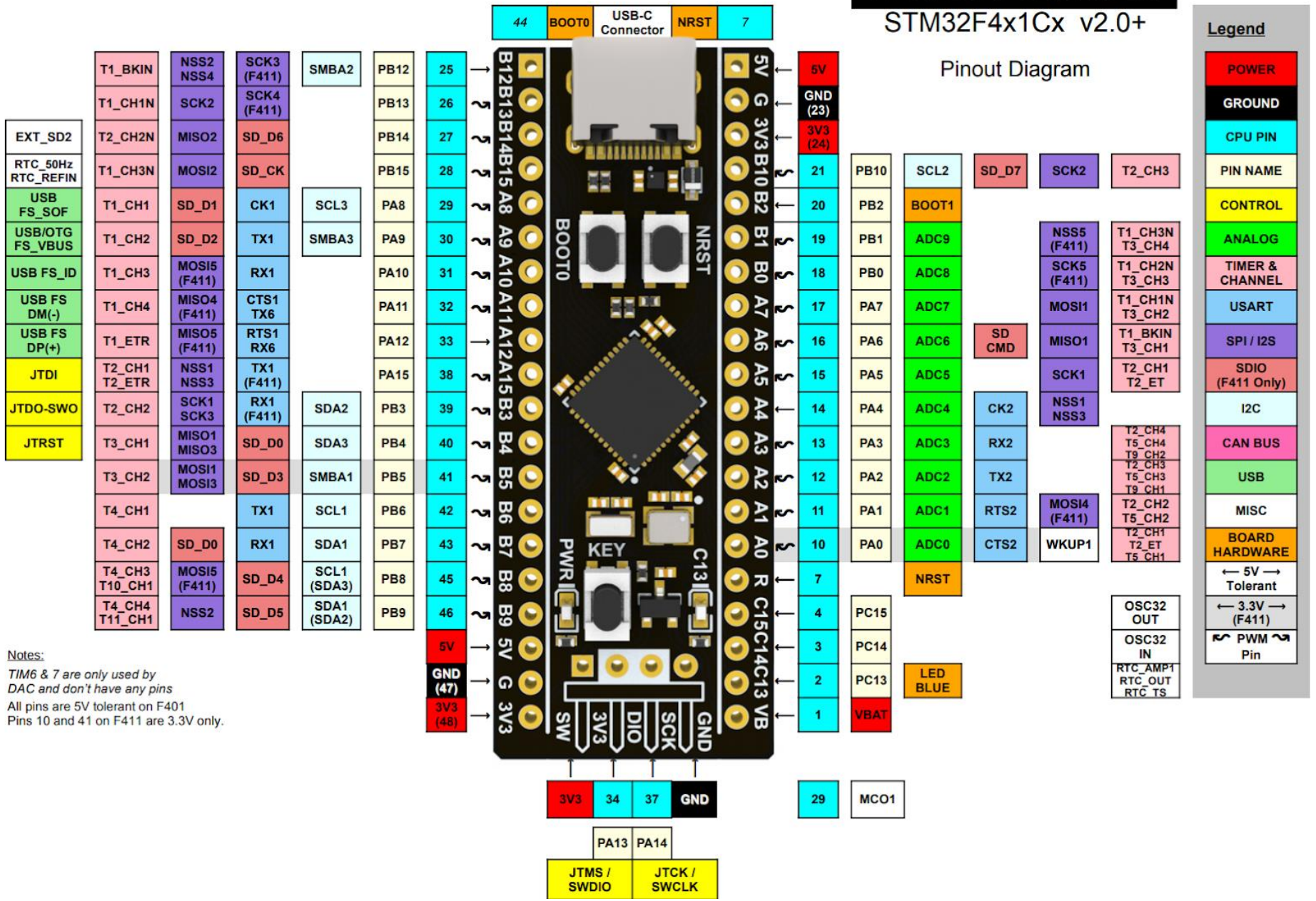
Reading Data From ADC

Thynk Loop

→Configure the sequence 1 to CH0
→Start the ADC conversion
→Pol the EOC flag for conversion End
→Read the data from DR register

→Configure the sequence 1 to CH1
→Start the ADC conversion
→Pol the EOC flag for conversion End
→Read the data from DR register

BlackPill – Pin Configurations



Notes:

TIM6 & 7 are only used by DAC and don't have any pins

All pins are 5V tolerant on F401
Pins 10 and 41 on F411 are 3.3V only.

GitHub Repo

Thynk Loop