



STM32 Fundamentals: Hands-on Workshop Series

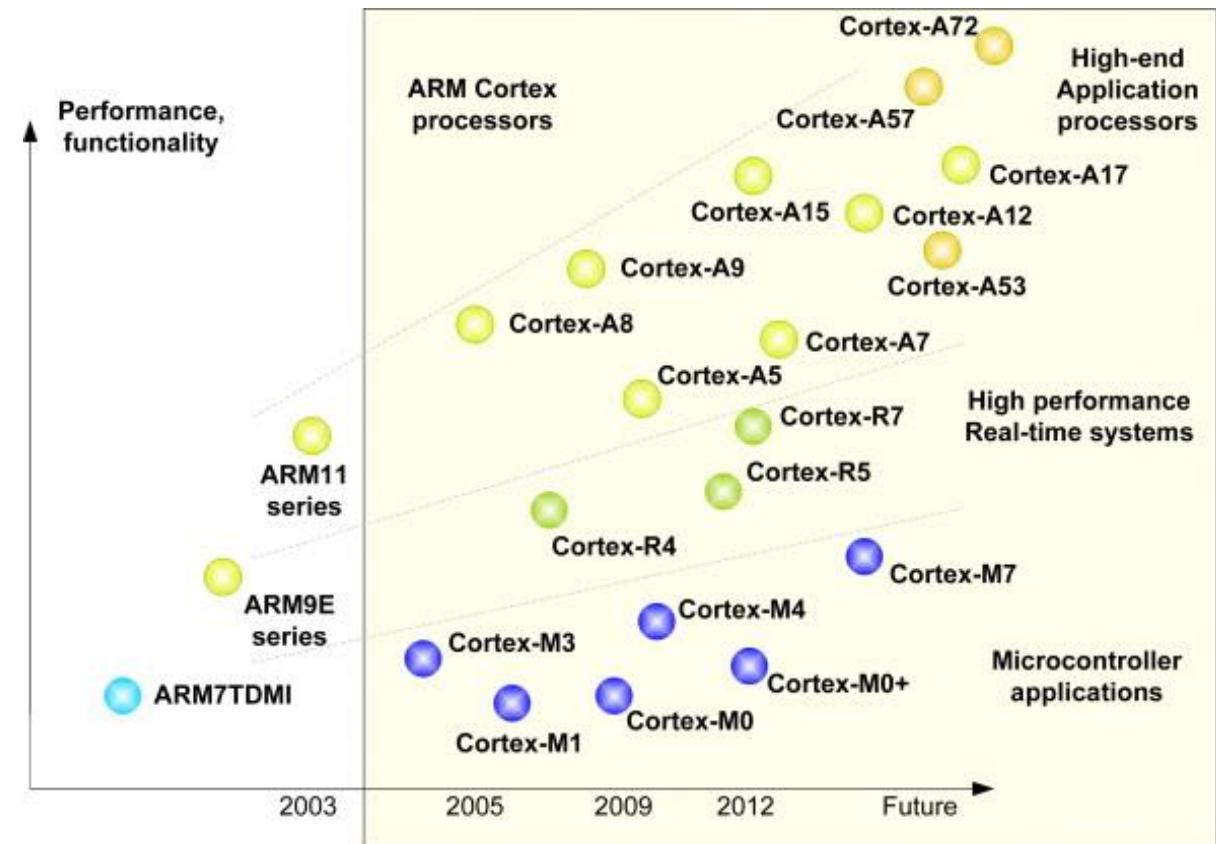
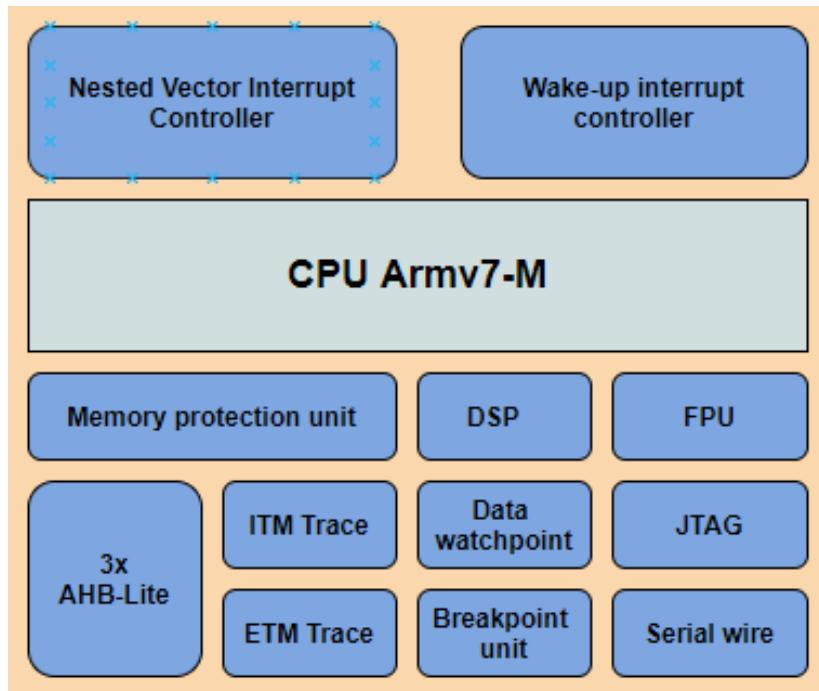
Module 2

Module Agenda

- ARM Cortex-M Architecture
- Components of ARM Cortex-M
 - NVIC
 - SysTick
 - MPU
- Bus Interfaces
- ARM Cortex-M Exception Model
- Low Power Mode

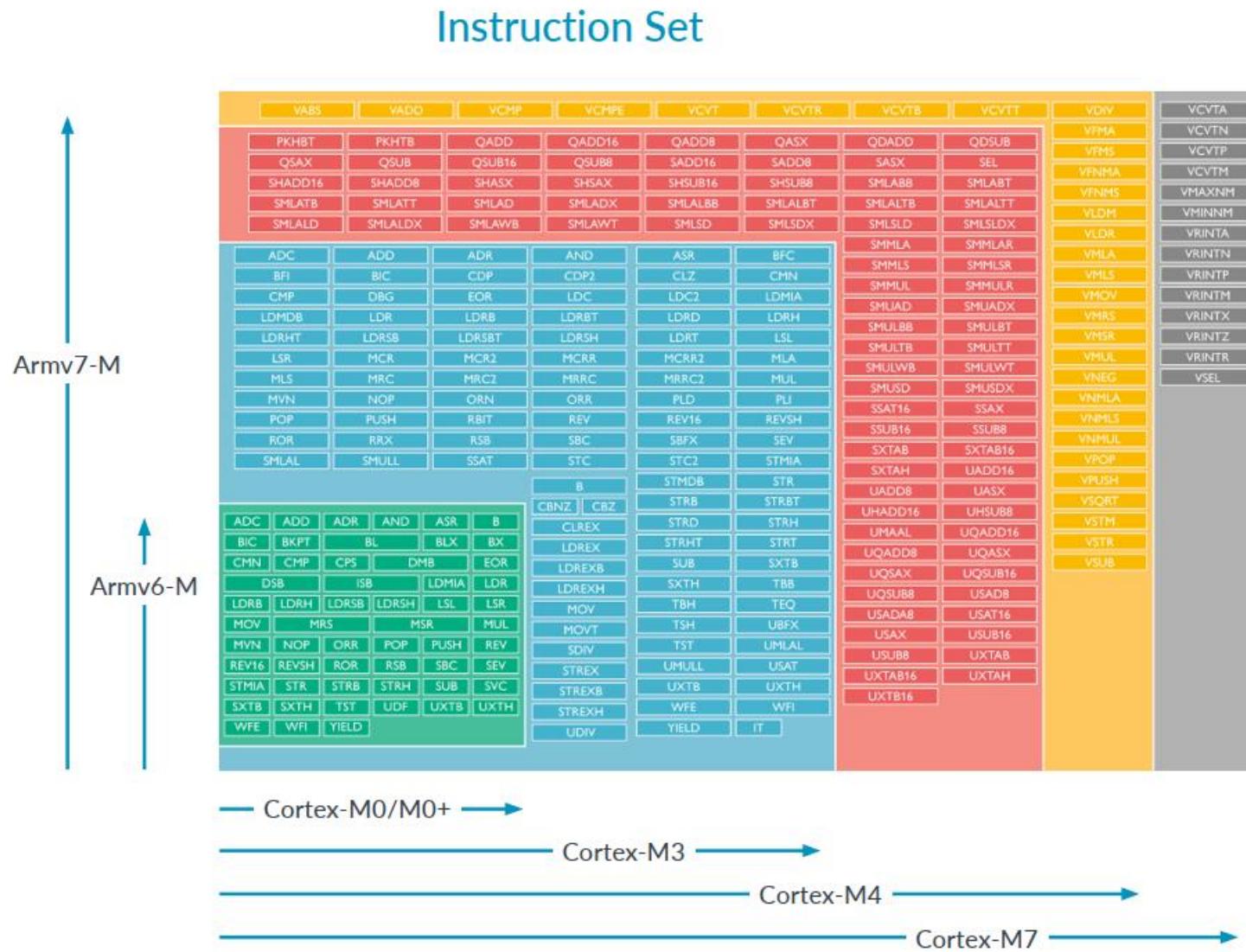
ARM Cortex-M Architecture

- Cortex-M0, -M0+, -M1 - Armv6-M
- Cortex-M3, -M4, -M7 - Armv7-M
- Cortex-M23, -M33 - Armv8-M
- Cortex-M55 - Armv9-M

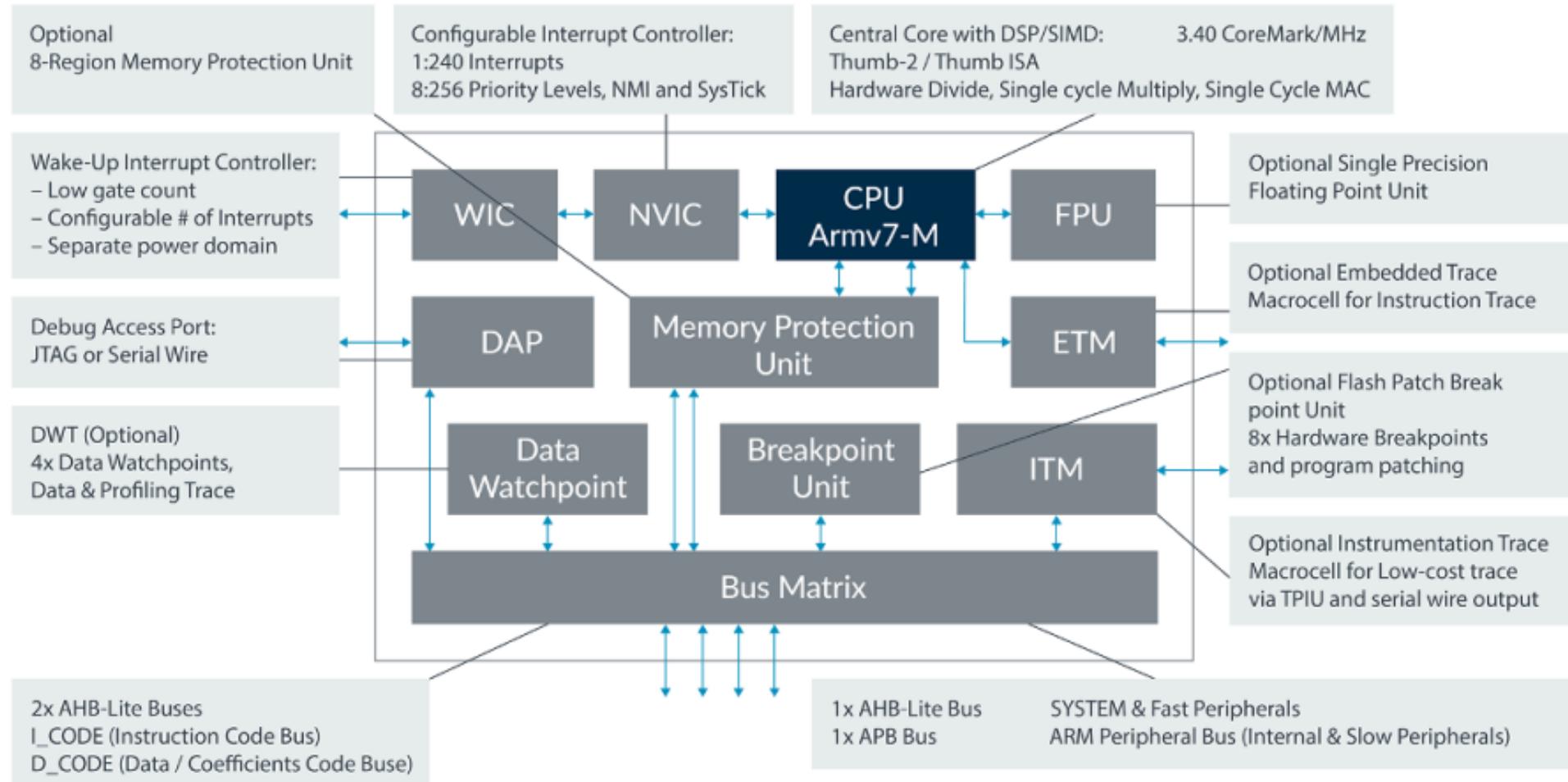


• ARM v7 cortex M reference manual

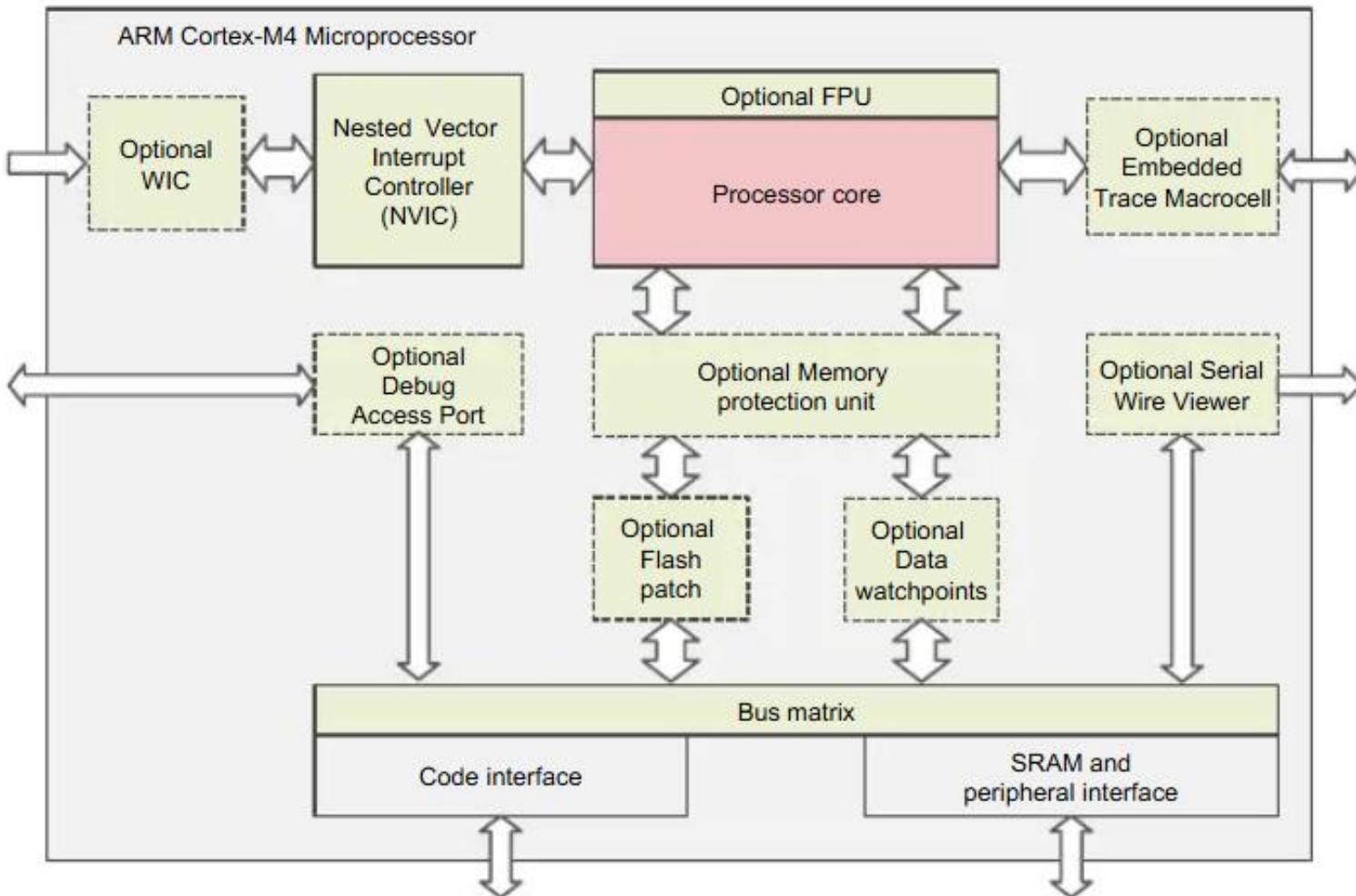
ARM Cortex-M Architecture



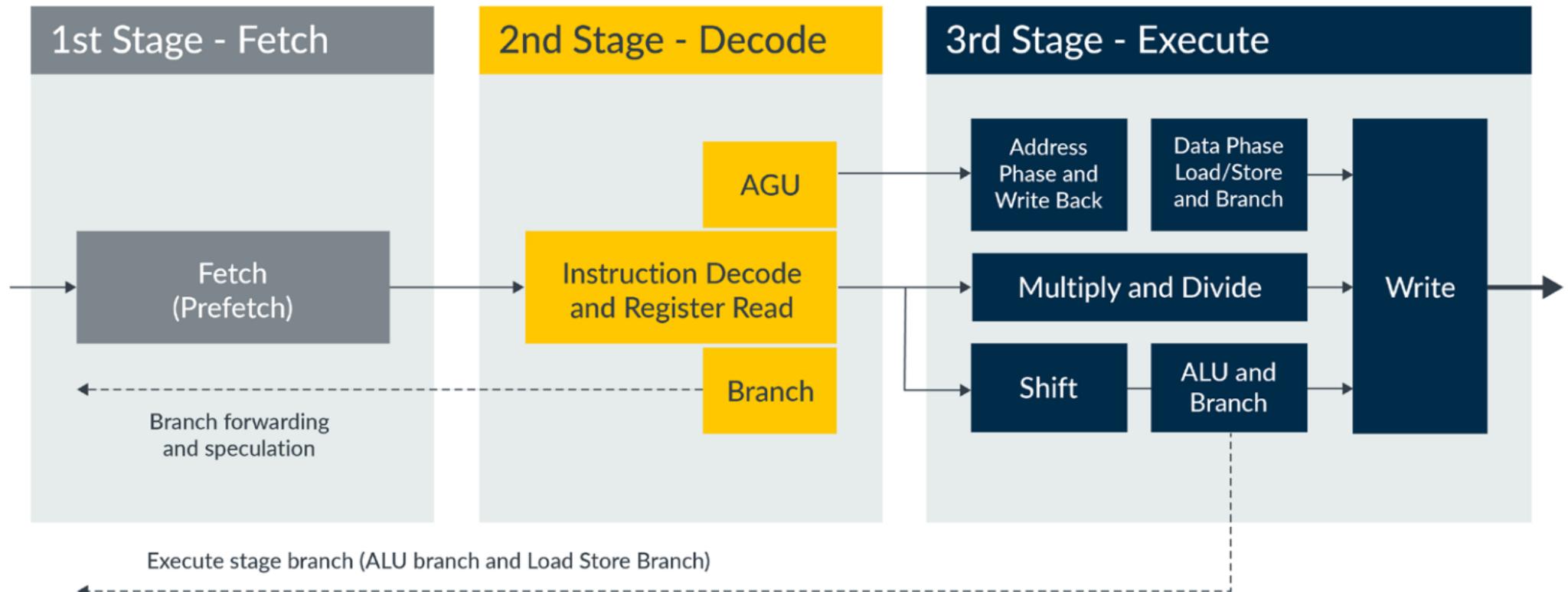
ARM Cortex-M Architecture



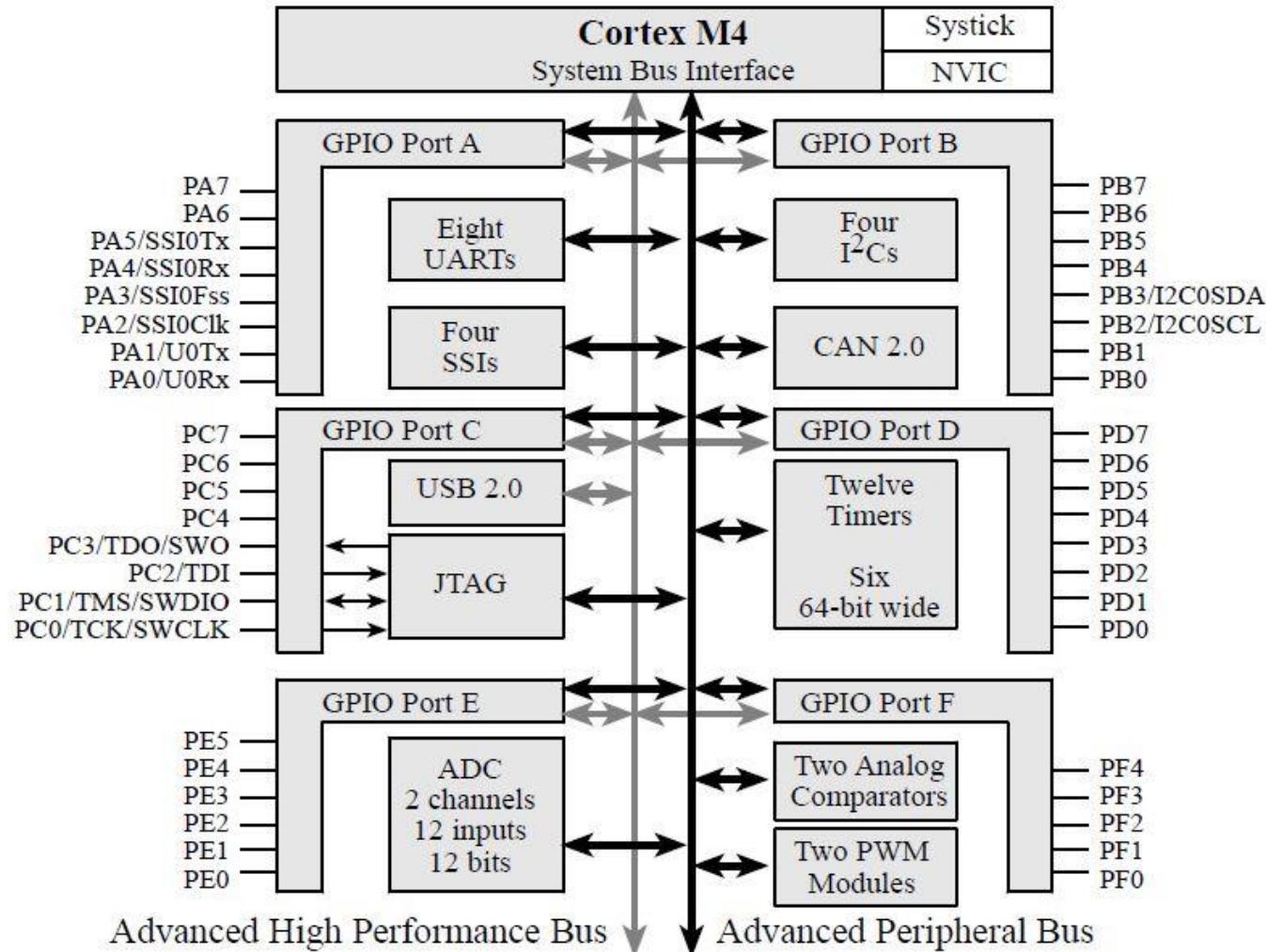
ARM Cortex-M Architecture



ARM Cortex-M Architecture



ARM Cortex-M Architecture

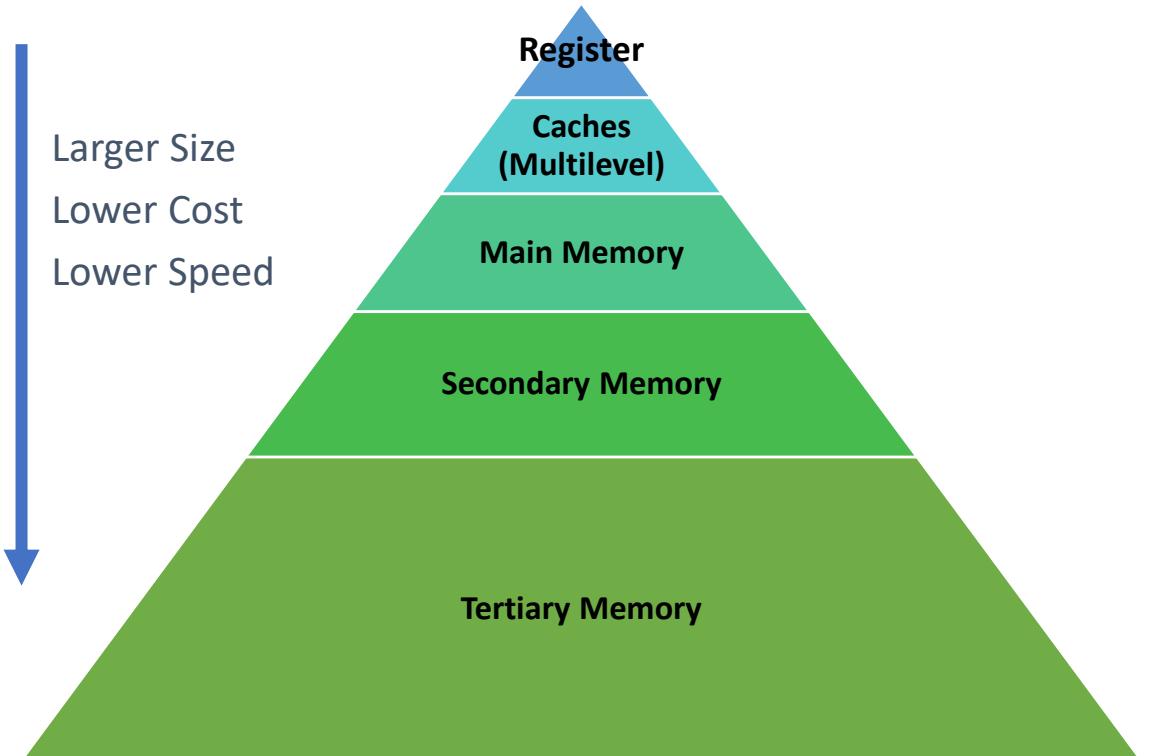


Memory Hierarchy

Memory Types

- Register: usually one CPU cycle to access
- Cache: CPU cache, translation lookaside buffer (TLB)
 - SRAM
- Main memory
 - DRAM
- Secondary memory: hard disk, solid-state drive
- Tertiary memory: tape libraries, cloud

Functional/Organizational View



Memory Hierarchy

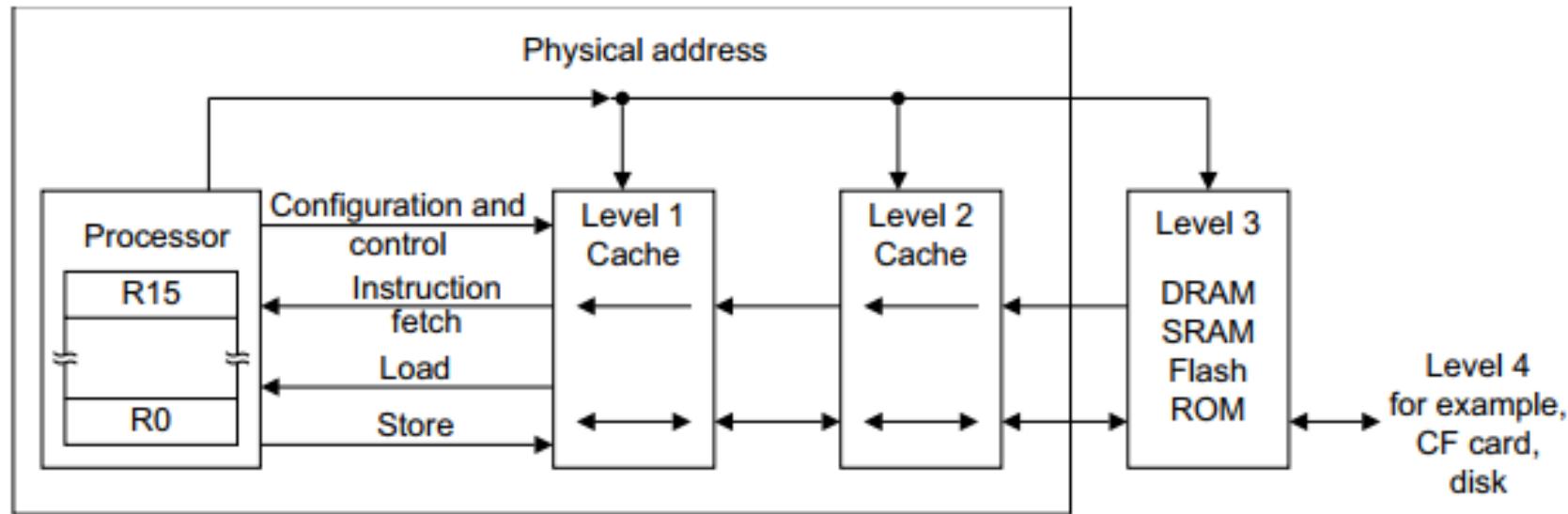


Figure A3-9 Multiple levels of cache in a memory hierarchy

Memory Technology Basics

SRAM vs DRAM

SRAM – Static Random Access Memory

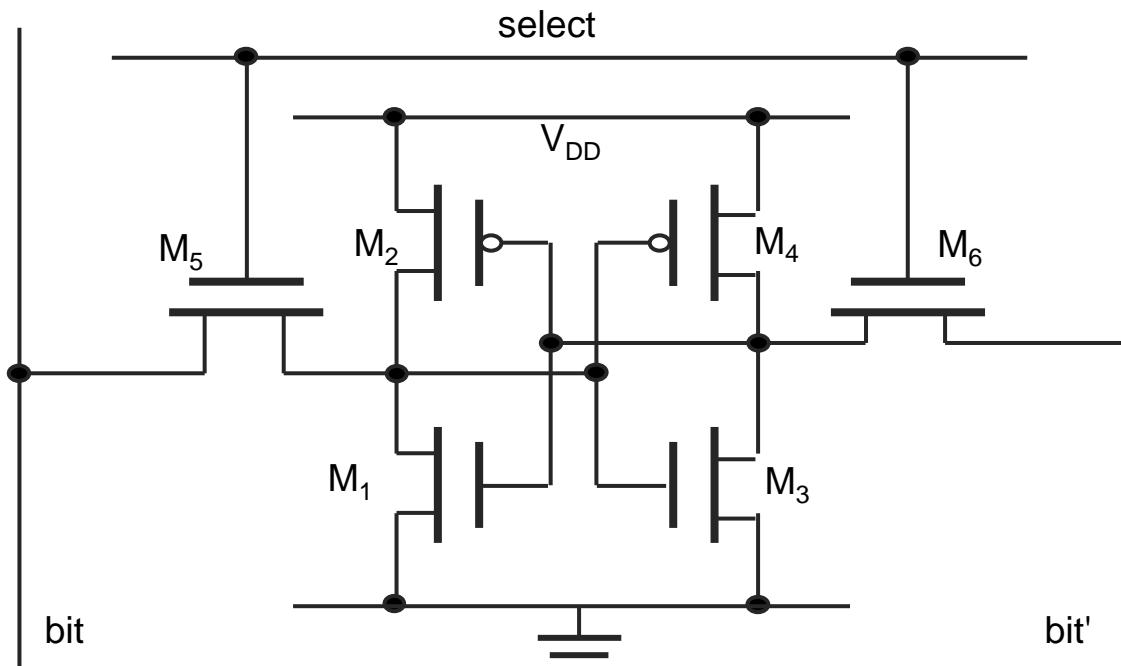
- Static – holds data as long as power is maintained
- Requires multiple transistors to retain one bit and has low density compared to DRAM, thus more expensive
- Faster than DRAM
- Used for caches (next module)

DRAM – Dynamic Random Access Memory

- Dynamic – must be refreshed periodically to hold data
- Requires only one transistor (and one capacitor) to retain one bit of data
- High density, thus cheaper than SRAM
- Used for main memory and sometimes for larger caches

SRAM Cell

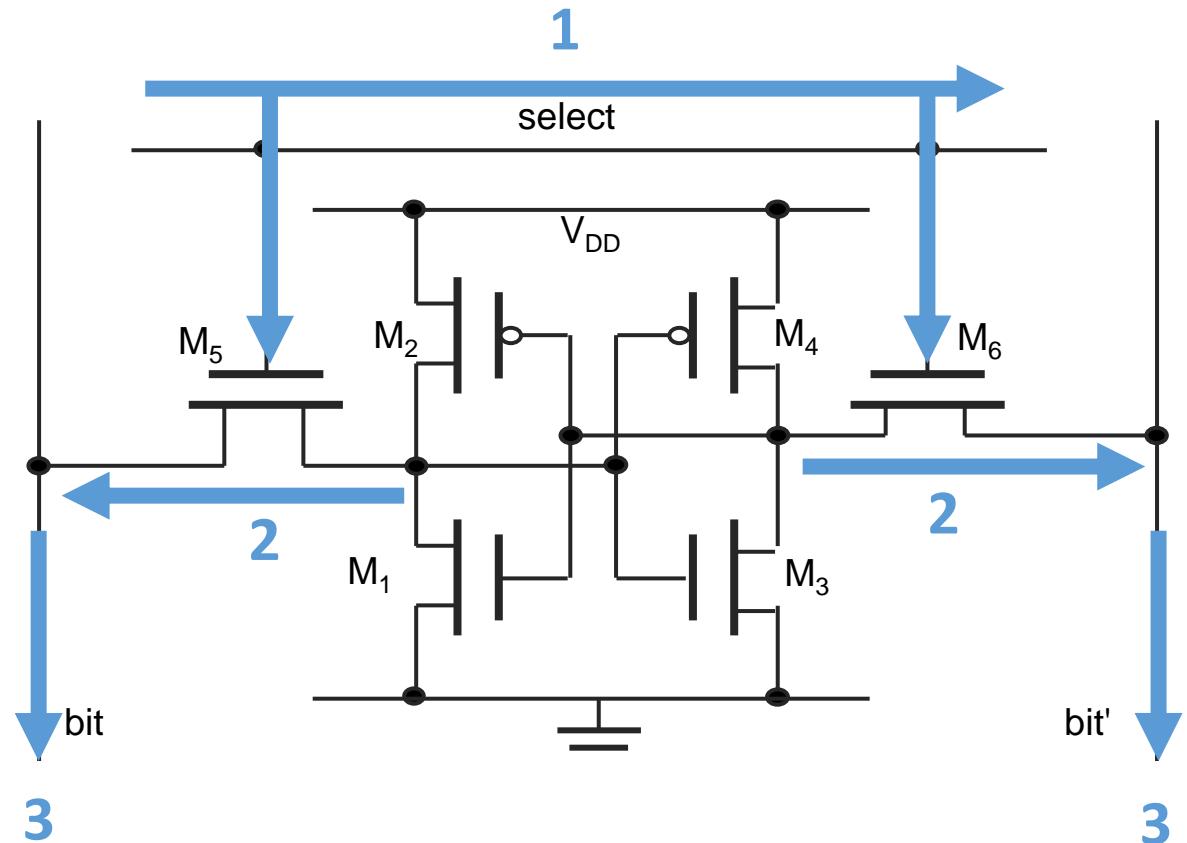
- An SRAM cell is typically made up of six transistors (MOSFETs).
 - A single bit is stored on 4 transistors (M1-M4), which form two inverters that are cross-coupled.
 - Access to the bit is controlled by two access transistors (M5 and M6), which are gated by the word line (select).
 - Data are read in and out through the bit lines.



Accessing SRAM

Read operation

- The address is decoded and the desired cell is then selected, in which case the select line is set to one.
- Depending on the value of the 4 transistors (M1-M4), one of the bit lines (bit or bit') will be charged to 1 and the other will be drained to 0.
- The states of the two bit lines are then read out as 1-bit data.



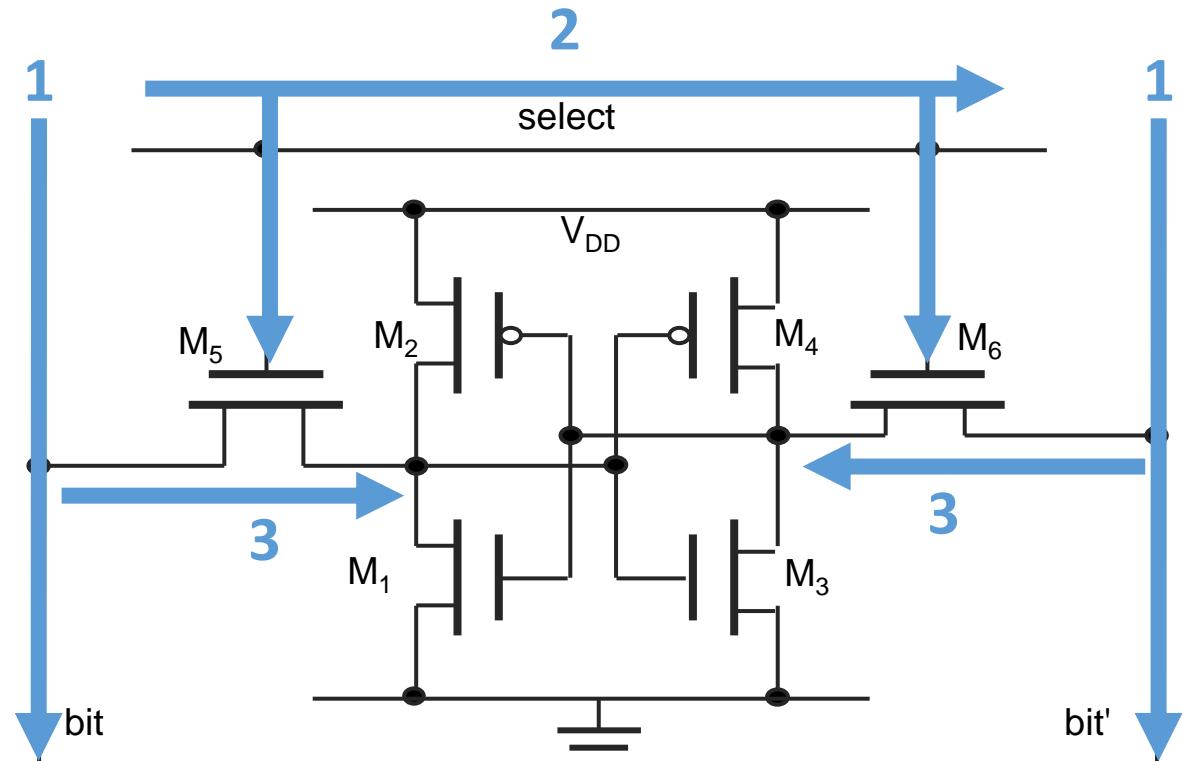
Accessing SRAM

Write operation

The two bit lines are pre-charged to the desired value (e.g., bit = VDD, bit' = VSS).

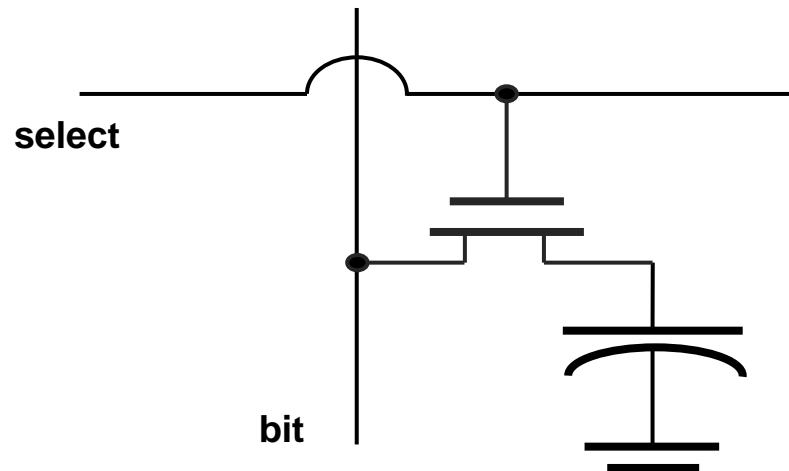
The address is decoded and the desired cell is then selected, in which case the select line is set to one.

The 4 transistors (M1-M4) are then forced to flip their states (either charged or discharged) since the bit lines normally have much higher capacitance than the 4 transistors.



DRAM

- A DRAM cell is typically made up of three or even one transistor.
 - A single bit is stored in one capacitor.
 - Access to the bit is controlled by a single access transistor, which is gated by the word line (select).
 - As in SRAM, data are read in and out through the bit line.

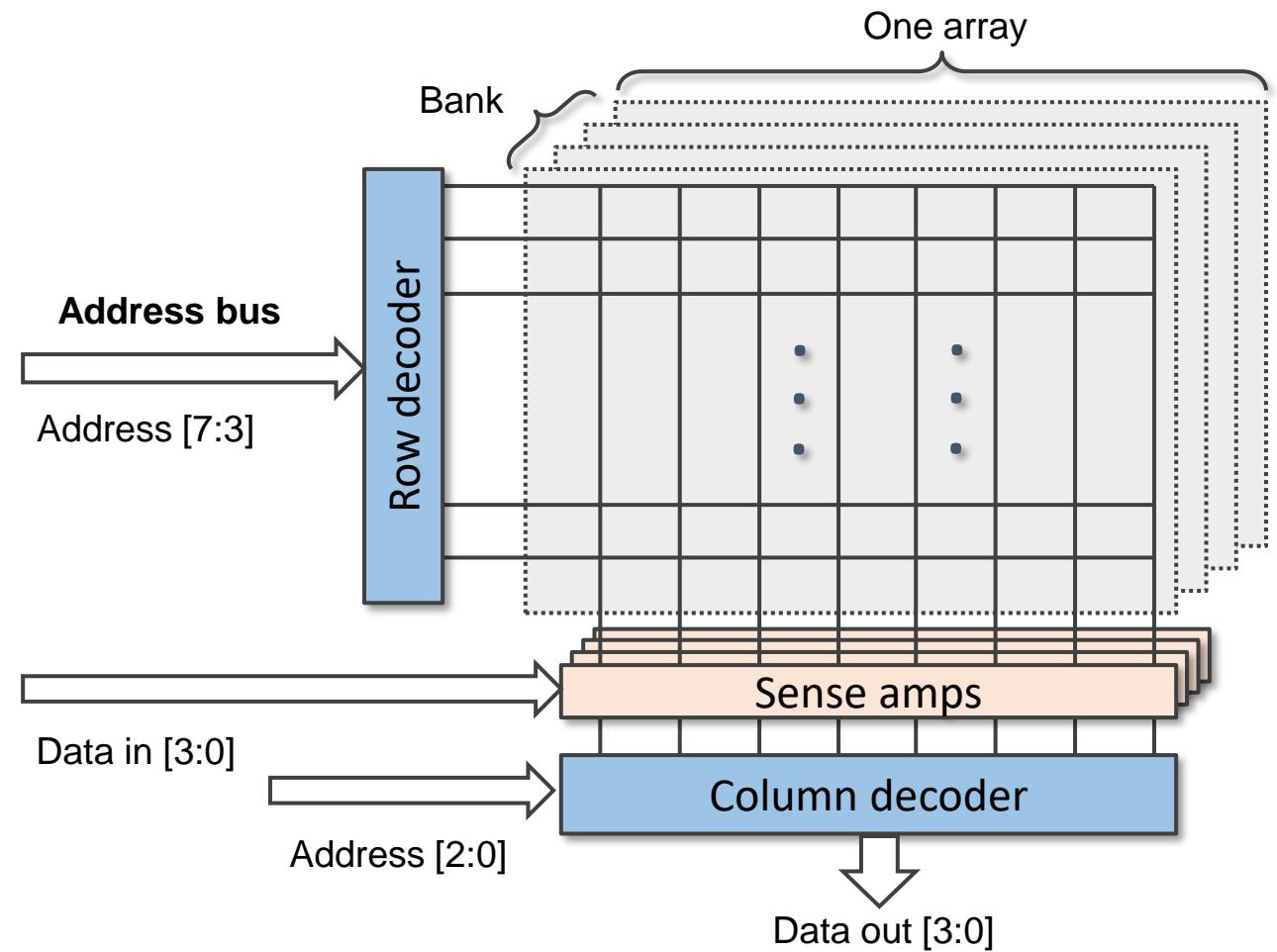


DRAM

- The status of the capacitor (charged or uncharged) indicates the bit state (1 or 0).
- Access is similar to SRAM but.
 - The capacitor is drained on a read and charged (if storing 1) on a write.
 - The cell needs to be refreshed (or recharged) periodically since the capacitor leaks its charge.
 - For example, every 7.8 ms
- DRAM is higher density than SRAM.
 - Therefore less expensive
- DRAM can be categorized according to its synchronization and data rate.
 - Most DRAM is now synchronous (SDRAM), so it has a clock, rather than asynchronous.
 - Double data rate (DDR) DRAM transfers data on both the rising and falling clock edges.

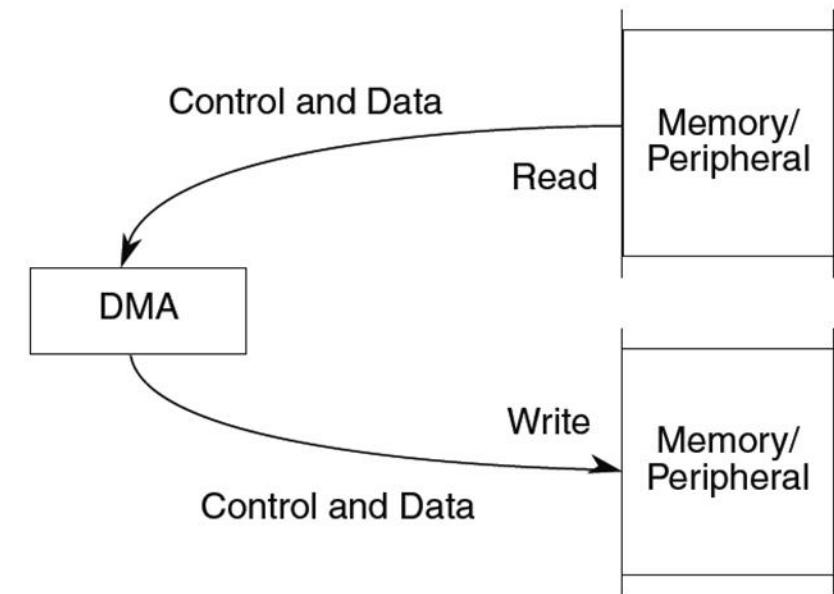
DRAM Organization

- DRAM cells are organized into arrays.
 - A whole row is accessed at once.
 - But only one bit is read out of the row.
- Multiple arrays are grouped into banks.
 - All arrays in a bank are accessed simultaneously.
 - A bank with N arrays provides N bits per access.

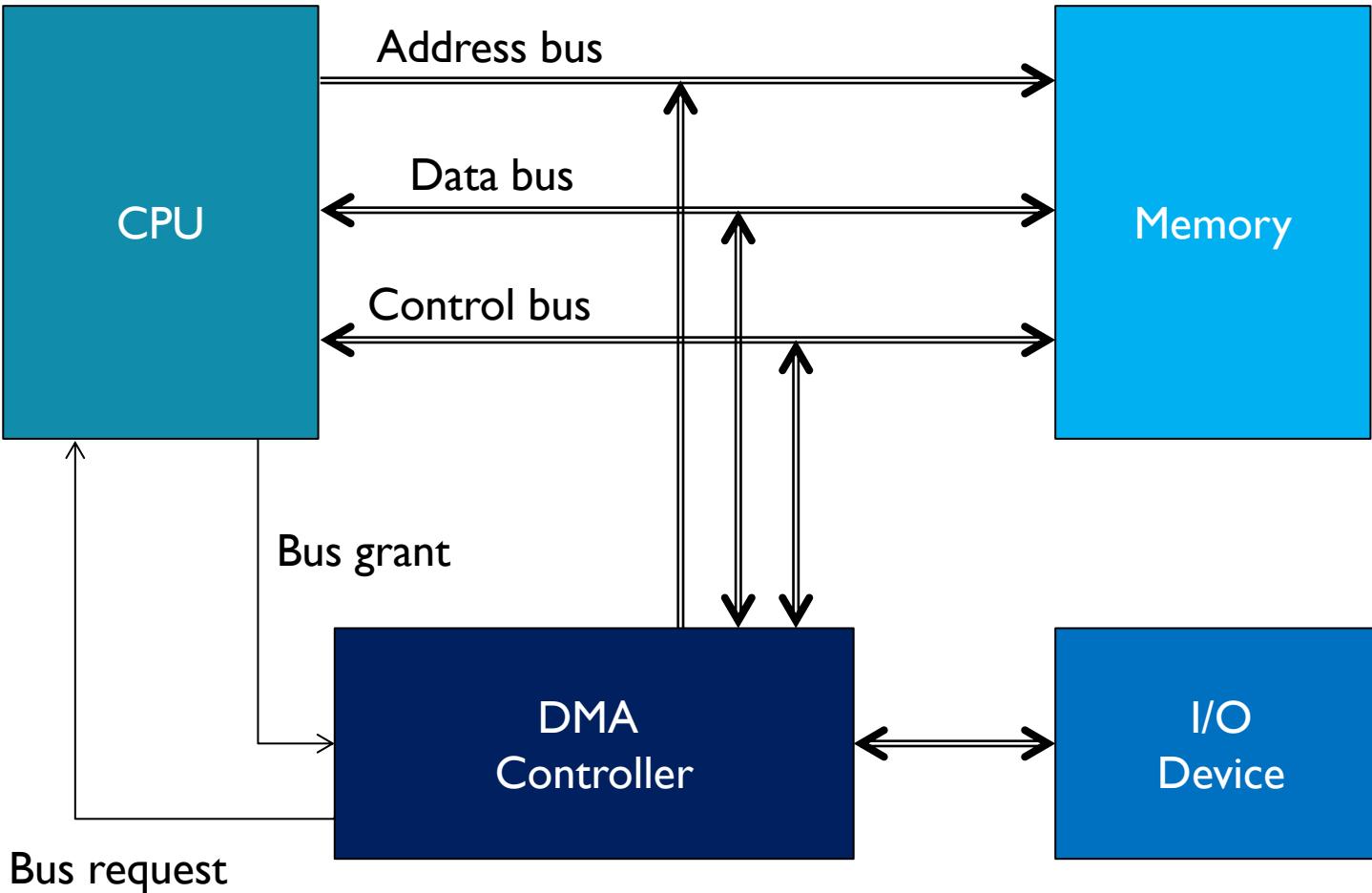


Direct Memory Access (DMA)

- Instead of involving the CPU, provide dedicated hardware to control the transfer.
 - A controller for direct memory access, or DMA.
 - CPU now just required to configure this DMA controller correctly.
- Typically supports multiple configurable options:
 - Number of data items to copy
 - Source and destination addresses
 - Fixed or changeable (e.g., increment and decrement)
 - Size of data item
 - Timing of transfer start
- A DMA controller can also work with interrupts, e.g., interrupt CPU at the end of a transfer.
- The main idea is to exempt the CPU from busy-waiting and frequent interruptions.



DMA Architecture



ARM v7 – Address Map

Address	Name	Device type	XN?	Cache	Description
0x00000000- 0x1FFFFFFF	Code	Normal	-	WT	Typically ROM or flash memory.
0x20000000- 0x3FFFFFFF	SRAM	Normal	-	WBWA	SRAM region typically used for on-chip RAM.
0x40000000- 0x5FFFFFFF	Peripheral	Device	XN	-	On-chip peripheral address space.
0x60000000- 0x7FFFFFFF	RAM	Normal	-	WBWA	Memory with write-back, write allocate cache attribute for L2/L3 cache support.

ARM v7 – Address Map

Address	Name	Device type	XN?	Cache	Description
0x80000000- 0x9FFFFFFF	RAM	Normal	-	WT	Memory with Write-Through cache attribute.
0xA0000000- 0xBFFFFFFF	Device	Device, shareable	XN	-	Shared device space.
0xC0000000- 0xDFFFFFFF	Device	Device, Non-shareable	XN	-	Non-shared device space.
0xE0000000- 0xFFFFFFFF	System	See <i>Description</i>	XN	-	System segment for the PPB and vendor system peripherals, see Table B3-2 .

System Controlled Space (SCS)

The *System Control Space* (SCS) is a memory-mapped 4KB address space that provides 32-bit registers for configuration, status reporting and control. The SCS registers divide into the following groups:

- Fault reporting.
- A system timer, **SysTick**.
- A *Nested Vectored Interrupt Controller* (NVIC).
- A *Protected Memory System Architecture* (PMSA).
- System debug.

SCS – Some Registers

B3.2.16 HardFault Status Register, HFSR

The HFSR characteristics are:

Purpose	Shows the cause of any HardFault.
Usage constraints	Write a one to a register bit to clear the corresponding fault.
Configurations	Always implemented.
Attributes	See Table B3-4 on page B3-596 .

B3.2.17 MemManage Fault Address Register, MMFAR

The MMFAR characteristics are:

Purpose	Shows the address of the memory location that caused an MPU fault.
Usage constraints	Valid only when MMFSR.MMARVALID is set, otherwise reads as UNKNOWN.
Configurations	Always implemented.
Attributes	See Table B3-4 on page B3-596 .

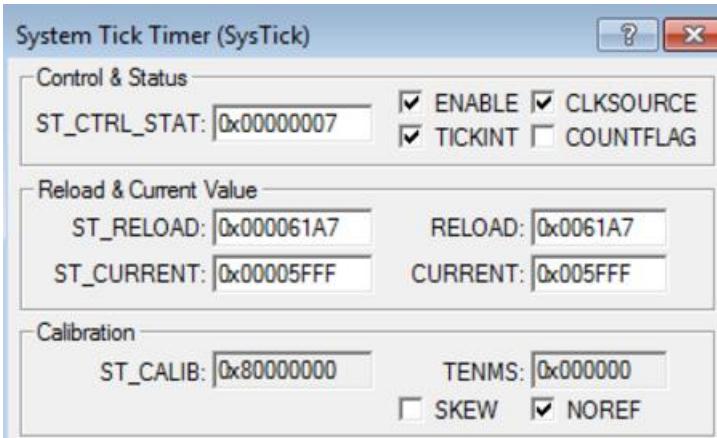
SCS – Some Registers

Address	Name	Type	Reset	Description
0xE000ED2C	HFSR	RW	0x00000000	<i>HardFault Status Register, HFSR</i> on page B3-612.
0xE000ED30	DFSR	RW	0x00000000 ^c	<i>Debug Fault Status Register, DFSR</i> on page C1-699.
0xE000ED34	MMFAR	RW	UNKNOWN	<i>MemManage Fault Address Register, MMFAR</i> on page B3-613.
0xE000ED38	BFAR	RW	UNKNOWN	<i>BusFault Address Register, BFAR</i> on page B3-614.
0xE000ED3C	AFSR	RW	UNKNOWN	<i>Auxiliary Fault Status Register, AFSR</i> on page B3-614, IMPLEMENTATION DEFINED.
0xE000ED40 - 0xE000ED84	-	-	-	Reserved for CPUID registers, see Chapter B4 The CPUID Scheme .
0xE000ED88	CPACR	RW	UNKNOWN	<i>Coprocessor Access Control Register, CPACR</i> on page B3-614.
0xE000ED8C	-	-	-	Reserved.

SysTick

The System Tick Timer (SysTick) dialog (for Cortex-M3, Cortex-M4, and Cortex-M7 cores) shows controls for the system timer. The system timer is an optional feature. If not implemented, then the SysTick registers are reserved.

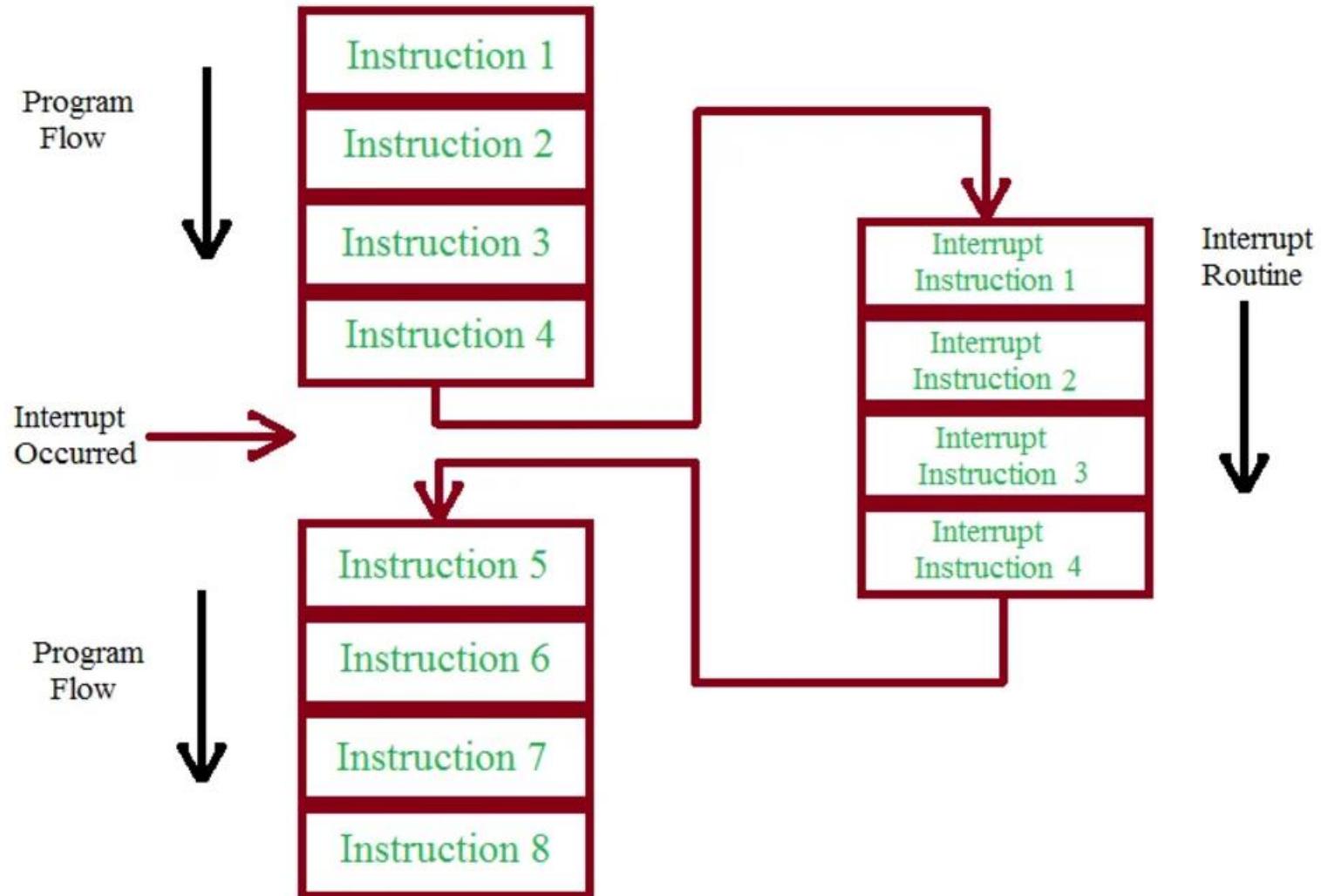
When enabled, the system timer counts down from the ST_RELOAD value to zero, then reloads (wraps) the value on the next clock edge and decrements on subsequent clock cycles



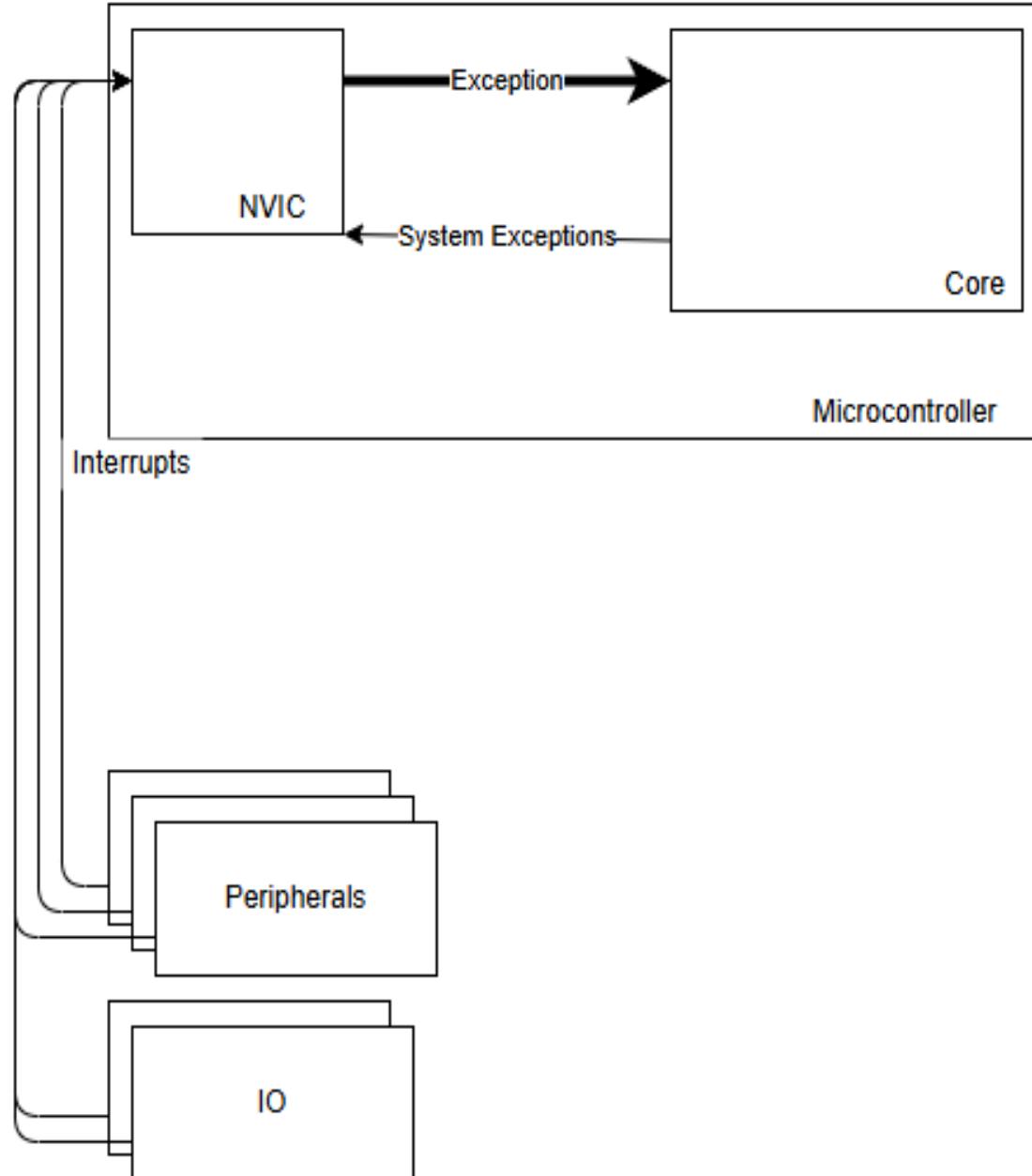
SysTick

Address	Name	Type	Reset	Description
0xE000E010	SYST_CSR	RW	0x0000000x ^a	<i>SysTick Control and Status Register, SYST_CSR</i>
0xE000E014	SYST_RVR	RW	UNKNOWN	<i>SysTick Reload Value Register, SYST_RVR</i> on page B3-622
0xE000E018	SYST_CVR	RW	UNKNOWN	<i>SysTick Current Value Register, SYST_CVR</i> on page B3-622
0xE000E01C	SYST_CALIB	RO	IMP DEF	<i>SysTick Calibration value Register, SYST_CALIB</i> on page B3-623
0xE000E020-	-	-	-	Reserved
0xE000E0FC				

Nested Vector Interrupt Controller (NVIC)



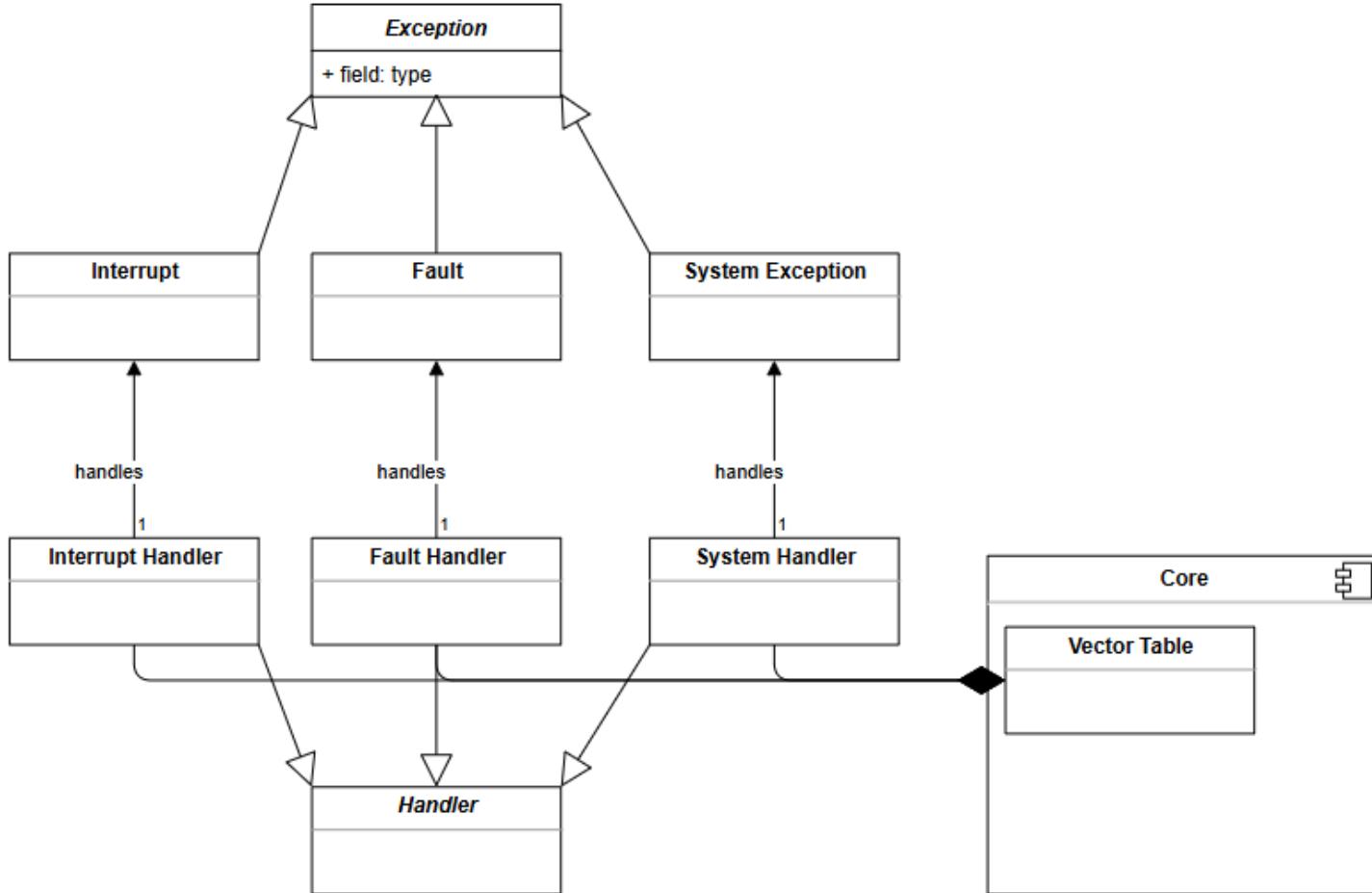
Role of NVIC



Nested Vector Interrupt Controller (NVIC)

Address	Name	Type	Reset	Description
0xE000E100- 0xE000E13C	NVIC_ISER0- NVIC_ISER15	RW	0x00000000	<i>Interrupt Set-Enable Registers, NVIC_ISER0-NVIC_ISER15 on page B3-628</i>
0xE000E180- 0xE000E1BC	NVIC_ICER0- NVIC_ICER15	RW	0x00000000	<i>Interrupt Clear-Enable Registers, NVIC_ICER0-NVIC_ICER15 on page B3-628</i>
0xE000E200- 0xE000E23C	NVIC_ISPR0- NVIC_ISPR15	RW	0x00000000	<i>Interrupt Set-Pending Registers, NVIC_ISPR0-NVIC_ISPR15 on page B3-629</i>
0xE000E280- 0xE000E2BC	NVIC_ICPR0- NVIC_ICPR15	RW	0x00000000	<i>Interrupt Clear-Pending Registers, NVIC_ICPR0-NVIC_ICPR15 on page B3-629</i>
0xE000E300- 0xE000E33C	NVIC_IABR0- NVIC_IABR15	RO	0x00000000	<i>Interrupt Active Bit Registers, NVIC_IABR0-NVIC_IABR15 on page B3-630</i>
0xE000E340- 0xE000E3FC	-	-	-	Reserved
0xE000E400- 0xE000E5EC	NVIC_IPR0- NVIC_IPR123	RW	0x00000000	<i>Interrupt Priority Registers, NVIC_IPR0-NVIC_IPR123 on page B3-630</i>
0xE000E5F0- 0xE000ECFC	-	-	-	Reserved

Exception Handler



Appendix

All About Registers

Register	Description, see
Access Control, Counter	<i>CNTACR_n, Counter Access Control Register</i> on page D5-2394
Access Control, Counter PL0	<i>CNTPL0ACR, Counter PL0 Access Control Register</i> on page D5-2403
Access Permissions, pre-ARMv6	<i>CP15 c5, Memory Region Access Permissions Registers, DAPR and IAPR, ARMv4 and ARMv5</i> on page D15-2610
ACTLR	<i>ACTLR, IMPLEMENTATION DEFINED Auxiliary Control Register, PMSA</i> on page B6-1802 <i>ACTLR, IMPLEMENTATION DEFINED Auxiliary Control Register, VMSA</i> on page B4-1518
ADFSR	<i>ADFSR and AIFSR, Auxiliary Data and Instruction Fault Status Registers, PMSA</i> on page B6-1804 <i>ADFSR and AIFSR, Auxiliary Data and Instruction Fault Status Registers, VMSA</i> on page B4-1519
AIDR	<i>AIDR, IMPLEMENTATION DEFINED Auxiliary ID Register, PMSA</i> on page B6-1803 <i>AIDR, IMPLEMENTATION DEFINED Auxiliary ID Register, VMSA</i> on page B4-1520
AIFSR	<i>ADFSR and AIFSR, Auxiliary Data and Instruction Fault Status Registers, PMSA</i> on page B6-1804 <i>ADFSR and AIFSR, Auxiliary Data and Instruction Fault Status Registers, VMSA</i> on page B4-1519
AMAIR0	<i>AMAIR0 and AMAIR1, Auxiliary Memory Attribute Indirection Registers 0 and 1, VMSA</i> on page B4-1521
AMAIR1	
Application Program Status	<i>The Application Program Status Register (APSR)</i> on page A2-49
APSR	<i>The Application Program Status Register (APSR)</i> on page A2-49
ATS12NSOPR	<i>Performing address translation operations</i> on page B4-1742
ATS12NSOPW	
ATS12NSOUR	
ATS12NSOUW	
ATS1CPR	
ATS1CPW	
ATS1CUR	
ATS1CUW	
ATS1HR	
ATS1HW	

Register	Description, see
Authentication Status, Debug	<i>DBGAUTHSTATUS, Authentication Status register</i> on page C11-2197
Authentication Status, Performance Monitors	<i>PMAUTHSTATUS, Performance Monitors Authentication Status register</i> on page D2-2349
Auxiliary Control	<i>ACTLR, IMPLEMENTATION DEFINED Auxiliary Control Register, PMSA</i> on page B6-1802 <i>ACTLR, IMPLEMENTATION DEFINED Auxiliary Control Register, VMSA</i> on page B4-1518
Auxiliary Fault Status	<i>ADFSR and AIFSR, Auxiliary Data and Instruction Fault Status Registers, PMSA</i> on page B6-1804 <i>ADFSR and AIFSR, Auxiliary Data and Instruction Fault Status Registers, VMSA</i> on page B4-1519
Auxiliary Feature 0	<i>ID_AFR0, Auxiliary Feature Register 0, PMSA</i> on page B6-1845 <i>ID_AFR0, Auxiliary Feature Register 0, VMSA</i> on page B4-1600
Auxiliary ID	<i>AIDR, IMPLEMENTATION DEFINED Auxiliary ID Register, PMSA</i> on page B6-1803 <i>AIDR, IMPLEMENTATION DEFINED Auxiliary ID Register, VMSA</i> on page B4-1520
Auxiliary Memory Attribute Indirection	<i>AMAIRO and AMAIR1, Auxiliary Memory Attribute Indirection Registers 0 and 1, VMSA</i> on page B4-1521
Block Transfer Status, ARMv6	<i>CP15 c7, Block Transfer Status Register</i> on page D12-2522
BPIALL	<i>Cache and branch predictor maintenance operations, PMSA</i> on page B6-1932
BPIALLIS	<i>Cache and branch predictor maintenance operations, VMSA</i> on page B4-1735
BPIMVA	
Breakpoint Control, Debug	<i>DBGBCR, Breakpoint Control Registers</i> on page C11-2199
Breakpoint Extended Value, Debug	<i>DBGBXVR, Breakpoint Extended Value Registers</i> on page C11-2205
Breakpoint Value, Debug	<i>DBGBVR, Breakpoint Value Registers</i> on page C11-2204
c0 - c15	<i>Full list of PMSA CP15 registers, by coprocessor register number</i> on page B5-1785 <i>Full list of VMSA CP15 registers, by coprocessor register number</i> on page B3-1475

Cache and branch predictor maintenance operations	<i>Cache and branch predictor maintenance operations, PMSA</i> on page B6-1932 <i>Cache and branch predictor maintenance operations, VMSA</i> on page B4-1735
Cache Behavior Override, ARMv6 Security Extensions	<i>CP15 c9, Cache Behavior Override Register, CBOR</i> on page D12-2527
Cache Dirty Status, ARMv6	<i>CP15 c7, Cache Dirty Status Register, CDSR</i> on page D12-2519
Cache Level ID	<i>CLIDR, Cache Level ID Register, PMSA</i> on page B6-1808 <i>CLIDR, Cache Level ID Register, VMSA</i> on page B4-1526
Cache Lockdown, pre-ARMv7	<i>CP15 c9, cache lockdown support</i> on page D15-2615
Cache Size ID	<i>CCSIDR, Cache Size ID Registers, PMSA</i> on page B6-1806 <i>CCSIDR, Cache Size ID Registers, VMSA</i> on page B4-1524
Cache Size Selection	<i>CSSELR, Cache Size Selection Register, PMSA</i> on page B6-1826 <i>CSSELR, Cache Size Selection Register, VMSA</i> on page B4-1551
Cache Type	<i>CTR, Cache Type Register, PMSA</i> on page B6-1827 <i>CTR, Cache Type Register, VMSA</i> on page B4-1552

Register	Description, see
Cacheability, pre-ARMv6	<i>CP15 c2, Memory Region Cacheability Registers, DCR and ICR, ARMv4 and ARMv5</i> on page D15-2609
CBOR, ARMv6 Security Extensions	<i>CP15 c9, Cache Behavior Override Register, CBOR</i> on page D12-2527
CCSIDR	<i>CCSIDR, Cache Size ID Registers, PMSA</i> on page B6-1806 <i>CCSIDR, Cache Size ID Registers, VMSA</i> on page B4-1524
CDSR, ARMv6	<i>CP15 c7, Cache Dirty Status Register, CDSR</i> on page D12-2519
Claim Tag Clear, Debug	<i>DBGCLAIMCLR, Claim Tag Clear register</i> on page C11-2210
Claim Tag Set, Debug	<i>DBGCLAIMSET, Claim Tag Set register</i> on page C11-2211
CLIDR	<i>CLIDR, Cache Level ID Register, PMSA</i> on page B6-1808 <i>CLIDR, Cache Level ID Register, VMSA</i> on page B4-1526
CNTACRn	<i>CNTACRn, Counter Access Control Register</i> on page D5-2394
CNTCR	<i>CNTCR, Counter Control Register</i> on page D5-2396
CNTCV	<i>CNTCV, Counter Count Value register</i> on page D5-2397
CNTFRQ	<i>CNTFRQ, Counter Frequency register, PMSA</i> on page B6-1810 <i>CNTFRQ, Counter Frequency register, system level</i> on page D5-2398 <i>CNTFRQ, Counter Frequency register, VMSA</i> on page B4-1528
CNTHCTL	<i>CNTHCTL, Timer PL2 Control register, Virtualization Extensions</i> on page B4-1529
CNTHP_CTL	<i>CNTHP_CTL, PL2 Physical Timer Control register, Virtualization Extension</i> on page B4-1531
CNTHP_CVAL	<i>CNTHP_CVAL, PL2 Physical Timer CompareValue register, Virtualization Extensions</i> on page B4-1531
CNTKCTL	<i>CNTKCTL, Timer PLI Control register, PMSA</i> on page B6-1811 <i>CNTKCTL, Timer PLI Control register, VMSA</i> on page B4-1533
CNTNSAR	<i>CNTNSAR, Counter Non-Secure Access Register</i> on page D5-2399
CNTP_CTL	<i>CNTP_CTL, PLI Physical Timer Control register, PMSA</i> on page B6-1813 <i>CNTP_CTL, PLI Physical Timer Control register, system level</i> on page D5-2400 <i>CNTP_CTL, PLI Physical Timer Control register, VMSA</i> on page B4-1535
CNTP_CVAL	<i>CNTP_CVAL, PLI Physical Timer CompareValue register, PMSA</i> on page B6-1815 <i>CNTP_CVAL, PLI Physical Timer CompareValue register, system level</i> on page D5-2401 <i>CNTP_CVAL, PLI Physical Timer CompareValue register, VMSA</i> on page B4-1537

CNTKCTL	<i>CNTKCTL, Timer PLI Control register, PMSA</i> on page B6-1811 <i>CNTKCTL, Timer PLI Control register, VMSA</i> on page B4-1533
CNTNSAR	<i>CNTNSAR, Counter Non-Secure Access Register</i> on page D5-2399
CNTP_CTL	<i>CNTP_CTL, PLI Physical Timer Control register, PMSA</i> on page B6-1813 <i>CNTP_CTL, PLI Physical Timer Control register, system level</i> on page D5-2400 <i>CNTP_CTL, PLI Physical Timer Control register, VMSA</i> on page B4-1535
CNTP_CVAL	<i>CNTP_CVAL, PLI Physical Timer CompareValue register, PMSA</i> on page B6-1815 <i>CNTP_CVAL, PLI Physical Timer CompareValue register, system level</i> on page D5-2401 <i>CNTP_CVAL, PLI Physical Timer CompareValue register, VMSA</i> on page B4-1537
CNTP_TVAL	<i>CNTP_TVAL, PLI Physical TimerValue register, PMSA</i> on page B6-1816 <i>CNTP_TVAL, PLI Physical TimerValue register, system level</i> on page D5-2402 <i>CNTP_TVAL, PLI Physical TimerValue register, VMSA</i> on page B4-1538
CNTPCT	<i>CNTPCT, Physical Count register, PMSA</i> on page B6-1817 <i>CNTPCT, Physical Count register, system level</i> on page D5-2402 <i>CNTPCT, Physical Count register, VMSA</i> on page B4-1539
CNTPL0ACR	<i>CNTPL0ACR, Counter PL0 Access Control Register</i> on page D5-2403

Register	Description, see
CNTSR	<i>CNTSR, Counter Status Register</i> on page D5-2405
CNTTIDR	<i>CNTTIDR, Counter Timer ID Register</i> on page D5-2406
CNTV_CTL	<i>CNTV_CTL, Virtual Timer Control register, PMSA</i> on page B6-1818 <i>CNTV_CTL, Virtual Timer Control register, system level</i> on page D5-2407 <i>CNTV_CTL, Virtual Timer Control register, VMSA</i> on page B4-1540
CNTV_CVAL	<i>CNTV_CVAL, Virtual Timer CompareValue register, PMSA</i> on page B6-1818 <i>CNTV_CVAL, Virtual Timer CompareValue register, system level</i> on page D5-2407 <i>CNTV_CVAL, Virtual Timer CompareValue register, VMSA</i> on page B4-1540
CNTV_TVAL	<i>CNTV_TVAL, Virtual TimerValue register, PMSA</i> on page B6-1819 <i>CNTV_TVAL, Virtual TimerValue register, system level</i> on page D5-2408 <i>CNTV_TVAL, Virtual TimerValue register, VMSA</i> on page B4-1541
CNTVCT	<i>CNTVCT, Virtual Count register, PMSA</i> on page B6-1820 <i>CNTVCT, Virtual Count register, system level</i> on page D5-2408 <i>CNTVCT, Virtual Count register, VMSA</i> on page B4-1542
CNTVOFF	<i>CNTVOFFn, Virtual Offset register, system level</i> on page D5-2409 <i>CNTVOFF, Virtual Offset register, VMSA</i> on page B4-1543
Component ID, Debug	<i>About the Debug Component Identification Registers</i> on page C11-2196
Component ID, Performance Monitors	<i>PMCID0, Performance Monitors Component ID register 0</i> on page D2-2352 - <i>PMCID3, Performance Monitors Component ID register 3</i> on page D2-2353
Configuration, Hyp	<i>HCR, Hyp Configuration Register, Virtualization Extensions</i> on page B4-1577
Configuration, Hyp Auxiliary	<i>HACR, Hyp Auxiliary Configuration Register, Virtualization Extensions</i> on page B4-1571
Configuration, Hyp Debug	<i>HDCR, Hyp Debug Configuration Register, Virtualization Extensions</i> on page B4-1580
Configuration, Jazelle Main	<i>JMCR, Jazelle Main Configuration Register, VMSA</i> on page B4-1636 <i>JMCR, Jazelle Main Configuration Register, PMSA</i> on page B6-1880

Configuration, Performance Monitors	<i>PMCFGGR, Performance Monitors Configuration Register</i> on page D2-2351
Configuration, Secure	<i>SCR, Secure Configuration Register, Security Extensions</i> on page B4-1697
Configuration, ThumbEE	<i>TEECR, ThumbEE Configuration Register, VMSA</i> on page B4-1709 <i>TEECR, ThumbEE Configuration Register, PMSA</i> on page B6-1928
Context ID	<i>CONTEXTIDR, Context ID Register, PMSA</i> on page B6-1821 <i>CONTEXTIDR, Context ID Register, VMSA</i> on page B4-1544
Context ID Sampling, Debug	<i>DBGCIDSRR, Context ID Sampling Register</i> on page C11-2209
CONTEXTIDR	<i>CONTEXTIDR, Context ID Register, PMSA</i> on page B6-1821 <i>CONTEXTIDR, Context ID Register, VMSA</i> on page B4-1544
Control	<i>SCTRLR, System Control Register, PMSA</i> on page B6-1921 <i>SCTRLR, System Control Register, VMSA</i> on page B4-1700
Control, Counter	<i>CNTCR, Counter Control Register</i> on page D5-2396

Register	Description, see
Coprocessor Access Control	<i>CPACR, Coprocessor Access Control Register, PMSA</i> on page B6-1823 <i>CPACR, Coprocessor Access Control Register, VMSA</i> on page B4-1547
Count Enable Clear	<i>PMCNTEENCLR, Performance Monitors Count Enable Clear register, PMSA</i> on page B6-1897 <i>PMCNTEENCLR, Performance Monitors Count Enable Clear register, VMSA</i> on page B4-1667
Count Enable Set	<i>PMCNTEENSET, Performance Monitors Count Enable Set register, PMSA</i> on page B6-1899 <i>PMCNTEENSET, Performance Monitors Count Enable Set register, VMSA</i> on page B4-1669
Count Value, Counter	<i>CNTCV, Counter Count Value register</i> on page D5-2397
Counter Access Control	<i>CNTACRn, Counter Access Control Register</i> on page D5-2394
Counter Control	<i>CNTCR, Counter Control Register</i> on page D5-2396
Counter Count Value	<i>CNTCV, Counter Count Value register</i> on page D5-2397
Counter Frequency	<i>CNTFRQ, Counter Frequency register, PMSA</i> on page B6-1810 <i>CNTFRQ, Counter Frequency register, system level</i> on page D5-2398 <i>CNTFRQ, Counter Frequency register, VMSA</i> on page B4-1528
Counter ID0-Counter ID11	<i>CounterIDn, Counter ID registers 0-II</i> on page D5-2410
Counter Non-Secure Access	<i>CNTNSAR, Counter Non-Secure Access Register</i> on page D5-2399
Counter PL0 Access Control	<i>CNTPL0ACR, Counter PL0 Access Control Register</i> on page D5-2403
Counter Status	<i>CNTSR, Counter Status Register</i> on page D5-2405
Counter Timer ID	<i>CNTTIDR, Counter Timer ID Register</i> on page D5-2406
CP15 Data Memory Barrier operation	<i>CP15DMB, CP15 Data Memory Barrier operation, PMSA</i> on page B6-1822 <i>CP15DMB, CP15 Data Memory Barrier operation, VMSA</i> on page B4-1546

CP15 Data Synchronization Barrier operation	<i>CP15DSB, CP15 Data Synchronization Barrier operation, PMSA</i> on page B6-1822 <i>CP15DSB, CP15 Data Synchronization Barrier operation, VMSA</i> on page B4-1546
CP15 Instruction Synchronization Barrier operation	<i>CP15ISB, CP15 Instruction Synchronization Barrier operation, PMSA</i> on page B6-1822 <i>CP15ISB, CP15 Instruction Synchronization Barrier operation, VMSA</i> on page B4-1546
CP15DMB	<i>CP15DMB, CP15 Data Memory Barrier operation, PMSA</i> on page B6-1822 <i>CP15DMB, CP15 Data Memory Barrier operation, VMSA</i> on page B4-1546
CP15DSB	<i>CP15DSB, CP15 Data Synchronization Barrier operation, PMSA</i> on page B6-1822 <i>CP15DSB, CP15 Data Synchronization Barrier operation, VMSA</i> on page B4-1546
CP15ISB	<i>CP15ISB, CP15 Instruction Synchronization Barrier operation, PMSA</i> on page B6-1822 <i>CP15ISB, CP15 Instruction Synchronization Barrier operation, VMSA</i> on page B4-1546
CPACR	<i>CPACR, Coprocessor Access Control Register, PMSA</i> on page B6-1823 <i>CPACR, Coprocessor Access Control Register, VMSA</i> on page B4-1547
CPSR	<i>The Current Program Status Register (CPSR)</i> on page B1-1147
CSSELR	<i>CSSELR, Cache Size Selection Register, PMSA</i> on page B6-1826 <i>CSSELR, Cache Size Selection Register, VMSA</i> on page B4-1551

Register	Description, see
CTR	<i>CTR, Cache Type Register, PMSA</i> on page B6-1827 <i>CTR, Cache Type Register, VMSA</i> on page B4-1552
Cycle Count	<i>PMCCNTR, Performance Monitors Cycle Count Register, PMSA</i> on page B6-1894 <i>PMCCNTR, Performance Monitors Cycle Count Register, VMSA</i> on page B4-1664
D0 - D31	<i>Advanced SIMD and Floating-point Extension registers</i> on page A2-56
DACR	<i>DACR, Domain Access Control Register, VMSA</i> on page B4-1554
DAPR, pre-ARMv6	<i>CP15 c5, Memory Region Access Permissions Registers, DAPR and IAPR, ARMv4 and ARMv5</i> on page D15-2610
Data Fault Address	<i>DFAR, Data Fault Address Register, PMSA</i> on page B6-1830 <i>DFAR, Data Fault Address Register, VMSA</i> on page B4-1556
Data Fault Status	<i>DFSR, Data Fault Status Register, PMSA</i> on page B6-1831 <i>DFSR, Data Fault Status Register, VMSA</i> on page B4-1557
Data Memory Barrier operation, CP15	<i>CP15DMB, CP15 Data Memory Barrier operation, PMSA</i> on page B6-1822 <i>CP15DMB, CP15 Data Memory Barrier operation, VMSA</i> on page B4-1546
Data Memory Region Access Permissions, pre-ARMv6	<i>CP15 c5, Memory Region Access Permissions Registers, DAPR and IAPR, ARMv4 and ARMv5</i> on page D15-2610
Data Memory Region Bufferability, pre-ARMv6	<i>CP15 c3, Memory Region Bufferability Register, DBR, ARMv4 and ARMv5</i> on page D15-2609
Data Memory Region Cacheability, pre-ARMv6	<i>CP15 c2, Memory Region Cacheability Registers, DCR and ICR, ARMv4 and ARMv5</i> on page D15-2609
Data Memory Region Extended Access Permissions, pre-ARMv6	<i>CP15 c5, Memory Region Extended Access Permissions Registers, DEAPR and IEAPR, ARMv4 and ARMv5</i> on page D15-2610

Data or unified Cache Lockdown, pre-ARMv7	<i>CP15 c9, cache lockdown support</i> on page D15-2615
Data or unified Memory Region, pre-ARMv6	<i>CP15 c6, Memory Region Registers, DMRR0-DMRR7 and IMRR0-IMRR7, ARMv4 and ARMv5</i> on page D15-2611
Data or unified TLB Lockdown, pre-ARMv7	<i>CP15 c10, TLB lockdown support, VMSA</i> on page D15-2622
Data Region Access Control	<i>DRACR, Data Region Access Control Register, PMSA</i> on page B6-1832
Data Region Base Address	<i>DRBAR, Data Region Base Address Register, PMSA</i> on page B6-1834
Data Region Size and Enable	<i>DRSR, Data Region Size and Enable Register, PMSA</i> on page B6-1835
Data Synchronization Barrier operation, CP15	<i>CP15DSB, CP15 Data Synchronization Barrier operation, PMSA</i> on page B6-1822 <i>CP15DSB, CP15 Data Synchronization Barrier operation, VMSA</i> on page B4-1546
Data TCM Non-Secure Access Control, ARMv6	<i>CP15 c9, TCM Non-Secure Access Control Registers, DTCM-NSACR and ITCM-NSACR</i> on page D12-2528
Data TCM Region, ARMv6	<i>CP15 c9, TCM Region Registers, DTCMRR and ITCMRR</i> on page D12-2525
Data Transfer, Debug	<i>DBGDTRRX, Host to Target Data Transfer register</i> on page C11-2247 <i>DBGDTRTX, Target to Host Data Transfer register</i> on page C11-2248

Register	Description, see
DBGAUTHSTATUS	<i>DBGAUTHSTATUS, Authentication Status register</i> on page C11-2197, Debug
DBGBCR0 - DBGBCR15	<i>DBGBCR, Breakpoint Control Registers</i> on page C11-2199, Debug
DBGBVR0 - DBGBVR15	<i>DBGBVR, Breakpoint Value Registers</i> on page C11-2204, Debug
DBGBXVR0 - DBGBXVR15	<i>DBGBXVR, Breakpoint Extended Value Registers</i> on page C11-2205, Debug
DBGCID0 - DBGCID3	<i>About the Debug Component Identification Registers</i> on page C11-2196, Debug
DBGCIDSР	<i>DBGCIDSР, Context ID Sampling Register</i> on page C11-2209, Debug
DBGCLAIMCLR	<i>DBGCLAIMCLR, Claim Tag Clear register</i> on page C11-2210, Debug
DBGCLAIMSET	<i>DBGCLAIMSET, Claim Tag Set register</i> on page C11-2211, Debug
DBGDEVID	<i>DBGDEVID, Debug Device ID register</i> on page C11-2212.
DBGDEVID1	<i>DBGDEVID1, Debug Device ID register I</i> on page C11-2215
DBGDEVID2	<i>Debug identification registers</i> on page C11-2184.
DBGDEVTYPE	<i>DBGDEVTYPE, Device Type Register</i> on page C11-2216, Debug
DBGDIR	<i>DBGDIR, Debug ID Register</i> on page C11-2217
DBGDRAR	<i>DBGDRAR, Debug ROM Address Register</i> on page C11-2220
DBGDRCR	<i>DBGDRCR, Debug Run Control Register</i> on page C11-2222
DBGDSAR	<i>DBGDSAR, Debug Self Address Offset Register</i> on page C11-2225
DBGDSCCR	<i>DBGDSCCR, Debug State Cache Control Register</i> on page C11-2227
DBGDSCR	<i>DBGDSCR, Debug Status and Control Register</i> on page C11-2229
DBGDSCRext	<i>Internal and external views of the DBGDSCR and the DCC registers</i> on page C8-2153, Debug
DBGDSCRint	
DBGDSMCR	<i>DBGDSMCR, Debug State MMU Control Register</i> on page C11-2245

DBGDTRRX	<i>DBGDTRRX, Host to Target Data Transfer register on page C11-2247</i> , Debug
DBGDTRRXext	<i>Internal and external views of the DBGDSCR and the DCC registers on page C8-2153</i> , Debug
DBGDTRRXint	
DBGDTRTX	<i>DBGDTRTX, Target to Host Data Transfer register on page C11-2248</i> , Debug
DBGDTRTXext	<i>Internal and external views of the DBGDSCR and the DCC registers on page C8-2153</i>
DBGDTRTXint	
DBGEACR	<i>DBGEACR, External Auxiliary Control Register on page C11-2249</i> , Debug
DBGECR	<i>DBGECR, Event Catch Register on page C11-2249</i> , Debug
DBGITCTRL	<i>DBGITCTRL, Integration Mode Control register on page C11-2250</i> , Debug
DBGITR	<i>DBGITR, Instruction Transfer Register on page C11-2251</i> , Debug
DBGLAR	<i>DBGLAR, Lock Access Register on page C11-2252</i> , Debug

Register	Description, see
DBGLSR	<i>DBGLSR, Lock Status Register</i> on page C11-2253, Debug
DBGOSDLR	<i>DBGOSDLR, OS Double Lock Register</i> on page C11-2254, Debug
DBGOSLAR	<i>DBGOSLAR, OS Lock Access Register</i> on page C11-2255, Debug
DBGOSLSR	<i>DBGOSLSR, OS Lock Status Register</i> on page C11-2256, Debug
DBGOSSRR	<i>DBGOSSRR, OS Save and Restore Register</i> on page C11-2258, Debug
DBGPCSR	<i>DBGPCSR, Program Counter Sampling Register</i> on page C11-2259, Debug
DBGPID0 - DBGPID4	<i>About the Debug Peripheral Identification Registers</i> on page C11-2194
DBGPRCR	<i>DBGPRCR, Device Powerdown and Reset Control Register</i> on page C11-2266, Debug
DBGPRSР	<i>DBGPRSР, Device Powerdown and Reset Status Register</i> on page C11-2270, Debug
DBGVCR	<i>DBGVCR, Vector Catch Register</i> on page C11-2274, Debug
DBGVIDSR	<i>DBGVIDSR, Virtualization ID Sampling Register</i> on page C11-2277, Debug
DBGWCR0 - DBGWCR15	<i>DBGWCR, Watchpoint Control Registers</i> on page C11-2279, Debug
DBGWFAR, CP14	<i>DBGWFAR, Watchpoint Fault Address Register</i> on page C11-2284, Debug
DBGWFAR, CP15, ARMv6	<i>CP15 c6, Watchpoint Fault Address Register, DBGWFAR</i> on page D12-2517, Debug
DBGWVR0 - DBGWVR15	<i>DBGWVR, Watchpoint Value Registers</i> on page C11-2285, Debug
DBR, pre-ARMv6	<i>CP15 c3, Memory Region Bufferability Register, DBR, ARMv4 and ARMv5</i> on page D15-2609

DCC	<i>Internal and external views of the DBGDSCR and the DCC registers on page C8-2153</i>
DCCIMVAC	<i>Cache and branch predictor maintenance operations, PMSA on page B6-1932</i>
DCCISW	<i>Cache and branch predictor maintenance operations, VMSA on page B4-1735</i>
DCCMVAC	
DCCMVAU	
DCCSW	
DCIMVAC	
DCISW	
DCLR, pre-ARMv7	<i>CP15 c9, cache lockdown support on page D15-2615</i>
DCLR2, pre-ARMv7	<i>CP15 c9, Format D Data or unified Cache Lockdown Register, DCLR2, ARMv4 and ARMv5 on page D15-2620</i>
DCR, pre-ARMv6	<i>CP15 c2, Memory Region Cacheability Registers, DCR and ICR, ARMv4 and ARMv5 on page D15-2609</i>
DEAPR, pre-ARMv6	<i>CP15 c5, Memory Region Extended Access Permissions Registers, DEAPR and IEAPR, ARMv4 and ARMv5 on page D15-2610</i>
Debug Component ID	<i>About the Debug Component Identification Registers on page C11-2196</i>
Debug Context ID Sampling	<i>DBGCIDSR, Context ID Sampling Register on page C11-2209</i>

Register	Description, see
Debug Device ID	<i>DBGDEVID, Debug Device ID register</i> on page C11-2212.
Debug Device ID 1	<i>DBGDEVID1, Debug Device ID register 1</i> on page C11-2215
Debug Device ID 2	<i>Debug identification registers</i> on page C11-2184
Debug Feature 0	<i>ID_DFR0, Debug Feature Register 0, PMSA</i> on page B6-1846 <i>ID_DFR0, Debug Feature Register 0, VMSA</i> on page B4-1601
Debug ID	<i>DBGDIDR, Debug ID Register</i> on page C11-2217
Debug Peripheral ID	<i>About the Debug Peripheral Identification Registers</i> on page C11-2194
Debug Program Counter Sampling	<i>DBGPCSR, Program Counter Sampling Register</i> on page C11-2259
Debug ROM Address	<i>DBGDRAR, Debug ROM Address Register</i> on page C11-2220
Debug Run Control	<i>DBGDRCR, Debug Run Control Register</i> on page C11-2222
Debug Self Address Offset	<i>DBGDSAR, Debug Self Address Offset Register</i> on page C11-2225
Debug State Cache Control	<i>DBGDSCCR, Debug State Cache Control Register</i> on page C11-2227
Debug State MMU Control	<i>DBGDSMCR, Debug State MMU Control Register</i> on page C11-2245
Debug Status and Control	<i>DBGDSCR, Debug Status and Control Register</i> on page C11-2229
Device ID 1, Debug	<i>DBGDEVID1, Debug Device ID register 1</i> on page C11-2215
Device ID 2, Debug	<i>Debug identification registers</i> on page C11-2184

Device ID 2, Debug	<i>Debug identification registers</i> on page C11-2184
Device ID, Debug	<i>DBGDEVID, Debug Device ID register</i> on page C11-2212
Device Powerdown and Reset Control, Debug	<i>DBGPRCR, Device Powerdown and Reset Control Register</i> on page C11-2266
Device Powerdown and Reset Status, Debug	<i>DBGPRS, Device Powerdown and Reset Status Register</i> on page C11-2270
Device Type, Debug	<i>DBGDEVTYPE, Device Type Register</i> on page C11-2216
Device Type, Performance Monitors	<i>PMDEVTYPE, Performance Monitors Device Type register</i> on page D2-2354
DFAR	<i>DFAR, Data Fault Address Register, PMSA</i> on page B6-1830 <i>DFAR, Data Fault Address Register, VMSA</i> on page B4-1556
DFSR	<i>DFSR, Data Fault Status Register, PMSA</i> on page B6-1831 <i>DFSR, Data Fault Status Register, VMSA</i> on page B4-1557
DMRR0-DMRR7, pre-ARMv6	<i>CP15 c6, Memory Region Registers, DMRR0-DMRR7 and IMRR0-IMRR7, ARMv4 and ARMv5</i> on page D15-2611
Domain Access Control	<i>DACR, Domain Access Control Register, VMSA</i> on page B4-1554
Double Lock, OS, Debug	<i>DBGOSDLR, OS Double Lock Register</i> on page C11-2254
DRACR	<i>DRACR, Data Region Access Control Register, PMSA</i> on page B6-1832
DRBAR	<i>DRBAR, Data Region Base Address Register, PMSA</i> on page B6-1834

Register	Description, see
DRSR	<i>DRSR, Data Region Size and Enable Register; PMSA on page B6-1835</i>
DTCM-NSACR, ARMv6	<i>CPI5 c9, TCM Non-Secure Access Control Registers, DTCM-NSACR and ITCM-NSACR on page D12-2528</i>
DTCMRR, ARMv6	<i>CPI5 c9, TCM Region Registers. DTCMRR and ITCMRR on page D12-2525</i>
DTLBIAALL	<i>TLB maintenance operations, not in Hyp mode on page B4-1738</i>
DTLBIASID	
DTLBIMVA	
DTLBLR, pre-ARMv7	<i>CPI5 c10, TLB lockdown support, VMSA on page D15-2622</i>
DWB, pre-ARMv7	<i>Data and instruction barrier operations, PMSA on page B6-1934</i> <i>Data and instruction barrier operations, VMSA on page B4-1744</i>
ENDIANSTATE	<i>Endianness mapping register, ENDIANSTATE on page A2-53</i>
Event	<i>The Event Register on page B1-1200</i>
Event Catch, Debug	<i>DBGECR, Event Catch Register on page C11-2249</i>
Event Count	<i>PMCCNTR, Performance Monitors Cycle Count Register, PMSA on page B6-1894</i> <i>PMCCNTR, Performance Monitors Cycle Count Register, VMSA on page B4-1664</i>
Event Counter Selection	<i>PMSELR, Performance Monitors Event Counter Selection Register, PMSA on page B6-1910</i> <i>PMSELR, Performance Monitors Event Counter Selection Register, VMSA on page B4-1682</i>
Event Type Select	<i>PXEVTYPE, Performance Monitors Event Type Select Register, PMSA on page B6-1915</i> <i>PXEVTYPE, Performance Monitors Event Type Select Register, VMSA on page B4-1689</i>

Extended Access Permissions, pre-ARMv6	<i>CP15 c5, Memory Region Extended Access Permissions Registers, DEAPR and IEAPR, ARMv4 and ARMv5</i> on page D15-2610
External Auxiliary Control, Debug	<i>DBGEACR, External Auxiliary Control Register</i> on page C11-2249
FAR	See <i>Fault Address</i>
Fault Address	<i>DFAR, Data Fault Address Register, PMSA</i> on page B6-1830 <i>DFAR, Data Fault Address Register, VMSA</i> on page B4-1556 <i>IFAR, Instruction Fault Address Register, PMSA</i> on page B6-1874 <i>IFAR, Instruction Fault Address Register, VMSA</i> on page B4-1630 <i>DBGWFAAR, Watchpoint Fault Address Register</i> on page C11-2284 <i>CP15 c6, Watchpoint Fault Address Register, DBGWFAAR</i> on page D12-2517, ARMv6
Fault Status	<i>DFSR, Data Fault Status Register, PMSA</i> on page B6-1831 <i>DFSR, Data Fault Status Register, VMSA</i> on page B4-1557 <i>IFSR, Instruction Fault Status Register, PMSA</i> on page B6-1875 <i>IFSR, Instruction Fault Status Register, VMSA</i> on page B4-1631
FCSE Process ID	<i>FCSEIDR, FCSE Process ID Register, VMSA</i> on page B4-1562
FCSEIDR	<i>FCSEIDR, FCSE Process ID Register, VMSA</i> on page B4-1562

Register	Description, see
Floating-point Exception	<i>FPEXC, Floating-Point Exception Control register, PMSA</i> on page B6-1837 <i>FPEXC, Floating-Point Exception Control register, VMSA</i> on page B4-1564
Floating-point Instruction	<i>The Floating-Point Instruction Registers, FPINST and FPINST2</i> on page D6-2431
Floating-point System ID	<i>FPSID, Floating-point System ID Register, PMSA</i> on page B6-1842 <i>FPSID, Floating-point System ID Register, VMSA</i> on page B4-1569
Format D Data Cache Lockdown, pre-ARMv7	<i>CP15 c9, Format D Data or unified Cache Lockdown Register, DCLR2, ARMv4 and ARMv5</i> on page D15-2620
FPEXC	<i>FPEXC, Floating-Point Exception Control register, PMSA</i> on page B6-1837 <i>FPEXC, Floating-Point Exception Control register, VMSA</i> on page B4-1564
FPINST, FPINST2	<i>The Floating-Point Instruction Registers, FPINST and FPINST2</i> on page D6-2431
FPSCR	<i>FPSCR, Floating-point Status and Control Register, PMSA</i> on page B6-1839 <i>FPSCR, Floating-point Status and Control Register, VMSA</i> on page B4-1566
FPSID	<i>FPSID, Floating-point System ID Register, PMSA</i> on page B6-1842 <i>FPSID, Floating-point System ID Register, VMSA</i> on page B4-1569
FSR	See <i>Fault Status</i>
HACR	<i>HACR, Hyp Auxiliary Configuration Register, Virtualization Extensions</i> on page B4-1571
HACTLR	<i>HACTLR, Hyp Auxiliary Control Register, Virtualization Extensions</i> on page B4-1571
HADFSR	<i>HADFSR and HAIFSR, Hyp Auxiliary Fault Syndrome Registers, Virtualization Extensions</i> on page B4-1572
HAIFSR	
HAMAIR0	<i>HAMAIR0 and HAMAIR1, Hyp Auxiliary Memory Attribute Indirection Registers 0 and 1</i> on page B4-1573
HAMAIR0	

HAXFSR	<i>HADFSR and HAIFSR, Hyp Auxiliary Fault Syndrome Registers, Virtualization Extensions on page B4-1572</i>
HC PTR	<i>HC PTR, Hyp Coprocessor Trap Register, Virtualization Extensions on page B4-1574</i>
HCR	<i>HCR, Hyp Configuration Register, Virtualization Extensions on page B4-1577</i>
HDCR	<i>HDCR, Hyp Debug Configuration Register, Virtualization Extensions on page B4-1580</i>
HDFAR	<i>HDFAR, Hyp Data Fault Address Register, Virtualization Extensions on page B4-1583</i>
HIFAR	<i>HIFAR, Hyp Instruction Fault Address Register, Virtualization Extensions on page B4-1584</i>
HMAIR0	<i>HMAIRn, Hyp Memory Attribute Indirection Registers 0 and 1, Virtualization Extensions on page B4-1585</i>
HMAIR1	
Host to Target Data Transfer, Debug	<i>DBGDTRRX, Host to Target Data Transfer register on page C11-2247</i>
HPFAR	<i>HPFAR, Hyp IPA Fault Address Register, Virtualization Extensions on page B4-1586</i>
HSCTRLR	<i>HSCTRLR, Hyp System Control Register, Virtualization Extensions on page B4-1587</i>
HSR	<i>HSR, Hyp Syndrome Register, Virtualization Extensions on page B4-1590</i>

Register	Description, see
HSTR	<i>HSTR, Hyp System Trap Register, Virtualization Extensions</i> on page B4-1591
HTCR	<i>HTCR, Hyp Translation Control Register, Virtualization Extensions</i> on page B4-1593
HTPIDR	<i>HTPIDR, Hyp Software Thread ID Register, Virtualization Extensions</i> on page B4-1595
HTTBR	<i>HTTBR, Hyp Translation Table Base Register, Virtualization Extensions</i> on page B4-1596
HVBAR	<i>HVBAR, Hyp Vector Base Address Register, Virtualization Extensions</i> on page B4-1598
Hyp Auxiliary Configuration	<i>HACR, Hyp Auxiliary Configuration Register, Virtualization Extensions</i> on page B4-1571
Hyp Auxiliary Control	<i>HACTLR, Hyp Auxiliary Control Register, Virtualization Extensions</i> on page B4-1571
Hyp Auxiliary Fault Syndrome	<i>HADFSR and HAIFSR, Hyp Auxiliary Fault Syndrome Registers, Virtualization Extensions</i> on page B4-1572
Hyp Auxiliary Memory Attribute Indirection 0 and 1	<i>HAMAIR0 and HAMAIR1, Hyp Auxiliary Memory Attribute Indirection Registers 0 and 1</i> on page B4-1573
Hyp Configuration	<i>HCR, Hyp Configuration Register, Virtualization Extensions</i> on page B4-1577
Hyp Coprocessor Trap	<i>HCPTR, Hyp Coprocessor Trap Register, Virtualization Extensions</i> on page B4-1574
Hyp Data Fault Address	<i>HDEAR, Hyp Data Fault Address Register, Virtualization Extensions</i> on page B4-1583
Hyp Debug Configuration	<i>HDCR, Hyp Debug Configuration Register, Virtualization Extensions</i> on page B4-1580
Hyp Instruction Fault Address	<i>HIFAR, Hyp Instruction Fault Address Register, Virtualization Extensions</i> on page B4-1584
Hyp IPA Fault Address	<i>HPEAR, Hyp IPA Fault Address Register, Virtualization Extensions</i> on page B4-1586
Hyp Memory Attribute Indirection 0 and 1	<i>HMAIRn, Hyp Memory Attribute Indirection Registers 0 and 1, Virtualization Extensions</i> on page B4-1585
Hyp Software Thread ID	<i>HTPIDR, Hyp Software Thread ID Register, Virtualization Extensions</i> on page B4-1595

Hyp Syndrome	<i>HSR, Hyp Syndrome Register, Virtualization Extensions</i> on page B4-1590
Hyp System Control	<i>HSCTRL, Hyp System Control Register, Virtualization Extensions</i> on page B4-1587
Hyp System Trap	<i>HSTR, Hyp System Trap Register, Virtualization Extensions</i> on page B4-1591
Hyp Translation Control	<i>HTCR, Hyp Translation Control Register, Virtualization Extensions</i> on page B4-1593
Hyp Translation Table Base	<i>HTTBR, Hyp Translation Table Base Register, Virtualization Extensions</i> on page B4-1596
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IAPR, pre-ARMv6	<i>CP15 c5, Memory Region Access Permissions Registers, DAPR and IAPR, ARMv4 and ARMv5</i> on page D15-2610
ICIALLU	<i>Cache and branch predictor maintenance operations, PMSA</i> on page B6-1932
ICIALLUIS	<i>Cache and branch predictor maintenance operations, VMSA</i> on page B4-1735
ICIMVAU	
ICLR, pre-ARMv7	<i>CP15 c9, cache lockdown support</i> on page D15-2615
ICR, pre-ARMv6	<i>CP15 c2, Memory Region Cacheability Registers, DCR and ICR, ARMv4 and ARMv5</i> on page D15-2609

Register	Description, see
ID_AFR0	<i>ID_AFR0, Auxiliary Feature Register 0, PMSA</i> on page B6-1845 <i>ID_AFR0, Auxiliary Feature Register 0, VMSA</i> on page B4-1600
ID_DFR0	<i>ID_DFR0, Debug Feature Register 0, PMSA</i> on page B6-1846 <i>ID_DFR0, Debug Feature Register 0, VMSA</i> on page B4-1601
ID_ISAR0	<i>ID_ISAR0, Instruction Set Attribute Register 0, PMSA</i> on page B6-1848 <i>ID_ISAR0, Instruction Set Attribute Register 0, VMSA</i> on page B4-1603
ID_ISAR1	<i>ID_ISAR1, Instruction Set Attribute Register 1, PMSA</i> on page B6-1850 <i>ID_ISAR1, Instruction Set Attribute Register 1, VMSA</i> on page B4-1605
ID_ISAR2	<i>ID_ISAR2, Instruction Set Attribute Register 2, PMSA</i> on page B6-1852 <i>ID_ISAR2, Instruction Set Attribute Register 2, VMSA</i> on page B4-1607
ID_ISAR3	<i>ID_ISAR3, Instruction Set Attribute Register 3, PMSA</i> on page B6-1854 <i>ID_ISAR3, Instruction Set Attribute Register 3, VMSA</i> on page B4-1609
ID_ISAR4	<i>ID_ISAR4, Instruction Set Attribute Register 4, PMSA</i> on page B6-1857 <i>ID_ISAR4, Instruction Set Attribute Register 4, VMSA</i> on page B4-1612
ID_ISAR5	<i>ID_ISAR5, Instruction Set Attribute Register 5, PMSA</i> on page B6-1859 <i>ID_ISAR5, Instruction Set Attribute Register 5, VMSA</i> on page B4-1614
ID_MMFR0	<i>ID_MMFR0, Memory Model Feature Register 0, PMSA</i> on page B6-1860 <i>ID_MMFR0, Memory Model Feature Register 0, VMSA</i> on page B4-1615
ID_MMFR1	<i>ID_MMFR1, Memory Model Feature Register 1, PMSA</i> on page B6-1862 <i>ID_MMFR1, Memory Model Feature Register 1, VMSA</i> on page B4-1617
ID_MMFR2	<i>ID_MMFR2, Memory Model Feature Register 2, PMSA</i> on page B6-1865 <i>ID_MMFR2, Memory Model Feature Register 2, VMSA</i> on page B4-1620

ID_MMFR3	<i>ID_MMFR3, Memory Model Feature Register 3, PMSA</i> on page B6-1868 <i>ID_MMFR3, Memory Model Feature Register 3, VMSA</i> on page B4-1623
ID_PFR0	<i>ID_PFR0, Processor Feature Register 0, PMSA</i> on page B6-1870 <i>ID_PFR0, Processor Feature Register 0, VMSA</i> on page B4-1626
ID_PFR1	<i>ID_PFR1, Processor Feature Register 1, PMSA</i> on page B6-1872 <i>ID_PFR1, Processor Feature Register 1, VMSA</i> on page B4-1628
ID, Counter	<i>CounterIDn, Counter ID registers 0-11</i> on page D5-2410
ID, Debug	<i>DBGDIDR, Debug ID Register</i> on page C11-2217
IEAPR, pre-ARMv6	<i>CP15 c5, Memory Region Extended Access Permissions Registers, DEAPR and IEAPR, ARMv4 and ARMv5</i> on page D15-2610
IFAR	<i>IFAR, Instruction Fault Address Register, PMSA</i> on page B6-1874 <i>IFAR, Instruction Fault Address Register, VMSA</i> on page B4-1630
IFSR	<i>IFSR, Instruction Fault Status Register, PMSA</i> on page B6-1875 <i>IFSR, Instruction Fault Status Register, VMSA</i> on page B4-1631
IMRR0-IMRR7, pre-ARMv6	<i>CP15 c6, Memory Region Registers, DMRR0-DMRR7 and IMRR0-IMRR7, ARMv4 and ARMv5</i> on page D15-2611

Register	Description, see
Instruction Cache Lockdown, pre-ARMv7	<i>CP15 c9, cache lockdown support</i> on page D15-2615
Instruction Fault Address	<i>IFAR, Instruction Fault Address Register, PMSA</i> on page B6-1874 <i>IFAR, Instruction Fault Address Register, VMSA</i> on page B4-1630
Instruction Fault Status	<i>IFSR, Instruction Fault Status Register, PMSA</i> on page B6-1875 <i>IFSR, Instruction Fault Status Register, VMSA</i> on page B4-1631
Instruction Memory Region Access Permissions, pre-ARMv6	<i>CP15 c5, Memory Region Access Permissions Registers, DAPR and IAPR, ARMv4 and ARMv5</i> on page D15-2610
Instruction Memory Region Cacheability, pre-ARMv6	<i>CP15 c2, Memory Region Cacheability Registers, DCR and ICR, ARMv4 and ARMv5</i> on page D15-2609
Instruction Memory Region Extended Access Permissions, pre-ARMv6	<i>CP15 c5, Memory Region Extended Access Permissions Registers, DEAPR and IEAPR, ARMv4 and ARMv5</i> on page D15-2610
Instruction Memory Region, pre-ARMv6	<i>CP15 c6, Memory Region Registers, DMRR0-DMRR7 and IMRR0-IMRR7, ARMv4 and ARMv5</i> on page D15-2611
Instruction Region Access Control	<i>IRACR, Instruction Region Access Control Register, PMSA</i> on page B6-1876
Instruction Region Base Address	<i>IRBAR, Instruction Region Base Address Register, PMSA</i> on page B6-1877
Instruction Region Size and Enable	<i>IRSR, Instruction Region Size and Enable Register, PMSA</i> on page B6-1878
Instruction Set Attribute	<i>About the Instruction Set Attribute registers</i> on page B7-1940
Instruction Set Attribute 0	<i>ID_ISAR0, Instruction Set Attribute Register 0, PMSA</i> on page B6-1848 <i>ID_ISAR0, Instruction Set Attribute Register 0, VMSA</i> on page B4-1603

Instruction Set Attribute 1	<i>ID_ISAR1, Instruction Set Attribute Register 1, PMSA</i> on page B6-1850 <i>ID_ISAR1, Instruction Set Attribute Register 1, VMSA</i> on page B4-1605
Instruction Set Attribute 2	<i>ID_ISAR2, Instruction Set Attribute Register 2, PMSA</i> on page B6-1852 <i>ID_ISAR2, Instruction Set Attribute Register 2, VMSA</i> on page B4-1607
Instruction Set Attribute 3	<i>ID_ISAR3, Instruction Set Attribute Register 3, PMSA</i> on page B6-1854 <i>ID_ISAR3, Instruction Set Attribute Register 3, VMSA</i> on page B4-1609
Instruction Set Attribute 4	<i>ID_ISAR4, Instruction Set Attribute Register 4, PMSA</i> on page B6-1857 <i>ID_ISAR4, Instruction Set Attribute Register 4, VMSA</i> on page B4-1612
Instruction Set Attribute 5	<i>ID_ISAR5, Instruction Set Attribute Register 5, PMSA</i> on page B6-1859 <i>ID_ISAR5, Instruction Set Attribute Register 5, VMSA</i> on page B4-1614
Instruction Synchronization Barrier operation, CP15	<i>CP15ISB, CP15 Instruction Synchronization Barrier operation, PMSA</i> on page B6-1822 <i>CP15ISB, CP15 Instruction Synchronization Barrier operation, VMSA</i> on page B4-1546
Instruction TCM Non-Secure Access Control, ARMv6	<i>CP15 c9, TCM Non-Secure Access Control Registers, DTCM-NSACR and ITCM-NSACR</i> on page D12-2528

Table D18-2 Full registers index (continued)

Register	Description, see
Instruction TCM Region, ARMv6	<i>CP15 c9, TCM Region Registers. DTCMRR and ITCMRR</i> on page D12-2525
Instruction TLB Invalidate All	<i>ITLBIAALL, Instruction TLB Invalidate All, VMSA only</i> on page B4-1634
Instruction TLB Invalidate by ASID	<i>ITLBIASSID, Instruction TLB Invalidate by ASID, VMSA only</i> on page B4-1634
Instruction TLB Invalidate by MVA	<i>ITLBIMVA, Instruction TLB Invalidate by MVA, VMSA only</i> on page B4-1634
Instruction TLB Lockdown Register, pre-ARMv7	<i>CP15 c10, TLB lockdown support, VMSA</i> on page D15-2622
Instruction Transfer Register, Debug	<i>DBGITR, Instruction Transfer Register</i> on page C11-2251
Integration Mode Control, Debug	<i>DBGITCTRL, Integration Mode Control register</i> on page C11-2250
Interrupt Enable Clear	<i>PMINTENCLR, Performance Monitors Interrupt Enable Clear register, PMSA</i> on page B6-1904 <i>PMINTENCLR, Performance Monitors Interrupt Enable Clear register, VMSA</i> on page B4-1674
Interrupt Enable Set	<i>PMINTENSET, Performance Monitors Interrupt Enable Set register, PMSA</i> on page B6-1906 <i>PMINTENSET, Performance Monitors Interrupt Enable Set register, VMSA</i> on page B4-1676
Interrupt Status	<i>ISR, Interrupt Status Register, Security Extensions</i> on page B4-1633
IRACR	<i>IRACR, Instruction Region Access Control Register, PMSA</i> on page B6-1876
IRBAR	<i>IRBAR, Instruction Region Base Address Register, PMSA</i> on page B6-1877
IRSR	<i>IRSR, Instruction Region Size and Enable Register, PMSA</i> on page B6-1878

ISETSTATE	<i>Instruction set state register, ISETSTATE</i> on page A2-50
ISR	<i>ISR, Interrupt Status Register, Security Extensions</i> on page B4-1633
ITCM-NSACR, ARMv6	<i>CP15 c9, TCM Non-Secure Access Control Registers, DTCM-NSACR and ITCM-NSACR</i> on page D12-2528
ITCMRR, ARMv6	<i>CP15 c9, TCM Region Registers, DTCMRR and ITCMRR</i> on page D12-2525
ITLBIAALL	<i>TLB maintenance operations, not in Hyp mode</i> on page B4-1738
ITLBIASID	
ITLBIMVA	
ITLBLR, pre-ARMv7	<i>CP15 c10, TLB lockdown support, VMSA</i> on page D15-2622
ITSTATE	<i>IT block state register, ITSTATE</i> on page A2-51
Jazelle ID	<i>JIDR, Jazelle ID Register, PMSA</i> on page B6-1879 <i>JIDR, Jazelle ID Register, VMSA</i> on page B4-1635
Jazelle Main Configuration	<i>JMCR, Jazelle Main Configuration Register, PMSA</i> on page B6-1880 <i>JMCR, Jazelle Main Configuration Register, VMSA</i> on page B4-1636
Jazelle OS Control	<i>JOSCR, Jazelle OS Control Register, PMSA</i> on page B6-1881 <i>JOSCR, Jazelle OS Control Register, VMSA</i> on page B4-1637

Register	Description, see
JIDR	<i>JIDR, Jazelle ID Register; PMSA on page B6-1879</i> <i>JIDR, Jazelle ID Register; VMSA on page B4-1635</i>
JMCR	<i>JMCR, Jazelle Main Configuration Register; PMSA on page B6-1880</i> <i>JMCR, Jazelle Main Configuration Register; VMSA on page B4-1636</i>
JOSCR	<i>JOSCR, Jazelle OS Control Register; PMSA on page B6-1881</i> <i>JOSCR, Jazelle OS Control Register; VMSA on page B4-1637</i>
Lock Access, Debug	<i>DBGALAR, Lock Access Register on page C11-2252</i>
Lock Access, OS	<i>DBGOSLAR, OS Lock Access Register on page C11-2255</i>
Lock Access, Performance Monitors	<i>PMLAR, Performance Monitors Lock Access Register on page D2-2355</i>
Lock Status, Debug	<i>DBGLSR, Lock Status Register on page C11-2253</i>
Lock Status, OS	<i>DBGOSLSR, OS Lock Status Register on page C11-2256</i>
Lock Status, Performance Monitors	<i>PMLSР, Performance Monitors Lock Status Register on page D2-2356</i>
LR	<i>ARM core registers on page A2-45</i> for application level description <i>ARM core registers on page B1-1143</i> for system level description

LR_abt	<i>ARM core registers on page B1-1143</i>
LR_fiq	
LR_irq	
LR_mon	
LR_svc	
LR_und	
LR_usr	
Main ID	<i>MIDR, Main ID Register, PMSA on page B6-1883</i> <i>MIDR, Main ID Register, VMSA on page B4-1642</i>
MAIR0	<i>MAIR0 and MAIR1, Memory Attribute Indirection Registers 0 and 1, VMSA on page B4-1639</i>
MAIR1	
Media and VFP Feature	<i>About the Media and VFP Feature registers on page B7-1944</i>
Memory Attribute Indirection 0	<i>MAIR0 and MAIR1, Memory Attribute Indirection Registers 0 and 1, VMSA on page B4-1639</i>
Memory Attribute Indirection 1	
Memory Model Feature 0	<i>ID_MMFR0, Memory Model Feature Register 0, PMSA on page B6-1860</i> <i>ID_MMFR0, Memory Model Feature Register 0, VMSA on page B4-1615</i>
Memory Model Feature 1	<i>ID_MMFR1, Memory Model Feature Register 1, PMSA on page B6-1862</i> <i>ID_MMFR1, Memory Model Feature Register 1, VMSA on page B4-1617</i>

Register	Description, see
Memory Model Feature 2	<i>ID_MMFR2, Memory Model Feature Register 2, PMSA</i> on page B6-1865 <i>ID_MMFR2, Memory Model Feature Register 2, VMSA</i> on page B4-1620
Memory Model Feature 3	<i>ID_MMFR3, Memory Model Feature Register 3, PMSA</i> on page B6-1868 <i>ID_MMFR3, Memory Model Feature Register 3, VMSA</i> on page B4-1623
Memory Region Access Permissions, pre-ARMv6	<i>CP15 c5, Memory Region Access Permissions Registers, DAPR and IAPR, ARMv4 and ARMv5</i> on page D15-2610
Memory Region Bufferability, pre-ARMv6	<i>CP15 c3, Memory Region Bufferability Register, DBR, ARMv4 and ARMv5</i> on page D15-2609
Memory Region Cacheability, pre-ARMv6	<i>CP15 c2, Memory Region Cacheability Registers, DCR and ICR, ARMv4 and ARMv5</i> on page D15-2609
Memory Region, pre-ARMv6	<i>CP15 c6, Memory Region Registers, DMRR0-DMRR7 and IMRR0-IMRR7, ARMv4 and ARMv5</i> on page D15-2611
Memory Remap	<i>VMSA CP15 c10 register summary, memory remapping and TLB control registers</i> on page B3-1473
MIDR	<i>MIDR, Main ID Register, PMSA</i> on page B6-1883 <i>MIDR, Main ID Register, VMSA</i> on page B4-1642
Monitor Vector Base Address	<i>MVBAR, Monitor Vector Base Address Register, Security Extensions</i> on page B4-1647
MPIDR	<i>MPIDR, Multiprocessor Affinity Register, PMSA</i> on page B6-1885 <i>MPIDR, Multiprocessor Affinity Register, VMSA</i> on page B4-1644
MPU Region Number	<i>RGNR, MPU Region Number Register, PMSA</i> on page B6-1919

MPU Type	MPUIR, MPU Type Register, PMSA on page B6-1888
MPUIR	
Multiprocessor affinity	MPIDR, Multiprocessor Affinity Register, PMSA on page B6-1885 MPIDR, Multiprocessor Affinity Register, VMSA on page B4-1644
MVBAR	MVBAR, Monitor Vector Base Address Register, Security Extensions on page B4-1647
MVFR0	MVFR0, Media and VFP Feature Register 0, PMSA on page B6-1889 MVFR0, Media and VFP Feature Register 0, VMSA on page B4-1648
MVFR1	MVFR1, Media and VFP Feature Register 1, PMSA on page B6-1892 MVFR1, Media and VFP Feature Register 1, VMSA on page B4-1651
NMRR	NMRR, Normal Memory Remap Register, VMSA on page B4-1653
Non-Secure Access Control	NSACR, Non-Secure Access Control Register, Security Extensions on page B4-1655
Non-Secure Access Control, ARMv6 differences	CP15 c1, VMSA Security Extensions support on page D12-2516
Non-Secure Access, Counter	CNTNSAR, Counter Non-Secure Access Register on page D5-2399
Normal Memory Remap	NMRR, Normal Memory Remap Register, VMSA on page B4-1653
NSACR	CP15 c9, TCM Non-Secure Access Control Registers, DTCM-NSACR and ITCM-NSACR on page D12-2528 NSACR, Non-Secure Access Control Register, Security Extensions on page B4-1655

Register	Description, see
OS Double Lock, Debug	<i>DBGOSDLR, OS Double Lock Register</i> on page C11-2254
OS Lock Access, Debug	<i>DBGOSLAR, OS Lock Access Register</i> on page C11-2255
OS Lock Status, Debug	<i>DBGOSLSR, OS Lock Status Register</i> on page C11-2256
OS Save and Restore, Debug	<i>DBGOSSRR, OS Save and Restore Register</i> on page C11-2258
Overflow Flag Status	<i>PMOVSR, Performance Monitors Overflow Flag Status Register, PMSA</i> on page B6-1908 <i>PMOVSR, Performance Monitors Overflow Flag Status Register, VMSA</i> on page B4-1678
PAR	<i>PAR, Physical Address Register, VMSA</i> on page B4-1658
PC	<i>ARM core registers</i> on page A2-45 for application level description <i>ARM core registers</i> on page B1-1143 for system level description
Performance Monitors Authentication Status	<i>PMAUTHSTATUS, Performance Monitors Authentication Status register</i> on page D2-2349
Performance Monitors Common Event Identification 0	<i>PMCEID0 and PMCEIDI, Performance Monitors Common Event ID registers, PMSA</i> on page B6-1895
Performance Monitors Common Event Identification 1	<i>PMCEID0 and PMCEIDI, Performance Monitors Common Event ID registers, VMSA</i> on page B4-1665
Performance Monitors Component ID 0-3	<i>PMCID0, Performance Monitors Component ID register 0</i> on page D2-2352 - <i>PMCID3, Performance Monitors Component ID register 3</i> on page D2-2353
Performance Monitors Configuration	<i>PMCFGR, Performance Monitors Configuration Register</i> on page D2-2351
Performance Monitors Control	<i>PMCR, Performance Monitors Control Register, PMSA</i> on page B6-1901 <i>PMCR, Performance Monitors Control Register, VMSA</i> on page B4-1671
Performance Monitors Count Enable Clear	<i>PMCNTENCLR, Performance Monitors Count Enable Clear register, PMSA</i> on page B6-1897 <i>PMCNTENCLR, Performance Monitors Count Enable Clear register, VMSA</i> on page B4-1667

Performance Monitors Count Enable Set	<i>PMCNTENSET, Performance Monitors Count Enable Set register; PMSA on page B6-1899</i> <i>PMCNTENSET, Performance Monitors Count Enable Set register; VMSA on page B4-1669</i>
Performance Monitors Cycle Count	<i>PMCCNTR, Performance Monitors Cycle Count Register; PMSA on page B6-1894</i> <i>PMCCNTR, Performance Monitors Cycle Count Register; VMSA on page B4-1664</i>
Performance Monitors Cycle Count Filter Control	see <i>PMXEVTYPEP, Performance Monitors Event Type Select Register; VMSA on page B4-1689</i> see <i>PMXEVTYPEP, Performance Monitors Event Type Select Register; PMSA on page B6-1915</i>
Performance Monitors Device Type	<i>PMDEVTYPE, Performance Monitors Device Type register on page D2-2354</i>
Performance Monitors Event Count	<i>PMXEVCNTR, Performance Monitors Event Count Register; PMSA on page B6-1914</i> <i>PMXEVCNTR, Performance Monitors Event Count Register; VMSA on page B4-1687</i>
Performance Monitors Event Counter Selection	<i>PMSELR, Performance Monitors Event Counter Selection Register; PMSA on page B6-1910</i> <i>PMSELR, Performance Monitors Event Counter Selection Register; VMSA on page B4-1682</i>
Performance Monitors Event Type Select	<i>PMXEVTYPEP, Performance Monitors Event Type Select Register; PMSA on page B6-1915</i> <i>PMXEVTYPEP, Performance Monitors Event Type Select Register; VMSA on page B4-1689</i>

Table D-1074 | PM Registers Index (continued)

Register	Description, see
Performance Monitors Interrupt Enable Clear	<i>PMINTENCLR</i> , <i>Performance Monitors Interrupt Enable Clear register</i> , PMSA on page B6-1904 <i>PMINTENCLR</i> , <i>Performance Monitors Interrupt Enable Clear register</i> , VMSA on page B4-1674
Performance Monitors Interrupt Enable Set	<i>PMINTENSET</i> , <i>Performance Monitors Interrupt Enable Set register</i> , PMSA on page B6-1906 <i>PMINTENSET</i> , <i>Performance Monitors Interrupt Enable Set register</i> , VMSA on page B4-1676
Performance Monitors Lock Access	<i>PMLAR</i> , <i>Performance Monitors Lock Access Register</i> on page D2-2355
Performance Monitors Lock Status	<i>PMLSR</i> , <i>Performance Monitors Lock Status Register</i> on page D2-2356
Performance Monitors Overflow Flag Status	<i>PMOVSR</i> , <i>Performance Monitors Overflow Flag Status Register</i> , PMSA on page B6-1908 <i>PMOVSR</i> , <i>Performance Monitors Overflow Flag Status Register</i> , VMSA on page B4-1678
Performance Monitors Overflow Flag Status Set	<i>PMOVSSET</i> , <i>Performance Monitors Overflow Flag Status Set register</i> , Virtualization Extensions on page B4-1680
Performance Monitors Peripheral ID 0-4	<i>PMPID0</i> , <i>Performance Monitors Peripheral ID register 0</i> on page D2-2357 - <i>PMPID4</i> , <i>Performance Monitors Peripheral ID register 4</i> on page D2-2361
Performance Monitors Software Increment	<i>PMSWINC</i> , <i>Performance Monitors Software Increment register</i> , PMSA on page B6-1912 <i>PMSWINC</i> , <i>Performance Monitors Software Increment register</i> , VMSA on page B4-1684
Performance Monitors User Enable	<i>PMUSERENR</i> , <i>Performance Monitors User Enable Register</i> , PMSA on page B6-1913 <i>PMUSERENR</i> , <i>Performance Monitors User Enable Register</i> , VMSA on page B4-1686
Peripheral ID, Debug	<i>About the Debug Peripheral Identification Registers</i> on page C11-2194
Peripheral ID, Performance Monitors	<i>PMPID0</i> , <i>Performance Monitors Peripheral ID register 0</i> on page D2-2357 - <i>PMPID4</i> , <i>Performance Monitors Peripheral ID register 4</i> on page D2-2361
PFF, pre-ARMv7	<i>Data and instruction barrier operations</i> , PMSA on page B6-1934 <i>Data and instruction barrier operations</i> , VMSA on page B4-1744

Physical Address	<i>PAR, Physical Address Register, VMSA</i> on page B4-1658
Physical Count	<i>CNTPCT, Physical Count register, PMSA</i> on page B6-1817 <i>CNTPCT, Physical Count register, system level</i> on page D5-2402 <i>CNTPCT, Physical Count register, VMSA</i> on page B4-1539
Physical Timer CompareValue, PL1	<i>CNTP_CVAL, PLI Physical Timer CompareValue register, PMSA</i> on page B6-1815 <i>CNTP_CVAL, PLI Physical Timer CompareValue register, system level</i> on page D5-2401 <i>CNTP_CVAL, PLI Physical Timer CompareValue register, VMSA</i> on page B4-1537
Physical Timer CompareValue, PL2	<i>CNTHP_CVAL, PL2 Physical Timer CompareValue register, Virtualization Extensions</i> on page B4-1531
Physical Timer Control, PL1	<i>CNTP_CTL, PLI Physical Timer Control register, PMSA</i> on page B6-1813 <i>CNTP_CTL, PLI Physical Timer Control register, system level</i> on page D5-2400 <i>CNTP_CTL, PLI Physical Timer Control register, VMSA</i> on page B4-1535
Physical Timer Control, PL2	<i>CNTHP_CTL, PL2 Physical Timer Control register, Virtualization Extension</i> on page B4-1531
Physical TimerValue, PL1	<i>CNTP_TVAL, PLI Physical TimerValue register, PMSA</i> on page B6-1816 <i>CNTP_TVAL, PLI Physical TimerValue register, system level</i> on page D5-2402 <i>CNTP_TVAL, PLI Physical TimerValue register, VMSA</i> on page B4-1538

Table D-15-2 | All registers index (continued)

Register	Description, see
PL1 Physical Timer CompareValue	<i>CNTP_CVAL, PLI Physical Timer CompareValue register, PMSA</i> on page B6-1815 <i>CNTP_CVAL, PLI Physical Timer CompareValue register, system level</i> on page D5-2401 <i>CNTP_CVAL, PLI Physical Timer CompareValue register, VMSA</i> on page B4-1537
PL1 Physical Timer Control	<i>CNTP_CTL, PLI Physical Timer Control register, PMSA</i> on page B6-1813 <i>CNTP_CTL, PLI Physical Timer Control register, system level</i> on page D5-2400 <i>CNTP_CTL, PLI Physical Timer Control register, VMSA</i> on page B4-1535
PL1 Physical TimerValue	<i>CNTP_TVAL, PLI Physical TimerValue register, PMSA</i> on page B6-1816 <i>CNTP_TVAL, PLI Physical TimerValue register, system level</i> on page D5-2402 <i>CNTP_TVAL, PLI Physical TimerValue register, VMSA</i> on page B4-1538
PL1 Timer Control	<i>CNTKCTL, Timer PLI Control register, PMSA</i> on page B6-1811 <i>CNTKCTL, Timer PLI Control register, VMSA</i> on page B4-1533
PL2 Physical Timer CompareValue	<i>CNTHP_CVAL, PL2 Physical Timer CompareValue register, Virtualization Extensions</i> on page B4-1531
PL2 Physical Timer Control	<i>CNTHP_CTL, PL2 Physical Timer Control register, Virtualization Extension</i> on page B4-1531
PMAUTHSTATUS	<i>PMAUTHSTATUS, Performance Monitors Authentication Status register</i> on page D2-2349
PMCCFILTR	An obsolete name for PMXEVTYPER31. See either: <ul style="list-style-type: none">• <i>PMXEVTYPER, Performance Monitors Event Type Select Register, VMSA</i> on page B4-1689• <i>PMXEVTYPER, Performance Monitors Event Type Select Register, PMSA</i> on page B6-1915
PMCCNTR	<i>PMCCNTR, Performance Monitors Cycle Count Register, PMSA</i> on page B6-1894 <i>PMCCNTR, Performance Monitors Cycle Count Register, VMSA</i> on page B4-1664
PMCEID0	<i>PMCEID0 and PMCEID1, Performance Monitors Common Event ID registers, PMSA</i> on page B6-1895
PMCEID1	<i>PMCEID0 and PMCEID1, Performance Monitors Common Event ID registers, VMSA</i> on page B4-1665
PMCFGGR	<i>PMCFGGR, Performance Monitors Configuration Register</i> on page D2-2351
PMCID0-3	<i>PMCID0, Performance Monitors Component ID register 0</i> on page D2-2352 - <i>PMCID3, Performance Monitors Component ID register 3</i> on page D2-2353
PMCNTENCLR	<i>PMCNTENCLR, Performance Monitors Count Enable Clear register, PMSA</i> on page B6-1897 <i>PMCNTENCLR, Performance Monitors Count Enable Clear register, VMSA</i> on page B4-1667
PMCNTENSET	<i>PMCNTENSET, Performance Monitors Count Enable Set register, PMSA</i> on page B6-1899 <i>PMCNTENSET, Performance Monitors Count Enable Set register, VMSA</i> on page B4-1669
PMCR	<i>PMCR, Performance Monitors Control Register, PMSA</i> on page B6-1901 <i>PMCR, Performance Monitors Control Register, VMSA</i> on page B4-1671
PMDEVTYPE	<i>PMDEVTYPE, Performance Monitors Device Type register</i> on page D2-2354
PMINTENCLR	<i>PMINTENCLR, Performance Monitors Interrupt Enable Clear register, PMSA</i> on page B6-1904 <i>PMINTENCLR, Performance Monitors Interrupt Enable Clear register, VMSA</i> on page B4-1674
PMINTENSET	<i>PMINTENSET, Performance Monitors Interrupt Enable Set register, PMSA</i> on page B6-1906 <i>PMINTENSET, Performance Monitors Interrupt Enable Set register, VMSA</i> on page B4-1676
PMLAR	<i>PMLAR, Performance Monitors Lock Access Register</i> on page D2-2355

Table D18-2 Full registers index (continued)

Register	Description, see
PMLSR	<i>PMLSR, Performance Monitors Lock Status Register</i> on page D2-2356
PMOVSR	<i>PMOVSR, Performance Monitors Overflow Flag Status Register, PMSA</i> on page B6-1908 <i>PMOVSR, Performance Monitors Overflow Flag Status Register, VMSA</i> on page B4-1678
PMOVSSET	<i>PMOVSSET, Performance Monitors Overflow Flag Status Set register; Virtualization Extensions</i> on page B4-1680
PMPID0-4	<i>PMPID0, Performance Monitors Peripheral ID register 0</i> on page D2-2357 - <i>PMPID4, Performance Monitors Peripheral ID register 4</i> on page D2-2361
PMSELR	<i>PMSELR, Performance Monitors Event Counter Selection Register, PMSA</i> on page B6-1910 <i>PMSELR, Performance Monitors Event Counter Selection Register, VMSA</i> on page B4-1682
PMSWINC	<i>PMSWINC, Performance Monitors Software Increment register, PMSA</i> on page B6-1912 <i>PMSWINC, Performance Monitors Software Increment register, VMSA</i> on page B4-1684
PMUSERENR	<i>PMUSERENR, Performance Monitors User Enable Register, PMSA</i> on page B6-1913 <i>PMUSERENR, Performance Monitors User Enable Register, VMSA</i> on page B4-1686
PMXEVCNTR	<i>PMXEVCNTR, Performance Monitors Event Count Register, PMSA</i> on page B6-1914 <i>PMXEVCNTR, Performance Monitors Event Count Register, VMSA</i> on page B4-1687
PMXEVTYPER	<i>PMXEVTYPER, Performance Monitors Event Type Select Register, PMSA</i> on page B6-1915 <i>PMXEVTYPER, Performance Monitors Event Type Select Register, VMSA</i> on page B4-1689
Powerdown and Reset Control	<i>DBGPRCR, Device Powerdown and Reset Control Register</i> on page C11-2266
Powerdown and Reset Status	<i>DBGPRSR, Device Powerdown and Reset Status Register</i> on page C11-2270
Prefetch Status, ARMv6	<i>CP15 c7, Block Transfer Status Register</i> on page D12-2522
Primary Region Remap	<i>PRRR, Primary Region Remap Register, VMSA</i> on page B4-1693
Processor Feature 0	<i>ID_PFR0, Processor Feature Register 0, PMSA</i> on page B6-1870 <i>ID_PFR0, Processor Feature Register 0, VMSA</i> on page B4-1626
Processor Feature 1	<i>ID_PFR1, Processor Feature Register 1, PMSA</i> on page B6-1872 <i>ID_PFR1, Processor Feature Register 1, VMSA</i> on page B4-1628
Program Counter Sampling, Debug	<i>DBGPCSR, Program Counter Sampling Register</i> on page C11-2259
PRRR	<i>PRRR, Primary Region Remap Register, VMSA</i> on page B4-1693
PSR	<i>Program Status Registers (PSRs)</i> on page B1-1147
Q0 - Q15	<i>Advanced SIMD and Floating-point Extension registers</i> on page A2-56
R0 - R15	<i>ARM core registers</i> on page A2-45 for application level description <i>ARM core registers</i> on page B1-1143 for system level description
R0_usr - R12_usr	<i>ARM core registers</i> on page B1-1143
R8_fiq - R12_fiq	
REVIDR	<i>REVIDR, Revision ID Register, PMSA</i> on page B6-1918 <i>REVIDR, Revision ID Register, VMSA</i> on page B4-1696
Revision ID	

Table D18-2 Full registers index (continued)

Register	Description, see
RGNR	<i>RGNR, MPU Region Number Register, PMSA</i> on page B6-1919
Run Control, Debug	<i>DBGDRCR, Debug Run Control Register</i> on page C11-2222
S0 - S31	<i>Advanced SIMD and Floating-point Extension registers</i> on page A2-56
SCR	<i>SCR, Secure Configuration Register, Security Extensions</i> on page B4-1697
SCTRLR	<i>SCTRLR, System Control Register, PMSA</i> on page B6-1921 <i>SCTRLR, System Control Register, VMSA</i> on page B4-1700
SDER	<i>SDER, Secure Debug Enable Register, Security Extensions</i> on page B4-1707
Secure Configuration	<i>SCR, Secure Configuration Register, Security Extensions</i> on page B4-1697
Secure Debug Enable	<i>SDER, Secure Debug Enable Register, Security Extensions</i> on page B4-1707
Software Increment	<i>PMSWINC, Performance Monitors Software Increment register, VMSA</i> on page B4-1684
Software Thread ID	<i>Miscellaneous operations, functional group</i> on page B5-1796, for PMSA description <i>Miscellaneous operations, functional group</i> on page B3-1494, for VMSA description
SP	<i>ARM core registers</i> on page A2-45 for application level description <i>ARM core registers</i> on page B1-1143 for system level description
SP_abt	<i>ARM core registers</i> on page B1-1143
SP_fiq	
SP_irq	
SP_mon	
SP_svc	
SP_und	
SP_usr	
SPSR	<i>The Saved Program Status Registers (SPSRs)</i> on page B1-1148
SPSR_abt	<i>ARM core registers</i> on page B1-1143
SPSR_fiq	
SPSR_irq	
SPSR_mon	
SPSR_svc	
SPSR_und	
Status and Control, Debug	<i>DBGDSCR, Debug Status and Control Register</i> on page C11-2229
Status, Counter	<i>CNTSR, Counter Status Register</i> on page D5-2405
System Control	<i>PMSA CP15 c1 register summary, system control registers</i> on page B5-1781 <i>VMSA CP15 c1 register summary, system control registers</i> on page B3-1468
System Control	<i>SCTRLR, System Control Register, PMSA</i> on page B6-1921 <i>SCTRLR, System Control Register, VMSA</i> on page B4-1700

Table D18-2 Full registers index (continued)

Register	Description, see
Target to Host Data Transfer, Debug	<i>DBGDTRTX</i> , Target to Host Data Transfer register on page C11-2248
TCM Data Region, ARMv6	<i>CP15 c9</i> , TCM Region Registers, <i>DTCMRR</i> and <i>ITCMRR</i> on page D12-2525
TCM Instruction or unified Region, ARMv6	<i>CP15 c9</i> , TCM Region Registers, <i>DTCMRR</i> and <i>ITCMRR</i> on page D12-2525
TCM Non-Secure Access Control, ARMv6	<i>CP15 c9</i> , TCM Non-Secure Access Control Registers, <i>DTCM-NSACR</i> and <i>ITCM-NSACR</i> on page D12-2528
TCM Selection, ARMv6	<i>CP15 c9</i> , TCM Selection Register, <i>TCMSR</i> on page D12-2524
TCM Type	<i>TCMTR</i> , TCM Type Register, <i>PMSA</i> on page B6-1927 <i>TCMTR</i> , TCM Type Register, <i>VMSA</i> on page B4-1708
TCMSR, ARMv6	<i>CP15 c9</i> , TCM Selection Register, <i>TCMSR</i> on page D12-2524
TCMTR	<i>TCMTR</i> , TCM Type Register, <i>PMSA</i> on page B6-1927 <i>TCMTR</i> , TCM Type Register, <i>VMSA</i> on page B4-1708
TEECR	<i>TEECR</i> , ThumbEE Configuration Register, <i>PMSA</i> on page B6-1928 <i>TEECR</i> , ThumbEE Configuration Register, <i>VMSA</i> on page B4-1709
TEEHBR	<i>TEEHBR</i> , ThumbEE Handler Base Register, <i>PMSA</i> on page B6-1929 <i>TEEHBR</i> , ThumbEE Handler Base Register, <i>VMSA</i> on page B4-1710
TEX remap	<i>VMSA CP15 c10 register summary</i> , memory remapping and TLB control registers on page B3-1473
ThumbEE Configuration	<i>TEECR</i> , ThumbEE Configuration Register, <i>PMSA</i> on page B6-1928 <i>TEECR</i> , ThumbEE Configuration Register, <i>VMSA</i> on page B4-1709
ThumbEE Handler Base	<i>TEEHBR</i> , ThumbEE Handler Base Register, <i>PMSA</i> on page B6-1929 <i>TEEHBR</i> , ThumbEE Handler Base Register, <i>VMSA</i> on page B4-1710
Timer ID, Counter	<i>CNTTIDR</i> , Counter Timer ID Register on page D5-2406
Timer PL1 Control	<i>CNTKCTL</i> , Timer PL1 Control register, <i>PMSA</i> on page B6-1811 <i>CNTKCTL</i> , Timer PL1 Control register, <i>VMSA</i> on page B4-1533
Timer PL2 Control	<i>CNTHCTL</i> , Timer PL2 Control register, Virtualization Extensions on page B4-1529
TLB Lockdown Register, pre-ARMv7	<i>CP15 c10</i> , TLB lockdown support, <i>VMSA</i> on page D15-2622
TLB Type	<i>TLBTR</i> , TLB Type Register, <i>VMSA</i> on page B4-1713

Table D18-2 Full registers index (continued)

Register	Description, see
TLBIALL	<i>TLB maintenance operations, not in Hyp mode</i> on page B4-1738
TLBIALLIS	
TLBIASID	
TLBIASIDIS	
TLBIMVA	
TLBIMVAA	
TLBIMVAAIS	
TLBIMVAIS	
TLBTR	<i>TLBTR, TLB Type Register, VMSA</i> on page B4-1713
TPIDRPRW	<i>TPIDRPRW, PLI only Thread ID Register, PMSA</i> on page B6-1930 <i>TPIDRPRW, PLI only Thread ID Register, VMSA</i> on page B4-1714
TPIDRURO	<i>TPIDRURO, User Read-Only Thread ID Register, PMSA</i> on page B6-1930 <i>TPIDRURO, User Read-Only Thread ID Register, VMSA</i> on page B4-1714
TPIDURRW	<i>TPIDURRW, User Read/Write Thread ID Register, PMSA</i> on page B6-1931 <i>TPIDURRW, User Read/Write Thread ID Register, VMSA</i> on page B4-1715
Translation Table Base	<i>VMSA CP15 c2 and c3 register summary, Memory protection and control registers</i> on page B3-1469
Translation Table Base 0	<i>TTBR0, Translation Table Base Register 0, VMSA</i> on page B4-1721
Translation Table Base 1	<i>TTBR1, Translation Table Base Register 1, VMSA</i> on page B4-1725
Translation Table Base Control	<i>TTBCR, Translation Table Base Control Register, VMSA</i> on page B4-1716
TTBCR	<i>TTBCR, Translation Table Base Control Register, VMSA</i> on page B4-1716
TTBR0	<i>TTBR0, Translation Table Base Register 0, VMSA</i> on page B4-1721
TTBR1	<i>TTBR1, Translation Table Base Register 1, VMSA</i> on page B4-1725
User Enable	<i>PMUSERENR, Performance Monitors User Enable Register, PMSA</i> on page B6-1913 <i>PMUSERENR, Performance Monitors User Enable Register, VMSA</i> on page B4-1686
UTLBIALL	Previous names for the CP15 c8 operations TLBIALL, TLBIASID, and TLBIMVA, see <i>TLB maintenance operations, not in Hyp mode</i> on page B4-1738
UTLBIASID	
UTLBIMVA	
V2PCWPR	See entry for ATS1CPR and <i>Naming of the address translation operations, and operation summary</i> on page B3-1434
V2PCWPW	See entry for ATS1CPW and <i>Naming of the address translation operations, and operation summary</i> on page B3-1434
V2PCWUR	See entry for ATS1CUR and <i>Naming of the address translation operations, and operation summary</i> on page B3-1434
V2PCWUW	See entry for ATS1CUW and <i>Naming of the address translation operations, and operation summary</i> on page B3-1434

Table D18-2 Full registers index (continued)

Register	Description, see
V2POWPR	See entry for ATS12NSOPR and <i>Naming of the address translation operations, and operation summary</i> on page B3-1434
V2POWPW	See entry for ATS12NSOPW and <i>Naming of the address translation operations, and operation summary</i> on page B3-1434
V2POWUR	See entry for ATS12NSOUR and <i>Naming of the address translation operations, and operation summary</i> on page B3-1434
V2POWUW	See entry for ATS12NSOUW and <i>Naming of the address translation operations, and operation summary</i> on page B3-1434
VBAR	<i>VBAR, Vector Base Address Register, Security Extensions</i> on page B4-1727
Vector Base Address	<i>VBAR, Vector Base Address Register, Security Extensions</i> on page B4-1727
Vector Catch, Debug	<i>DBGVCR, Vector Catch Register</i> on page C11-2274
Virtual Count	<i>CNTVCT, Virtual Count register, PMSA</i> on page B6-1820 <i>CNTVCT, Virtual Count register, system level</i> on page D5-2408 <i>CNTVCT, Virtual Count register, VMSA</i> on page B4-1542
Virtual Offset	<i>CNTVOFFn, Virtual Offset register, system level</i> on page D5-2409 <i>CNTVOFF, Virtual Offset register, VMSA</i> on page B4-1543
Virtual Timer CompareValue	<i>CNTV_CVAL, Virtual Timer CompareValue register, PMSA</i> on page B6-1818 <i>CNTV_CVAL, Virtual Timer CompareValue register, system level</i> on page D5-2407 <i>CNTV_CVAL, Virtual Timer CompareValue register, VMSA</i> on page B4-1540
Virtual Timer Control	<i>CNTV_CTL, Virtual Timer Control register, PMSA</i> on page B6-1818 <i>CNTV_CTL, Virtual Timer Control register, system level</i> on page D5-2407 <i>CNTV_CTL, Virtual Timer Control register, VMSA</i> on page B4-1540
Virtual TimerValue	<i>CNTV_TVAL, Virtual TimerValue register, PMSA</i> on page B6-1819 <i>CNTV_TVAL, Virtual TimerValue register, system level</i> on page D5-2408 <i>CNTV_TVAL, Virtual TimerValue register, VMSA</i> on page B4-1541
Virtualization ID Sampling, Debug	<i>DBGVIDSR, Virtualization ID Sampling Register</i> on page C11-2277
Virtualization Multiprocessor ID	<i>VMPIDR, Virtualization Multiprocessor ID Register, Virtualization Extensions</i> on page B4-1728
Virtualization Processor ID	<i>VPIDR, Virtualization Processor ID Register, Virtualization Extensions</i> on page B4-1729
Virtualization Translation Control	<i>VTCSR, Virtualization Translation Control Register, Virtualization Extensions</i> on page B4-1730
Virtualization Translation Table Base	<i>VTTBR, Virtualization Translation Table Base Register, Virtualization Extensions</i> on page B4-1733
VMPIDR	<i>VMPIDR, Virtualization Multiprocessor ID Register, Virtualization Extensions</i> on page B4-1728
VPIDR	<i>VPIDR, Virtualization Processor ID Register, Virtualization Extensions</i> on page B4-1729
VTCSR	<i>VTCSR, Virtualization Translation Control Register, Virtualization Extensions</i> on page B4-1730
VTTBR	<i>VTTBR, Virtualization Translation Table Base Register, Virtualization Extensions</i> on page B4-1733

Table D18-2 Full registers index (continued)

Register	Description, see
Watchpoint Control, Debug	<i>DBGWCR, Watchpoint Control Registers</i> on page C11-2279
Watchpoint Fault Address, CP14, Debug	<i>DBGWEAR, Watchpoint Fault Address Register</i> on page C11-2284
Watchpoint Fault Address, CP15, ARMv6	<i>CP15 c6, Watchpoint Fault Address Register, DBGWEAR</i> on page D12-2517
Watchpoint Value, Debug	<i>DBGWVR, Watchpoint Value Registers</i> on page C11-2285