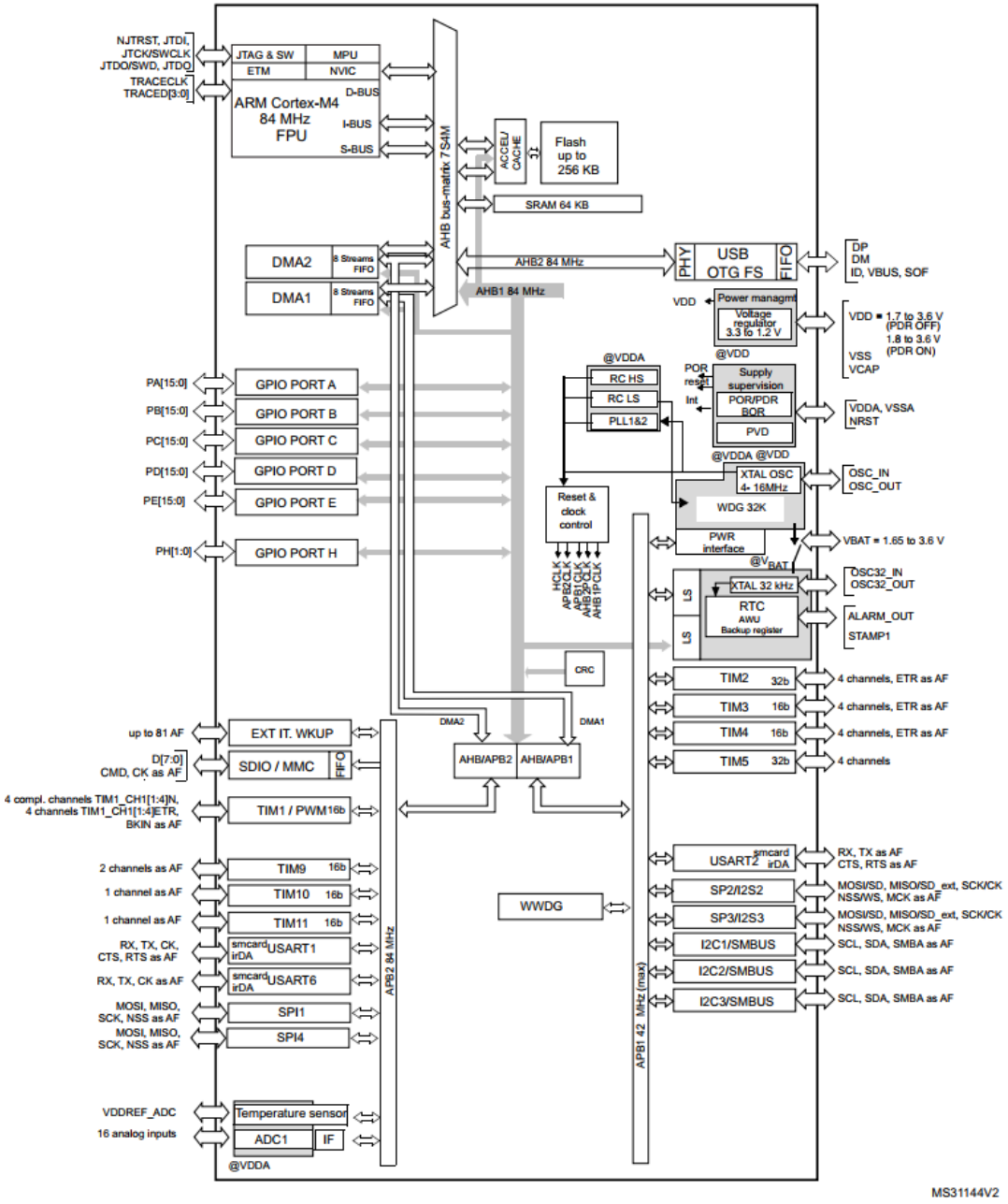
Module 10.1

AGENDA

1. USART Experiment 3
2. ADC- Multichannel
3. Independent Watchdog timer
4. Timer interrupt

Datasheet – PG14

STM32F401 Architecture



Datasheet – PG14

Independent Watch Dog

Sequence:

1. Set KR to 0x5555;
2. Set PR
3. SET RLR
4. Wati for SR to be 0
5. Set KR to 0xCCCC

Set KR to 0xAAAA for refresh within the timeout

Calculation of RLR

IWDG settings and reset flag

- Setting IWDG time-base:
  - IWDG time-base prescaled from LSI1 or LSI2 clocks (32 kHz)
    - 7 pre-dividers: 4 to 256 selectable by IWDG_PR register (and 12-bit watchdog counter reload value, RLR[11:0])
  - Set the IWDG timeout by using the following formula:

$$t_{IWDG} = t_{LSI} \times 4 \times 2^{PR} \times (RL + 1)$$

where t_{LSI} = 1/32000 = 31.25 µs, PR and RL are fields of IWDG registers

- The cause of the IWDG reset can be identified via RCC registers

Datasheet – PG14

Timer - Interrupt

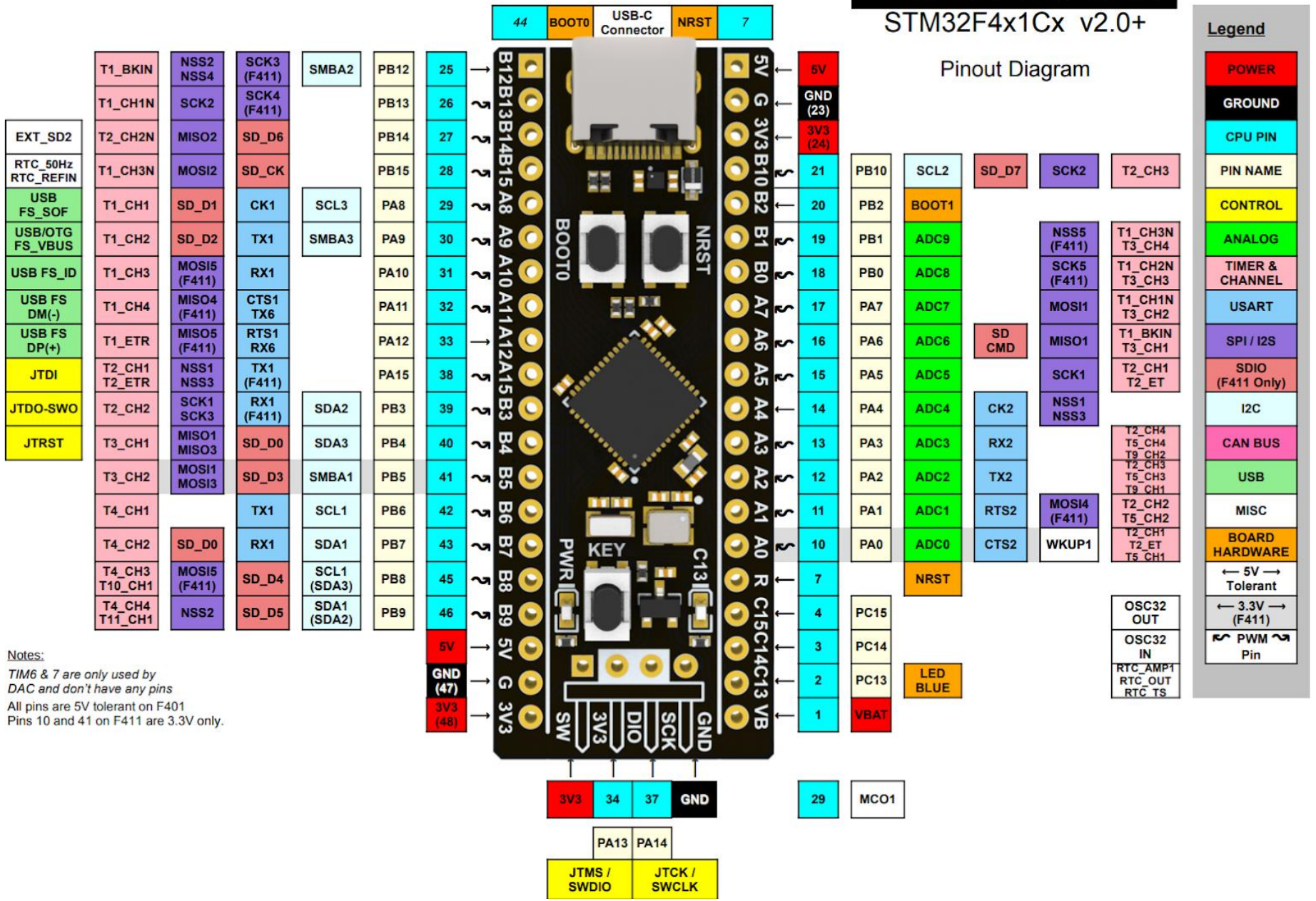
Thynk Loop

Sequence:

1. Configure the timer for your specific timing (ex 1ms)
2. Enable update interrupt in DIER
3. Enable timer
4. Configure timer NVIC
    1. NVIC_EnableIRQ(TIMx_IRQn);
    2. NVIC_SetPriority(TIMx_IRQn, 1);
5. Create **`TIM2_IRQHandler`**
    1. Check for the update interrupt flag in SR. if yes reset

Datasheet – PG14

BlackPill – Pin Configurations



GitHub Repo

Thynk Loop