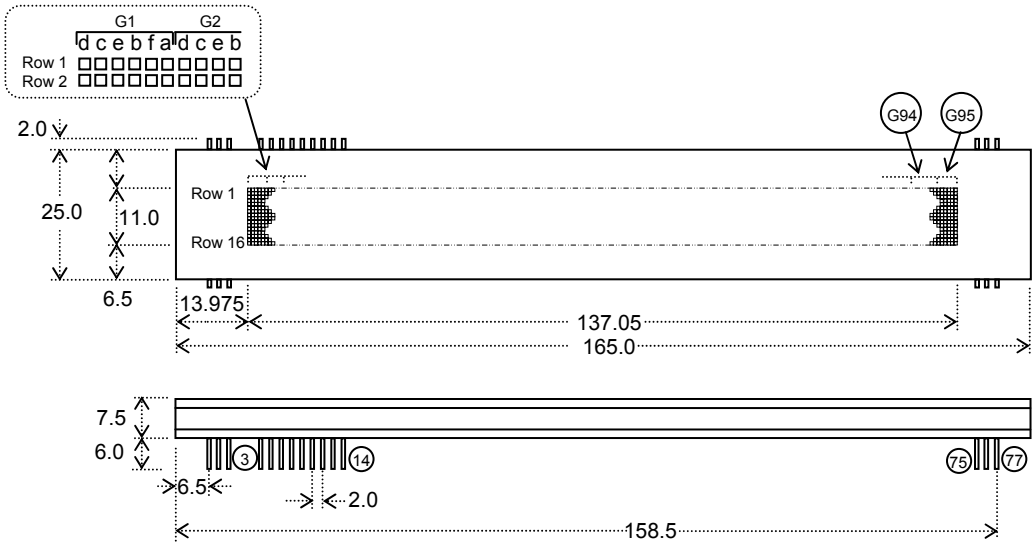
Graphic Dot Matrix Chip In Glass VFD MN28016A

- **280 x 16 Graphic Dot Matrix**
- **Chip in Glass Driver IC**
- **High Brightness Blue Green Display**
- **Synchronous Serial Interface**
- **Low Pinout Count**
- **Wide Operating Temperature**

This VF glass includes a 192 bit serial shift register, latched driver which connects to the anode and grid electrodes. An external host is required to provide a multiplexing data stream to refresh the display. The signal inputs can be connected to the ports of a CMOS microprocessor. The a.c. filament supply (F1, F2) can be derived from a source of 10KHz to 200KHz. Consult our application notes for further information.



Dimensions in mm
See full spec for tolerances

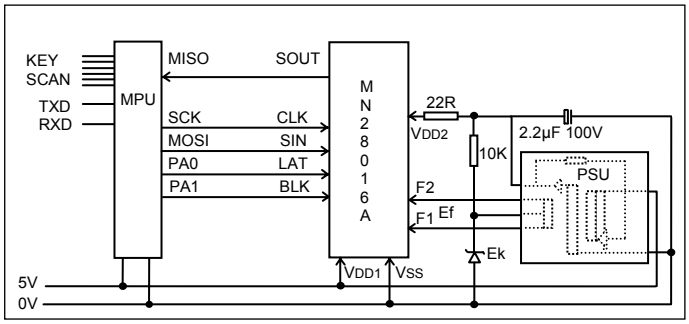
PIN OUT

Pin	Sig
1	F1
2	F1
3	F1
4	NP
5	NP
6	V_{DD2}
7	V_{SS}
8	V_{SS}
9	CLK
10	BLK
11	LAT
12	SOUT
13	V_{DD1}
14	SIN
75	F2
76	F2
77	F2

ELECTRICAL SPECIFICATION

Parameter	Sym	Min	Typ	Max	Unit	Condition
Logic Voltage	V_{DD1}	4.5	5.0	5.5	V	V_{SS}=0V
Logic Current	I_{DD1}	-	2.0	4.0	mA	V_{DD1}=5V
Filament Voltage	E f	5.7	6.3	6.9	Vac	V_{DD2}=0V
Filament Current	I f	135.0	150.0	165.0	mAac	V_{DD2}=0V
Display Voltage	V_{DD2}	46.0	55.0	58.0	V	V_{SS}=0V
Display Current	I_{DD2}	-	15.0	30.0	mA	V_{DD2}=55V
Filament Bias	E_K	-	5.0	-	V	V_{SS}=0V
Logic High Input	V_{IH}	x0.8	-	V_{DD1}	V	V_{SS}=0V
Logic Low Input	V_{IL}	0	-	+0.7	V	V_{SS}=0V
Logic High Input	I_{IH}	-	-	5.0	µA	V_{DD1}=5V
Logic Low Input	I_{IL}	-400	-250	-35	µA	V_{DD1}=5V

INTERFACE EXAMPLE

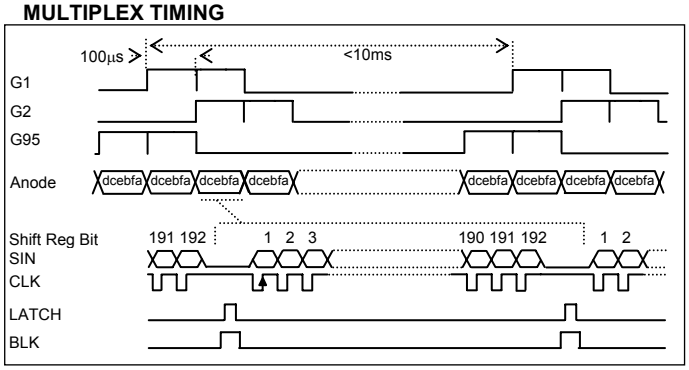


ENVIRONMENTAL and OPTICAL SPECIFICATION

Parameter	Value
Display Area (XxY mm)	137.05 x 11.0
Dot Size/Pitch (XxY mm)	0.34 x 0.5 / 0.49 x 0.7
Luminance	500 cd/m^2 Typ.
Colour of Illumination	Blue-Green (Filter for colours)
Operating Temperature	-40°C to +85°C
Storage Temperature	-50°C to +85°C
Operating Humidity (non condensing)	5 to 95% @ 25°C

1. The power on rise time should be less than 50ms.
2. The 22R resistor at the V_{DD2} input is required to prevent current surge during switching.
3. If scanning of the display stops with V_{DD2} applied, the BLK input must be set high to prevent damage to the display.

MULTIPLEX TIMING



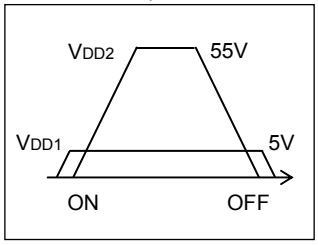
SHIFT REGISTER ASSIGNMENT

Electrode	Bit Numbers
Grid G95-G1	2-96
Row 16 'dcebfa'	97-102
Row 15 'dcebfa'	103-108
Row 14 'dcebfa'	109-114
:	:
Row 3 'dcebfa'	175-180
Row 2 'dcebfa'	181-186
Row 1 'dcebfa'	187-192

INTERFACE TIMING

Parameter	Time
CLK Cycle	200ns min
CLK High	80ns min
CLK Low	80ns min
SIN Setup	40ns min
SIN Hold	30ns min
LAT High	300ns min
CLK then LAT	250ns min
BLK Hold	10µs min

POWER SEQUENCE



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Subject to change without notice.
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