Ti-Shen (Andy), Chueh

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EDUCATION

University of Southern California — Los Angeles, CA
M.S. in Electrical Engineering — *Jan. 2021 - Dec. 2022*
Related Coursework: Computer Systems Organization, MOS VLSI Circuit Design

National Tsing Hua University — Hsinchu, Taiwan
B.S. in Engineering and System Science — *Sept. 2016 - June 2019*
Related Coursework: Electronics, Electric Circuits, Electronics Lab, Integrated Circuit Design, Programming Languages, Signal and System

EXPERIENCE

Nanoelectronic X-FET Green Devices Lab — Hsinchu, Taiwan
Research: N+/P Hybrid Poly-Si Shell Structure Junctionless-FETs — *Feb. 2018 - Jan. 2019*
- Outlined the advantages of junctionless field-effect transistors (JL-FETs)
- Presented two types of JL-FETs fabrication (Planar Shell & Nanowire Channel Shell)
- Compared the simulation results with the experiment data
- Exhibited the characteristic of I_D–V_G, I_D–V_D and DIBL
- Analyzed the temperature sensitivity in planar shell & nanowire channel shell JL-FETs

PROJECTS

Digital Logic design | *Modelsim* — *Jan. 2021 - May 2021*
- Utilized simple Verilog coding in Min and Max Finder RTL design
- Analyzed and interpreted waveform differences between Moore and Mealy state machines
- Designed 4-bit ALU and simulated the design with different test-bench
- Completed Single-Clock and Two-Clock FIFO Design
- Performed the needed stalling and forwarding in Pipeline CPU design
- Implemented simple pipelined system to design 3-Element Adder
- Handled the data dependencies by designing appropriate forwarding unit (FU) and hazard detection and stalling unit (HDU)
- Improved readability provided by RTL coding compared to structural coding at block-level design

Layout designs | *Cadence* — *Jan. 2021 - May 2021*
- Sized and drew the schematic and layout of each logic cells
- Calculated the rising and falling propagation delay with different sizing of transistors
- Designed 6x6-bits Wallace Tree multiplier, 16-bit Ripple Carry Adder, and 16-bit D Flip Flop with asynchronous reset
- Performed the functional verification of the 12-bits Multiply-Accumulator
- Achieved maximum worst-case delay (1.91 ns), maximum achievable clock frequency (101 MHz) and clock period (20896.38 μm^2 * ns)

TECHNICAL SKILLS

Programming: Java, Matlab, Verilog RTL, MySQL, VHDL
Developer Tools: Cadence, Modelsim