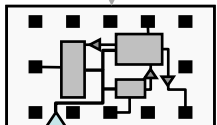
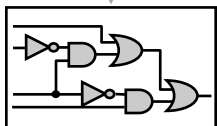


ENTITY test is  
port a: in bit;  
end ENTITY test;



DRC  
LVS  
ERC

