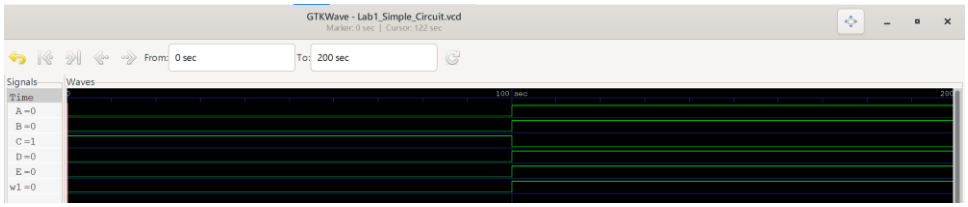
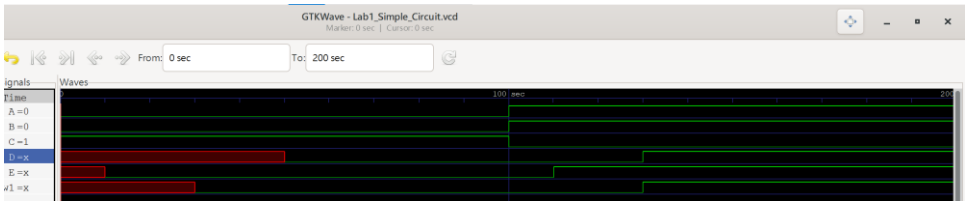
Lab1_110550085

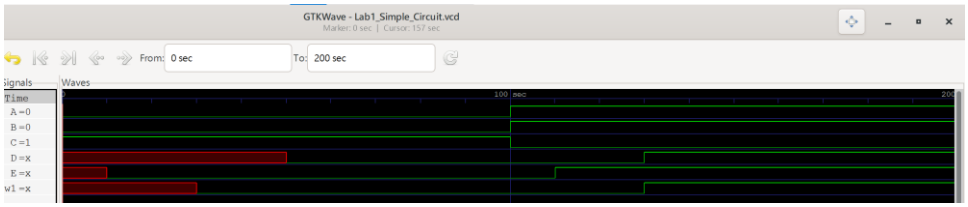
(1)





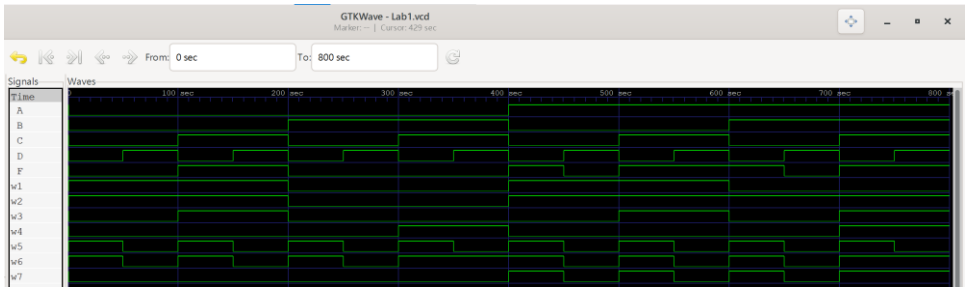
The upper one is the result of Simple_Circuit.v
The lower one is the result of Simple_Circuit_prop_delay.v
We can see that the lower one has a propagation delay of
50 sec for D, 10 sec for E, and 30 sec for w1.

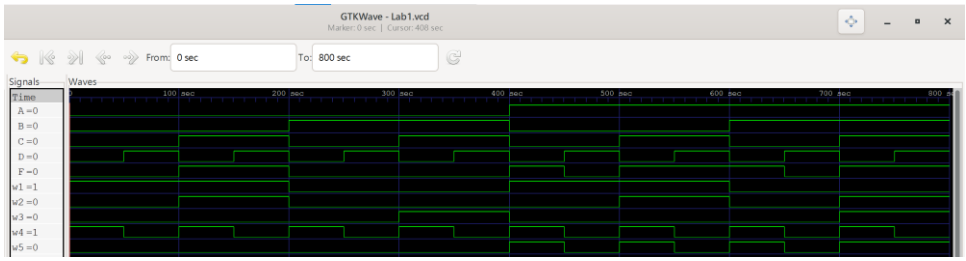
(2)



It’s the result that comes after the change, we can see that there’s **no difference** because in hardware description language, the three gates are constructed simultaneously, and the change of order of declaration doesn’t change the result.

(3)





The three pictures are the results of Lab1_gatelevel.v, Lab1_dataflow.v, and Lab1_gatelevel_UDP.v, respectively. We can see that three picture all indicate the same result that F(A, B, C, D)= **Σm(2, 3, 8, 10, 11, 12, 14, 15)**, which is exactly the result of the logic diagram.

(4)

No, it is not the least gate input count logic diagram.

We can write it as F=(A+B')C+(BC+D')A,

Then F=(A+B')C+(BC+D')A,

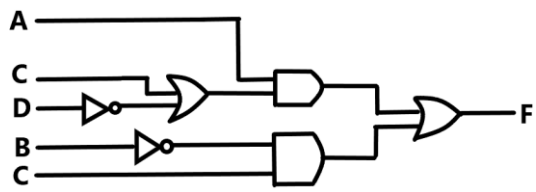
F=AC+B'C+ABC+AD',

F=AC+B'C+AD',

F=A(C+D')+B'C.

This boolean expression has gate input cost of 8+2=10.

And it can be drawn like this:



(5)

這次做這個實驗其實並不是很順利，在寫 module 時犯了很多小失誤，也花了很多時間 Debug，我也深刻感受到在做數位電路設計時，任何的小失誤都可以是致命的。像是這次期中考，我也犯了很多小失誤，以至於明明

會八十分以上的題目，硬是被扣到不及格收預警。但經過這次的實驗，使我對 Verilog（尤其是 Testbench）的撰寫和使用有了稍微深一點的認識，也對終端機的使用有了一點概念，我想，在一次次的學習中，我必能漸漸改進以往的缺失，並為未來更好的自己做好準備！