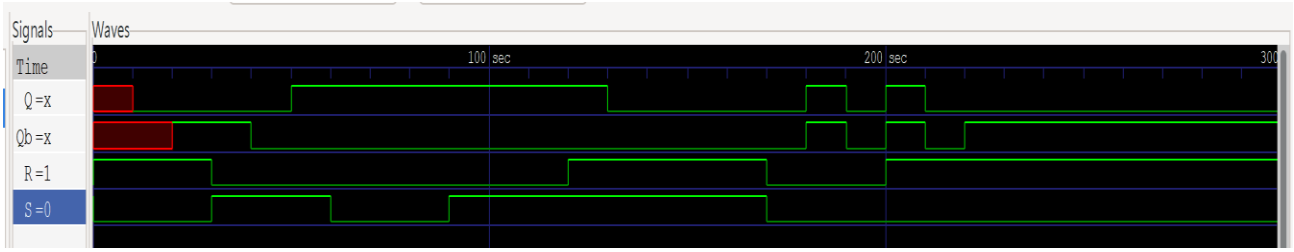
Lab3_110550085

(1)

Waveform:

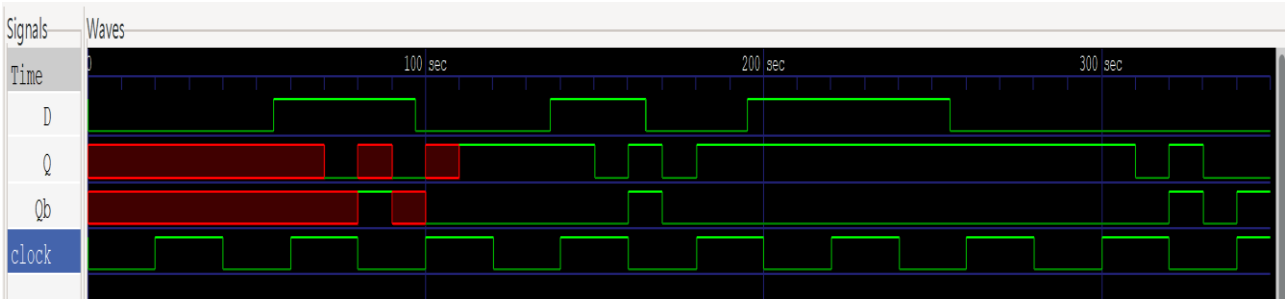


We can know this result is correct by observing the characteristic table of the SR-Latch (also can be confirmed manually), notice that for every change it takes 20 time units to reach the desired result:

S	R	Q^+
0	0	No change ($Q^+ = Q$)
0	1	Reset ($Q^+ = 0$)
1	0	Set ($Q^+ = 1$)
1	1	Indeterminate

(2)

Waveform:



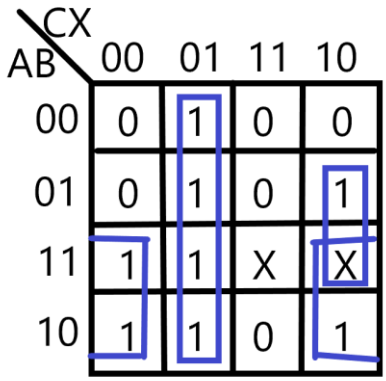
We can know this result is correct by observing the Q and Qb for every 30 time units after the edge occurs, since the delay for the flip flop is 30 time units.

(3)

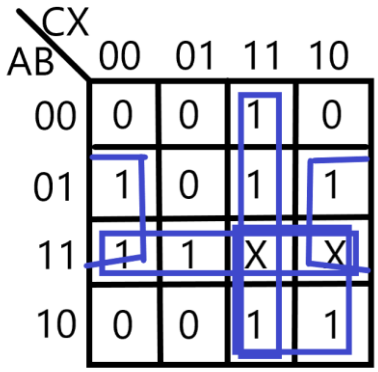
State-Diagram-Based:

For the state-diagram-based one, first use two reg to store current state(state) and next_state, then use parameter to represent the seven states, from 000 to 010), every time when clock is positive-triggered or reset is negative-triggered, check reset, if it equals to 0, then set the state to 000, otherwise, set it to the next_state.
Also, for the next_state, use case to determine what the it should be according to the state diagram.

Structural-Model:
For the structural model one, we first calculate the SoP form of DA, DB, and DC, the Karnaugh map is shown below:



DA=Ax'+C'x+BCx'

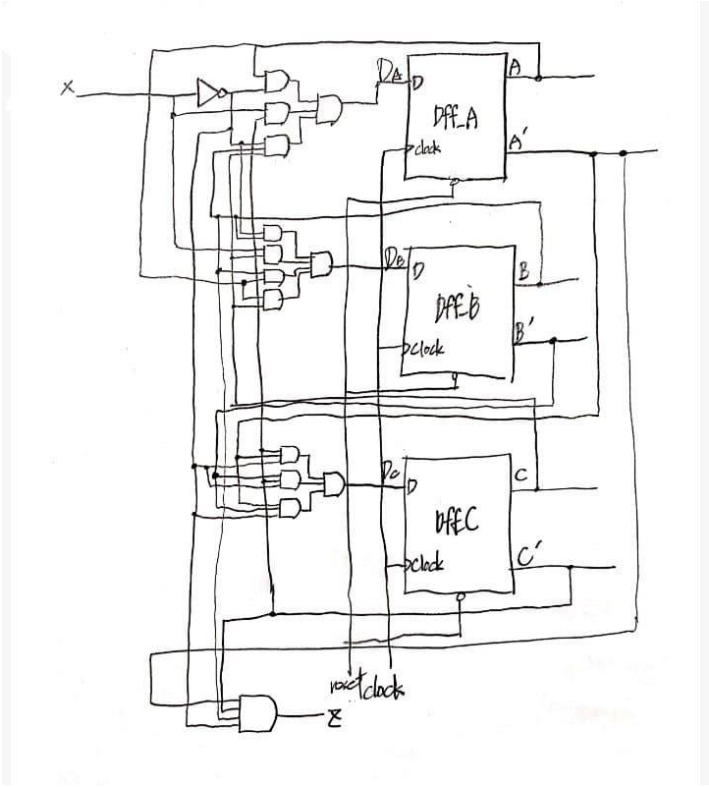


DB=Bx'+Cx+AB+AC

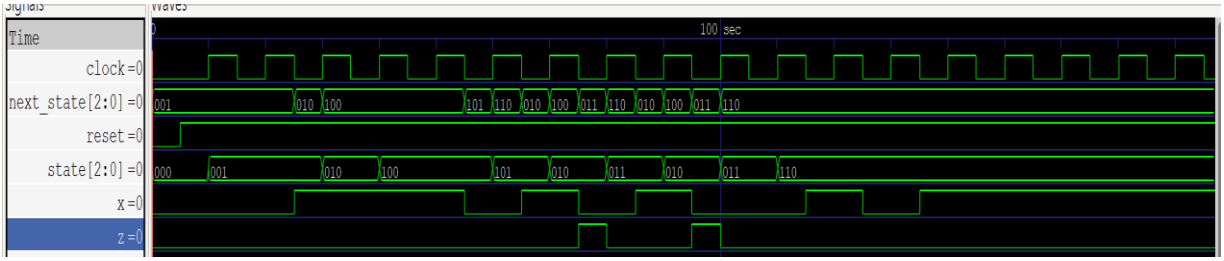
AB \ CX	00	01	11	10
00	1	0	0	1
01	1	0	0	0
11	0	0	X	X
10	1	0	0	0

$$DC=A'C'X'+B'C'X'+A'B'X'$$

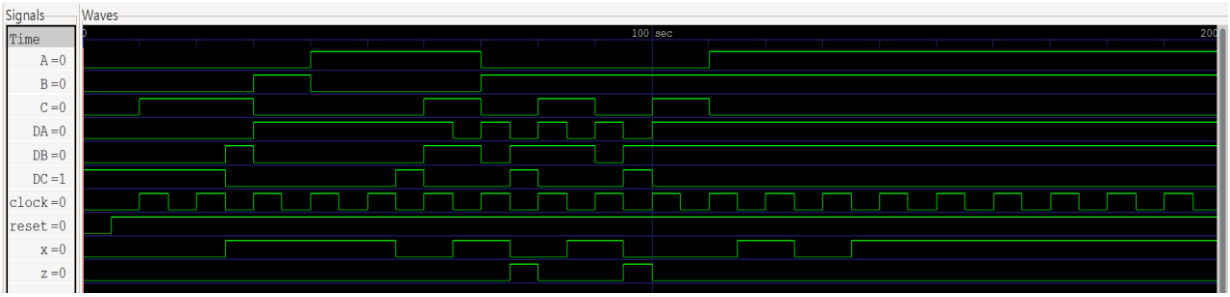
And z=A'BC'X', which can be observed easily.
With the K-maps, we can draw the circuit of the Mealy-type Sync Seq Circuit.



Waveform:
State-Diagram-Based:



Structural-Model:



To design the testbench, first set reset and clock to 0, then at #5, set reset to 1 to test whether reset is functionable, and then, set clock tick to every 5 time units, so clock would be triggered every 10 time units. Then, set x by the sequence of 00111010100101, start from #5 and change every 10 time units, thus we can see every state in the waveform, and can also see that after changing to 110, z never becomes 1 even though 010 is seen.

The desired result is shown in the chart below:

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Input	0	0	1	1	1	0	1	0	1	0	0	1	0	1	
State	S0	S1	S1	S2	S4	S4	S5	S2	S3	S2	S3	S6	S6	S6	S6
Output	0	0	0	0	0	0	0	1	0	1	0	0	0	0	

We can know that both the two waveforms are correct by checking the states and the output z in the waveforms, notice that in the structural model, the state is shown in the form of ABC.

(4)

這次實驗我遇到最大的困難是解釋結果，有了前兩次 Lab 的經驗，寫出 code 已稍微順利一些，但因為 delay 很長，導致在 latch 和 D flip-flop 的 waveform 中，要判定結果變得有些困難，結果這份報告中耗時最久的是完成 report。這次 report 中我也有不少收穫，更加了解了 Latch 和 flip-flop 的運作原理，也熟悉了 parameter 和 fork join 的用法，還在第三題中了解到要怎麼寫出完整的測資，希望有了這些經驗，在未來的實驗課中能夠有

更好的表現。