1.Calcultions

According to the CMOS Design Assignment, a NOR gate needs to be designed. The specific circuit diagram and the parameters provided are as follows:

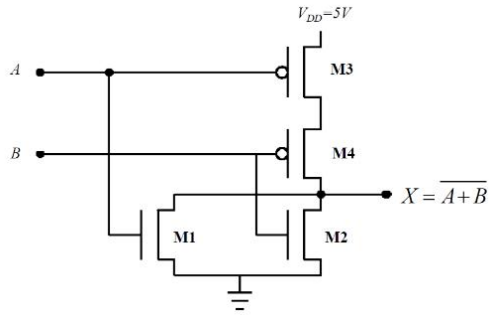

Figure 1: The circuit for two-input NOR gate [1]

Table 1: The specifications of the Design

Operating voltage of the device VDD	5V
Threshold voltage of n-channel MOSFETs VTn	0.2V
Threshold voltage of p-channel MOSFETs VTp	-0.2V
oxide capacitance Co	$5*10^{-4}$ Fm^{-2}
Electron mobility	0.1 m^2 $V^{-1}S^{-1}$
hole mobility	0.05 m^2 $V^{-1}S^{-1}$
Minimum feature size	0.2μm
maximum alignment error	0.1μm

First, the transfer characteristic of a CMOS inverter is shown in the following figure:

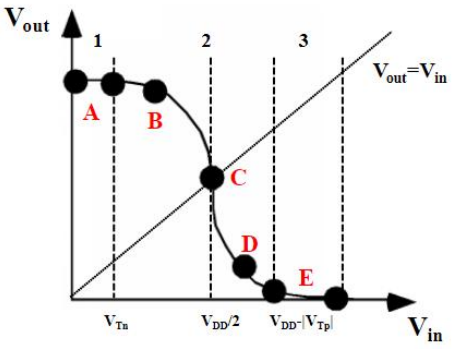

Figure 2: The transfer characteristics of a CMOS inverter [1]

According to the hints, MOSFET's operating point is assumed to be point C. Therefore, the voltage V_A and V_B satisfy the following equation:

$$V_A = V_B = V_{out} = \frac{1}{2}V_{DD} = 2.5V \quad (1)$$

To determine the working region of M3 and M4, firstly assume M3 is in the linear region and M4 is in the saturation, and then verify the correctness of the assumptions based on the results obtained.

Since M3 and M4 are connected in series, the currents flowing through M3 and M4 are equal, therefore:

$$I_{d3} = I_{d4} \quad (2)$$

Because M3 is assumed to be in the linear region and M4 in the saturation region, according to the current in the linear region: $I_D = \beta[(V_{GS} - V_T) * V_{DS} - \frac{V_D^2}{2}]$ and current in the saturation region: $I_D = \frac{\beta}{2}(V_{GS} - V_T)^2$, assuming that the voltage between M3 and M4 is $V_{3,4}$, the following equation can be derived:

$$I_{d3} = I_{d4} = \beta\left[(V_{GS3} - V_T) * V_{DS3} - \frac{V_{DS3}^2}{2}\right] = \frac{\beta}{2}(V_{GS4} - V_T)^2 \quad (3)$$

Where $V_{GS3} = 2.5V - 5V = 2.5V$, $V_{DS3} = (V_{3,4} - 5)V$, $V_{GS4} = (2.5 - V_{3,4})V$. Therefore, simplifying the equation for equal series currents yields:

$$\beta\left[(2.5-(-0.2))*(V_{3,4}-5)-\frac{(V_{3,4}-5)^2}{2}\right]=\frac{\beta}{2}(2.5-V_{3,4}-(-0.2))^2 \quad (4)$$

Solving the equation yields:

$$V_{3,4}\approx 1.07V \; or \; 4.33V$$

According to the conditions to be satisfied for the PMOS linear region: $V_{DS}>V_{GS}-V_T$ and pMOS conditions in the saturation region: $V_{DS}<V_{GS}-V_T$.

When $V_{3,4}\approx 1.07V$, for M3 MOSFET, $V_{DS}(-3.93)<V_{GS}(-2.5)-V_T(-0.2)$. M3 is in the saturation region, which is inconsistent with the previous condition of assuming M3 is in the linear region.

When $V_{3,4}=4.33V$, for M3 MOSFET, $V_{DS}(-0.67)>V_{GS}(-1.83)-V_T(-0.2)$, M3 is in the linear region. For M4 MOSFET, $V_{DS}(-1.83)<V_{GS}(-1.83)-V_T(-0.2)$, M4 is in the saturation region. Both M3 and M4's working regions are consistent with the previous assumptions, indicating that the assumptions are valid. The final voltage between M3 and M4 is $V_{3,4}=4.33V$.

According to the conditions to be satisfied for the nMOS linear region: $V_{DS}<V_{GS}-V_T$ and nMOS conditions in the saturation region: $V_{DS}>V_{GS}-V_T$.

For M2 MOSFET, $V_{DS}(2.5)>V_{GS}(2.5)-V_T(0.2)$. M2 is in the saturation region.
For M1 MOSFET, $V_{DS}(2.5)>V_{GS}(2.5)-V_T(0.2)$. M1 is in the saturation region.
Therefore,

$$I_{d1}=I_{d2}=\frac{\beta}{2}(V_{GS}-V_T)^2 \quad (5)$$

Because of the current division principle $I_{d4}=2*I_{d2}=2I_{d1}$ and:

$$\beta=\mu C_O\frac{W}{L} \quad (6)$$

Where μ is the channel mobility. Electron mobility is 0.1 m2 V-1S-1 and hole mobility is 0.05 m2 V-1S-1. CO is the gate capacitance per unit area. $\frac{W}{L}$ is the aspect ratio of gate width to length. Therefore,

$$2*I_{d2}=I_{d4}=2\mu_n C_O\frac{W_n}{L_n}(V_{GS2}-V_{Tn})=\mu_p C_O\frac{W_p}{L_p}\left(V_{GS4}-V_{Tp}\right) \quad (7)$$

The equation to be solved yields:

$$8*\frac{W_n}{L_n}=\frac{W_p}{L_p} \quad (8)$$

According to the Hints，the length of nMOS and pMOS can be defined as 2λ. And the width of nMOS is defined 4λ and the width of pMOS will be $8*L_p=32\lambda$. The minimum feature size 0.2 μm is the smallest dimension that can be defined on a chip. Therefore, the channel length L:2λ will be equal to 0.2 μm, which means that $\lambda=0.1\mu m$

2. Layout

2.1 The design rules and explanations

For the n-well region, the minimum distance between the n-well region and the p^+ junction is 3λ. [2] And the minimum spacing between the n-well and the junctions of nMOS is 5λ. [2] Since the lateral diffusion capability is large, once the n-well diffuses to a short circuit with the n-channel, and the n-well is connected to the n-channel, the circuit will not work. [2]

For metal, the minimum metal width is 3λ. And the minimum metal spacing is 3λ. And the metal needs to overlap the underlaying contacts by at least λ. The minimum width in general for metal region is 2λ. However, according to the hints, the width of VDD and GND is expanded to 4λ in our design.

For poly-Si region, the minimum width and spacing is 2λ. The minimum spacing between poly-Si and active edge is λ. If the poly-Si gate does not fully cross the active region, which will result in junctions being implanted everywhere in the active region except under the gate. This catastrophic misalignment will result in a short circuit between the source and the drain. Therefore, the poly-Si region must exceed the active region by at least 2λ. [2]

For contact, the active contact size is 2λ and the minimum active contact spacing is 2λ, the minimum contact to metal and active edge spacing is λ. If the distance between the contact and poly-Si regions is too small, these two regions may overlap in the microcircuit, which will result in a short circuit in the poly-Si region, turning the transistor off. [2]

For active region, the active region should surround the contact at least λ. If the overlap between the edge of the active region and the contact is not enough, there will be short circuit. Additionally, the active region must extend past the poly-Si region gate by at least 5λ. [2]

2.2 The Nor gate layout

The software for designing the layout is used in the design. In the layout diagram, each cell represents a distance of λ:0.1μm, which is also the value of the maximum alignment error. For aesthetic and visual purposes, five different coloured lines are used to mark the different regions, where the pink line surrounds the n-diffusion active region, the green line surrounds the p-diffusion active region, the blue line surrounds

the metal region, the black region is the contact region, the red line surrounds the poly-Si region and the yellow line surrounds the n-well region.

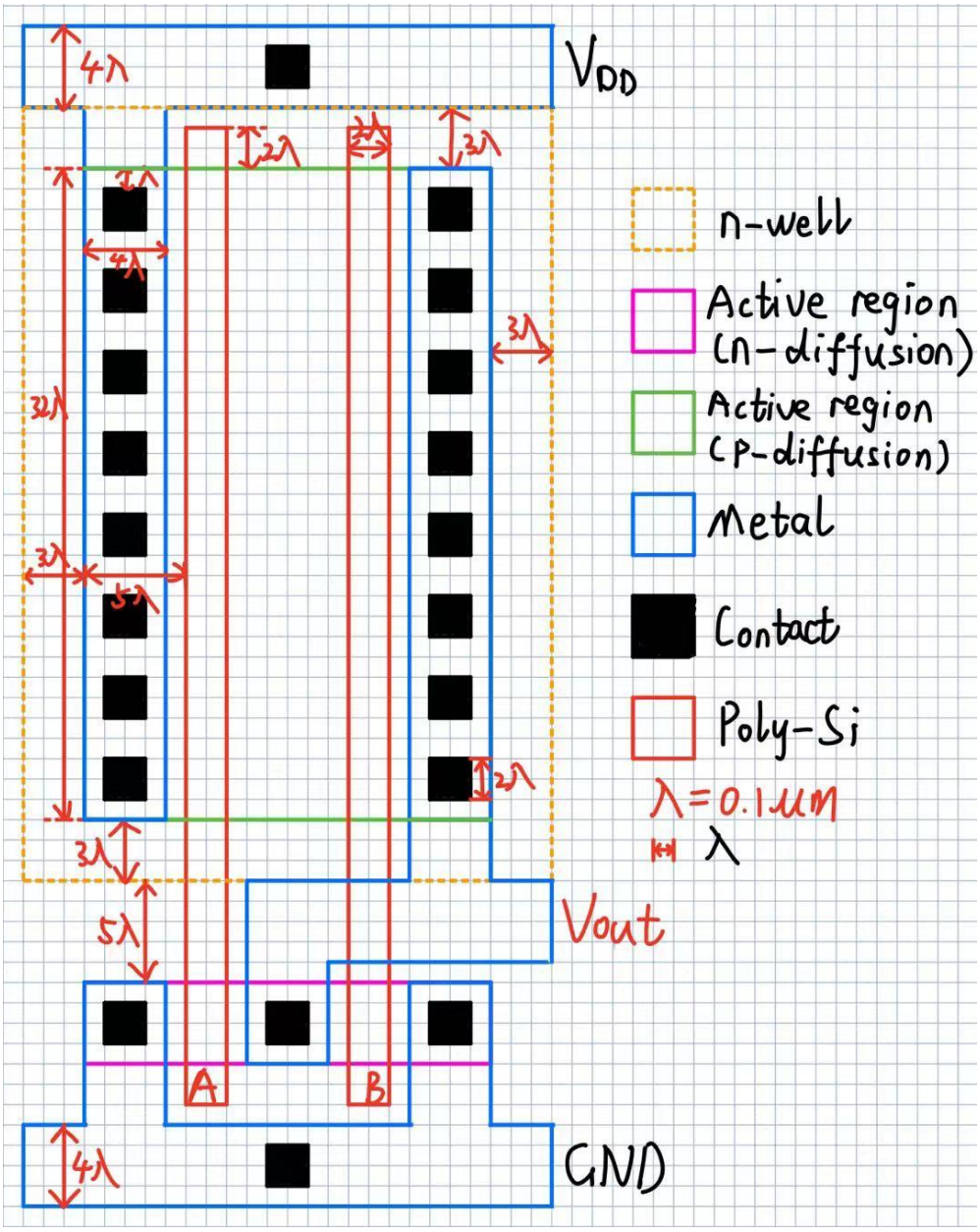

Figure 3: The layout of the two-input NOR gate circuit

References:

[1] I.Mitrovic. Design Assignment [Online]. Available: https://liverpool.instructure.com/courses/47037/

[2] I.Mitrovic. Layout and design rules [Online]. Available: https://liverpool.instructure.com/courses/47037/ pages/