# Xi’an JIAOTONG-LIVERPOOL UNIVERSITY

**西 交 利 物 浦 大 学**

# CourseWork Submission CoVer Sheet

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***Abstract***

*This task requires us to understand the whole IC design process and draw the corresponding* ***Layout*** *according to the circuit. After providing the Full layout, we also need to draw the four masks:* ***Active Layer, Poly-Si, Contact and Metal masks****. This report is mainly divided into three sections. The first part is the* ***introduction*** *of the assignment. In the main body, I have completed and* ***answer each******task requirement*** *in detail. Finally, I made a* ***summary*** *of the whole process.*

*For task 1, we first analyzed the logic circuit and judged that this logic circuit was composed of a NOR Gate and NOT Gate. Therefore, we finally consider that the logic function of the circuit is* ***OR****.*

*For task 2, I need to calculate the aspect ratio:* ***W/L*** *of each MOSFET under different Vout conditions. In the process of calculation, we need to judge the working mode of each MOSFET according to the known conditions and calculate the W/L of each MOSFET according to the corresponding mode. I summarized the* ***final results in the tables****.*

*For Task 3, I need to explain the* ***process*** *of* ***NMOSFET*** *in the manufacturing process, which is roughly divided into four parts: Active region, Gate, Contact, and Metal. For each section, I list its Top and Cross-section views. At the top and bottom of each figure, there are also some specific explanations.*

*For Task 4, I use the TSMC 7nm technology: 2λ (feature size) to draw our* ***full layout and the four masks****. Moreover, we need to pay extra attention to the design rules during the drawing process because each layer has its unique design rules. To reduce the layout area as much as possible, I also need to design the arrangement of each MOSFET and resistors, and the resistors need to be arranged in a “Snake” way.*

*Finally, I have made a* ***summary*** *of the whole process. Completing this assignment made me more clearly understand the design and manufacturing process of IC.*

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1. **Introduction**

**1.1 Introduction of Integrated circuit**

An integrated circuit is a group of electronic circuits on a small piece of semiconducting material (usually silicon). A large number of micro MOSFET are integrated into a small chip, which results in circuits that are smaller, faster, and cheaper than those made of discrete electronic components.

Integrated circuits are now used in almost all electronic devices and have revolutionized the electronic world. Computers, mobile phones and other digital household appliances have now become an integral part of the fabric of modern society because of the small size and low cost of integrated circuits.

**1.2 Introduction of the process of the IC design**

After the teacher's explanation, we know that the complete IC design is composed of 4 layers, which are: Active layer, poly-si layer, Contact layer and Metal layer. We need to define the active area and thin oxide region in Mask 1. Secondly, we need to define the poly-silicon gate in Mask 2. On the Contact layer, we need to delineate the Contact window, too. On the last Metal layer, we need to draw the Metal pattern.

**1.3 Task Introduction**

In this task, we are going to design a simple integrated circuit at Silicon Layout level. At the same time, we should be familiar with the manufacturing process flow of the whole Integrated Circuit. Moreover, we also need to understand the function of the circuit and calculate the aspect ratio (W/L) of each component under different  (0.2V, 0.1V and 0.01V). After the calculation, we need to provide the entire manufacturing process of NMOSFET. Because the production of NMOSFET requires a 4-mask process, in the article, I will introduce four masks in detail. In the end, we need to follow TSMC 7nm technology, (2(feature size): 7nm) to produce a full circuit design layout, and I will minimize the full layout following the MOSIS design rules. Additionally, the four masks will also be provided in the report.

**2.MOSIS Layout Design Rules**

**Due to the limitation of material processing, the design rules need to be taken into account when drawing the layout. The Design Rule is mainly divided into six parts:**

**2.1 Active Area Rule**

In this section, we specify the minimum Width and Spacing. Therefore, we need to design the layout according to this rule.

**2.2 Poly-Silicon Rules**

In this Mask, we need to note the minimum poly width and spacing. In addition, we also need to consider this part together with the Active region. Especially, the Poly inside and outside of active area also need to be highly considered.

**2.3 Metal Rules**

In this section, we limit the Metal's minimum width and spacing.

**2.4 Contact Rules**

In Design Rules, we need to pay special attention to this area. When designing Contact, we need to consider Contact together with poly and Active region. In particular, note that the minimum spacing between two Active Contact Spacing is .

**2.5 Supply Rail Metal**

In this design, according to the design rule, we can know the minimum  and will be .

**2.6 Resistor Rules**

When designing resistors, we need to set the width of resistors to a minimum: 

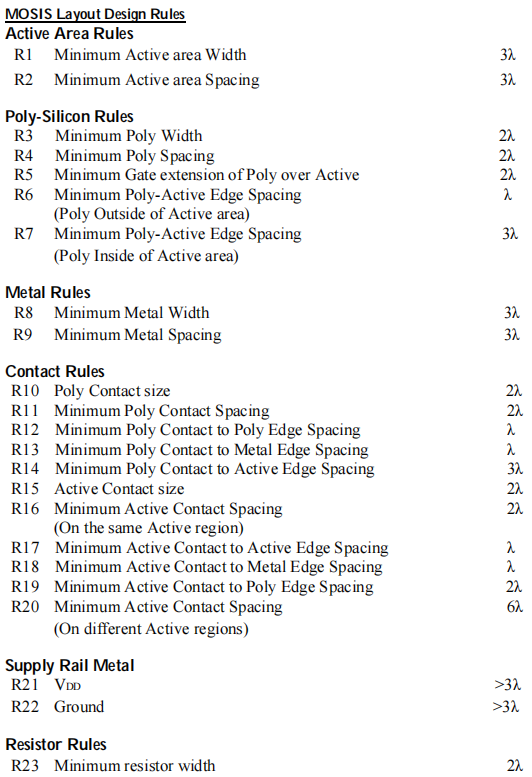


Figure 1:The design rules

**3.The logic function of the circuit**

According to the requirements, we can know the circuit is :

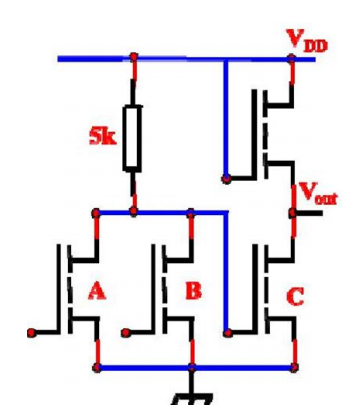
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Figure 2: Logic Circuit [1]

By observing the circuit, we find that the logic circuit consists of four MOSFETs and a  resistor. A NOR GATE and an inverter are formed as follows:

未命名绘图

Figure 3: The logic circuit

For NOT Gate，we can know the Truth table is：

Table 1: The truth table for NOT Gate

|  |  |
| --- | --- |
| Vin | Vout |
| 1 | 0 |
| 0 | 1 |

By simplifying the logic circuit above, we can get:

未命名绘图

Figure 4: Simple logic circuit

Therefore, from the figure, we can see that the function of this circuit is OR Gate. OR Gate has multiple input terminals, one output terminal, as long as one of the input is high level, the output is high level. The output is low only when all the inputs are low.

Where the Boolean expression of this logic circuit is:

 (1)

The specific Truth Table of the circuit is as follows:

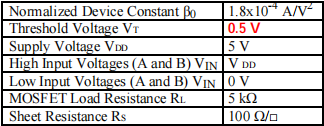
Table 2: Truth table for the logic circuit

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | out |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |

**4. Calculate the W/L of each MOSFET**

According to the requirements, we know the value of some parameters, including sheet resistance which can help me to calculate the size of the resistor. In addition, some other parameters can be seen in the following table:

Table 3: Process Parameters

****

Since the transistor has two states: Linear Mode and Saturation Mode, we should also consider the state of each MOSFET under different Vout conditions in the calculation process. Since the corresponding formulas of each state are different, we should pay special attention to this part.

**For the Liner mode, the transistor needs to satisfy .**

When ，

 (1)

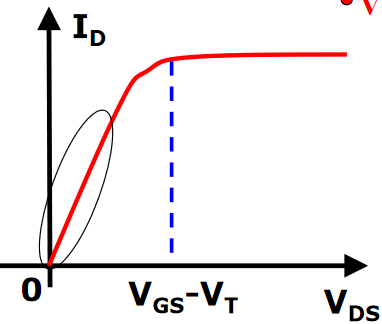
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Figure 5: Transistor in Linear Mode [2]

**For the Saturation mode, the transistor needs to satisfy .**

When ,

 (2)

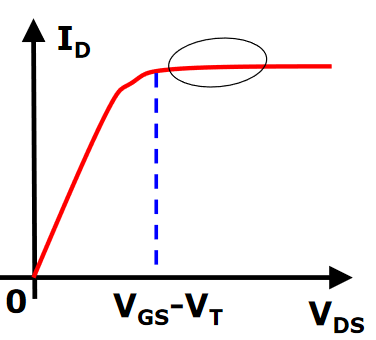
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Figure 6: Transistor in Saturation Mode [2]

**4.1 When Vout=0.2V**

1. Calculate the NOR Gate part:

We already know: , . If we assume that the resistance of A, B MOSFET is the same, which is equivalent to two resistors in parallel.

Therefore, we can get:

 (1)

Consider ,we can get：

 (2)

We already known：

 (3)

By substituting equation (3) into equation (2), we know that:

 (4)

Therefore, we can know：

 (5)

 (6)

Because we already known ,

We can get：

 (7)

According to , we can know:

 (8)

Because we know ，according to :

We can get :

 (9)

We know ：

 (10)

1. Calculate the W/L in Inverter part

If we assume that the NMOSFET on the upper right represents a resistance of 

We can get:

 (1)

Because：

 (2)

We have already known:

 (3)

We can get:

 (4)

Therefore, we can know:

 (5)

Because we already known:

 (6)

We can get:

 (7)

From the figure, we can know that:

 (8)

Therefore, we can know for MOSFET on the top right:

 (9)

Therefore,we can know that for Lower right MOSFET:

 (10)

Therefore, in the case of , the W/L of each NMOSFET results as follows(Let's assume that the top right MOSFET is D):

Table 4: The results for the VOUT=0.2V

|  |  |
| --- | --- |
| No. | W/L |
| A | 3 |
| B | 3 |
| C | 6 |
| D | 0.5 |

**4.2 When VOUT=0.1V**

1. Calculate the NOR Gate part:

We already know: , . If we assume that the resistance of A,B MOSFET is the same, which is equivalent to two resistors in parallel.

Therefore, we can get:

 (1)

Consider , we can get:

 (2)

We have already known：

 (3)

By substituting equation (3) into equation (2), we know that:

 (4)

Therefore, we can know that:

 (5)

Therefore, we can know:

 (6)

Because we already known ,

We can get：

 (7)

According to , we can know:

 (8)

Because we know ，according to :

We can get :

 (9)

We know ：

 (10)

1. Calculate the W/L in the Inverter part

If we assume that the NMOSFET on the upper right represents a resistance of 

We can get:

 (1)

Because：

 (2)

We have already known:

 (3)

We can get:

 (4)

Therefore, we can know:

 (5)

Because we already known:

 (6)

We can get:

 (7)

From the figure, we can know that:

 (8)

Therefore, we can know for MOSFET on the top right:

 (9)

Therefore, we can know that for Lower right MOSFET:

 (10)

Therefore, in the case of , the W/L of each NMOSFET results as follows(Let's assume that the top right MOSFET is D):

Table 5: The results for the VOUT=0.1V

|  |  |
| --- | --- |
| No. | W/L |
| A | 6 |
| B | 6 |
| C | 12 |
| D | 0.5 |

**4.3 When VOUT=0.01V**

1. Calculate the NOR Gate part:

We already know: , . If we assume that the resistance of A,B MOSFET is the same, which is equivalent to two resistors in parallel.

Therefore，we can get:

 (1)

Consider ,we can get:

 (2)

We already known：

 (3)

By substituting equation (3) into equation (2), we know that:

 (4)

Therefore, we can know：

 (5)

 (6)

Because we already known ,

We can get：

 (7)

According to , we can know:

 (8)

Because we know ，according to :

We can get :

 (9)

We know ：

 (10)

1. Calculate the W/L in the Inverter part

If we assume that the NMOSFET on the upper right represents a resistance of 

We can get:

 (1)

Because：

 (2)

We have already known:

 (3)

We can get:

 (4)

Therefore, we can know:

 (5)

Because we already known:

 (6)

We can get:

 (7)

From the figure, we can know that:

 (8)

Therefore, we can know for MOSFET on the top right:

 (9)

Therefore, we can know that for Lower right MOSFET:

 (10)

Therefore, in the case of , the W/L of each NMOSFET results as follows(Let's assume that the top right MOSFET is D):

Table 6: The results for the VOUT=0.01V

|  |  |
| --- | --- |
| No. | W/L |
| A | 60 |
| B | 60 |
| C | 120 |
| D | 0.5 |

**5.The Process Flow of NMOSFET**

We used the 4-mask process in the production of NMOSFET. In this part, I will introduce the process flow from step one to the last one step by step. For each step, we'll follow it with detailed comments. According to my understanding, I divide the whole parts into four steps, and each step can get the Mask.

**5.1 Mask 1: Active region**

First, Si Substrate (P) is required to form **** Field Oxide after the Layering process. After this, we obtain Mask 1 through the Oxide Etching (Patterning) process. According to Figure, the Active region is the green part in the image.

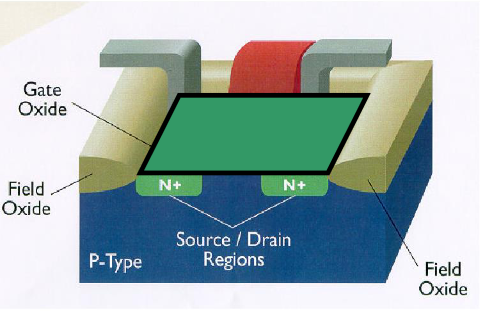


Figure 7:Top view of step 1 [3]

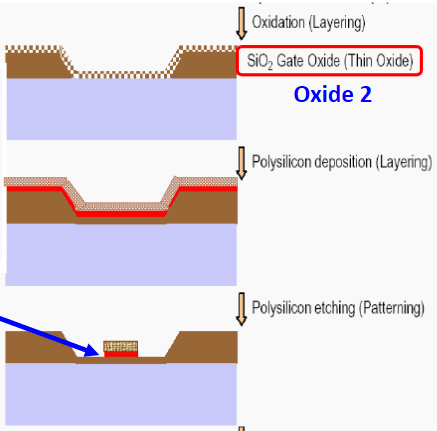


Figure 8: cross-section [3]

From the image, we can see that SI Slice is oxidized to form Oxide 1. Also, according to the Design Rule, the size of mask1 must be a multiple of the Minimum Feature Size.

**5.2 Mask 2: Gate**

After getting the Mask 1, we need to get SiO2 Gate Oxide (Thin Oxide) through the Oxidation (Layering process). After that, we need to obtain Mask 2 through poly-silicon deposition and etching process. According to Figure, the red part is Mask 2

****

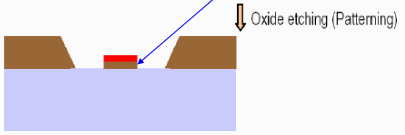
****

Figure 9: Cross-section view of step2 [3]

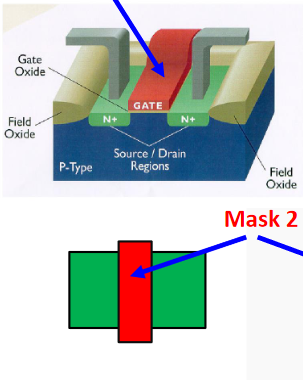
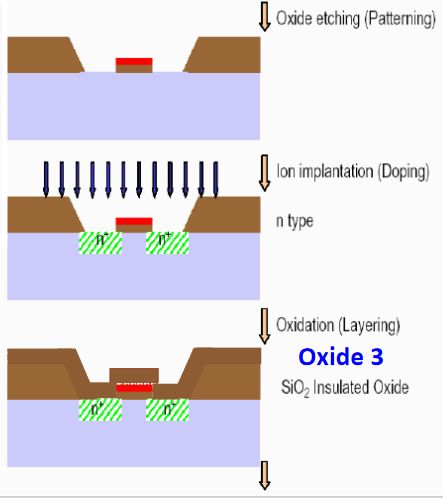


Figure 10: Top view of step 2 [3]

From the image, we can see that the slice of silicon is re-oxidized to form OXIDE2. At the same time, New thinner oxide is filled with the window. Moreover, the oxide and polysilicon are photoengraved after the mask for the etching of polysilicon gate electrode.

**5.3 Mask 3: contacts**

After obtaining Mask 2, we first need to conduct Patterning and Doping (Ion implantation) to obtain the region. Then, we need to perform Oxidation and Oxide Etching operation to get Contact Windows: Mask 3. The detailed operation process is shown below:

****

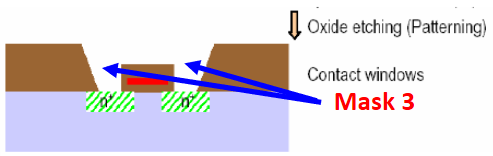
****

Figure 11: cross-section view of step3 [3]

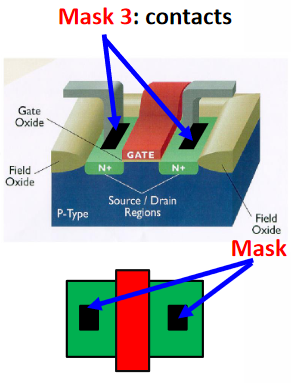
****

Figure 12: Top view of step 3 [3]

As we can see from The image, The SiO2 Insulated Oxide formed Oxide3. The Oxide is etched from the source to drain. And we can increase the conductivity by dopes the polysilicon. Because of the particularity of Contacts, the contact or via holes are opened. In addition, according to the design rules, the size of each hole must be equal to the minimum feature size.

**5.4 Mask 4: metal**

After getting Contact Windows, we first need to perform Oxide Etching (Patterning). Then, the Metal deposition (Layering) and Metal etching (Patterning) operations are performed to obtain Mask 4: Metal

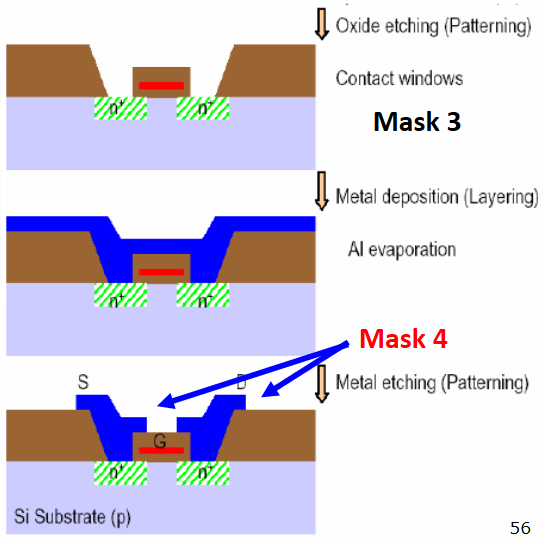
****

Figure 13: Cross-section view of step 4 [3]

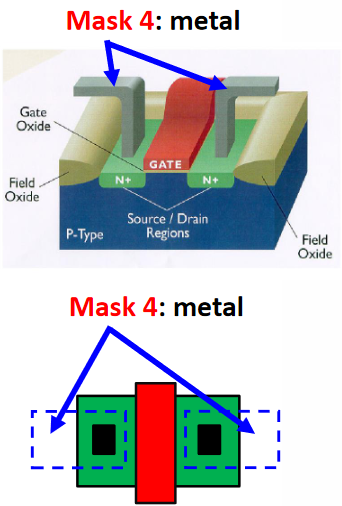


Figure 14: Top view of step 4

From the image, we can see that first, the aluminium evaporates and covers the entire sheet, and finally, we also need to cover it with photoresist. Aluminium makes contact with the source and drain down the contacts. Importantly, the width of the aluminium must cover the contact holes.

**6. Full layout and 4 masks**

When I drawing the full layout, I need to consider the different layers. Therefore, each layer is represented by different drawing forms. The specific representation method is shown in the following figure. In this figure, we also define the width of 2λ (feature size) on the square paper, and the width of 1 is a small grid.

In addition, I pay more attention to design rules when drawing the full layouts and four masks. After drawing each Mask, I will compare the final masks with the Full layout to avoid making mistakes. After a lot of careful design, I created the final full layout and drew all of its 4 masks below. Among them, the width of my full layout is 48 and the length is 58, so my minimum area is :

 (1)

Because we use the TSMC 7nm technology, 2 λ (feature size): 7nm.

Therefore, we can calculate our minimum area is:

 (2)

I tried to keep all the MOSFETs together as much as possible according to the design rules. And the resistance is designed like a “snake” to get the smallest full layout.

**6.1 The cover of the layout**

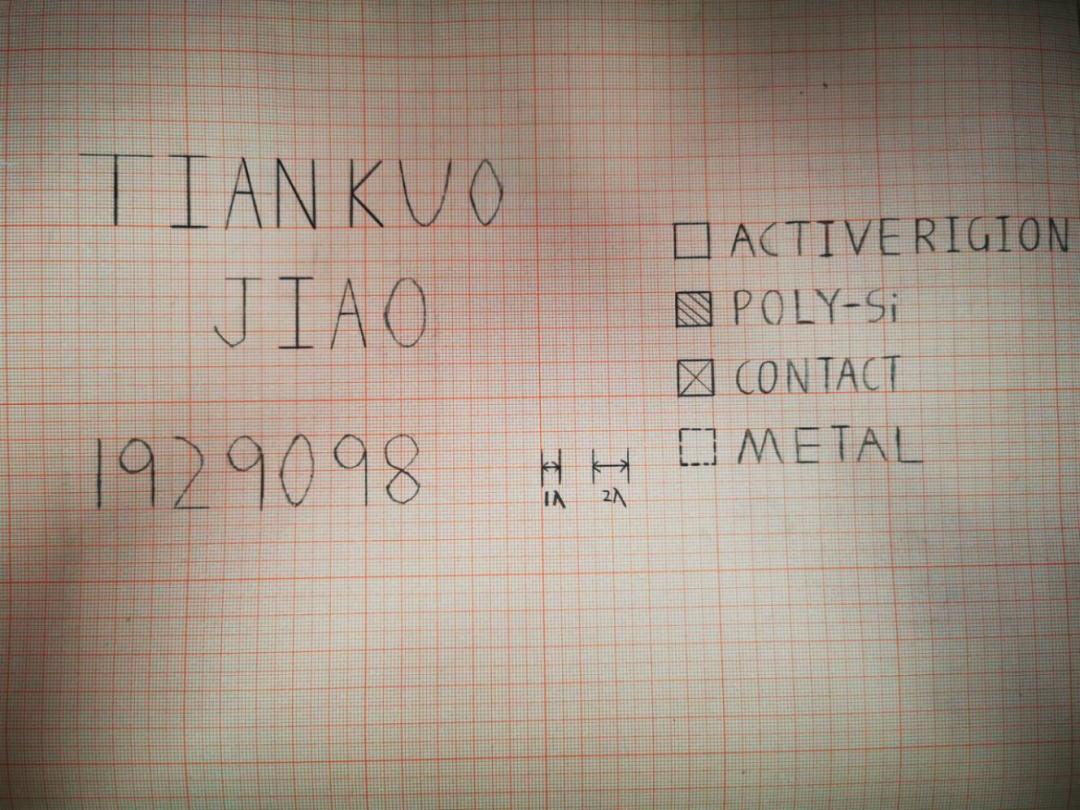


Figure 15: The cover of the whole layout

In this part, we define the feature size and distinguish each layer by different forms. Therefore, the structure between each layer can be seen more clearly.

**6.2 The full layout of the design**

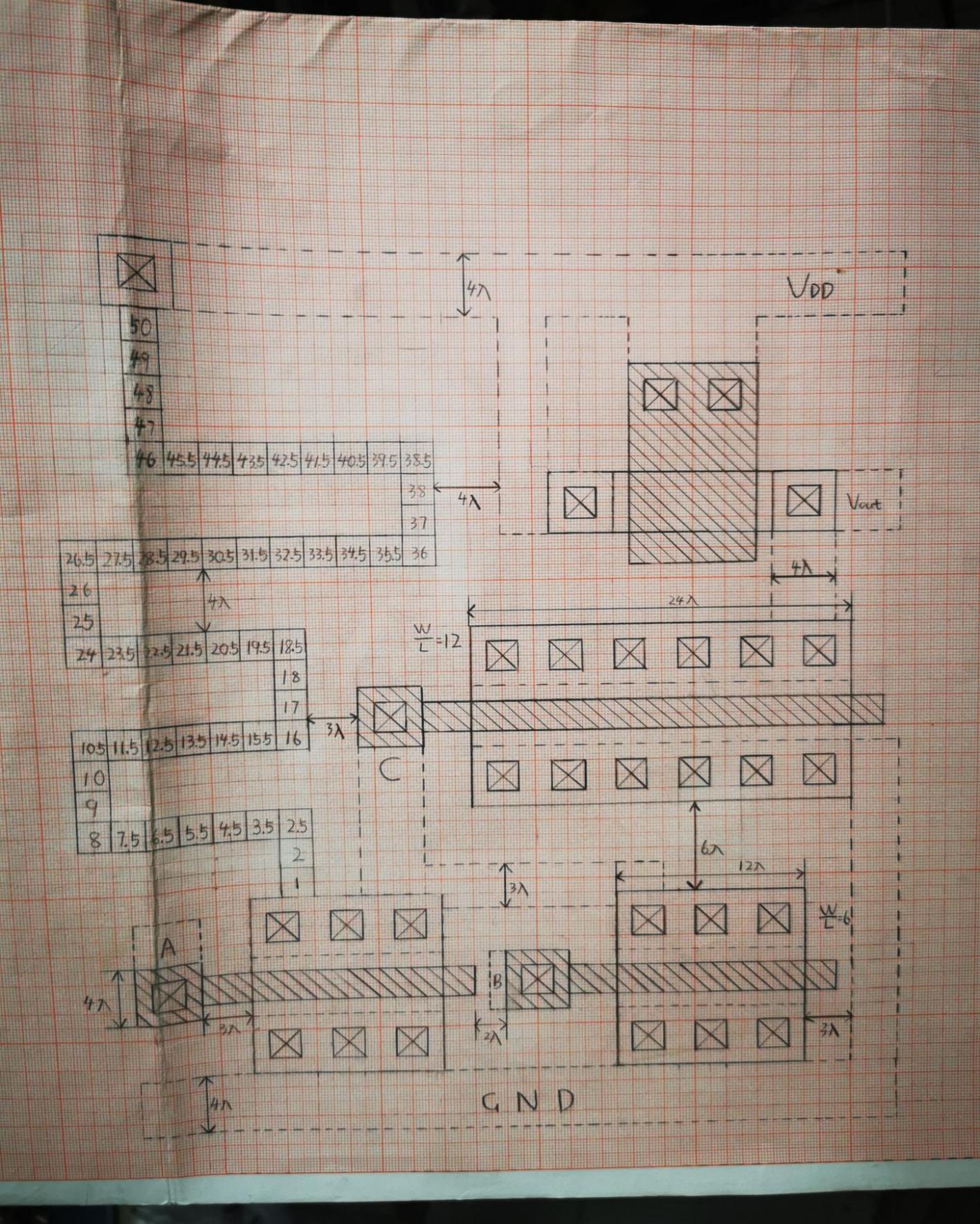


Figure 16: The full layout of the design

This figure is my full layout. In this part, we have noticed the design rule of each layer. For example, the minimum distance between Metal and other Metal is 3, and the minimum width of GND and VDD is 4. The minimum distance between each active region is 6, which means we can't place our three mosfets and resistors randomly. For the design of resistance, since the resistance value of the resistance is  and the sheet resistance  is , it means that we need to draw 50 minimum resistors, each of which has a minimum resistance of a  grid. To achieve the requirements of minimum area, we need to make resistors like “snake”. Moreover, make sure that the distance between each row of resistors is 4.

**6.3 The mask 1 of the layout**

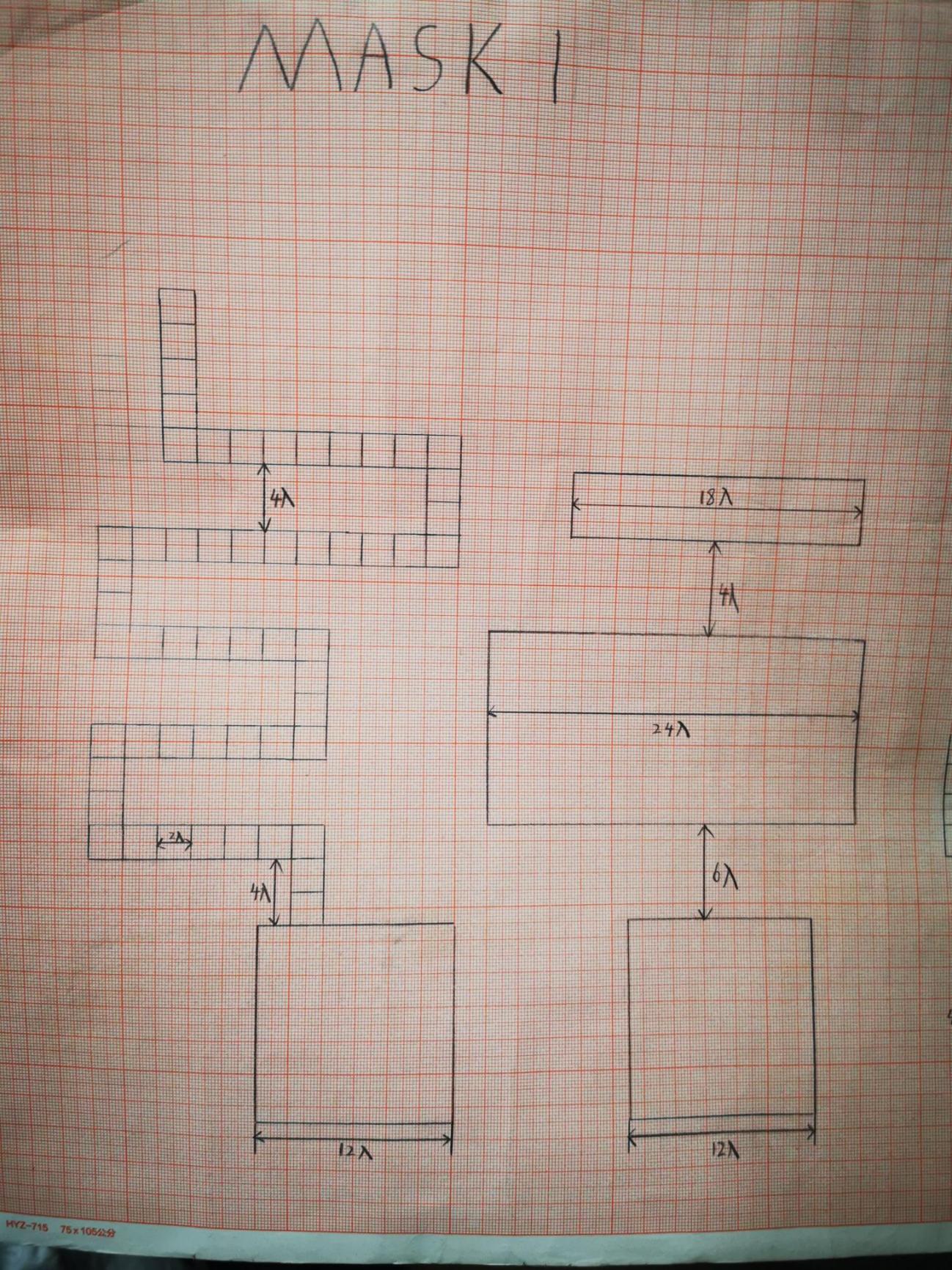


Figure 17: The mask 1:Active layer

For the first Mask, we need to draw the active region of the Full layout, especially note that we need to draw the resistance, which is also on the active layer. After drawing the four major active regions, we connect the resistor to the active region of the first MOSFET.

**6.4 The mask 2 of the design**

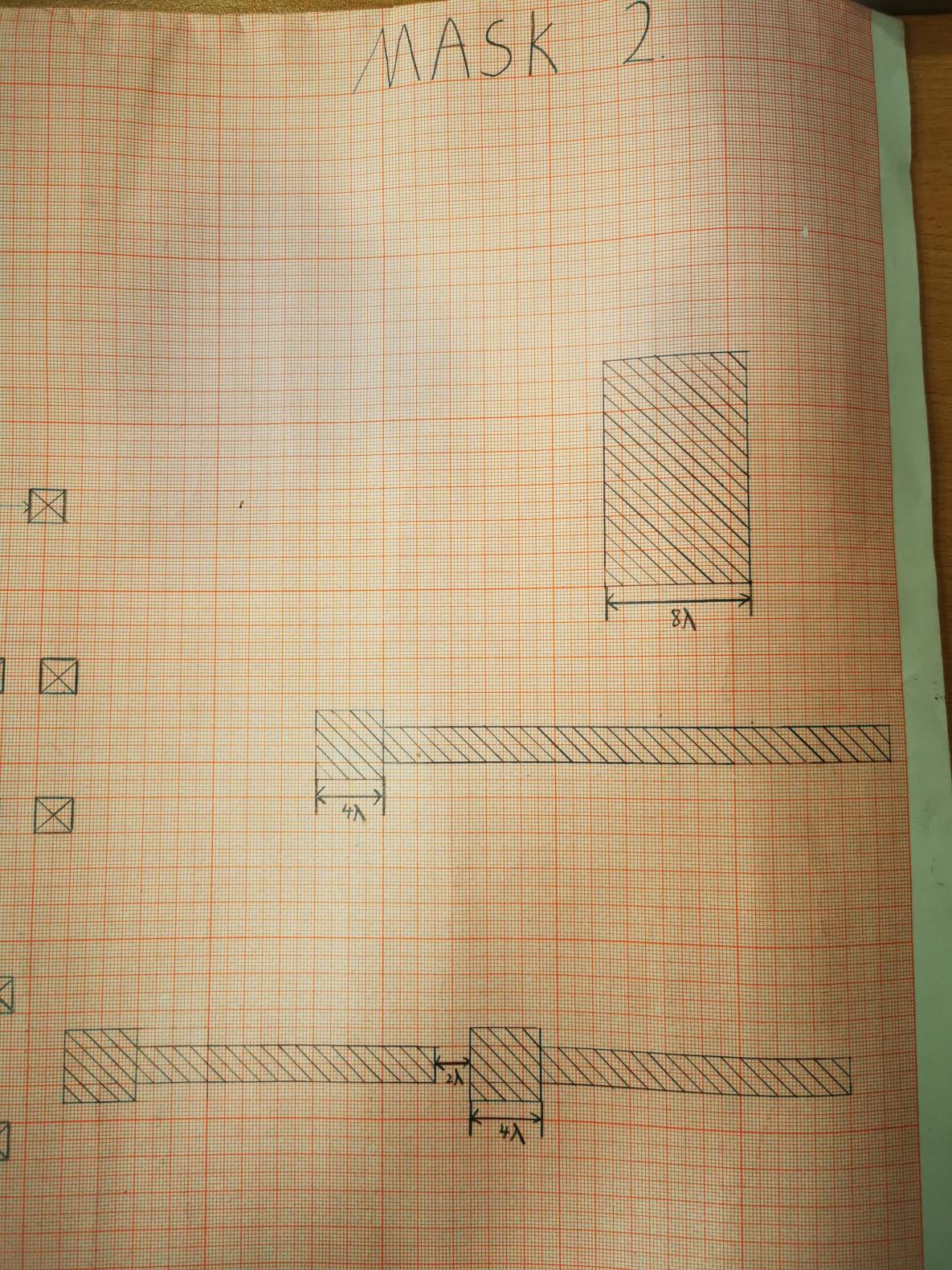


Figure 18: The Mask 2:Poly-Si layer

Mask 2 is the poly-silicon layer. In this layer, we need to draw the poly-silicon part of the full layout. Since for the poly-silicon layer, we still need to consider the design rule. The minimum spacing between two poly-silicon must not be less than 2.

**6.5 The mask 3 of the design**

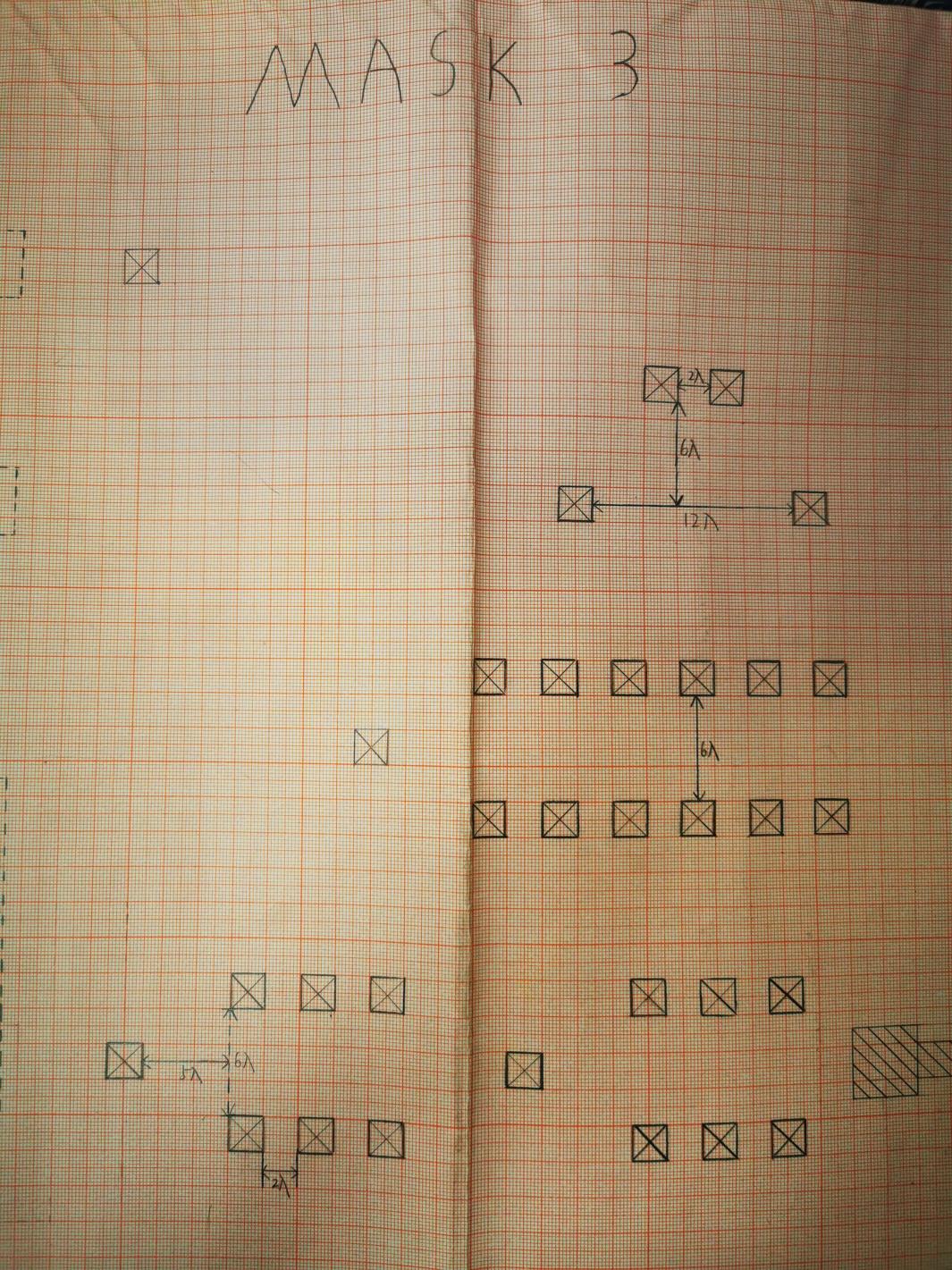


Figure 19: The mask 3: Contact layer

Mask 3 is in the contact layer. We need to put each contact of the Full layout in this layer. After our calculation, in the case of , the W/L of the bottom left two MOSFET is 6, the W/L of the bottom right MOSFET is 12, and the upper Mosfet is 0.5. Therefore, we drew each MOSFET contact according to the results.

**6.6 The mask 4 of the design**

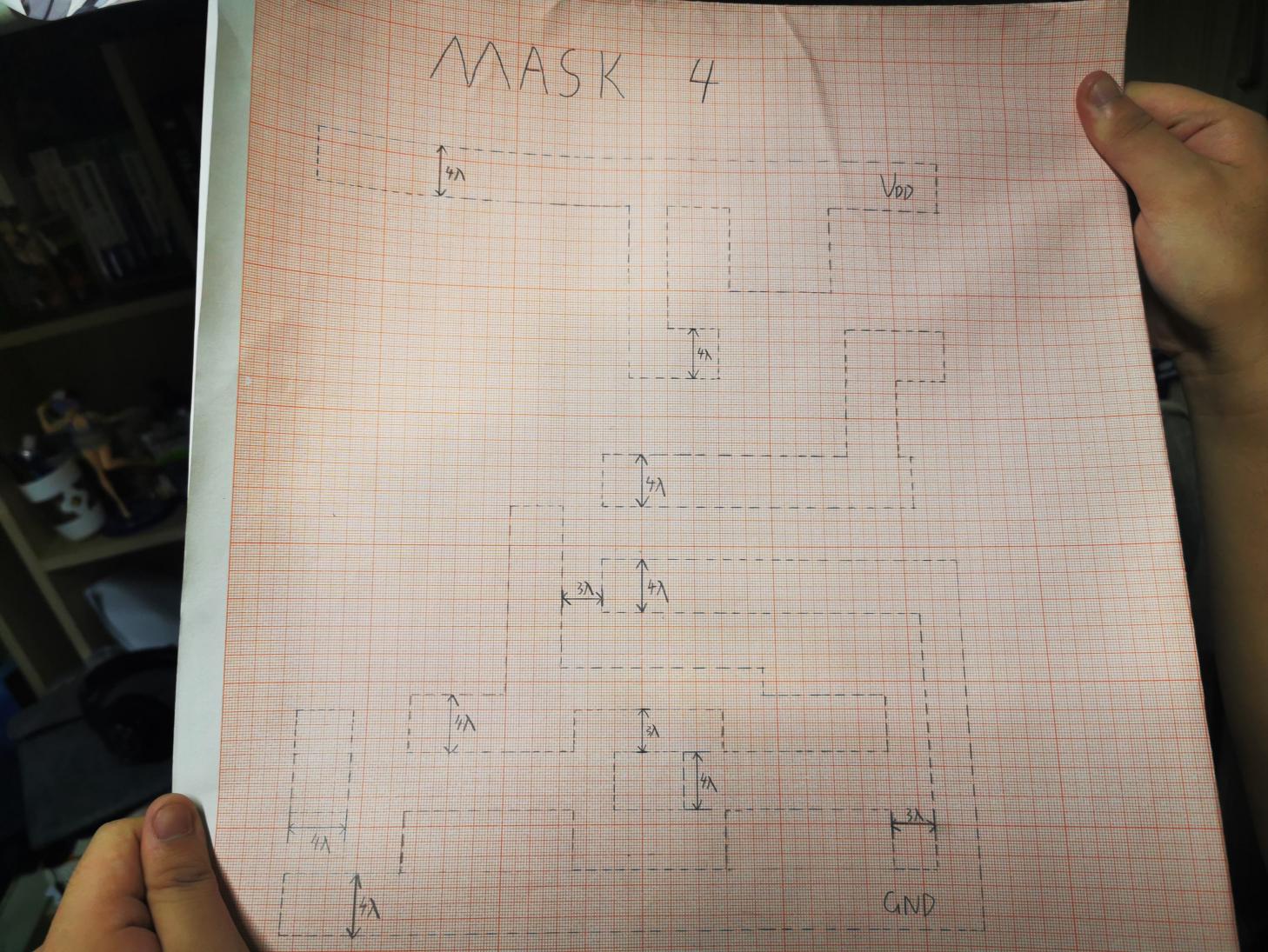


Figure 20: The mask 4: the metal layer

The last layer is the Metal Layer. In this layer, since the GND and VDD parts are both Metal, we need to draw not only the Metal contained in each Mosfet, but also the GND and VDD parts. We also need to pay extra attention to Design rules when drawing the Metal.

1. **Conclusion**

In this task, I learned how to draw the **Integrated circuit**. First of all, we need to pay attention to the **Design Rules** during the drawing process. Each time we draw a Mosfet, we need to consider whether the distance is following design rules in the same layer, and we need to consider the relationship between the other layers. Finally, we successfully drew the whole layout and re-drew each mask. In addition, for each task, we explain it in detail.

For Task 1, we determine that the entire circuit consists of a NOR Gate and a NOT Gate. Finally, after logical analysis of the circuit, the whole circuit forms an **OR** **logic**. The detailed explanation and **Truth table** can be found in this part.

For Task 2, we need to calculate **W/L** for each MOSFET with a different Vout. Since MOSFET has **two modes of working**: Liner mode and Saturation mode. The mode of each MOSFET should be identified and calculated based on the results. The procedure of each calculation and the calculation results can be found in this part.

For Task 3, we need to state the **flow** of the NMOSFET during the manufacturing process. When manufacturing MOSFET, we need a total of **four masks, which are Active Region, Gate, Contact and Metal**. In this section, we explain the top and cross views of each process in each mask. Detailed information can be found in this section.

For Task 4, we first drew the **Full layout** according to the design rule and marked each important distances. For different layers, we also distinguish them through different forms of expression, which will be convenient for the process of designing. After drawing the full layout, we **drew each mask** completely and correctly. Under each Mask, I explained my design without missing the requirements of the Design Rule. The detailed design can be viewed in the task.

Overall, I gained a lot from this design, I learned the correct way to draw an IC. Also, I tried my best to overcome many difficulties when I completed this assignment. Because the hand-drawing process is very attractive to me at this time, I would like to experience the whole IC design process in the future.

1. **Reference List**
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3. Department of Electrical and Electronic Engineering, “ nMOS logic IC design ”, [Online].Available: <https://www.learningmall.cn/pluginfile.php/148597/mod_resource/content/1/10_nMOSIC_Lecture_Gary.pdf>
4. Department of Electrical and Electronic Engineering, “ IC Fabrication Techniques II”, [Online].Available: <https://www.learningmall.cn/pluginfile.php/148597/mod_resource/content/1/10_nMOSIC_Lecture_Gary.pdf>