UNIVERSITY OF LIVERPOOL

Experiment 5 - Design of an Operational Amplifier Using Multisim

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Abstract

In this experiment, an operational amplifier was designed using Multisim software. The designed circuit consisted of four stages, including the Differential amplifier, Emitter follower, Common emitter, and Emitter follower stages. The designed circuit diagram can be viewed in the Circuit connection and the process for calculating resistance values was written in Calculations section. In the results section, all the tasks required for the experiment were completed and all the result figures and comments from the simulation were included. In part III, experiments with phase compensating capacitors were also carried out with corresponding results and comments. In addition, bonus experiment (common-mode signals) was also carried out in the result section. For each design specifications, detailed explanations were also written below the Design specifications table. In addition, two questions on the lab script were answered in detail, and the detailed explanations can be found in the Discussion section. The limitations and recommendations for this experiment can also be found in the discussion section.

Declaration

I confirm that I have read and understood the University's definitions of plagiarism and collusion from the Code of Practice on Assessment. I confirm that I have neither committed plagiarism in the completion of this work nor have I colluded with any other party in the preparation and production of this work. The work presented here is my own and in my own words except where I have clearly indicated and acknowledged that I have quoted or used figures from published or unpublished sources (including the web). I understand the consequences of engaging in plagiarism and collusion as described in the Code of Practice on Assessment.

Contents

1 Introduction

1.1 Background of Operational amplifier

The operational amplifier (Op-amp) is a linear device, which has the basic characteristics required for ideal DC amplification and is therefore widely used for signal conditioning, filtering or performing mathematical operations, including addition, subtraction, integration and differentiation. The structure of operational amplifier is as follows 1:

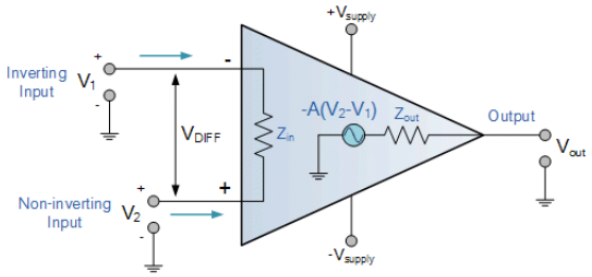


Figure 1: Operational Amplifier Basics [1]

Operational amplifiers generally contain two input and one output ports. One of the inputs is called the inverting input and is marked with a minus sign (-). The other input is called the non-inverting input and is marked with a plus sign (+). In order to realize the function of the operational amplifier, the following parameters need to be satisfied:

1. **Open Loop Gain** A_v

   Open-loop gain is the gain of an operational amplifier without positive or negative feedback. As the main function of an operational amplifier is to amplify the input signal, the greater its open-loop gain, the better its amplification. In addition, some functions of the op-amp can only be achieved when the open-loop gain is large. The open-loop gain in this design should be greater than 500000.

2. **Input impedance** Z_{in}

   The input impedance is the ratio of the input voltage to the input current. The higher the impedance of the input resistor, the lower the error of the operational amplifier. For this experiment, a differential input impedance of more than 100kΩ is required.

3. **Output impedance** Z_{out}

   Output impedance is equivalent to the internal resistance of an operational amplifier. When the value of the output impedance is small, the voltage of the load will be larger. Therefore, the output impedance should be as small as possible. In this simulation, the output resistance is designed to be less than 1KΩ.

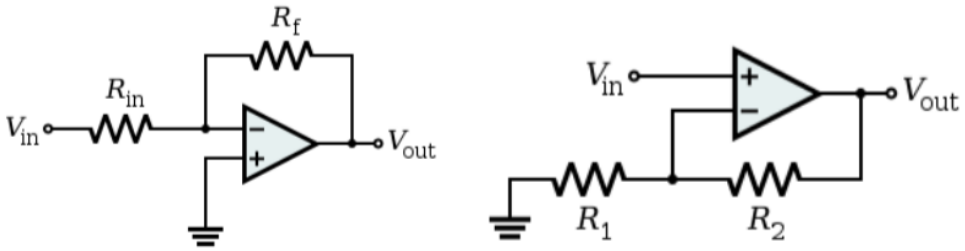
4. **Bandwidth (BW)**

   The ideal op-amp should have a very large frequency response. A relatively high Bandwidth op-amp can amplify signals from DC to relatively high AC frequencies.

5. **Offset Voltage**

The output of the amplifier will be zero when the voltage difference between the inverting and non-inverting inputs is zero or both inputs are grounded. In this simulation, the offset voltage needs to be obtained from the image obtained from the experimental simulation.

Op-amp can be used in different circuits, which include the following circuit:



(a) Inverting amplifier circuit (b) Non-inverting amplifier circuit

Figure 2: Operational amplifier and circuit applications

For inverting amplifier circuit the voltage gain is $A_v = -\frac{R_f}{R_{in}}$. For Non-inverting amplifier circuit the voltage gain is $A_v = 1 + \frac{R_2}{R_1}$. In addition, the op-amp is one type of a differential amplifier. [2]

1.2 Objectives

In this simulation, an operational amplifier was designed using Multisim software. The various parameters need to be satisfied are as follows 1:

Table 1: Design Specification

Parameter	Specification
differential input impedance	>100kΩ
Open loop voltage gain	>500000
Output impedance	<1 k
DC output voltage	≈ 0
DC offset voltage	None given
Frequency response	Down to DC (0 Hz)
Total current consumption	<5 mA
Bandwidth with compensation capacitor	None given

2 Circuit connection and Calculations

2.1 Circuit connection

The design of the operational amplifier consists of four main parts: the differential input stage emitter follower stage, 2 emitter follower stages, common emitter stage, which are shown in the following diagram 3:

In this simulation experiment, Multisim software was used for the construction of the simulation circuit. With reference to the Elec 271 lectures, the following circuit was designed, which contains 4 main parts 4:

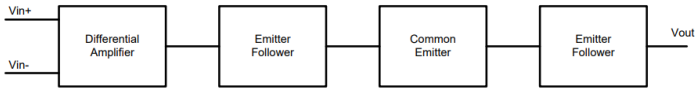


Figure 3: Block diagram of the op-amp [2]

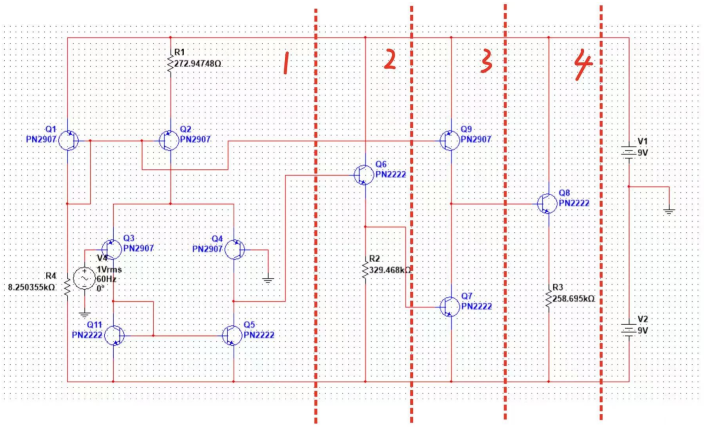


Figure 4: Four stages of the designed circuit

The first and third stages (differential input stage and common emitter) provide two high voltage gains. The second stage (emitter follower) is matched to the gain stage to avoid load effects. And the fourth stage (emitter follower) provides low output resistance for satisfying the requirements.

2.2 Calculations

2.2.1 Obtain the forward beta values for PN2907 and PN2222

A review of Multisim's parameters for two transistors shows that the default the maximum forward beta value for the PN2907 is approximately 232. For the PN2222 transistor, the default the maximum forward beta value is approximately 256. In the next section, the beta values for the two transistors will be simulated and calculated by analyzing experimental diagram and compare them with the actual values. The parameters of the two different transistors are as follows Figure 5

Model

.MODEL MPS3644__BJT_PNP__1 PNP

Tools Views

Na...	Description	Value	Units	Use default
Level	Device model level	Gummel-Poon (Le...		
IS	Transport saturation current	650.6E-18	A	☐
BF	Ideal maximum forward beta	231.7		☐
NF	Forward current emission coefficient	1.0		☑
VAF	Forward Early voltage	115.7	V	☐
IKF	Corner for forward beta high current roll-off	1.079	A	☐
ISE	B-E leakage saturation current	54.81f	A	☐
NE	B-E leakage emission coefficient	1.829		☐

(a) The parameters for PN2907

Model

.MODEL PN2222__BJT_NPN__1 NPN

Tools Views

Na...	Description	Value	Units	Use default
Level	Device model level	Gummel-Poon (Le...		
IS	Transport saturation current	14.34f	A	☐
BF	Ideal maximum forward beta	255.9		☐
NF	Forward current emission coefficient	1.0		☑
VAF	Forward Early voltage	74.03	V	☐
IKF	Corner for forward beta high current roll-off	.2847	A	☐
ISE	B-E leakage saturation current	14.34f	A	☐
NE	B-E leakage emission coefficient	1.307		☐

(b) The parameters for PN2222

Figure 5: The parameters for two transistors

2.2.2 Obtain the resistance of R1

The differential input resistance for the designed circuit is:

$$R_{id} = 2r_{be} = \frac{2\beta_0}{g_m} = \frac{2\beta_0}{40I_c} \tag{1}$$

The bias current in differential amplifier is :

$$I_0 = 2I_c = \frac{2 * 2 * \beta_0}{40R_{id}} \tag{2}$$

Because we assume the input resistance is **110,000**, which is larger than 100,000, and substitute the value of β_0=232 to the Equation 2, we can get:

$$I_0 = 2I_c = \frac{2 * 2 * 232}{40 * 110000} \approx 0.2109mA \tag{3}$$

According to the lecture notes, for Widlar current mirror:

$$I_{ref} = I_0 * e^{\frac{I_0 * R_1}{V_T}} \tag{4}$$

To get the value of R_1, we set:

$$I_{ref} = 10 * I_0 = 2.109mA \tag{5}$$

Then,

$$R_1 = \frac{V_T}{I_0} * \ln 10 \tag{6}$$

Substitute $V_T \approx 25mV$ and I_O=0.2109mA into the Equation 6, we can get:

$$R_1 = \frac{25}{0.2109} * \ln 10 \approx 272.948\Omega \tag{7}$$

2.2.3 Obtain the Resistance of R4

According to the Ohm's Law, the resistance of R4 is:

$$R_4 = \frac{V_{CC} - V_{EE} - 0.6}{I_{ref}} \tag{8}$$

Substitute $V_{CC} = 9V$, $V_{EE} = -9V$ and $I_{ref} = 2.109mA$ into the Equation 8, we can get:

$$R_4 = \frac{9 + 9 - 0.6}{2.109} \approx 8.25K\Omega \tag{9}$$

Or the current I_{ref} can also be calculated by the other method. First,

$$I_O R_1 = V_T * ln(\frac{I_{ref}}{I_O}) \tag{10}$$

We assumed that:

$$I_O R_1 = V_T \tag{11}$$

Then,

$$I_{ref} = I_O * e^1 \approx 0.5733mA \tag{12}$$

According to the Equation:

$$R_4 = \frac{V_{CC} - V_{EE} - 0.6}{I_{ref}} \tag{13}$$

Substitute the Equation 12 to Equation 13:

$$R_4 = \frac{V_{CC} - V_{EE} - 0.6}{I_{ref}} = \frac{18 - 0.6}{0.5733} \approx 30.35K\Omega \tag{14}$$

Note: This is just another algorithm. In my simulation, the resistance value of R_4 would be $8.25K\Omega$, which is calculated by the first method.

2.2.4 Obtain the Resistance of R2

The output resistance of amp stage is:

$$R_O^{DA} = \frac{\frac{V_{AN}}{I_c} * \frac{V_{AP}}{I_c}}{\frac{V_{AN}}{I_c} + \frac{V_{AP}}{I_c}} \tag{15}$$

According to the default parameters, for the transistor PN2907, the forward early voltage is 115.7 and for the transistor PN2222, the forward early voltage is 74.03. Additionally, the current I_c is equal to $0.5I_O$, which is approximately 0.105mA. Substitute early voltages for these two transistors into Equation 15, we can get:

$$R_O^{DA} = \frac{\frac{115.7}{0.105} * \frac{74.03}{0.105}}{\frac{115.7}{0.105} + \frac{74.03}{0.105}} \approx 428.827K\Omega \tag{16}$$

According to the lab script [2], the input impedance for Emitter follower is approximately ten times as large as the output impedance for differential amplifier. That means:

$$R_{in}^{EF} \approx 10 * R_{out}^{DA} = 4288.27K\Omega \tag{17}$$

For the input impedance of CC coupling stage:

$$R_i(CC) = r_{be}(CC) + (1 + \beta_0) * R_2//R_L \tag{18}$$

Because:

$$r_{be}(CC) = \frac{\beta_0}{40I_c} \tag{19}$$

Substitute $I_c = \frac{V_{be}}{R_2}$ into Equation 19, we can get:

$$r_{be}(CC) = \frac{\beta_0 * R_2}{40 * V_{be}} = \frac{256 * R_2}{40 * 0.6} \tag{20}$$

Additionally,

$$R_2//R_L = \frac{R_2 * r_{be}(CE)}{R_2 + r_{be}(CE)} \tag{21}$$

For the same reason, the value for $r_{be}(CE)$ is:

$$r_{be}(CE) = \frac{\beta_0}{40 * I_c} \tag{22}$$

And the value for I_c is calculated by the following equation by using the Ohm's Law:

$$I_c = \frac{V_{CC} - V_{EE} - V_{be}}{R4} = I_c = \frac{9 + 9 - 0.6}{8.2503K\Omega} \approx 2.109mA \tag{23}$$

Substitute the value of I_c into Equation 22, we can get:

$$r_{be}(CE) = \frac{256}{40 * 2.109mA} = 3.035K\Omega \tag{24}$$

Substitute the Equation 17, 20 and 24 into Equation 18,we can get:

$$4288.2K\Omega = \frac{256 * R_2}{40 * 0.6} + (1 + 256) * R_2//3.0346 \tag{25}$$

Solving the equation for 25 yields:

$$R2 \approx 329.468K\Omega \tag{26}$$

2.3 Obtain the resistance of R3

The output resistance of the designed Op-amp is assumed approximately **800**Ω, which is less than 1000 Ω. According to the lecture notes, the output for the CC stage is calculated by the following formula:

$$R_O = \frac{r_{be} + R_s}{1 + \beta_0}//R_E \tag{27}$$

Where, R_s is the output resistance of the CE stage. Therefore,

$$R_s = r_{ce}(npn)//r_{ce}(pnp) = \frac{\frac{V_{AN}}{I_c} * \frac{V_{AP}}{I_c}}{\frac{V_{AN}}{I_c} + \frac{V_{AP}}{I_c}} \tag{28}$$

Because the current mirror is formed, the value of I_c in Emitter follower(Q7) is approximately to I_c in transistor Q1. Additionally, the current I_c in Q1 is equal to I_{ref}, which means:

$$I_c \approx 2.109mA \tag{29}$$

Substitute the Equation 29 into the Equation 28, we can get:

$$R_s = r_{ce}(npn)//r_{ce}(pnp) = \frac{\frac{115.7}{2.109mA} * \frac{74.03}{2.109mA}}{\frac{115.7}{2.109mA} + \frac{74.03}{2.109mA}} \approx 21.497K\Omega \tag{30}$$

The resistance $r_{be}(CC)$ calculated by the following formula:

$$r_{be}(CC) = \frac{\beta_0}{40 * I_c} = \frac{256}{40 * I_c} \tag{31}$$

We assumed the output voltage is approximately 0V, then:

$$R_E = \frac{V_{EE} - 0V}{I_c} = \frac{9}{I_c} \tag{32}$$

Substitute Equation 30, 31, 32 into 27, we can get:

$$0.8 = \frac{\frac{256}{40*I_c} + 21.497}{256} // \frac{9}{I_c} = \frac{\frac{\frac{256}{40*I_c}+21.497}{256} * \frac{9}{I_c}}{\frac{\frac{256}{40*I_c}+21.497}{256} + \frac{9}{I_c}} \tag{33}$$

Solving the equation for 33 yields:

$$I_c(CC) \approx 0.03479mA \tag{34}$$

Apply Ohm's law:

$$R3 = \frac{9}{Ic} \approx 258.695K\Omega \tag{35}$$

3 Results

3.1 Part I: Transistor output characteristics

In order to calculate the resistance correctly in the experiment, we need to obtain the output characteristics and various parameters of the two Transistors. Among them, the value of β can be calculated from the output characteristic curve of the transistor. Also, by extending the output characteristic curve, the transistor's early voltage can be obtained. The specific calculation is as follows.

3.1.1 Obtain the forward beta β

First, the DC current gain β is calculated as follows 36:

$$\beta = \frac{I_C}{I_B} \tag{36}$$

Additionally, according to the lecture notes, the formula to calculate the AC current gain β_0 can be seen as follows 37:

$$\beta_0 = \frac{\triangle I_C}{\triangle I_B} \tag{37}$$

After building the circuit according to the lab script [2], we calculated the β of the transistor PN2222 by taking I_c to be approximately equal to 2mA, and the circuit diagram was built as follows 6:

The specific DC Transfer Characteristic is shown below 7 :

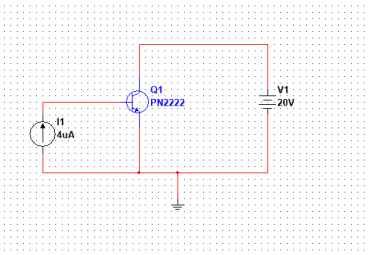


Figure 6: The circuit for PN2222

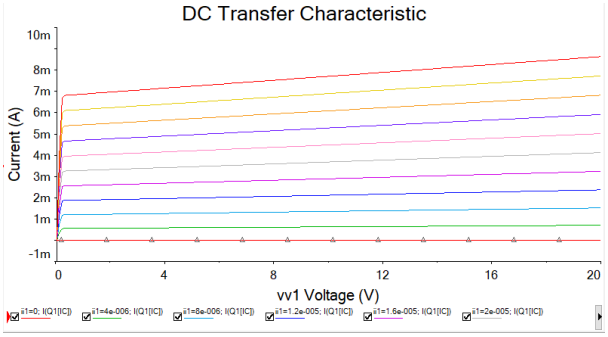


Figure 7: DC transfer characteristic for PN2222

When I_c is approximately equal to 2mA, I_B is approximately equal to 12uA. According to the formula 36

$$\beta = \frac{I_C}{I_B} = \frac{2mA}{12uA} \approx 167 \tag{38}$$

Alternatively, to calculate the ac current gain, two curves $I_B = 8uA$ and $I_B = 12uA$ are considered, according to the equation 37:

$$\beta_0 = \frac{\triangle I_C}{\triangle I_B} = \frac{1.924mA - 1.2334mA}{12uA - 8uA} = 172.65 \tag{39}$$

Similarly, we replace the transistor PN2222 with PN2907. The resulting circuit diagram is as follows 8:

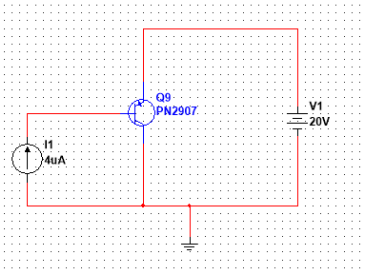


Figure 8: The circuit for PN2907

The specific DC Transfer Characteristic is shown below 9:

When I_c is approximately equal to -2mA, I_B is approximately equal to 8uA. According to the formula 36:

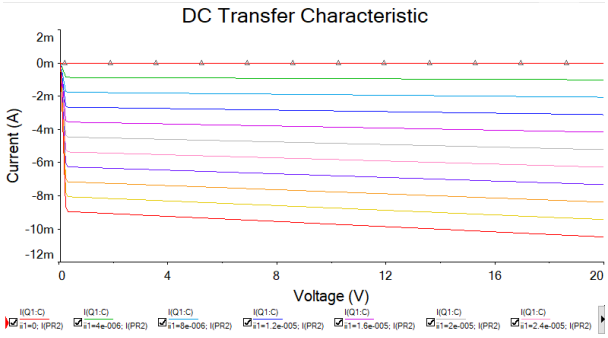


Figure 9: DC transfer characteristic for PN2907

$$\beta = \frac{I_C}{I_B} = \frac{2mA}{8uA} = 250 \tag{40}$$

Alternatively, to calculate the ac current gain, two curves $I_B = 8uA$ and $I_B = 12uA$ are considered, according to the equation 37:

$$\beta_0 = \frac{\triangle I_C}{\triangle I_B} = \frac{-1.8069mA - (-2.7279mA)}{12uA - 8uA} = 230.25 \tag{41}$$

By comparing the β values with valued obtained from the parameter table 5, we found that the β of the two groups were not exactly equal, probably because of the inaccurate selection of points in the calculation of β from the transfer characteristic curve. Since the curve of the saturation region is not a constant value, using different points to calculate β may affect the results of the calculation. Furthermore, since Multisim's transistor parameters only provide the maximum β value, it is quite normal for the experimentally calculated β value to be less than the maximum. However, for experimental convenience, the maximum value of β is used in the calculation process.

3.1.2 Obtain the early voltage

The Early effect is the change in the effective width of the base in a bipolar junction transistor (BJT) due to a change in the applied base-to-collector voltage. The voltage at the point of intersection of the tangent line of the output characteristic curve backwards with the x-axis is called early voltage. The following figure 10 shows the method :

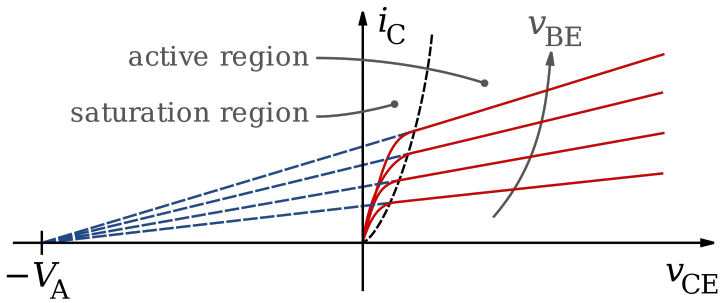


Figure 10: The Early voltage V_A [3]

In our simulations, according to the above figure 5 of the two transistor's parameter table. The PN2222 has an early voltage value of approximately 74.03 V and the PN2907 has an early voltage of

approximately 115.7 V.

3.2 Part II: Achieving the specification of the operational amplifier

3.2.1 Task-1

By calculating the resistance of the four resistors, the circuit design has been completed. In addition, the following requirement is also achieved:

$$R_{in}^{EF} = 10 * R_{out}^{DA} \tag{42}$$

The final designed circuit diagram is as follows 11

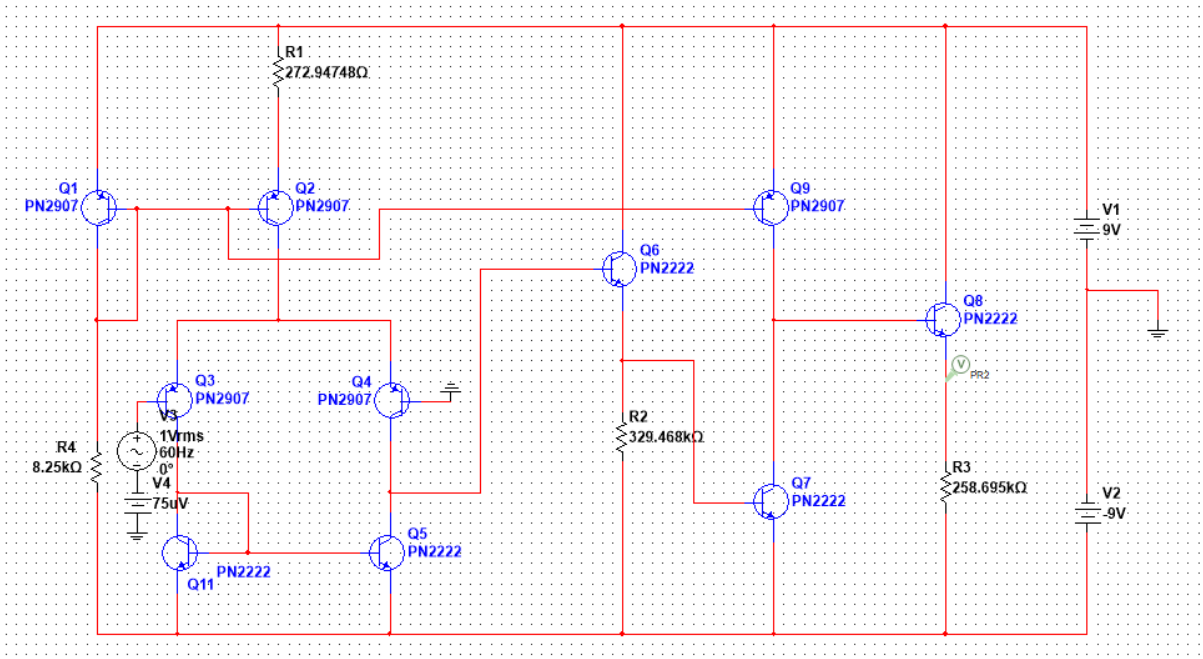


Figure 11: Complete operational amplifier in Mulisitm

This circuit diagram includes the setting of DC offset, the exact value of DC offset can be viewed in the following task. As can be seen from the above figure, the first stage is the differential amplifier. The second and fourth stages are the Emitter follower and the third stage is the Common Emitter. Differential amplifier stage and Common Emitter stage will provide the high voltage gains for the circuit. The second stage (Emitter follower) is responsible for matching the gain stages to avoid loading effects. The fourth stage (Emitter follower) is responsible for providing a lower output resistance. In our design, the output resistor is 800Ω and input resistance is set to $110,000\Omega$.

3.2.2 Task-2

In the simulation, a signal source is connected to the left side of the differential amplifier and the other input port is grounded. In the DC sweep window, the voltage range is set from -9V to 9V and the increment value is set to 0.01V. The final circuit diagram and the parameters are as follows 12:

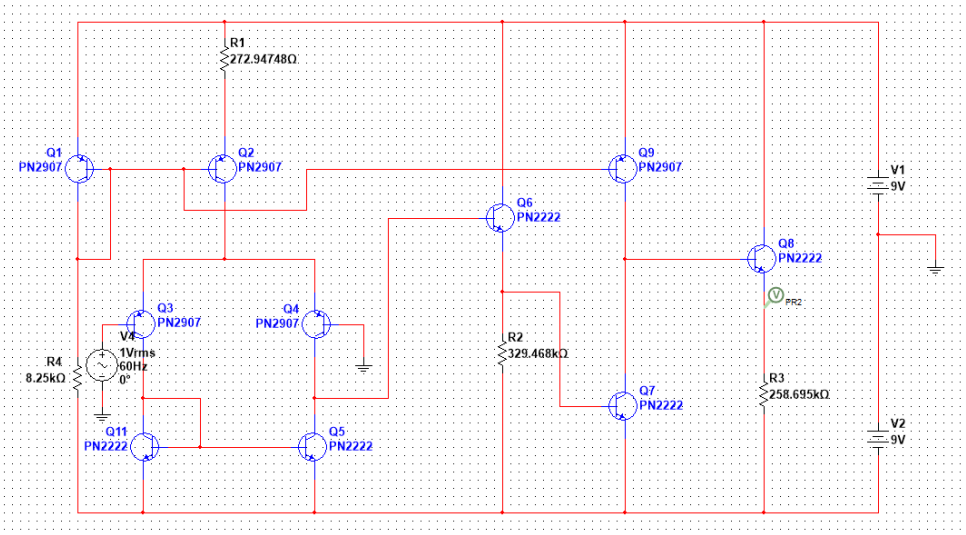


Figure 12: The designed circuit for task 2

As can be seen from the figure above, the signal source is connected to the left of the differential amplifier. Since this signal does not regulate the DC sweep, the parameters need to be set in the Analysis and simulation window. In the voltage range of -9V to 9V, the following output is obtained:

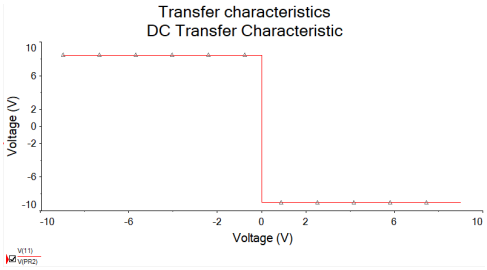


Figure 13: Transfer characteristics of amplifier by performing a DC Sweep from -9V to 9V

Due to the relatively large voltage range of the input, the range of the amplification in the middle is not clearly observable. Therefore, a **narrow the sweep range** is needed to obtain a more accurate voltage amplification range. After changing the voltage range several times, the small voltage range is found with the following specific parameters:

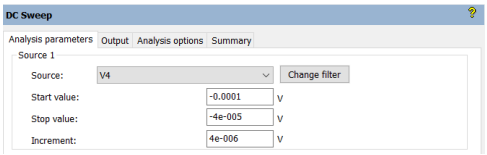


Figure 14: Accurate parameters for DC Sweep

After adjusting the voltage range, a relatively accurate transfer characteristics curve was obtained. The specific curve is as follows 15:

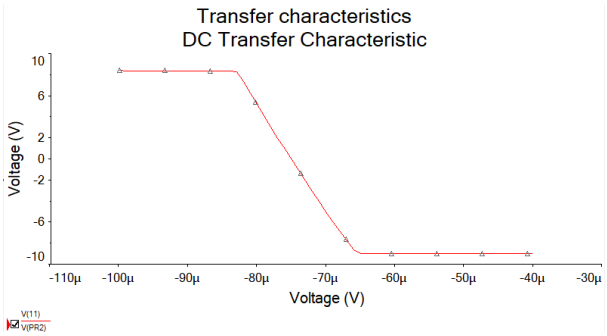


Figure 15: An accurate voltage sweep range

As can be seen from the figure 15, the amplification range of the circuit is about from -84uV to 64uV. Since the centre line of the amplification area of the circuit does not coincide with the y-axis, which means that the output signal has a voltage offset, a DC offset need to be designed to balance the amplifier in the next task.

3.2.3 Task-3

The simulation figure with data for the DC sweep on the narrowed range can be seen as follows:

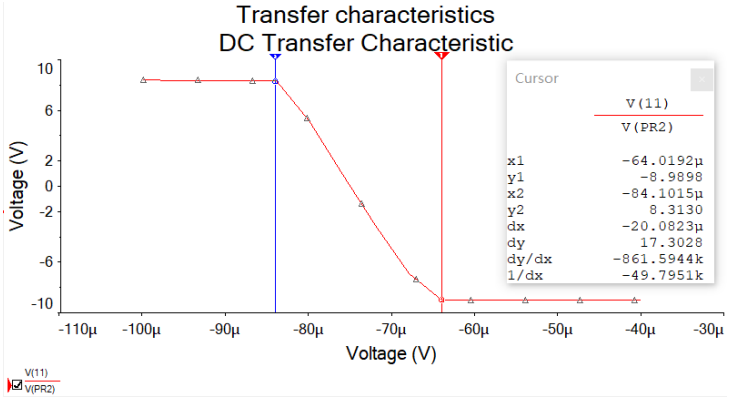


Figure 16: DC sweep on narrowed range with data

The open loop voltage gain can be obtained by the ratio of δy over δx. In this experiment, voltage gain can be calculated by dividing the output voltage difference by the input voltage difference in the amplification range. The specific calculation formula is as follows 43

$$A_{ol} = \frac{y_1 - y_2}{x_1 - x_2} \tag{43}$$

Substituting the data yields:

$$|A_{ol}| = \left|\frac{y_1 - y_2}{x_1 - x_2}\right| = \left|\frac{-8.9898 - 8.3130}{-64.0192u - (-84.1015u)}\right| \approx |-861594.5385| = 861594.5385 \tag{44}$$

The voltage gain of the designed circuit is greater than 500000 (861594>500000), which meets the design requirements. Alternatively, we the curve for voltage gain can be derived directly, which can be seen as follows:

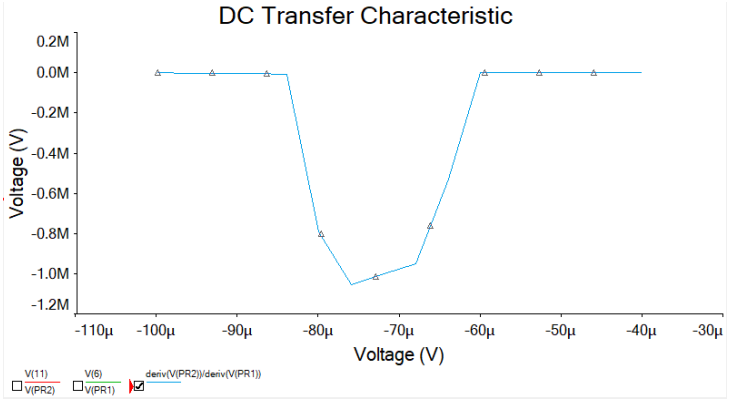


Figure 17: Open loop voltage gain

As can be seen from the figure above, the direct voltage gain is very close to the open loop voltage gain from previous calculation. The maximum voltage gain is close to 1,000,000, which is also greater than the 500,000 required for the experiment. Since the voltage gain in Figure 16 will not be the same at different points in the amplification region, which is probably because the characteristic curve is not perfectly **linear**. The voltage gain calculated from the slope is the average voltage gain in the amplification region, which leads that the voltage gain at different voltages in Figure 17 is not equal.

3.2.4 Task-4

Due to the complex circuit design, a relatively small DC offset voltage may be generated and this offset DC voltage should be balanced as much as possible in order to facilitate the experiment. As can be seen from Task 3, the DC transfer characteristic curve shows a voltage offset. Since the centre of the transfer characteristic curve obtained in the previous circuit does not correspond to a horizontal coordinate of 0, a DC offset need to be set to shift the curve to the right. The value of the DC offset can be determined from the horizontal coordinate of the centre of the amplification range curve. The centre point has the following horizontal coordinates

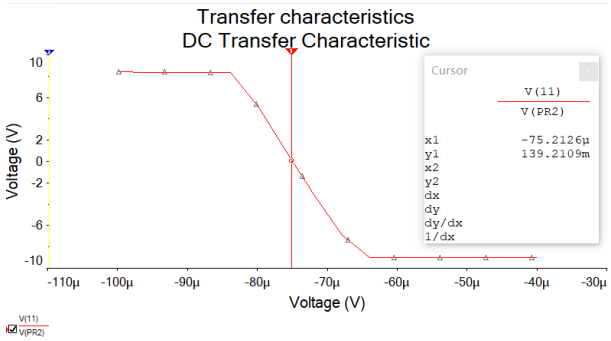


Figure 18: The horizontal coordinates corresponding to the centre of the curve

Since the centre point has a horizontal coordinate of (-75.212u,0), we need to set a DC offset of 75.212uV to shift the curve. The circuit diagram for adding DC offset is as follows 19.

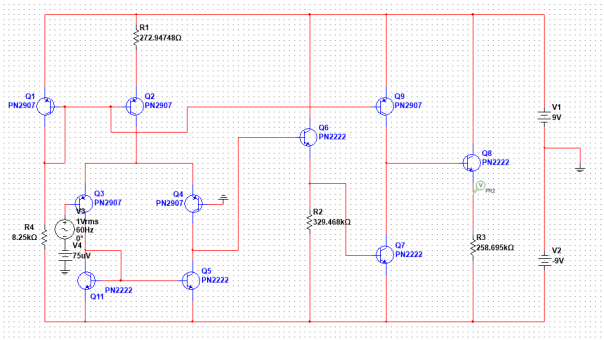


Figure 19: New designed circuit with DC offset

With the above circuit, the following new Transfer characteristic curve can be obtained:

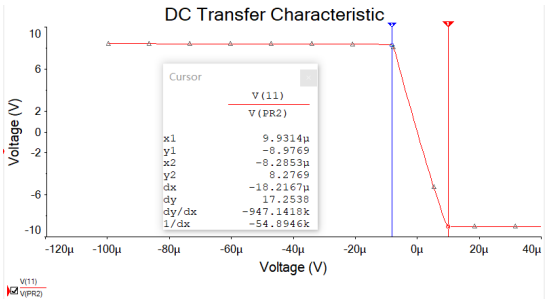


Figure 20: Transfer characteristic with DC offset

The figure shows that the centre of the curve has a horizontal coordinate of approximately 0. After above analysis, the required dc voltage offset is close to 75.212uV, and after setting this offset value, the requirement (centre the output close to zero volts) is satisfied. Also, as can be seen from the above figure, the addition of DC offset changes the amplification range of the circuit to a range of -8.2853uV to 9.9314uV.

3.2.5 Task-5

For this task, the function of Transient need to be used and designed circuit is as follows (with DC offset) 21:

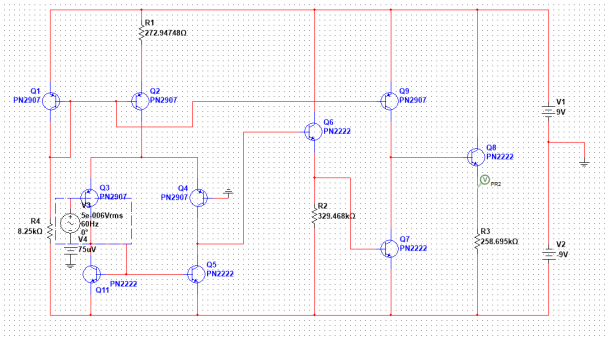


Figure 21: The circuit for Task 5

With the addition of DC offset, the amplification range is from -8.2853uV to 9.9314uV. Since only RMS values can be input in the experiment, the maximum and minimum values of the waveform should be within the amplification range in order to ensure that all waveforms are in the amplification range. The relationship between the maximum value of the waveform and the RMS value is:

$$\sqrt{2}V_{RMS} = |V_{max,min}| \tag{45}$$

Substituting the -8.2853uV gives the maximum RMS value:

$$V_{RMS(max)} = \left| \frac{1}{\sqrt{2}} * (-8.2853uV) \right| \approx 5.8585uV \tag{46}$$

In order to minimise the error, a set of input RMS values: 1uV,3uV,5uV are chosen for the experiment. As the frequency of the AC power is set at 60Hz, the End time is chosen to be 0.083s in order to ensure a sufficient period. The specific Transient window parameters are designed as follows.

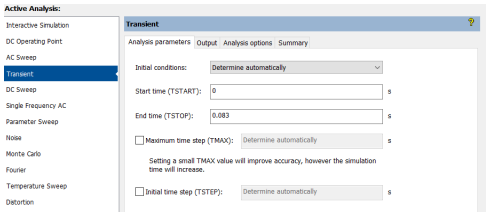


Figure 22: Transient parameters

The result for 1uV input RMS voltage of the experiment is 23 :

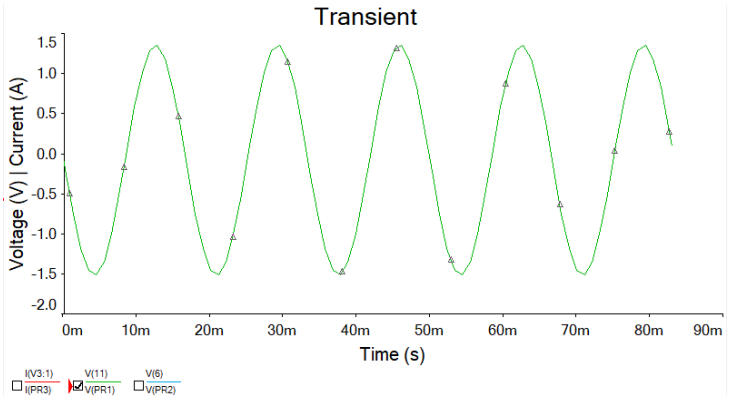


Figure 23: The output waveform in 1uV RMS voltage from transient simulation

In calculating the gain of the amplifier, the points of maximum value of the output and input waveform are chosen. The maximum value of the output waveform is approximately 1.35V and the maximum value of the input waveform is $\sqrt{2} * 1uV \approx 1.41uV$. Therefore, the gain can be calculated:

$$A_{ol} = \frac{output_{max}}{input_{max}} = \frac{1.35V}{1.41uV} \approx 957446 \tag{47}$$

The result for 3uV input RMS voltage of the experiment is 23 :

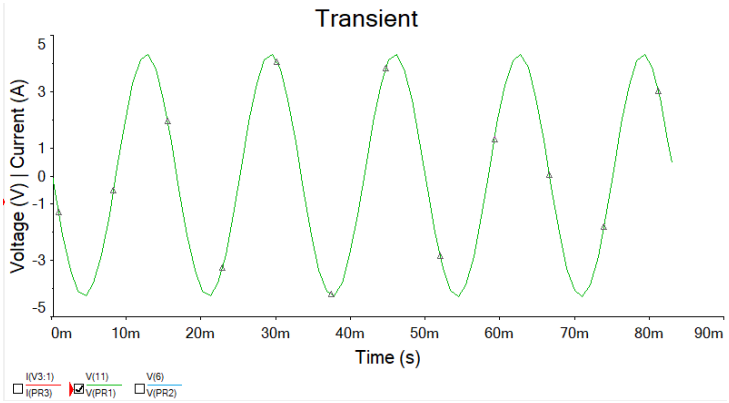


Figure 24: The output waveform in 3uV RMS voltage from transient simulation

In calculating the gain of the amplifier, the points of maximum value of the output and input waveform are chosen. The maximum value of the output waveform is approximately 4.28V and the maximum value of the input waveform is $\sqrt{2} * 3uV \approx 4.24uV$. Therefore, the gain can be calculated:

$$A_{ol} = \frac{output_{max}}{input_{max}} = \frac{4.28V}{4.24uV} \approx 1009433 \tag{48}$$

The result for 5uV input RMS voltage of the experiment is in the following figure 25:

In calculating the gain of the amplifier, the points of maximum value of the output and input waveform are chosen. The maximum value of the output waveform is approximately 7.26V and the maximum value of the input waveform is $\sqrt{2} * 5uV = 7.07uV$. Therefore, the gain can be calculated:

$$A_{ol} = \frac{output_{max}}{input_{max}} = \frac{7.26V}{7.07uV} \approx 1026874 \tag{49}$$

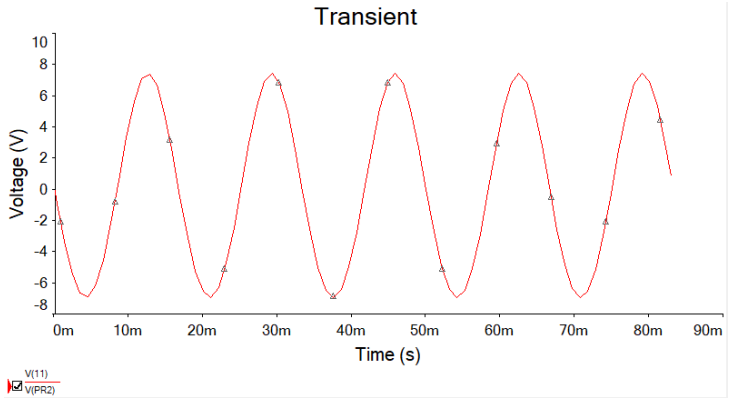


Figure 25: The output waveform in 5uV RMS voltage from transient simulation

The three different sets of input voltages and their corresponding voltage gain have been arranged as follows 2:

Table 2: Three different sets of input voltages and corresponding voltage gain

Max input voltage(uV)	Max Output(V)	Voltage gain
1.41	1.35	957446
4.24	4.28	1009433
7.07	7.26	1026874

As can be seen by 17, different input voltages correspond to different voltage gains, which results in unequal amplifications for all three sets of experiments. However, the gains of the three sets of experiments above are all very close to each other, which is as expected. The average voltage gain of the three sets of data is calculated to be 997917. As the minimum open loop voltage gain required for the experiment is 500000, the designed circuit achieved the gain required for the experiment.

In addition, for experimental accuracy, an experiment beyond the maximum amplified voltage is also carried out. An input voltage of 15uV is used and the results will be:

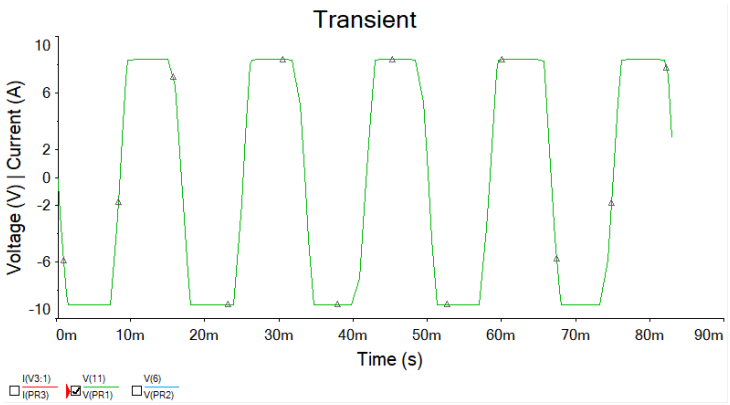


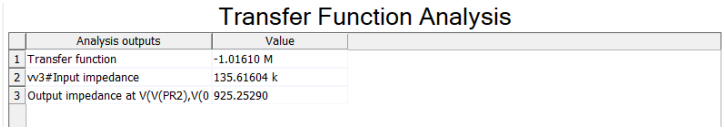
Figure 26: The output waveform in 15uV RMS voltage from transient simulation

As can be seen from the figure, the curve becomes flat at the higher part of each period of the curve, which is because the circuit has a limit on the maximum voltage value that can be amplified. Once the

input voltage value exceeds the maximum voltage, then the voltage in excess will not be amplified. The maximum voltage value obtained after amplification cannot exceed the voltage of the supply DC and the maximum voltage is the DC voltage.

3.2.6 Task-6

The result of the transfer function simulation is as follows:



Transfer Function Analysis

	Analysis outputs	Value
1	Transfer function	-1.01610 M
2	vv3#Input impedance	135.61604 k
3	Output impedance at V(V(PR2),V(0	925.25290

Figure 27: Transfer Function simulation

1. **For voltage gain**

   As the voltage gain required by the experiment is greater than 500000, the transfer function simulation shows a voltage gain of approximately 10161000, which is much greater than 500000. The voltage gain calculated from the transfer characteristic curve in the previous tasks is also approximately equal to the value from the transfer function simulation. The voltage gain of the circuit satisfies the experimental requirements. In addition, the voltage gain obtained from the transfer function simulation and the other tasks are also relatively close. Alternatively, the calculated voltage gain matches the voltage gain obtained by the transfer function. The specific calculation process can be seen in this part.

2. **For input impedance**

   The experimental requirement for differential impedance is greater than 100KΩ, and the simulated value is 135.6160KΩ, which means that the input impedance satisfies the experimental requirement. The input impedance in the circuit is designed to be 110KΩ, which is also closer to the design value. There is an error between the designed resistor values and the real simulated input resistor values, but the error is within acceptable limits. The error may be due to the fact that some resistances, such as $r_{bb'}$ and $r_{b'c}$, which have been ignored in the calculations. A more detailed error analysis can be found in the discussion section.

3. **For output impedance**

   The output impedance required for the experiments is less than 1KΩ. The value of output impedance by the transfer function simulation is approximately 925Ω, which fulfils the requirements of the experiment. The output impedance in the process of calculation is assumed to 800Ω and the difference between the simulated and designed impedance is small and within the experimental requirements. Again, the output resistance obtained from the transfer simulation differs from the assumed resistance value, but the error between the two is still within an acceptable range. The error in the resistance may also be due to the fact that some resistances have been ignored in the calculations. Similarly, the detailed error analysis for this section will be in the Discussion section.

To calculate the gain of Operational amplifier, the voltage gain for each stage has to be calculated separately and finally summed up to get the voltage gain of the whole circuit.

1. **Calculate the voltage gain of the differential amplifier**

   According to the lecture notes, the voltage gain for single output is:

$$A_d = -20 * I_O * R_C \tag{50}$$

   Where I_C is the calculated in the above section, which is about 0.2mA. For R_c, because the active load replaced the resistor in the differential amplifier stage, the value of R_c will be approximately equal to:

$$R_C = r_{ce4}//r_{ce5}//R_L \tag{51}$$

   Where the value of R_L is the input impedance of the emitter follower, which is about $4288.2K\Omega$. The formula to calculate the $r_{ce4}//r_{ce5}$ will be :

$$r_{ce4}//r_{ce5} = \frac{\frac{V_{AN}}{I_c} * \frac{V_{AP}}{I_c}}{\frac{V_{AN}}{I_c} + \frac{V_{AP}}{I_c}} \tag{52}$$

   Substituting the data yields:

$$r_{ce4}//r_{ce5} = \frac{\frac{115.7}{0.105mA} * \frac{74.03}{0.105mA}}{\frac{115.7}{0.105mA} + \frac{74.03}{0.105mA}} \approx 428.8K\Omega \tag{53}$$

   Substituting Equation 53 into Equation 51 yields

$$R_C = r_{ce4}//r_{ce5}//R_L = 428.8K\Omega//4288.27K\Omega \approx 389.89K\Omega \tag{54}$$

   Substituting Equation 54 into 50 yields

$$A_d = -20 * I_O * R_C = -20 * 0.2mA * 389.89K\Omega \approx -1559.56 \tag{55}$$

2. **Calculate the voltage gain of the first emitter follower**

   The formula to calculate the voltage gain is:

$$A_v = \frac{g_m R_2//r_{be}(CE)}{1 + g_m R_2//r_{be}(CE)} \tag{56}$$

   According to the current mirror, the current I_E flowing through transistor Q7 is approximately 2.1mA. According to the following equation, the base current of Q7 can be calculated:

$$I_B = \frac{I_c}{1+\beta} = \frac{2.1mA}{255.9+1} \approx 8.17uA \tag{57}$$

   In addition, the current flowing through R_2 is

$$I_{R_2} = \frac{0.6V}{329.468K\omega} \approx 1.82uA \tag{58}$$

   The sum of the two currents is I_E of Q6. Therefore, the value of I_E is 9.99uA. The relationship between I_E and I_c gives:

$$I_{c6} = \frac{\beta}{1+\beta} * I_E \approx 9.95uA \tag{59}$$

Therefore, the resistance of r_{be} is:

$$r_{be} = \frac{\beta}{40 * I_c} = \frac{255.9}{40 * 2.109mA} \approx 3.033K\Omega \tag{60}$$

Substituting 60 and 59 into 56 yields:

$$A_v = \frac{g_m R_2 // r_{be}(CE)}{1 + g_m R_2 // r_{be}(CE)} = \frac{40 * 9.95uA * 3.03K\Omega // 329K\Omega}{1 + 40 * 9.95uA * 3.03K\Omega // 329K\Omega} \approx 0.5 \tag{61}$$

3. **Calculate the voltage gain of the common emitter amplifier**

   According to the hints, the formula to calculate the voltage gain of common emitter will be :

$$A_v = \frac{1}{V_T} * \frac{V_{An} * V_{Ap}}{V_{An} + V_{Ap}} = \frac{1}{25mV} * \frac{115.7 * 74.03}{115.7 + 74.03} \approx 1805 \tag{62}$$

4. **Calculate the voltage gain of the second emitter follower**

   Since this stage's circuit is a typical common follower circuit, according to the lecture notes, the voltage gain of this circuit is approximately equal to 1.

After summing up the different voltage gains of the four stages above, the final voltage gain will be:

$$A_v = A_{v1} * A_{v2} * A_{v3} * A_{v4} = -1559.56 * 0.5 * 1805 * 1 \approx -1407502 \tag{63}$$

As explained above, the calculated voltage gain is slightly higher than the voltage gain obtained by the transfer function because the effects of some capacitors and resistors are ignored in the calculation.

3.2.7 Task-7

In this section, the current display, voltage display and power display are shown separately. The current display is shown schematically as follows 28:

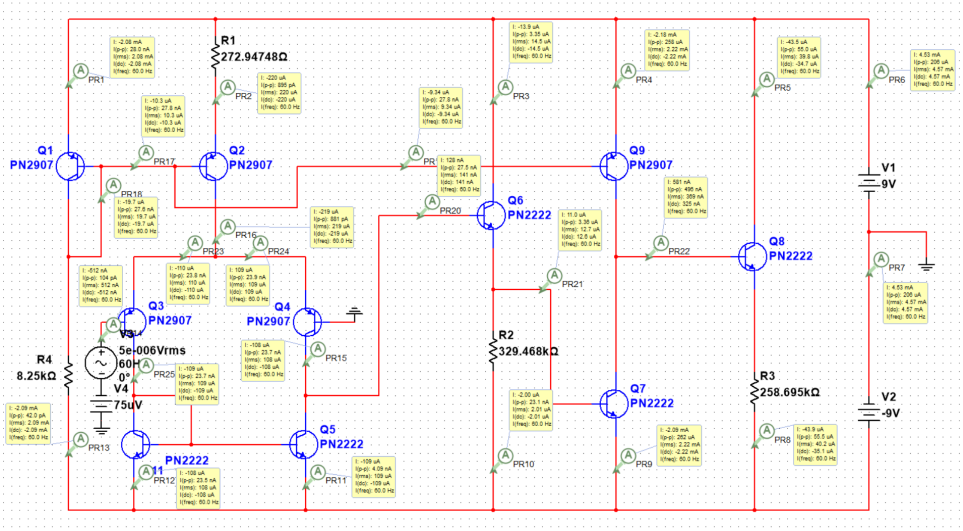


Figure 28: The schematic diagram with current probes

As can be seen from the figure 28, the DC currents of PR1 and PR4 are essentially equal. As the circuit forming a current mirror, the equal currents are as expected. The assumption of $I_{ref} = 10 * I_O$ made in the calculation is also verified in the figure. In addition, the total current consumption is approximately 4.57mA, which is less than maximum current required for the experiment(5mA). The voltage is shown schematically as follows 29:

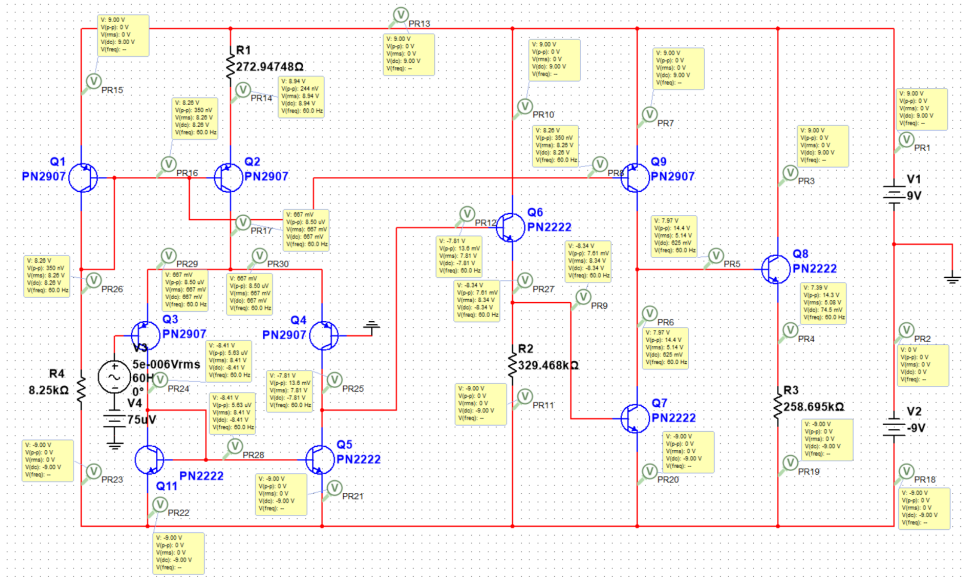


Figure 29: The schematic diagram with voltage probes

As can be seen from the figure above 29, when the RMS voltage of the input voltage is 5uV, the RMS value of the output voltage is 5.08V. Therefore, according to the formula, the voltage gain of the circuit is: $A_v = \frac{5.08V}{5uV} \approx 1016000$, which is consistent with the results obtained previously.

A schematic of the power demonstration is shown below 30:

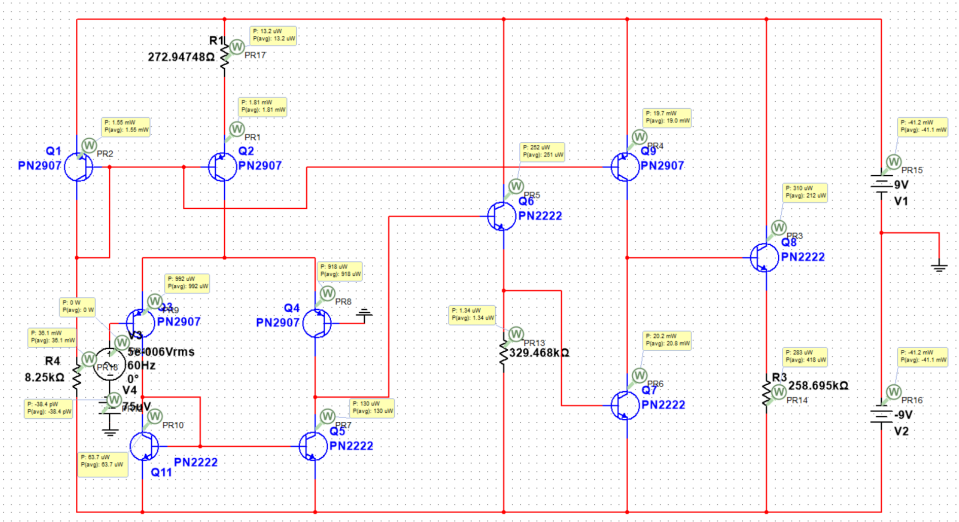


Figure 30: The schematic diagram with power probes

Both DC power supplies consume 41.1mW, which meets the requirements of the experiment. Also, as a whole, the power consumed by each component is relatively small.

3.3 Part III: Obtaining the frequency response of the designed amplifier

3.3.1 Task-1

The results for the frequency response of the amplifier can be seen as follows:

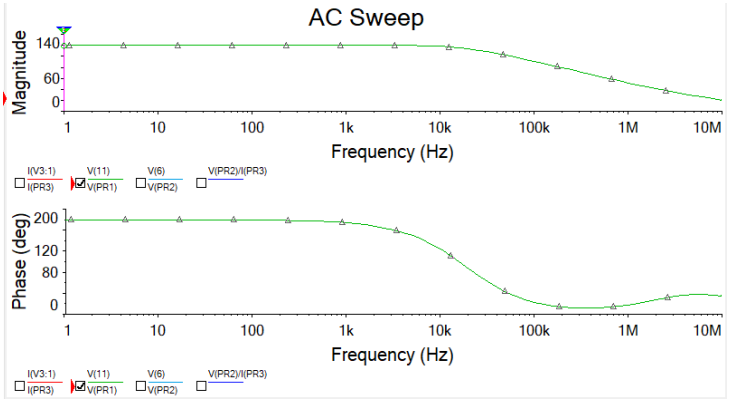


Figure 31: The frequency response

As can be seen from the above diagram of AC sweep, for the Magnitude part of the bode plot, the magnitude remains stable in the frequency range 0-10kHz, with a value of approximately 120dB. After 10KHz, the magnitude decreases as the frequency increases. In addition, the bandwidth is defined as the 3dB points on the bode plot. [4] Thus, from the first Magnitude plot, the bandwidth can be derived to be about 12KHz.

For the part of phase part, the value of phase nearly remains constant in the frequency range 0-1KHz, at about 180 degree. In the frequency range 1K-100KHz, the phase gradually decreases and tends

to 0 degree. In the frequency range 100KHz-10MHz, the degree of phase gradually increases again. Additionally, the circuit system has a positive gain and phase margin according to the method for finding the gain margin and phase margin presented in the lecture. The process of calculating the specific phase margin and gain margin can be seen in the discussion section.

Alternatively, the input impedance can be calculated according to the following equation.

$$Input_{impedance} = \frac{V_{input}}{I_{input}} \tag{64}$$

The bode plot obtained is as follows:

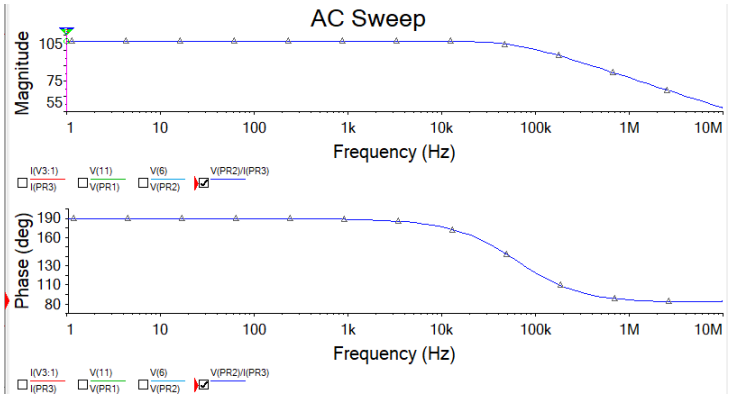


Figure 32: The input impedance

As can be seen from the above figure, for the Magnitude part, when the frequency range is 0-10KHz, the magnitude remains constant at 102dB. When the frequency range is 10KHz-10MHz, the value of magnitude decreases gradually.

For the phase part, the value of phase is 180 degrees when the frequency range is 0-1KHz, and gradually decreases to 93 degrees when the frequency range is 1KHz-1.5MHz. In the frequency range of 1.5MHz-10MHz, the phase remains essentially at 93 degrees.

3.3.2 Task-2

After adding a 30pF phase compensating capacitor between the collector of the common emitter stage and the base of the first emitter follower, the following new circuit can be designed:

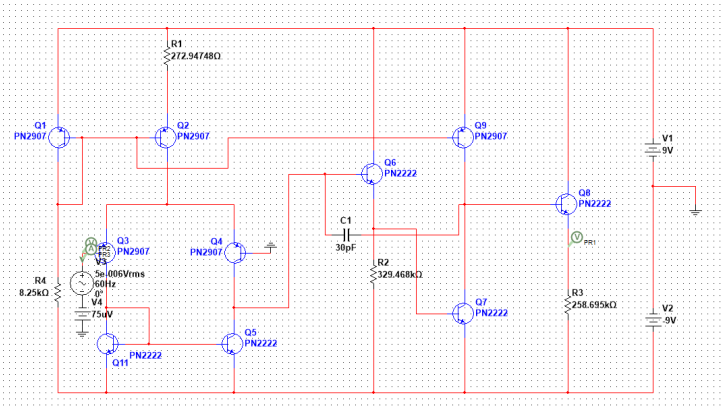


Figure 33: New circuit with phase compensating capacitor

The following frequency response can be obtained by repeating the operations of the previous task:

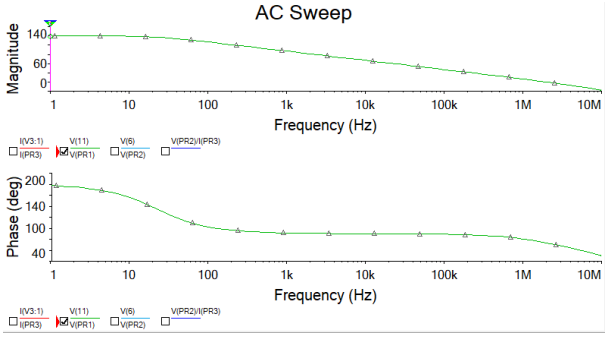


Figure 34: Frequency response with phase compensating capacitor

For magnitude part, the magnitude remains constant at frequencies of 1-10Hz, with a value of approximately 120dB. As the frequency becomes greater than 10Hz, the magnitude gradually decreases. At a frequency of 10 MHz, the magnitude is minimised to approximately 2dB. According to the definition, when $f = f_\beta$, the gain is reduced by -3dB and the corner frequency f_β defines the bandwidth of the amplifier. [5] Thus, the figure shows that the bandwidth of the amplifier is approximately 10 Hz with compensating capacitor.

For phase part, the degree of phase decreases in the frequency range 0-1KHz. In the frequency range of 1KHz-100KHz, the phase remains constant, with the magnitude remaining at around 90 degrees. In the frequency range of 100KHz-10MHz, the phase decreases as the frequency increases. The comparison with the above task shows that the circuit with the added phase compensating capacitor has a greater frequency range of stable phases, which means that the circuit can operate properly over a greater frequency range. Similarly, the circuit system has a positive gain and phase margin according to the method for finding the gain margin and phase margin presented in the lecture. Compared to the circuit without the phase compensating capacitor, this system has a greater gain and phase margin, indicating that the stability of the circuit has been improved by the addition of the capacitor.

Similarly, the input impedance experiments are carried out and the results can be seen as follows.

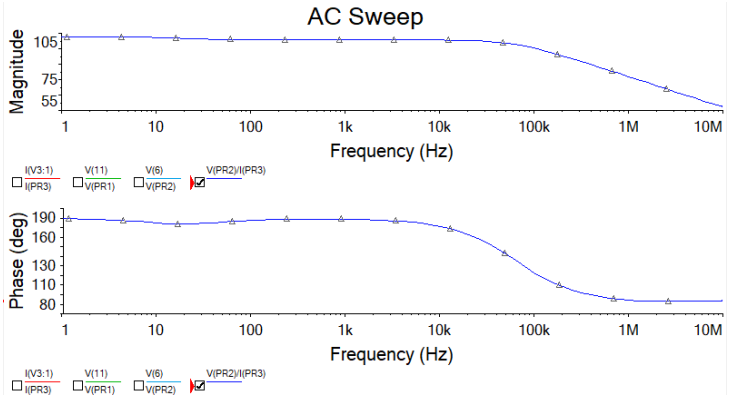


Figure 35: The input impedance with phase compensating capacitor

For the magnitude part, the magnitude also remains constant in the range 0-100 KHz, with a value of approximately 102dB. As the frequency becomes greater than 100 KHz and less than 10 MHz, the magnitude gradually decreases. The results are similar to those obtained in the previous experiments without the capacitor.

For the phase part, the phase remains essentially flat in the range 0-10 KHz, with a value of approximately 180 degrees, but in the frequency range 0-100 Hz, the phase value first drops and then rises, but the magnitude of drop and rise are very small. In the frequency range of 10K-1MHz, the phase is decreasing. In the frequency range 1M-10MHz, the phase remains constant, with a value of approximately 92 degrees.

3.4 BONUS

3.4.1 Common-mode signals without phase compensating capacitor

First, the circuit is designed without the phase compensating capacitor. After replacing the input signal with a common-mode signal, the circuit diagram of the new design is as follows.

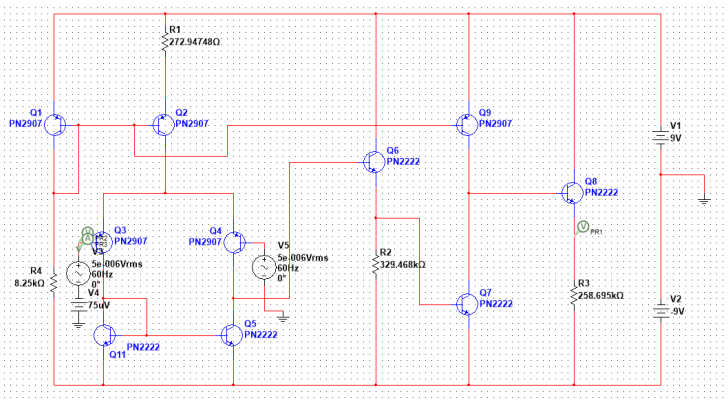


Figure 36: The circuit for common-mode signals

The frequency response can be seen as follows:

For the Magnitude part, the magnitude is approximately 0.529m dB in the frequency range 0-10KHz. In the frequency range 10K-10MHz, the magnitude first falls and then rises.But the gain remains

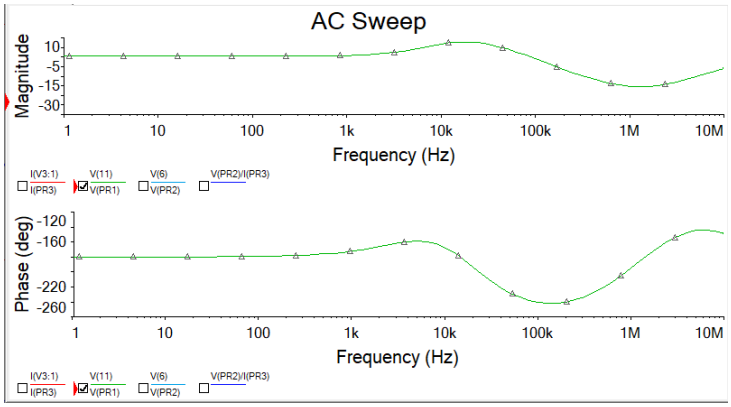


Figure 37: The frequency response of the amplifier to common-mode signal

small in the frequency range 0-10 MHz. This is as expected, because the two common mode signals counterbalance each other.

For the phase part, the value of phase nearly remains constant in the frequency range 0-1KHz, with a value of approximately -180 degrees. In the frequency range 1K-10KHz, phase shows a crest, but it's not obvious. In the frequency range 10K-10MHz, the value of phase falls and then rises.

The frequency response of the input impedance can be seen in the following diagram 38

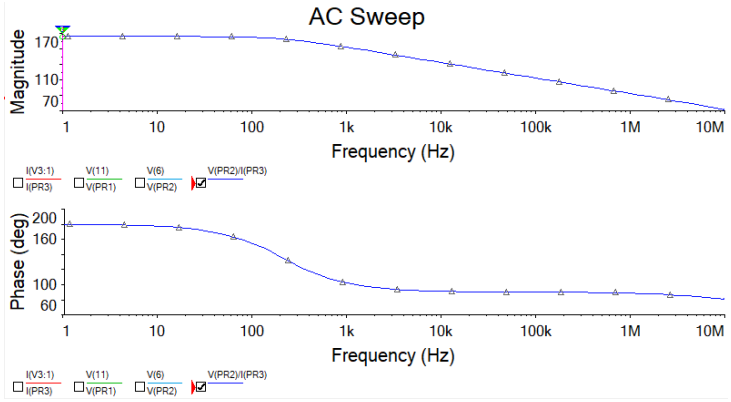


Figure 38: The frequency response of the input impedance to common-mode signal

For the Magnitude part, the magnitude nearly remains constant in the frequency range 0-100 Hz, with a value of approximately 156.9dB. In the frequency range 100-10 MHz, the magnitude gradually decreases.

For Phase part, the value of phase almost remains constant in the frequency range 0-10Hz, with a value of approximately 180 degrees. In the frequency range of 10-10KHz, the phase gradually decreases to 90 degrees. In the frequency range 10K-10MHz, the phase value also nearly remains constant at 90 degrees.

If the DC offset is added to the input on the right, the frequency response will change. The specific result is shown as follows 39

For the gain part of bode plot, the magnitude rises from -160dB to -40dB in the range 0-50 KHz. In the range 50 KHz-10 MHz, the magnitude remains more or less -40dB. The phase part in this situation does not change significantly from the previous results. For the frequency response of input impedance, the presence or absence of a DC on the right side of the input does not affect the result.

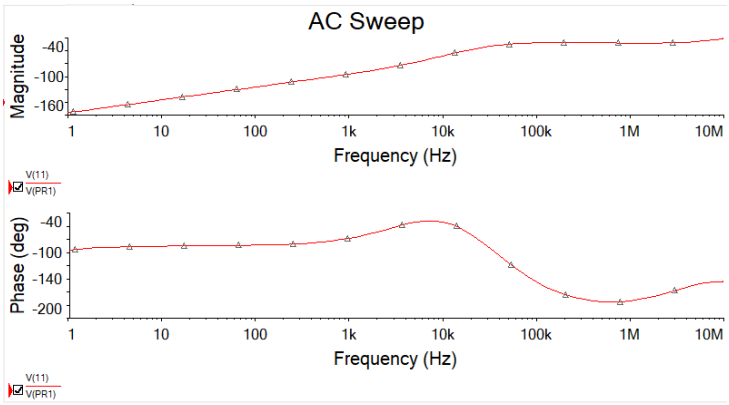


Figure 39: Results of including the DC offset on the right input side

3.4.2 Common-mode signals with phase compensating capacitor

Next, the circuit with a phase compensating capacitor is designed. After changing the inputs to common-mode signals, the specific circuit diagram is as follows:

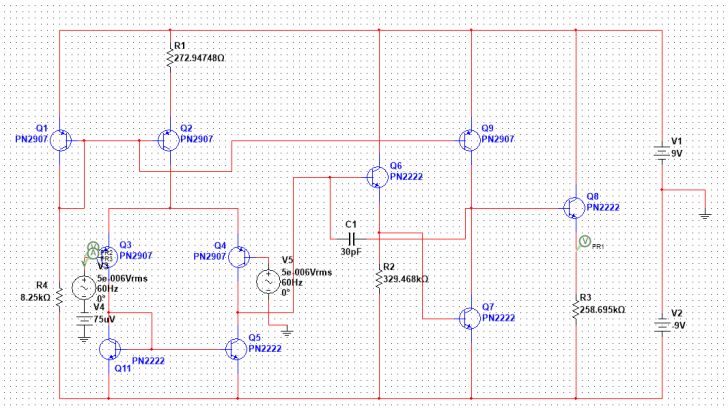


Figure 40: The circuit for common-mode signals with phase compensating capacitor

In this experiment, the frequency range was extended to 10 GHz to better observe the changes in the Bode plot. The frequency response can be seen as follows:

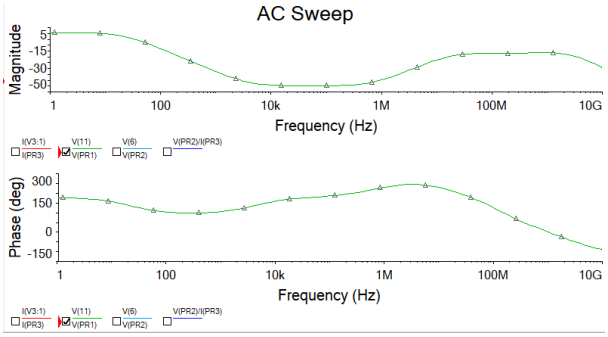


Figure 41: The frequency response of the amplifier to common-mode signal with phase compensating capacitor

For the Magnitude part, the magnitude also remains constant in the frequency range 0-10Hz, with

a value of approximate 300m dB. When the frequency range is in the range 10-10MHz, the magnitude value first decreases and then increases. In the frequency range of 10Mhz-10GHz, the magnitude remains more or less constant at around -17dB.

However, for the phase part, the phase changes in the 0-1MHz range, but the magnitude of the change is relatively small. This suggests that the addition of the compensating capacitor allows the circuit to maintain a largely constant phase over a wider frequency range. The value of phase gradually decreases over the 1M-10GHz range.

The frequency response of the input impedance can be seen in the following diagram:

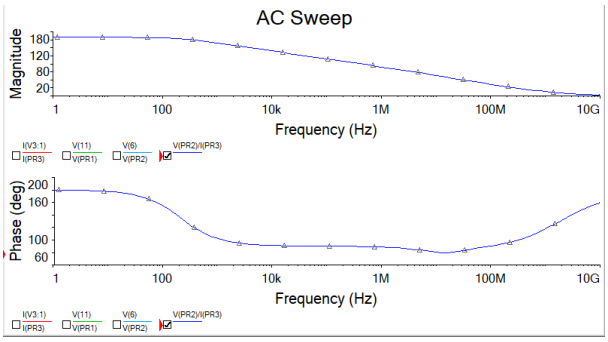


Figure 42: The frequency response of the input impedance to common-mode signal with capacitor

For the Magnitude part, the magnitude remains more or less constant in the frequency range 0-100 Hz, with a value of approximately 165 dB. In the frequency range 100-10GHz, the magnitude gradually decreases.

For the Phase part, the value of phase also remains constant in the frequency range 0-10Hz, at approximately 180 degrees. In the range 10-1000Hz, the phase value decreases gradually. In the range 1K-10MHz, the phase value remains more or less constant at 90 degrees. In the frequency range 10M-10GHz, the phase value gradually increases. The comparison with the absence of the capacitor shows that the phase maintains a constant frequency range for a longer period of time, indicating that the circuit has a better and more stable frequency range.

Similarly, if a DC offset is added to the right-hand input, the specific result is plotted as follows.

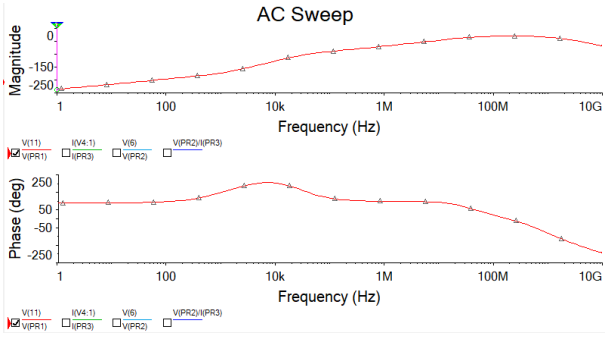


Figure 43: Results of including the DC offset on the right input side with compensating capacitor

For the gain part of the bode plot, the magnitude rises from -236dB to -70dB in the 0-10MHz range, and remains essentially at -50dB in the 10MHz-10GHz range.

For the phase part, the magnitude remains essentially at 87 degrees in the frequency range 0-10MHz, but with a peak in the middle frequency range. In the frequency range after 10MHz, the phase keeps decreasing.

The frequency response for input impedance is the same as in the previous results figure.

3.5 Design specifications table with comments

The design specifications table can be found below:

Table 3: Design specifications table

Parameter	Specification	My value
differential input impedance	>100kΩ	135.62k
Open loop voltage gain	>500000	1016080
Output impedance	<1 k	925.253Ω
DC output voltage	$\approx 0V$	74.5mV
DC offset voltage	None given	75uV
Frequency response	Down to DC (0 Hz)	Maximum gain≈120dB$(0Hz)$,f$_H \approx 10KHz$
Total current consumption	<5 mA	4.57mA
Bandwidth with compensation capacitor	None given	≈10Hz

The individual comments on the design parameters are written below:

1. **Differential input impedance**

   The differential input impedance is assumed when calculating the required resistance value. In the calculation, an input impedance of 110KΩ is used, while the actual value is $135K\Omega$ in transfer function simulation. Since the required input impedance is very large, the error between the actual and calculated values is acceptable. In order to get more voltage into the circuit, a relatively large input impedance needs to be used.

2. **Open loop voltage gain**

   In the transfer function simulation experiment, the open loop voltage gain was approximately 1.01M. In task 3, the voltage gain calculated using the slope was approximately 0.86M. In task 5, the amplification was approximately 1.02M by measuring the amplified sinusoidal signal. The experimental requirement is for the open loop gain to be greater than 0.5M, and the results obtained in all three cases meet the experimental requirement. Additionally, the voltage gain is also calculated before, which is in line with the simulated value. Since the voltage gain of the circuit is relatively large, the results obtained from different tasks may have errors, but the errors are within acceptable limits. The specific error analysis can be viewed in the next section.

3. **Output impedance**

   In the experiment, the output impedance was assumed to be 800Ω for calculating the final resistance. While the transfer function simulation gave a result of 925.253Ω. There is an error between the calculated and the actual value, but both values are less than $1K\Omega$, and both meet the requirements of the experiment.

4. **DC output voltage**

   As the circuit has internal voltage offset, an additional DC offset voltage should be connected to the circuit to regulate and balance the output voltage to approximately 0V when there is no signal

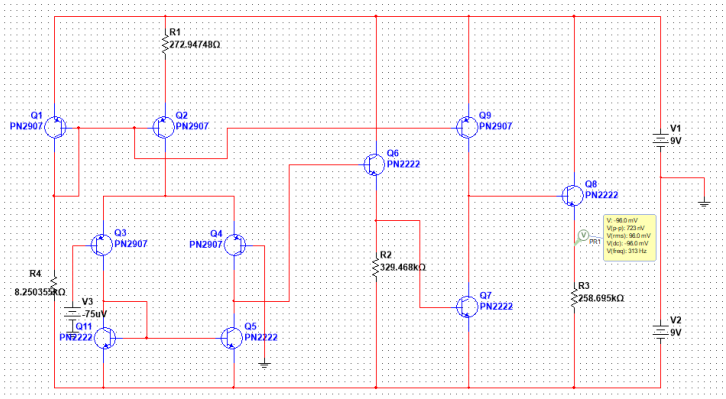


Figure 44: Diagram of the circuit when there is no signal input

input. When there is no input signal connected to the differential amplifier, the circuit diagram is as follows:

As can be seen above, the DC output voltage can be seen to be 96mV. As the DC output voltage of 96mV is very small, it can be approximated to approximately 0V, which is consistent with the requirements of the experiment. This voltage implies the DC output voltage when no input signal is present. In order to improve the efficiency of the circuit, this value should be kept as low as possible. However, in real circuits the DC output voltage cannot be eliminated. The DC offset voltage may not have been set very accurately, resulting in a small voltage (96mV) at the DC output, but as this voltage is relatively small, it meets the requirements of the experiment.

5. **DC offset voltage**

In task 4, the DC offset voltage is obtained to be approximately equal to 75uV. This is not required in the experimental requirements and this value can vary depending on the design of the circuit. In the experiments, this value is calculated by the difference between the horizontal coordinate of the centre of the amplification range and horizontal coordinates of the origin. In order to make the centre point of the amplification range lie on the y-axis, a DC offset voltage needs to be used. Additionally, as the signal generator used may have an offset voltage, a DC voltage need to be used to balance the amplifier.

6. **Frequency response**

The frequency response results of the circuit is 45:

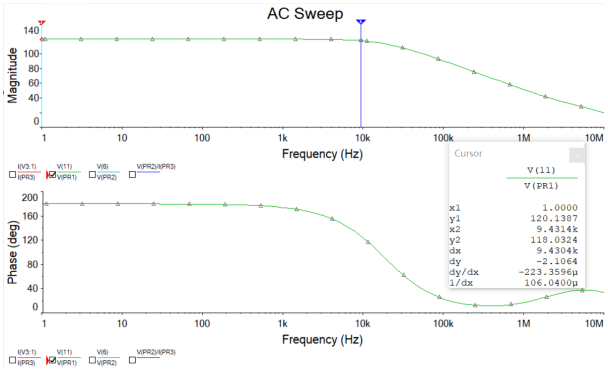


Figure 45: Frequency response for the circuit

As can be seen from the results figure above, the gain value is approximately equal to 120dB at a frequency of 0Hz. This value does not change significantly even after the phase compensation capacitor is added. As the frequency is gradually increased and becomes greater than 100 KHz, the magnitude begins to decrease significantly. The specific expression is as follows 65:

$$A_v = -g_m * R_t * \frac{r_{b'e}}{(r_{b'e} + r_{bb'} + R_s)(1 + j(\frac{f}{f_H}))} \tag{65}$$

The expression above shows that when the frequency is much smaller than f_H, the phase reverses and reaches a maximum. This explains why the magnitude plot remains essentially constant at frequencies less than f_H. Similarly, the bandwidth of the amplifier is about 10KHz as can be seen from the figure.

7. **Total current consumption**

   As can be seen from task 7, the total current consumption is approximately equal to 4.57mA. Since the experiment requires 5mA, the circuit meets the requirements of the experiment. The circuit is designed to keep the current as small as possible to reduce power and increase efficiency.

8. **Bandwidth with compensation capacitor**

   According to the definition, when $f = f_\beta$, the gain is reduced by -3dB and the corner frequency f_β defines the bandwidth of the amplifier. [5]. The specific diagram is as follows 46

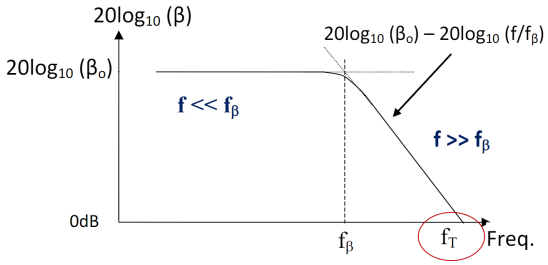


Figure 46: Diagram of Corner frequency [5]

As can be seen from figure 34, the bandwidth of the amplifier is approximately 10 Hz after the phase compensating capacitor is added.

4 Discussions

4.1 General question

4.1.1 What can you deduce about the stability of your amplifier from the Bode plots in Part III?

The open-loop Bode plot provides information on the relative stability of the closed-loop system. [6] There are two ways to determine the stability of a system from a Bode plot, which includes the gain margin and phase margin methods. These two ways of determining system stability are described below:

1. **Gain margin**

   When the gain margin is positive and the larger it is, the more stable the system is. [7] The gain margin refers to the amount of gain that can be increased or decreased to make the system stable. Generally speaking, the gain margin can be obtained directly from the Bode plot by calculating

the vertical distance between the magnitude curve and the X-axis at a frequency where the Bode phase plot = 180°. The following are the gain margin and phase margin for stable and unstable systems 47:

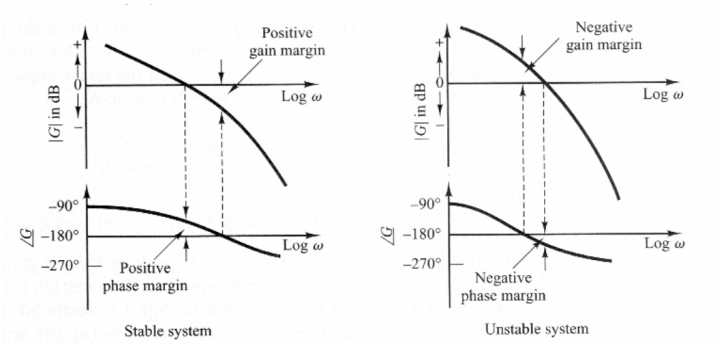


Figure 47: Diagram of the gain margin and phase margin of a stable and unstable system [8]

This is explained specifically as follows: If a system can provide a unity gain (0dB gain) to a waveform at a certain frequency, while providing a phase difference of -180. Then it is possible to replace the input waveform with the output waveform, which maintains the stability of the system. Also, the oscillation is required to be self-sustaining. [6]. This shows that an open loop gain greater than 0dB at a frequency with a phase of -180 degrees will produce an unstable system. Whereas at a frequency of -180 degrees, an open loop gain of less than 0dB would indicate that the waveform would be a stable system with a decreasing oscillation.[6]

The expression to calculate the gain margin is:

$$GM = (0 - G)dB \tag{66}$$

Where G is the gain, which is read from the vertical axis of the magnitude plot at crossover frequency.

(a) **The gain margin for the system without capacitor**

Following the method for calculating the gain margin, the point corresponding to -180 degrees need to be first found in the phase part and then the frequency corresponding to this point can be determined. The result of AC sweep is as follows:

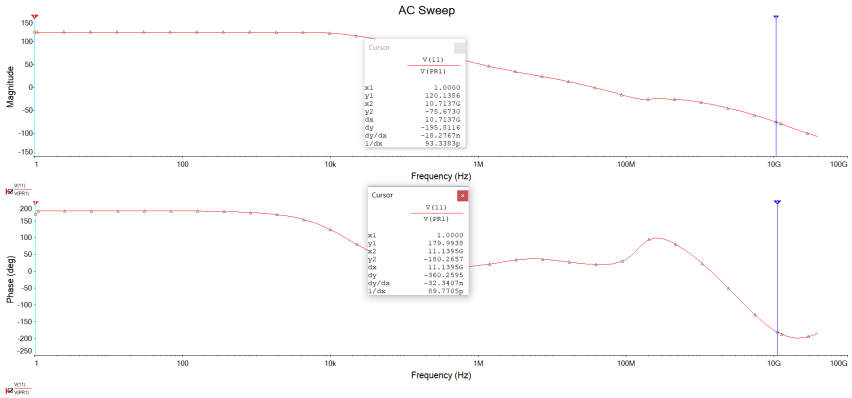


Figure 48: The gain margin for the system without capacitor

The figure shows that when the phase is -180 degrees, the corresponding frequency is about 11.1 GHz. Then the gain in the gain part of the bode plot is -75.673 at the same frequency. The gain margin of the system is positive according to the definition of the gain margin, which means that the system is stable.

(b) **The gain margin for the system with capacitor**

The results obtained from task 2 in part II are as follows:

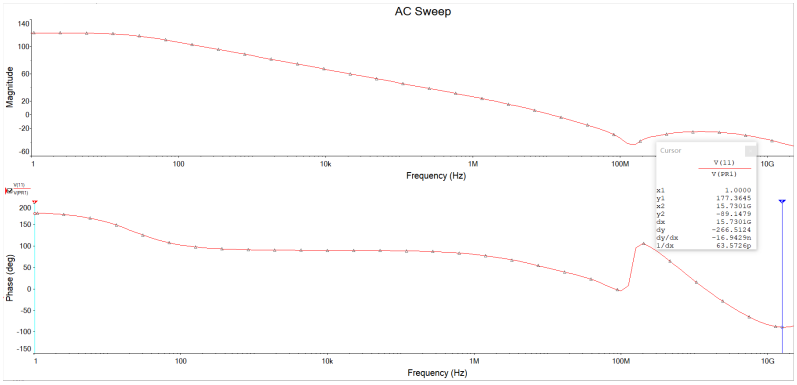


Figure 49: The gain margin for the system with capacitor

As can be seen from the diagram, there is no point corresponding to -180 degrees in the bode plot of the phase section. A search of the sources shows that the gain margin of this system tends to infinity when there is no point of -180 degrees in the system. [9] When the gain margin is infinity, it means that the system will remain stable no matter how much increasing the gain. Therefore, this system is stable and has a larger gain margin compared to the circuit without the added capacitor, indicating that the system is more stable.

2. **Phase margin**

The more positive and larger the phase margin (PM) is, the more stable the system is. Phase margin refers to the amount of phase that can be increased or decreased to make a system stable.[6] The phase margin is measured in degrees. As with the gain margin, the value of the phase margin can be obtained directly from the Bode plot. The phase margin is obtained by calculating the vertical distance between the phase curve (on the Bode plot) and the X-axis at a frequency where the Bode magnitude plot = 0 dB. This point is known as the gain crossover frequency. The specific calculation formula is 67:

$$PM = \phi - (-180^{\circ}) \tag{67}$$

The method of determining whether the system is stable by the phase margin can be seen in the above figure 47, when the phase margin is larger, the more stable the system is:

(a) **The phase margin for the system without capacitor**

To calculate the phase margin, first we need to find the point where the magnitude is equal to 0. The result can be seen as follows 50:

The figure shows that when the magnitude is equal to 0 the corresponding frequency is about 36.05 MHz. In the phase part of the plot, the corresponding phase at the same frequency is 20.76 degrees, which means that the system has a positive phase margin. This indicates that the system is stable.

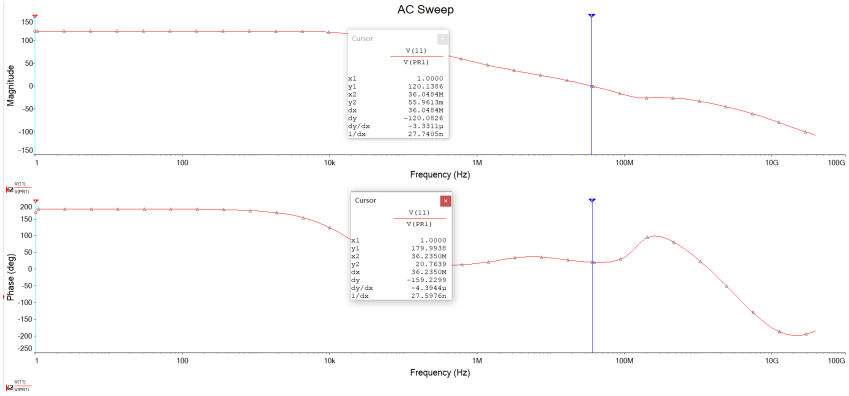


Figure 50: The phase margin for the system without capacitor

(b) **The phase margin for the system with capacitor**

To obtain the phase margin from the bode plot, the point of 0 gain need to be found. The result can be seen below:

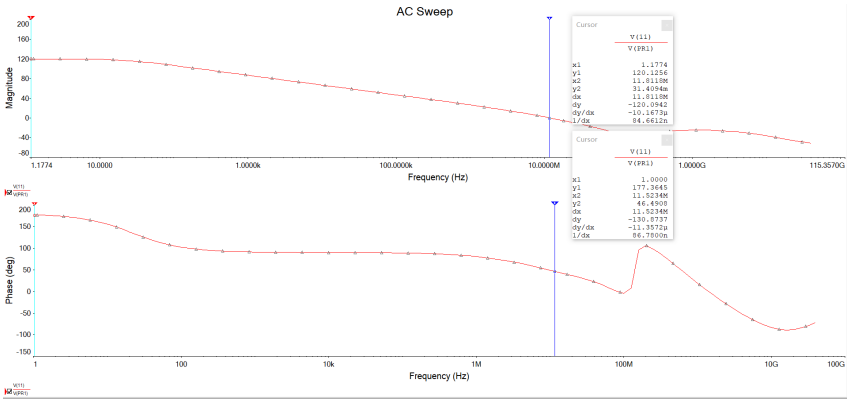


Figure 51: The phase margin for the system with capacitor

It can be seen from the figure that the frequency corresponding to the point when gain is equal to 0 is approximately 11.8MHz. The point corresponding to 11.8MHz is approximated in the phase part of the bode plot, and the phase of this point is approximately 46.5 degrees. According to 47, it can be found that the phase margin of the system is positive and therefore the system is stable. This system has a larger phase margin (20.76<46.5) compared to the system without the phase compensating capacitor, indicating that the system is more stable.

4.1.2 What is the purpose of the 'Phase compensating capacitor'?

In the AC sweep simulation, a 30pF capacitor is added as a phase compensating capacitor between the collector of the common emitter stage and the base of the first emitter follower. Since the frequency range without the capacitor is too small, the addition of the compensating capacitor increases the phase stability range. This can be seen in the figure of the experiment above.

Before the addition of the compensating capacitor, the frequency range in which the phase remains constant is approximately 0-1KHz, but after the addition of the phase compensating capacitor, the phase remains stable in the range 100Hz-1MHz. The bandwidth of the frequency response becomes larger. In other words, the circuit becomes more stable with the addition of the compensating capacitor, and the

capacitor also achieves miller compensation. The capacitor changes the dominant pole to less frequency and the second dominant pole to higher frequency, which obtain a higher unity gain frequency through doing this way. [10]

The phase compensating capacitor is also used to achieve the stable operation when negative feedback is applied. The phase compensating capacitor accompanies the Miller compensation. The following is a comparison of the capacitor with and without phase compensation.

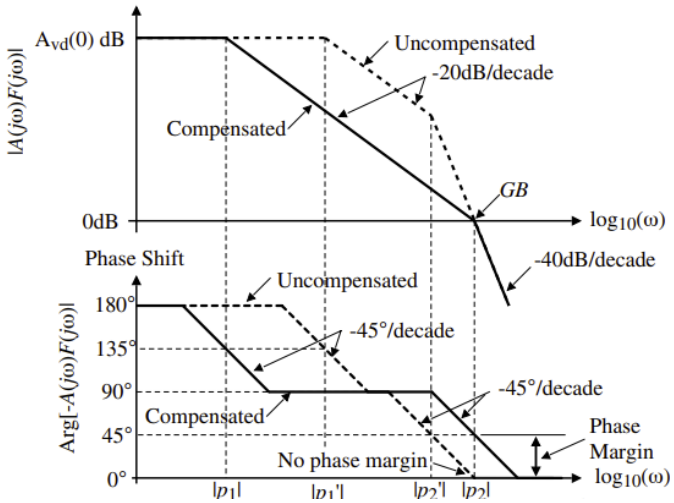


Figure 52: The comparison of bode plot with and without phase compensation capacitors [11]

As can be seen from the above figure, the stable frequency range of the Phase part becomes longer after the addition of the capacitor, which is consistent with the experimentally obtained result, indicating that the phase compensation capacitor can increase the stable phase in a wider frequency range.

In addition, this circuit will be used as an operational amplifier. As the circuit used in the experiment is not ideal, the circuit has the effect of phase shifting for signals of a certain frequency range, so the output signal will be unstable or even oscillating. The best way to solve the problem of phase shift in this case is to add a phase compensation capacitor. This is because if a frequency compensation circuit is used on the op amp, the capacitor will compensate the amplifier in terms of frequency response, making the op amp more stable.

4.2 Error analysis

4.2.1 The output impedance

By using the transfer function simulation, a value for the output impedance is obtained of approximately 925Ω. However, it is assumed as the output impedance is 800Ω when calculating the resistance. Although both the real and calculated values meet the requirements of the experiment, the error is relatively large. The absolute error is calculated by the formula:

$$Err\% = \frac{925 - 800}{800} * 100\% \approx 15.6\% \tag{68}$$

This error may arise because the approximate resistances are mostly taken in calculating process and have not used the real values. For example, it is assumed $I_c = I_E$ in our calculations and ignoring the base current. However the simulation software does not ignore these factors, which causes a certain amount of error. In addition, the results of previous calculations also have an effect, and once there are

certain errors in the previous calculation process, these errors will also add up, resulting in the actual and calculated values not being exactly equal. However this error is still within acceptable limits.

4.2.2 The open loop gain

In the transfer function simulation, an open loop voltage gain of approximately 1.01M was obtained. In task 3, the voltage gain was calculated using a slope of approximately 0.86M. In task 5, an amplification of approximately 1.00M was obtained by measuring the amplified sinusoidal signal. Although the experimental requirement is an open loop gain of more than 0.5M, the results obtained on all three occasions met the experimental requirement. However, the open loop gains obtained for the same experimental circuit were not identical, especially in Task 3 where the voltage gain calculated from the slope differed significantly from the other two voltage gains.

This is probably due to the fact that the calculation point was not chosen accurately when calculating the slope. As the calculation points were chosen artificially, which may not be accurate. This can lead to errors with the true values. In this case in particular, even a small deviation from the chosen calculation point can have a significant impact on the final result. However, since the voltage gain of the circuit is relatively large, the results obtained from different tasks may be inaccurate, but the error is within acceptable limits.

In addition, the voltage gain is also calculated, and although the error between the calculated and simulated values is relatively large, it is within acceptable limits. This is probably due to the fact that the resistance of some resistors has been omitted from the calculation.

4.2.3 The calculations of four resistors

There are two methods of calculation in calculating the resistance R_4 of the other branch of CM. The following assumptions were used in the design of the experiment 69.

$$I_{ref} = 10 * I_O \tag{69}$$

However, we can also calculate the resistance in the alternative way assumed on the experimental hints, and the alternative calculation is as follows:

$$I_{ref} = I_O * exp(\frac{I_O * R_E}{V_T}) \tag{70}$$

Let $I_O * R_E = V_T$, the current will be:

$$I_{ref} = I_O * exp(1) \tag{71}$$

Both ways of obtaining I_{ref} are correct, but the results may produce very different results, which may also be the cause of the error. Also, since some of the coefficients used to calculate the resistance values may not be accurate, including β, V_A etc.

In addition, some resistances are ignored in the calculation of each resistance, but these can also have an effect on the results of the experiment. For example, for the following figure 53:

As the resistance of $r_{b'c}$ is very large, it is ignored in the calculation to simplify the process. In addition, the ohmic resistance of the semiconductor bulk $r_{bb'}$ is also ignored. Although the effect of these two resistances on the calculation is small, the error caused by ignoring them should be taken into account.

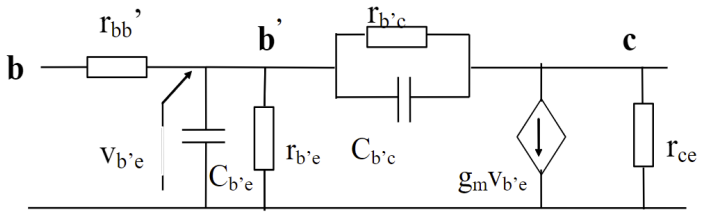


Figure 53: Hybrid-pi model [12]

4.3 Problem I have experienced and the problem-solving methods

During the process of the experiment, I encountered many difficulties. One of the difficulties that bothered me most was the calculation of the resistances. Having no experience in calculating the resistance of such complex circuits, I spent a lot of time in the early stages of the experiment trying to calculate the exact resistance value of each resistor. However, there were some problems that I still had not solved after spending a lot of time. My solution was to ask TAs for ideas on how to calculate them. I am very grateful for the TA's dedication in the lab class. After the TA's explanation, I gained new insights into some problems and eventually solved them.

Another difficulty I encountered was that the output characteristic curve did not change after adding the offset voltage, and after many attempts I finally managed to add the offset voltage. My solution was to keep trying new ways of solving the problem, one might fail, but another might work.

4.4 Limitation and suggestion

The experiment was generally successful, but there were some minor limitations. For example, in the real experiment it was difficult to find exactly the same resistors as we had calculated, and we needed to use some standard resistors to complete the experiment. If the experiment specifies the resistance of the standard resistors and allows us to match the calculated resistors with the most suitable ones, then the simulation will be closer to the real experiment. Students will also learn how to construct real circuits.

5 Conclusions

The experiment was generally very successful and all parameters of the designed circuit met the requirements of the experiment. The designed circuit has an amplification of around 1M, which is very much in line with the requirements of the experiment. The errors that occur between the designed and actual values are also explained in detail in the previous section. Through this experiment, I was able to understand the rules of real circuit design and to note the design details of the parameters of real circuits. In addition, I have mastered the role of the phase compensating capacitor. In the next circuit design, particular attention should be paid to the calculation of the resistance, which needs to be as accurate as possible in order to minimise errors.

References

[1] Electronics tutorials, "Operational amplifier basics," https://www.electronics-tutorials.ws/opamp/, 2022.

[2] N.Sedghi, “Experiment 5 - design of an operational amplifier using multisim,” https://liverpool.instructure.com/courses/46000/pages/experiment-5?module_item_id=1258994, University of Liverpool, 2021.

[3] C.Mechkov, “Can the early voltage be physically explained?” https://www.researchgate.net/post/Can-the-Early-voltage-be-physically-explained, 2018.

[4] Stackexchange, “Find resonance, bandwidth from bode plot,” https://electronics.stackexchange.com/, 2014.

[5] ELECTRONIC CIRCUITS AND SYSTEMS, “Part 6 - frequency responce of a bjt,” https://liverpool.instructure.com/courses/47890/files/, 2022.

[6] Stackexchange, “Stability from bode plot,” https://electronics.stackexchange.com/, 2017.

[7] Electrical 4U, “Bode plot, gain margin and phase margin (plus diagrams),” https://www.electrical4u.com/bode-plot-gain-margin-phase-margin/, 2021.

[8] H.Jenkins, “Stability, gain margins, phase margins,” http://faculty.mercer.edu/jenkins_he/documents/GainMarginandPhaseMargin.pdf, Mercer university, 2022.

[9] J.S.Augusto, “In which condition gain margin will be infinite?” https://www.quora.com/In-which-condition-gain-margin-will-be-infinite?msclkid=00716a6dc16111ec82cf7993cc9e57cf, 2021.

[10] Edaboard, “Phase compensating capacitor,” https://www.edaboard.com/threads/phase-compensating-capacitor.124735/, 2008.

[11] P.E.Allen, “Compensation of op amps,” https://pallen.ece.gatech.edu/Academic/ECE_6412/, 2002.

[12] ELECTRONIC CIRCUITS AND SYSTEMS, “Part 1 bjt small signal model,” https://liverpool.instructure.com/courses/47890/files/, 2022.