## Report

In order to do the experiment that determines the best fit configuration, I have following methodology for optimization:

Use cacheesim to model and simulate different cache configurations with realistic workloads. Simulations can provide detailed insights into access times, miss rates, and power consumption.

Analyze access patterns of typical workloads(The given trace files) to understand the impact of B and S on hit and miss rates.

Calculate the overhead for different configurations. Highly associative caches require more tag bits per block, increasing the metadata storage.

Systematically vary B and S to find configurations that meet the optimization criteria. Pay special attention to points where further increases in B or S yield minimal improvements in access time or significantly increase metadata storage, area, or power.

The shell script I used to execute the program with different configurations is as follows:

```
#!/bin/bash
 1
 2
 3 # Fixed parameters
 4 c=15
 5 C=17
 6
   trace_file="./traces/gcc.trace"
 7
    output="test.log"
8
9
    # Iterate over the parameters within the specified ranges
10
    for b in {5..7}; do
        for s in {0..5}; do
11
            for S in {1..6}; do # Start S greater than s to meet the restriction
12
13
                for P in {0..2}; do
                    for I in "LIP" "MIP"; do
14
                         for r in "LFU" "LRU"; do
15
16
                             # Ensure the size of the L2 cache is strictly
    greater than the size of the L1 cache
17
                             if ((C > c)) \&\& ((S > s)) \&\& ((C - S > c - s)); then
                                 ./run.sh -c "$c" -b "$b" -s "$s" -C "$C" -S "$S"
18
    -P "$P" -I "$I" -r "$r" -f "$trace_file" >>"$output"
19
                             fi
20
                         done
21
                    done
22
                done
23
            done
24
        done
25
    done
26
```

The following python script is to find the smallest Average Access Time(AAT) for L1:

```
1 def find_smallest_l1_aat(file_path):
```

```
smallest_aat = None
 3
        with open(file_path, 'r') as file:
 4
            for line in file:
 5
 6
                if line.startswith("L1 average access time (AAT):"):
 7
                    # Extract the numeric value of AAT
                    aat = float(line.split(":")[1].strip())
 8
 9
                    # Initialize smallest_aat or compare with the current
10
    smallest
11
                    if smallest_aat is None or aat < smallest_aat:</pre>
                         smallest_aat = aat
12
13
14
        return smallest_aat
15
16 | # Replace 'test.log' with the actual path to your log file
   file_path = 'test.log'
17
    smallest_aat = find_smallest_l1_aat(file_path)
18
19 print(f"The smallest L1 average access time (AAT) is: {smallest_aat}")
```

File  $gcc.\ trace$ : The smallest average access time (AAT) for L1 among the provided configurations is  $2.044\ ns$ , which is achieved with the cache settings of:

```
Cache Settings
 2
 3
    L1 (C,B,S): (15,7,5). Replacement policy: LRU. Prefetcher disabled.
    L2 (C,B,S): (17,7,6). Replacement policy: LRU. +1 prefetcher. Prefetch
    insertion policy: LIP.
 5
 6
   Cache Statistics
 7
    _____
8
   Reads: 315500
    Writes: 184500
9
10
11 L1 accesses: 500000
12 L1 hits: 495015
13 L1 misses: 4985
14 L1 hit ratio: 0.990
    L1 miss ratio: 0.010
15
16 L1 average access time (AAT): 2.044
17
18 L2 reads: 4985
    L2 writes: 2055
19
20 L2 read hits: 3818
21 L2 read misses: 1167
22 L2 prefetches: 840
23 L2 read hit ratio: 0.766
24 L2 read miss ratio: 0.234
25 L2 average access time (AAT): 29.510
```

```
    L1 Cache (C=15, B=7, S=5): 14,336 bits
    L2 Cache (C=17, B=7, S=6): 55,296 bits
```

File leela.trace: The smallest average access time (AAT) for L1 among the provided configurations is  $1.799\ ns$ , which is achieved with the cache settings of:

```
1 | Cache Settings
 2
    -----
 3 L1 (C,B,S): (15,7,4). Replacement policy: LRU. Prefetcher disabled.
   L2 (C,B,S): (17,7,5). Replacement policy: LRU. +1 prefetcher. Prefetch
    insertion policy: LIP.
5
6
   Cache Statistics
    _____
8 Reads: 352008
9
    Writes: 147992
10
11
   L1 accesses: 500000
12 L1 hits: 499464
13 L1 misses: 536
14 L1 hit ratio: 0.999
15 L1 miss ratio: 0.001
16 L1 average access time (AAT): 1.799
17
18 L2 reads: 536
19 L2 writes: 14
20 L2 read hits: 323
21 L2 read misses: 213
22 L2 prefetches: 123
23 L2 read hit ratio: 0.603
24 L2 read miss ratio: 0.397
25 L2 average access time (AAT): 45.839
```

L1 Cache (C=15, B=7, S=4): 14,080 bits
L2 Cache (C=17, B=7, S=5): 54,272 bits

File  $linpack.\ trace$ : The smallest average access time (AAT) for L1 among the provided configurations is  $4.136\ ns$ , which is achieved with the cache settings of:

```
1 | Cache Settings
   -----
2
 3 L1 (C,B,S): (15,7,3). Replacement policy: LRU. Prefetcher disabled.
   L2 (C,B,S): (17,7,4). Replacement policy: LRU. +1 prefetcher. Prefetch
    insertion policy: LIP.
5
6 Cache Statistics
7
   _____
8 Reads: 332993
9
   Writes: 167007
10
11 L1 accesses: 500000
12 L1 hits: 478869
13 L1 misses: 21131
14 L1 hit ratio: 0.958
15
    L1 miss ratio: 0.042
16 L1 average access time (AAT): 4.136
17
18 L2 reads: 21131
19 L2 writes: 20875
20 L2 read hits: 10490
```

```
L2 read misses: 10641
L2 prefetches: 10494
L2 read hit ratio: 0.496
L2 read miss ratio: 0.504
L2 average access time (AAT): 56.457
```

L1 Cache (C=15, B=7, S=3): 13,824 bits
 L2 Cache (C=17, B=7, S=4): 53,248 bits

File  $matmul\_naive.trace$ : The smallest average access time (AAT) for L1 among the provided configurations is  $3.321 \ ns$ , which is achieved with the cache settings of:

```
1 | Cache Settings
 2
    -----
   L1 (C,B,S): (15,7,5). Replacement policy: LFU. Prefetcher disabled.
 3
    L2 (C,B,S): (17,7,6). Replacement policy: LFU. +1 prefetcher. Prefetch
    insertion policy: LIP.
 5
6
   Cache Statistics
 7
    _____
8 Reads: 494452
9
   Writes: 5548
10
11 L1 accesses: 500000
12 L1 hits: 385860
13 L1 misses: 114140
14 L1 hit ratio: 0.772
   L1 miss ratio: 0.228
15
16 L1 average access time (AAT): 3.321
17
18 L2 reads: 114140
19 L2 writes: 981
20 L2 read hits: 113249
21 L2 read misses: 891
22 L2 prefetches: 808
23 L2 read hit ratio: 0.992
24 L2 read miss ratio: 0.008
25 L2 average access time (AAT): 6.881
```

L1 Cache (C=15, B=7, S=5): 14,336 bits
L2 Cache (C=17, B=7, S=6): 55,296 bits

File  $matmul\_tiled.\ trace$ : The smallest average access time (AAT) for L1 among the provided configurations is  $1.909\ ns$ , which is achieved with the cache settings of:

```
Cache Settings
Cache Settings
Cache Settings
L1 (C,B,S): (15,7,3). Replacement policy: LRU. Prefetcher disabled.
L2 (C,B,S): (17,7,4). Replacement policy: LRU. +1 prefetcher. Prefetch insertion policy: MIP.

Cache Statistics
Reads: 482548
```

```
9 Writes: 17452
10
11 L1 accesses: 500000
12 L1 hits: 498182
13 L1 misses: 1818
14 L1 hit ratio: 0.996
15 L1 miss ratio: 0.004
16 L1 average access time (AAT): 1.909
17
18 L2 reads: 1818
19 L2 writes: 311
20 L2 read hits: 1135
21 L2 read misses: 683
22 L2 prefetches: 610
23 L2 read hit ratio: 0.624
24 L2 read miss ratio: 0.376
25 L2 average access time (AAT): 43.669
```

L1 Cache (C=15, B=7, S=3): 13,824 bits
L2 Cache (C=17, B=7, S=4): 53,248 bits

File mcf.trace: The smallest average access time (AAT) for L1 among the provided configurations is  $1.918 \ ns$ , which is achieved with the cache settings of:

```
1 | Cache Settings
2
 3 L1 (C,B,S): (15,7,4). Replacement policy: LRU. Prefetcher disabled.
   L2 (C,B,S): (17,7,5). Replacement policy: LRU. +1 prefetcher. Prefetch
    insertion policy: MIP.
6 Cache Statistics
 7
    _____
8 Reads: 304587
9
   Writes: 195413
10
11 L1 accesses: 500000
12 L1 hits: 498969
13 L1 misses: 1031
14 L1 hit ratio: 0.998
   L1 miss ratio: 0.002
15
16 L1 average access time (AAT): 1.918
17
18 L2 reads: 1031
19 L2 writes: 709
20 L2 read hits: 256
21 L2 read misses: 775
22 L2 prefetches: 766
23 L2 read hit ratio: 0.248
24 L2 read miss ratio: 0.752
25 L2 average access time (AAT): 81.270
```

L1 Cache (C=15, B=7, S=4): 14,080 bits
 L2 Cache (C=17, B=7, S=5): 54,272 bits