A.4　Operation Code Map

Table A.51 is an operation code map.

Table A.51 Operation Code Map

Instruction		Code		Fx: 0000	Fx: 0001	Fx: 0010	Fx: 0011–1111
MSB			LSB	MD: 00	MD: 01	MD: 10	MD: 11
0000	Rn	Fx	0000				
0000	Rn	Fx	0001				
0000	Rn	Fx	0010	STC　　SR,Rn	STC　　GBR,Rn	STC　　VBR,Rn	
0000	Rm	Fx	0011	BSRF　Rm*		BRAF　Rm*	
0000	Rn	Rm	01MD	MOV.B Rm,@(R0,Rn)	MOV.W Rm,@(R0,Rn)	MOV.L Rm,@(R0,Rn)	MUL.L Rm,Rn*
0000	0000	Fx	1000	CLRT	SETT	CLRMAC	LDTLB
0000	0000	Fx	1001	NOP	DIV0U		
0000	0000	Fx	1010				
0000	0000	Fx	1011	RTS	SLEEP	RTE	
0000	Rn	Fx	1000				
0000	Rn	Fx	1001			MOVT　Rn	
0000	Rn	Fx	1010	STS MACH,Rn	STS MACL,Rn	STS　PR,Rn	
0000	Rn	Fx	1011				
0000	Rn	Fx Rh	11MD	MOV.B @(R0,Rm),Rn	MOV.W @(R0,Rm),Rn	MOV.L @(R0,Rm),Rn	MAC.L @Rm+,@Rn+*
0001	Rn	Rm	disp	MOV.L Rm,@(disp:4,Rn)			
0010	Rn	Rm	00MD	MOV.B Rm,@Rn	MOV.W Rm,@Rn	MOV.L Rm,@Rn	
0010	Rn	Rm	01MD	MOV.B Rm,@-Rn	MOV.W Rm,@-Rn	MOV.L Rm,@-Rn	DIV0S Rm,Rn
0010	Rn	Rm	10MD	TST　Rm,Rn	AND　Rm,Rn	XOR　Rm,Rn	OR　Rm,Rn
0010	Rn	Rm	11MD	CMP/STR Rm,Rn	XTRCT Rm,Rn	MULU.W Rm,Rn	MULS.W Rm,Rn
0011	Rn	Rm	00MD	CMP/EQ Rm,Rn		CMP/HS Rm,Rn	CMP/GE Rm,Rn
0011	Rn	Rm	01MD	DIV1 Rm,Rn	DMULU.L Rm,Rn*	CMP/HI Rm,Rn	CMP/GT Rm,Rn
0011	Rn	Rm	10MD	SUB　Rm,Rn		SUBC　Rm,Rn	SUBV　Rm,Rn
0011	Rn	Rm	11MD	ADD　Rm,Rn	DMULS.L Rm,Rn*	ADDC　Rm,Rn	ADDV　Rm,Rn
0100	Rn	Fx	0000	SHLL　Rn LSL	DT　Rn*	SHAL　Rn LSL (same)	

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Table A.51 Operation Code Map (cont)

Instruction		Code		Fx: 0000	Fx: 0001	Fx: 0010	Fx: 0011–1111
MSB			LSB	MD: 00	MD: 01	MD: 10	MD: 11
0100	Rn	Fx	0001	SHLR Rn *LSR*	CMP/PZ Rn	SHAR Rn *ASR*	
0100	Rn	Fx	0010	STS.L MACH,@–Rn	STS.L MACL,@–Rn	STS.L PR,@–Rn	
0100	Rn	Fx	0011	STC.L SR,@–Rn	STC.L GBR,@–Rn	STC.L VBR,@–Rn	
0100	Rn	Fx	0100	ROTL Rn *ROL*		ROTCL Rn *RLC*	
0100	Rn	Fx	0101	ROTR Rn *ROR*	CMP/PL Rn	ROTCR Rn *RRC*	
0100	Rm	Fx	0110	LDS.L @Rm+,MACH	LDS.L @Rm+,MACL	LDS.L @Rm+,PR	
0100	Rm	Fx	0111	LDC.L @Rm+,SR	LDC.L @Rm+,GBR	LDC.L @Rm+,VBR	
0100	Rn	Fx	1000	SHLL2 Rn	SHLL8 Rn	SHLL16 Rn	
0100	Rn	Fx	1001	SHLR2 Rn	SHLR8 Rn	SHLR16 Rn	
0100	Rm	Fx	1010	LDS Rm,MACH	LDS Rm,MACL	LDS Rm,PR	
0100	Rm/Rn	Fx	1011	JSR @Rm	TAS.B @Rn	JMP @Rm	
0100	Rm	Fx Rn	1100	*SHAD Rm,Rn*			
0100	Rm	Fx Rn	1101	*SHLD Rm,Rn*			
0100	Rn	Fx	1110	LDC Rm,SR	LDC Rm,GBR	LDC Rm,VBR	*0100: STC Rm,SPC* *0011: STC Rm,SSR*
0100	Rn	Rm	1111	MAC.W @Rm+,@Rn+			
0101	Rn	Rm	disp	MOV.L @(disp:4,Rm),Rn			
0110	Rn	Rm	00MD	MOV.B @Rm,Rn	MOV.W @Rm,Rn	MOV.L @Rm,Rn	MOV Rm,Rn
0110	Rn	Rm	01MD	MOV.B @Rm+,Rn	MOV.W @Rm+,Rn	MOV.L @Rm+,Rn	NOT Rm,Rn
0110	Rn	Rm	10MD	SWAP.B Rm,Rn	SWAP.W Rm,Rn	NEGC Rm,Rn	NEG Rm,Rn
0110	Rn	Rm	11MD	EXTU.B Rm,Rn	EXTU.W Rm,Rn	EXTS.B Rm,Rn	EXTS.W Rm,Rn
0111	Rn		imm	ADD #imm:8,Rn			
1000	00MD	Rn	disp	MOV.B R0,@(disp:4,Rn)	MOV.W R0,@(disp:4,Rn)		
1000	01MD	Rm	disp	MOV.B @(disp:4,Rm),R0	MOV.W @(disp:4,Rm),R0		
1000	10MD		imm/disp	CMP/EQ #imm:8,R0	BT label:8		BF label:8

Table A.51 Operation Code Map (cont)

Instruction		Code	Fx: 0000	Fx: 0001	Fx: 0010	Fx: 0011–1111
MSB		LSB	MD: 00	MD: 01	MD: 10	MD: 11
1000	11MD	imm/disp		BT/S label:8*		BF/S label:8*
1001	Rn	disp	MOV.W @(disp:8,PC),Rn			
1010		disp	BRA label:12			
1011		disp	BSR label:12			
1100	00MD	imm/disp	MOV.B R0, @(disp:8, GBR)	MOV.W R0, @(disp:8, GBR)	MOV.L R0, @(disp:8, GBR)	TRAPA #imm:8
1100	01MD	disp	MOV.B @(disp:8, GBR),R0	MOV.W @(disp:8, GBR),R0	MOV.L @(disp:8, GBR),R0	MOVA @(disp:8, PC),R0
1100	10MD	imm	TST #imm:8,R0	AND #imm:8,R0	XOR #imm:8,R0	OR #imm:8,R0
1100	11MD	imm	TST.B #imm:8, @(R0,GBR)	AND.B #imm:8, @(R0,GBR)	XOR.B #imm:8, @(R0,GBR)	OR.B #imm:8, @(R0,GBR)
1101	Rn	disp	MOV.L @(disp:8,PC),Rn			
1110	Rn	imm	MOV #imm:8,Rn			
1111		...				

Note: SH-2 CPU instructions