

BIT	9 (d512)	8 (d256)	7 (d128)	6 (d64)	5 (d32)	4 (d16)	3 (d8)	2 (d4)	1 (d2)	0 (d1)
VOLTATGE (V)	<u>2,5</u>	<u>1,25</u>	.625	<u>.3125</u>	<u>.15625</u>	<u>.078125</u>	.0390625	.0195312	.0097656	<u>.0048828</u>

Pl.: $V_{ref} = 5V$, $V_{in} = 4,3 V$

Cycle 1 >>> MSB = 1

SAR = 1000000000 = 2,5V

$V_{in} > V_{DAC}$, SAR = 1000000000

Set 1

Cycle 2:

SAR = 1100000000 = 3,75V

$V_{in} > V_{DAC}$, SAR = 1100000000

Set 1

Cycle 3:

SAR = 1110000000 = 4,375V

$V_{in} < V_{DAC}$, SAR = 1100000000

Reset to 0

Cycle 4:

SAR = 1101000000 = 4,0625V

$V_{in} > V_{DAC}$, SAR = 1101000000

Set 1

Cycle 5:

SAR = 1101100000 = 4,21875V

$V_{in} > V_{DAC}$, SAR = 1101100000

Set 1

Cycle 6:

SAR = 1101110000 = 4,296875V

$V_{in} > V_{DAC}$, SAR = 1101110000

Set 1

Cycle 7:

SAR = 1101111000 = 4,3359375V

$V_{in} < V_{DAC}$, SAR = 1101110000

Reset to 0

Cycle 7:

SAR = 1101110100 = 4,3164062V

$V_{in} < V_{DAC}$, SAR = 1101110000

Reset to 0

Cycle 8:

SAR = 1101110010 = 4,3066406V

$V_{in} < V_{DAC}$, SAR = 1101110000

Reset to 0

Cycle 9:

SAR = 1101110001 = 4,3017578V

$V_{in} < V_{DAC}$, SAR = 1101110001

Set 1

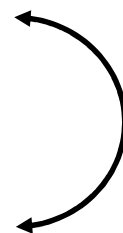
ADCH = b00000011

ADCL = b01110001

ADC virtual register:

bin 1101110001

dec 881



This part depends on the comparator sensitivity