BIT	9 (d512)	8 (d256)	7 (d128)	6 (d64)	5 (d32)	4 (d16)	3 (d8)	2 (d4)	1 (d2)	0 (d1)
VOLTATGE (V)	<u>2,5</u>	<u>1,25</u>	.625	<u>.3125</u>	<u>.15625</u>	.078125	.0390625	.0195312	.0097656	<u>.0048828</u>

PI.: $V_{ref} = 5V$, $V_{in} = 4.3 V$

Cycle 1 >>> MSB = 1

SAR = 1000000000 = 2,5V

Vin > VDAC, SAR = 1000000000

Set 1

Cycle 2:

SAR = 1100000000 = 3,75V

Vin > VDAC, SAR = **11**00000000

Set 1

Cycle 3:

SAR = **11**10000000 = 4,375V

Vin < VDAC, SAR = **110**0000000

Reset to 0

Cycle 4:

SAR = **110**1000000 = 4,0625V

Vin > VDAC, SAR = **1101**000000

Set 1

Cycle 5:

SAR = **1101**100000 = 4,21875V

Vin > VDAC, SAR = **11011**00000

Set 1

Cycle 6:

SAR = **11011**10000 = 4,296875V

Vin > VDAC, SAR = **110111**0000

Set 1

Cycle 7:

SAR = **110111**1000 = 4,3359375V

Vin < VDAC, SAR = **1101110**000

Reset to 0

Cycle 7:

SAR = **1101110**100 = 4,3164062V

Vin < VDAC, SAR = **11011100**00

Reset to 0

Cycle 8:

SAR = **11011100**10 = 4,3066406V

Vin < VDAC, SAR = **110111000**0

Reset to 0

Cycle 9:

SAR = **110111000**1 = **4,30**17578V

Vin < VDAC, SAR = **1101110001**

Set 1

ADCH = b00000011ADCL = b01110001

ADC virtual register:

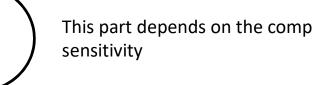
bin 1101110001

dec **881**

| input voltage = ADC * (5 / 1023);

\$81 * (5 / 1023) = **4,30**5962854349951 V

This part depends on the comparator



Tibor Rojko 30.07.2019