Chapter 18
Modulators

INTRODUCTION

We will present systematized design information on three types of modulators in this chapter. Each of these modulators requires a corresponding demodulator, detector, discriminator, or decoder at the other end of the system to restore the information to its original form. These other circuits are discussed in Chaps. 7, 8, 14, and 16.

The first circuit we present will be the amplitude modulator—sometimes called the linear modulator. This circuit is similar in function to that used by AM broadcast stations to superimpose an audio signal on a high-frequency carrier signal. Multipliers, discussed in Chap. 19, can also be used for AM modulation.

Frequency modulation, or voltage-to-frequency conversion, is covered in Chap. 21.

The second circuit to be presented is the pulse-amplitude modulator. This is similar to the amplitude modulator except that the circuit is optimized for pulse-handling efficiency. The last circuit will be a pulse-width modulator. This is a good modulator to use in digital systems which operate at fixed pulse voltages. It is also quite useful in high-power systems such as motor drives and switching power supplies.

18.1 AMPLITUDE MODULATOR

ALTERNATE NAMES AM modulator, linear modulator, linear amplitude modulator.

EXPLANATION OF OPERATION The carrier frequency is applied to the v_c terminal as shown in Fig. 18.1. The modulation input, at a lower frequency than v_c, is applied to v_m. An inverted replica of v_m appears at v_1. Its amplitude and offset are controlled by R_2 and R_4. The offset adjustment R_4 controls the modulation depth. The amplitude adjustment R_2 determines the final peak-to-peak amplitude of v_o.

On positive v_c cycles, switches S_1 and S_4 are turned on. In this state they look like a resistor (R_{on}) of 50 to 500 Ω, depending on the type of CMOS switch chosen. During this same time, switches S_2 and S_3 are off. In the off

state these devices look like a resistor (R_{off}) of many megohms. On negative v_c cycles just the opposite occurs: S_1 and S_4 are off and S_2 and S_3 are on.

Chopped versions of v_1 appear at v_2 and v_3. Figure 18.2 shows that v_2 and v_3 are chopped on opposite half cycles of v_c. The amplitudes of v_2 and v_3 are smaller than v_1 depending on the size of the $R_8/(R_6 + R_8)$ and $R_{11}/(R_7 + R_{11})$ ratios. Voltage waveform v_2 is then inverted to create v_4. Waveforms v_3 and v_4 are combined in the summing amplifier A_4. Figure 18.2 shows the final v_o result. The peak-to-peak magnitude of v_o can again be adjusted using R_{12}, if required.

The only significant error source in this circuit is the magnitudes of R_{on} and R_{off} relative to R_6, R_7, R_8, and R_{11}. For example, when S_1 is off and S_2 is on, the voltage at v_2 should be zero. Instead, it is approximately $v_2(\text{off}) \approx v_1 R_{on}/R_{off}$. Conversely, when S_1 is on and S_2 is off, the voltage at v_2 should be exactly $R_8/(R_6 + R_8)$. In this case switch errors give us $v_2(\text{on}) \approx v_1 R_8/(R_{on} + R_6 + R_8)$. If R_8 is small, the error is significant. The errors at v_3 are similar in nature and are listed in the design equations.

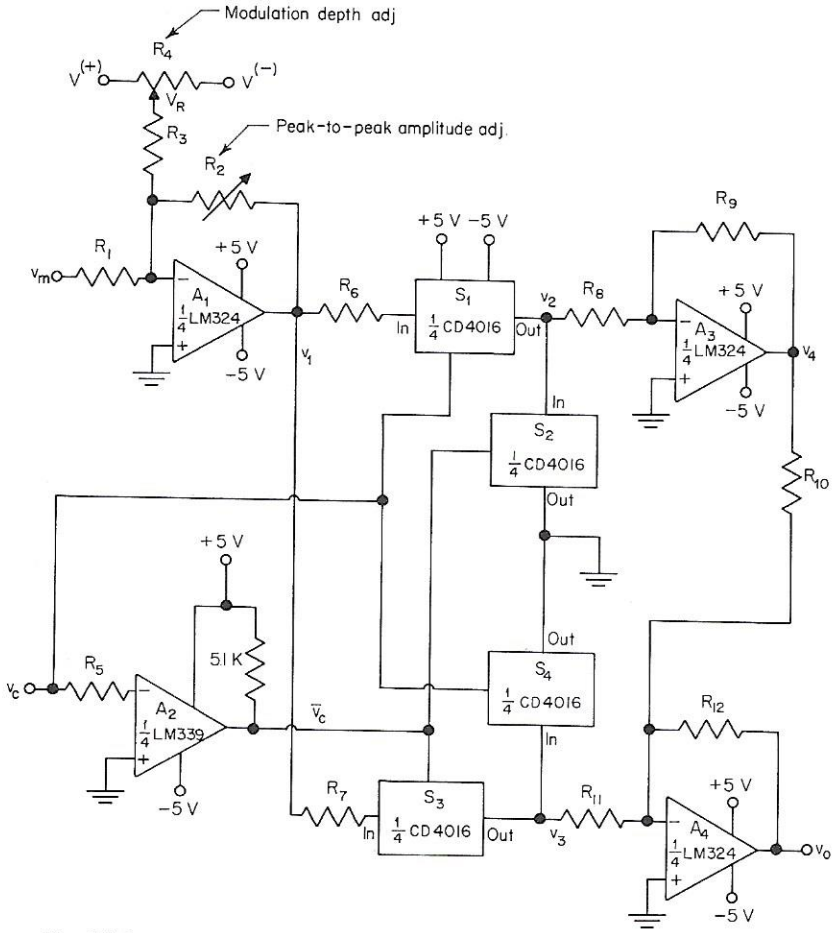

Fig. 18.1 A precision amplitude modulator which uses CMOS switches.

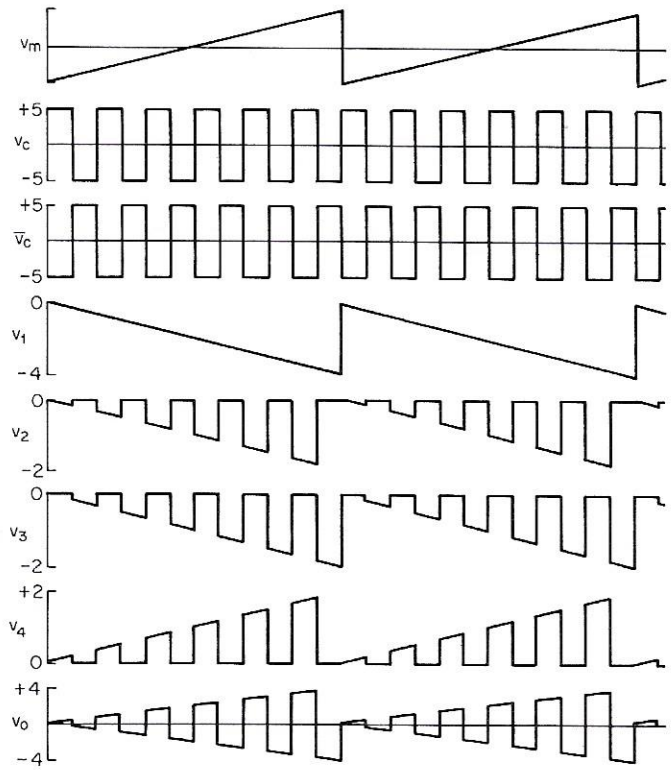

Fig. 18.2 Voltage waveforms at various locations in Fig. 18.1. A sawtooth modulation waveform is assumed.

DESIGN PARAMETERS

Parameter	Description
A_1	Buffer amplifier which sets modulation depth and system gain
A_2	Comparator used to invert v_c
A_3	Amplifier used to invert v_2
A_4	Summing amplifier used to combine v_3 and v_4
I_{b4}	Input bias current of A_4
R	Common value for R_6 to R_{11}
R_1 to R_2	Determines system gain for v_m
R_3 to R_4	Sets modulation depth
R_5	Limits current into A_2
R_6, R_8 to R_{10}	Establishes magnitude of negative portion of output waveform
R_7, R_{11}	Establishes magnitude of positive portion of output waveform
R_{12}	Can be used in conjunction with R_2 to adjust system gain
R_{on}, R_{off}	S_1 to S_4 on and off resistances
R_{in}	Input resistance seen by v_m input
S_1 to S_4	CMOS switches
v_o	Circuit output-voltage waveform
Δv_o	DC offset in v_o caused by A_4
v_1 to v_4	Voltage waveforms as shown in Figs. 18.1 and 18.2
v_c, $\bar{v}_c$	Carrier input voltage and its inverse

Parameter	Description
v_m	Modulation input voltage
V_N	Most negative value of V_R
V_P	Most positive value of V_R
V_R	Reference voltage used to adjust modulation depth
$V^{(+)}$	Power-supply voltages

DESIGN EQUATIONS

Eq. No.	Description	Equation
1	Output voltage v_o when S_1 is on and S_2 is off (neglecting switch errors and op amp errors)	$v_o(-) = \frac{-R_2 R_9 R_{12}}{R_{10}(R_6 + R_8)} \left(\frac{v_m}{R_1} + \frac{V_R}{R_3}\right)$
2	Output voltage v_o when S_3 is on and S_4 is off (neglecting switch errors and op amp errors)	$v_o(+) = \frac{R_2 R_{12}}{(R_7 + R_{11})} \left(\frac{v_m}{R_1} + \frac{V_R}{R_3}\right)$
3	Peak-to-peak output voltage v_o when switch errors are included	$v_o(\pm) \approx \frac{\pm R_2 R_{12} R_{\text{off}}}{(R + R_{\text{on}})(R + R_{\text{off}}) + R\,R_{\text{off}}} \left(\frac{v_m}{R_1} + \frac{V_R}{R_3}\right)$
4	Voltage v_1 as a function of v_m and V_R	$v_1 = -R_2 \left(\frac{v_m}{R_1} + \frac{V_R}{R_3}\right)$
5	Voltage v_2 while S_1 is on and S_2 is off	$v_2 = \frac{R_8 v_1}{R_6 + R_8}$
6	Voltage v_3 while S_3 is on and S_4 is off	$v_3 = \frac{R_{11} v_1}{R_7 + R_{11}}$
7	Voltage v_4	$v_4 = -\frac{R_9 v_2}{R_8}$
8	Voltage v_o	$v_o = -R_{12} \left(\frac{v_4}{R_{10}} + \frac{v_3}{R_{11}}\right)$
9	Resistor values R_1	$R_1 \geqq R_{\text{in}}$ required
10	R_2	$R_2 < \frac{R_1(\lvert V^{(\pm)}\rvert - 2)}{\lvert v_m\rvert \text{ max}}$ or $< \frac{R_3(\lvert V^{(\pm)}\rvert - 2)}{\lvert V_R\rvert_{\text{max}}}$ whichever is smaller
11	R_3, R_4	$R_3 = R_4 = R_1$
12	R_5	R_5 = zero to 100 kΩ (use manufacturer's recommendation for A_2)
13	R_6 to R_{11}	$R = R_6 = R_7 = R_8 = R_9 = R_{10} = R_{11} = (R_{\text{on}}\,R_{\text{off}})^{1/2}$
14	R_{12}	$R_{12} = 2R_{11}$
15	Output offset due to I_{b4}	$\Delta v_o = I_{b4}\,R_{12}$

DESIGN PROCEDURE

We assume all op amps are operating from the same $V^{(\pm)}$ supplies. If a larger output is required, all stages or perhaps only A_4 can be connected to higher-

voltage supplies. Fewer power supplies are required if the comparator (A_2), the four switches, and the three op amps can use the same voltages.

DESIGN STEPS

Step 1. Choose a comparator, switches, and op amps which utilize the same supply voltages. The ± supply voltages must be at least 2 V higher than the ± peak values expected at v_o.

Step 2. Choose R_1 to be greater than or equal to the minimum allowed input resistance at v_m.

Step 3. Choose a range of values for V_R which is slightly larger than the expected positive and negative peaks of v_m. Set V_P and V_N equal to the two limits of this range.

Step 4. Use Eqs. 11 and 12 to obtain values for R_3, R_4, and R_5. Resistor R_5 is usually between 1 and 5 kΩ, but the comparator (A_2) specification sheet should be consulted.

Step 5. Solve both portions of Eq. 10 to determine an optimum value for R_2. Let R_2 be less than the smaller value calculated.

Step 6. Use the CMOS switch specification to estimate R_{on} and R_{off} for these particular values of $V^{(\pm)}$, v_1(max), and $\pm v_c$. Calculate values for R_6 through R_{11} using Eq. 13.

Step 7. Rearrange Eq. 1 as follows to compute a value for R_{12} (let $R = R_6 = R_8 = R_9 = R_{10}$):

$$R_{12} = \frac{4\ R\ R_1\ v_o(\text{peak})}{3\ R_2\ v_m(\text{peak})}$$

To rearrange this equation, we assumed the nominal value for V_R would be $v_m/2$.

If R_{12} is too large, the bias current of A_4 will cause an output offset. Calculate this offset using $\Delta v_o = I_{b4}\ R_{12}$. If the offset is more than can be tolerated, decrease R_{12} until a satisfactory offset is achieved. This change will lower the overall circuit gain, so an opposite change to the circuit transfer function must be made elsewhere. The best option is to lower all the R resistors by the same magnitude that R_{12} was lowered. This will slightly increase switching errors, but this is usually of less concern than a dc offset in v_o.

Step 8. Solve Eqs. 1 and 2 to make sure the correct positive and negative peak output voltages will be achieved.

Step 9. Solve Eq. 3 to determine the worst-case expected errors in v_o.

EXAMPLE OF AN AM MODULATOR DESIGN Suppose we wish to modulate a 2-kHz carrier with transponder information between 3 and 100 Hz. The modulation signal has a maximum peak-to-peak amplitude of 4 V. The modulated carrier is required to have a peak-to-peak amplitude of 6 V.

Design Requirements

$v_m = \pm 2$ V centered on zero
$v_o = \pm 3$ V centered on zero
$V^{(\pm)} = \pm 5$ V
$R_{in} \geq 5{,}000\ \Omega$
$\Delta v_o(\text{max}) = \pm 0.1$ V

Device Data (+25°C)

$R_{on} = 580\ \Omega$
$R_{off} = 4 \times 10^8\ \Omega$ (125-nA leakage with 5 V)
$I_{b4} = 500$ nA (out of device, since this op amp has a PNP input stage)

Step 1. We choose one-fourth of an LM339 quad comparator for A_2. This device works quite well from supply voltages of ±5 V. If a ±5-V v_c is not available, the other three sections of the comparator can be utilized to square up and level shift the carrier input to the proper waveform. The 4016 quad CMOS switch is used for S_1 through S_4. Three sections of the LM324 quad op amp are utilized for A_1, A_3, and A_4. Both these devices also operate fairly efficiently from ±5 V. Slightly better performance can be achieved in switch performance using ±10 V, however.

Step 2. We will let $R_{in} = R_1 = 10$ kΩ. This satisfies the 5-kΩ minimum input resistance.

Step 3. We will let $V_P = +5$ V and $V_N = -5$ V so that the same supply voltages can be used. This means, of course, that the ±5 V must now be regulated. Otherwise, the depth of modulation (percent modulation) will vary with supply voltage.

Step 4. Equation 11 provides us with $R_3 = R_4 = R_1 = 10$ kΩ. For the LM339 comparator we can let $R_5 =$ zero.

Step 5. The two portions of Eq. 10 are computed as follows:

$$R_2 < \frac{R_1[|V^{(\pm)}| - 2]}{|v_m| \text{ max}}$$

$$< \frac{10^4\,(5-2)}{2}$$

$$< 15{,}000\ \Omega$$

Also,

$$R_2 < \frac{R_3[|V^{(\pm)}| - 2]}{|V_R| \text{ max}}$$

$$< \frac{10^4\,(5-2)}{5}$$

$$< 6{,}000\ \Omega$$

We therefore let $R_2 = 5{,}000\ \Omega$.

Step 6. The common value for R_6 through R_{11} is $R = (R_{on}R_{off})^{1/2} = 482$ kΩ.

Step 7. A value for R_{12} is found from

$$R_{12} = \frac{4RR_1\,v_o(\text{peak})}{3R_2\,v_m(\text{peak})} = \frac{4(482{,}000)10^4(3)}{3(5{,}000)\,2} = 1.928\ \text{MΩ}$$

This resistance seems quite high, so we now calculate the dc offset in v_o due to A_4 input bias current:

$$v_o = I_{b4}R_{12} = (-5 \times 10^{-7})\ 1.928 \times 10^6 = -0.965\ \text{V}$$

This is about ten times too large, so we make the following resistor changes (these changes will lower Δv_o to 0.0964 V):

$$R_{12} = 193\ \text{kΩ}$$
$$R = R_6 = R_7 = R_8 = R_9 = R_{10} = R_{11} = 48\ \text{kΩ}$$

Step 8. As a double check on our calculations above, we put values into Eqs. 1 and 2 to find the peak-to-peak v_o (assume $V_R = v_m(\text{peak})/2$)

$$v_o(-) = \frac{-R_2R_9R_{12}}{R_{10}(R_6 + R_8)}\left[\frac{v_m(\text{peak})}{R_1} + \frac{v_m(\text{peak})}{2\,R_3}\right]$$

$$= \frac{-5{,}000(48{,}000)193{,}000}{48{,}000(48{,}000 + 48{,}000)}\left[\frac{2}{10^4} + \frac{2}{2(10^4)}\right] = -3.015625\ \text{V}$$

$$v_o(+) = \frac{R_2 R_{12}}{R_7 + R_{11}} \left[\frac{v_m(\text{peak})}{R_1} + \frac{v_m(\text{peak})}{2\,R_3} \right]$$

$$= \frac{5{,}000(193{,}000)}{48{,}000 + 48{,}000} \left[\frac{2}{10^4} + \frac{2}{2(10^4)} \right] = +3.015625 \text{ V}$$

These peak voltages can be trimmed if R_2 or R_{12} is made adjustable.

Step 9. The peak-to-peak output voltage with switch errors accounted for is now calculated using Eq. 3:

$$v_o(\pm) \approx \frac{\pm R_2 R_{12} R_{\text{off}}}{(R + R_{\text{on}})(R + R_{\text{off}}) + R R_{\text{off}}} \left[\frac{v_m(\text{peak})}{R_1} + \frac{v_m(\text{peak})}{2\,R_3} \right]$$

$$\approx \frac{\pm 5{,}000(193{,}000)\ 4 \times 10^8}{(48{,}000 + 580)(48{,}000 + 4 \times 10^8) + 48{,}000(4 \times 10^8)} \left[\frac{2}{10^4} + \frac{2}{2(10^4)} \right]$$

$$\approx \pm 2.997334$$

Even though the R resistors had to be lowered by a factor of 10, the switch errors cause only an 18.2-mV error (3.015625 − 2.997334).

REFERENCES

1. Kelly, R. G.: Linear Modulator Has Excellent Temperature Stability, *EEE*, July 1968, p. 102.
2. Althouse, J.: Linear Amplifier Circuit Eliminates Transformers, *Electronics*, Mar. 21, 1966, p. 99.

18.2 PULSE-AMPLITUDE MODULATOR

ALTERNATE NAMES Pulse-height modulator, PAM, analog gate, gated amplifier, single-channel multiplexer, sampling gate.

EXPLANATION OF OPERATION This circuit is quite similar to the amplitude modulator in the previous section. In this case, however, a unipolar output is required; so the circuit is about 50 percent the size of Fig. 18.1. The pulses are applied to v_c and the modulation waveform drives the circuit at v_m. For the circuit shown in Fig. 18.3, v_c must cross through zero. If a logic circuit such as a TTL device is driving v_c, the + input of A_2 should be biased to +1.4 V. The object, of course, is to switch A_2 on and off so that $\bar{v}_c$ (an inverted v_c) appears at its output.

The modulation input v_m can be centered about zero, or it can be exclusively positive or negative. The modulation depth adjustment R_4 is used to place v_1 at the correct bias point.

Each time v_c goes high, S_1 turns on and S_2 turns off. During this time the voltage at v_2 is $v_1 R_6/(R_5 + R_6)$. In between pulses, when v_c is low, S_1 is off and S_2 is on. During this time the voltage at v_2 is very small ($\approx v_1 R_{\text{on}}/R_{\text{off}}$). The voltage at v_o is inverted with a magnitude of $v_o = -v_2 R_7/R_6$.

DESIGN PARAMETERS

Parameter	Description
A_1	Amplifier which controls the modulation gain and the depth of modulation
A_2	Comparator used to invert v_c
A_3	Buffer amplifier used to provide a low circuit output resistance and a constant load resistance to the switch circuit
I_{b3}	Input bias current of A_3