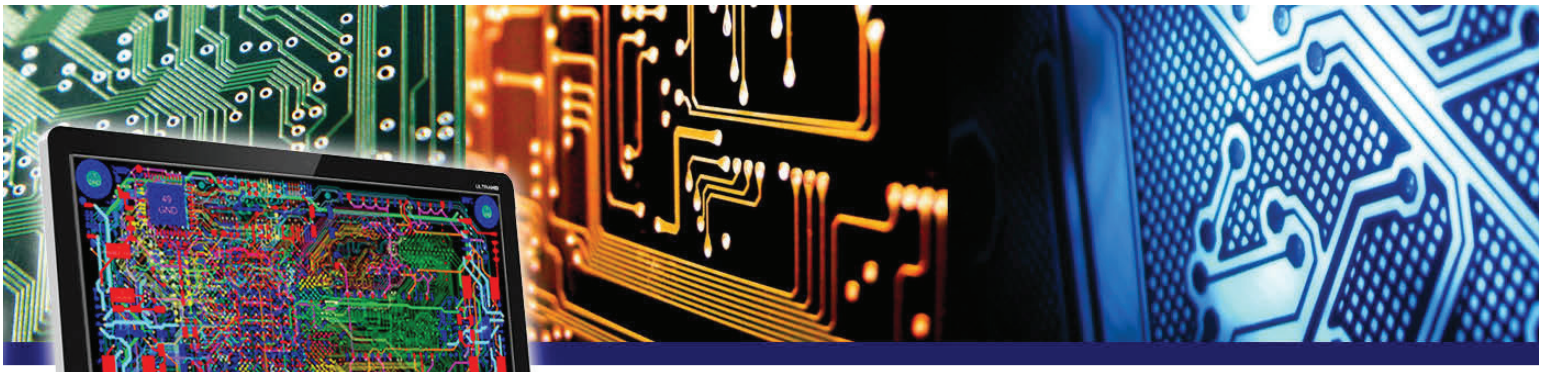

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Ground Pours - To pour or not to pour?

Barry Olney | In-Circuit Design Pty Ltd | Australia

Copper ground pours are created by filling open unused areas with copper generally on the outer layers of the board then connecting the copper fill with stitching vias to ground. Usually, small isolated areas < 2.5 mm square are deleted automatically by the software during the pouring operation.

Some PCB Designers do this as a matter of habit stating that they have always done this for various reasons. Also, many reference designs supplied by chip manufacturers use this ground pour technique so you may need to follow their recommendations if you want the design to work especially at high speeds – WRONG!

Below is a short list of some of the pros and cons often heard.

Possible advantages of copper pours:

- Provides additional shielding and noise reduction if there are internal signal layers.
- Provides some additional heat sinking.
- Uses less etchant during PCB fabricating.
- Reduces the possibility of PCB warping during reflow by balancing the amount of continuous copper on each side of the board.

Possible disadvantages of copper pours:

- Patch antennas resemble a ground pour. These small areas may act as antennae and emit noise.
- If the copper is thick, the full perimeter heat sink makes desoldering in repair and service operations more difficult unless thermal reliefs are used.
- Every via blocks potential routes (unless blind and buried vias are used), so stitching makes everything more difficult.

Other issues to consider:

Poured ground is useful on two layer boards that lack solid reference planes. It reduces crosstalk due to capacitive coupling. Ground pours work particularly well in high impedance, analogue designs (analogue to digital converters, switch mode power supplies etc) that lack solid planes. If these devices are present on a multilayer digital board they need to be isolated from the digital circuitry.

On a multilayer board with solid power and ground planes, the ground pour serves no purpose as there is already a solid plane of metal covering the entire board area. The ground pour simply raises that same, grounded metal up one layer to the surface of the board, instead of leaving it down on layer 2.

In the multilayer digital environment, ground pours do not significantly reduce crosstalk. Also, ground pours have the disadvantage of altering the impedance of traces that run adjacent to a ground pour area causing reflections.

Fig. 1 below illustrates how the electric fields (blue) and the magnetic fields (red) terminate or couple to the nearest metal object. The electric field on the microstrip signals (outer layer on left) mainly terminates on the ground plane while the magnet field also couples to the nearby trace. This is the desired affect when using differential signals but not if you use discontinuous ground pours.

The remaining electric and magnetic fields radiate from the microstrip signals causing noise or electromagnetic emissions.

Reducing this field coupling requires continuous return current conductors running parallel to the signal traces over the entire board, keeping the return current close to the source signal current. Solid reference planes provide this function. Isolated, discontinuous regions of ground pours do not help reduce the field coupling between traces or radiation from the board.

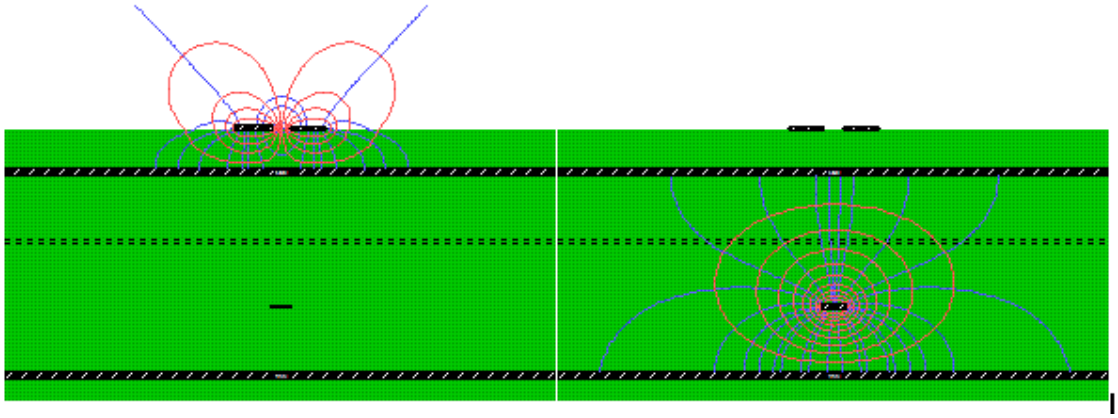


Fig. 1 The electric fields (blue) and the magnetic fields (red) of aggressor nets.

Please note that the embedded stripline signal (right) causes all electric and most of the magnetic fields to terminate in the planes above and below almost totally eliminating noise or electromagnetic emissions. Using embedded stripline signals typically reduces the EMI by approximately 45db compared to outer layer microstrip signals (all other factors being equal).

Let's take a look at how the impedance of the trace adjacent to the ground pour changes in value.

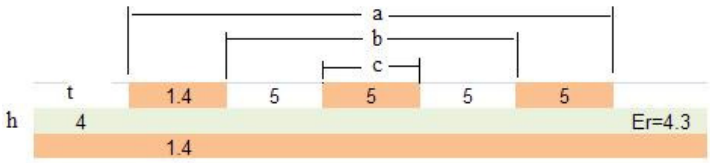
In the screenshot below (Fig. 2), I have used the ICD Stackup Planner (available for download from www.icd.com.au) to calculate the characteristic impedance (Zo) of a single trace on the outer layer of a multilayer PCB.

ICD Stackup Planner – www.icd.com.au 20/10/2010

Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
1	Top	Conductive			1.4	5	5	58.46	100.02		Signal
		Dielectric	4.3	4							Prepreg
2	GND	Conductive			1.4						Plane

Fig. 2 Microstrip trace on outer layer of the board

In this case, the Zo is 58.46 ohm. If we run another signal close (5 MIL) to the single trace then the differential impedance is 100.02 ohm. From this we can assume that the odd mode impedance of each trace is then half the differential impedance making them 50.01 ohms each. So, we can see that the impedance decreases as copper comes into the proximity of the lone trace just as it decreases when we reduce the signal layer to plane layer spacing. Also, as the coupling increases, the single ended impedance won't change but the odd mode impedance decreases.



where

a = 25	b = 15
c = 5	t = 1.4
h = 4	Er=4.3

Fig. 3 Symmetric coplanar waveguide with ground plane

The following equations are use to determine the impedance of the symmetric coplanar waveguide with ground plane illustrated in Fig.3.

$$Zo = \frac{\eta o}{2 * \sqrt{Eeff}} * \left[\frac{1}{\frac{K(k1)}{K(k1')}} + \frac{1}{\frac{K(k2)}{K(k2')}} + \frac{1}{\frac{2 * t}{b - a}} \right]$$

where

$$Eeff = \frac{\frac{K(k1)}{K(k1')} + \frac{Er * K(k2)}{K(k2')} + \frac{2 * t}{b - a}}{\frac{K(k1)}{K(k1')} + \frac{K(k2)}{K(k2')} + \frac{2 * t}{b - a}}$$

$$k1 = \frac{c}{b} \sqrt{\frac{b^2 - a^2}{c^2 - a^2}}$$

$$k2 = \frac{\tanh\left(\frac{\pi * a}{4 * h}\right)}{\tanh\left(\frac{\pi * b}{4 * h}\right)}$$

$$kn' = \sqrt{1 - kn^2}\,, n = 1\,, 2$$

Solving the above equations for Zo, given the stated variables, returns a Zo = 43.45 ohm. Increasing the width of the ground pour on either side of the middle trace has little affect on Zo.

The difference in impedance for the possible senarios represents a maximum variation of 26% in Zo.

Lone trace	Zo = 58.46 Ω
Ground pour on one side	Zo = 50.01 Ω
Ground pour on both sides	Zo = 43.45 Ω

In conclusion, ground pours may be effective on high impedance, analogue two layer boards but do not significantly reduce crosstalk on high speed, low impedance digital multilayer boards. Also, ground pours have the disadvantage of altering the impedance of traces that run adjacent to a ground pour area causing reflections and are therefore not recommended for use in the digital domain.

References:

Transmission Line Design Handbook – Brian Wadell
High Speed Digital Design – A Handbook of Black Magic – Howard Johnson
ICD Stackup Planner (available for download from www.icd.com.au)