$\vec{A} = \begin{Bmatrix} a_1 \\ a_2 \\ \vdots \\ a_{256} \end{Bmatrix}$ $\vec{B} = \begin{Bmatrix} b_1 \\ b_2 \\ \vdots \\ b_{256} \end{Bmatrix}$ $\vec{A} - \vec{B} = \begin{Bmatrix} a_1 - b_1 \\ a_2 - b_2 \\ \vdots \\ a_{256} - b_{256} \end{Bmatrix}$ 256 subtractions

Problem C)

a) In an AArch32 Advanced SIMD program, this for-loop needs to iterate 4 time(s) for subtraction (assuming that the processor does not handle the vector operation beyond its capacity in terms of the number of vector registers).

b) To execute a vector instruction (e.g. VSUB) in an iteration of this for-loop, the AArch32 processor with the Advanced SIMD extension needs to use its ALU 64 time(s) for subtractions.

c) Each time when it is used, the ALU of the AArch32 processor with the Advanced SIMD extension substracts 1 pair(s) of elements.

→ each time only one at a time

Have 128 vector registers (16 bit numbers)

128/2 because 64 for Vector A, 64 for Vector B

Loop

64 for each iterations, to get to 256, 4 iterations