

VIETNAM NATIONAL UNIVERSITY HO CHI MINH CITY  
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY  
FACULTY OF COMPUTER SCIENCE AND ENGINEERING



## Electrical Electronic Circuits

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### Lab Report

## Lab 3

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## Listings

## 1 BJT in Saturation Mode

Change the value of  $R_1$  to  $1 \text{ k}\Omega$  and run the simulation again. Capture the simulation results and explain the values of  $I_B$ ,  $I_C$ , and  $V_{CE}$ . The default transistor gain is  $\beta = 100$ , and the saturation voltages are  $V_{CE(\text{sat})} = 0.65 \text{ V}$  and  $V_{BE} = 0.7 \text{ V}$ .

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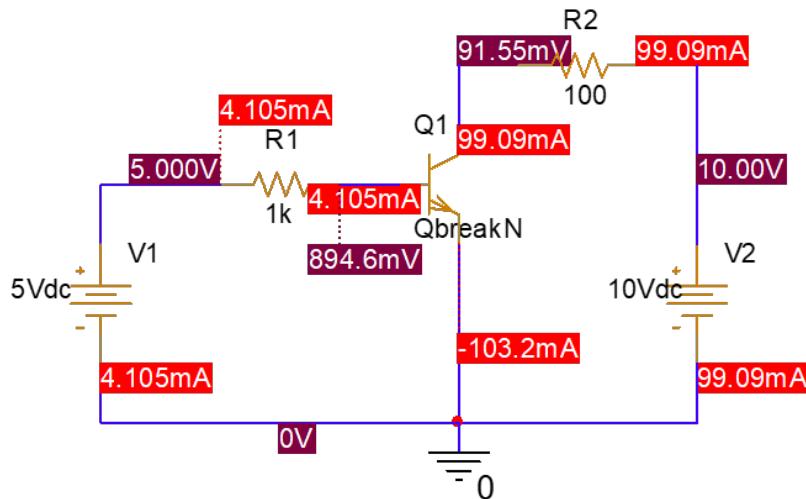


Figure 1.1: Simulation results for the BJT when  $R_1 = 1 \text{ k}\Omega$ .

The results in PSpice are explained as follows:

- According to Ohm's Law,

$$I_B = \frac{V_{CC} - V_{BE}}{R_1} = \frac{5V - 0.7V}{1k\Omega} = 4.3\text{mA}$$

- It is assumed that the transistor is in linear (or active) mode,

$$I_C = \beta \cdot I_B = 100 \cdot 4.3 \text{ mA} = 430 \text{ mA} = 0.43 \text{ A}$$

- Finally, in order to confirm the assumption above,

$$V_{CE} = V_{CC} - I_C \cdot R_2 = 10V - 0.43A \cdot 100\Omega = -33V$$

Since  $V_{CE} < 0$ , our assumption is not correct. The transistor stays in saturation mode. Therefore,  $I_C$  is determined as follows:



$$I_C = \frac{V_{CC} - V_{CE(\text{sat})}}{R_2} = \frac{10\text{V} - 0.65\text{V}}{100\Omega} = 93.5\text{mA}$$

## 2 DC Sweep Simulation

The schematic in the first exercise with  $R1 = 1k$  is re-used in this exercise. However, a DC-Sweep simulation mode is performed with V1 is varied from 0V to 5V (0.1V for the step), as follows:

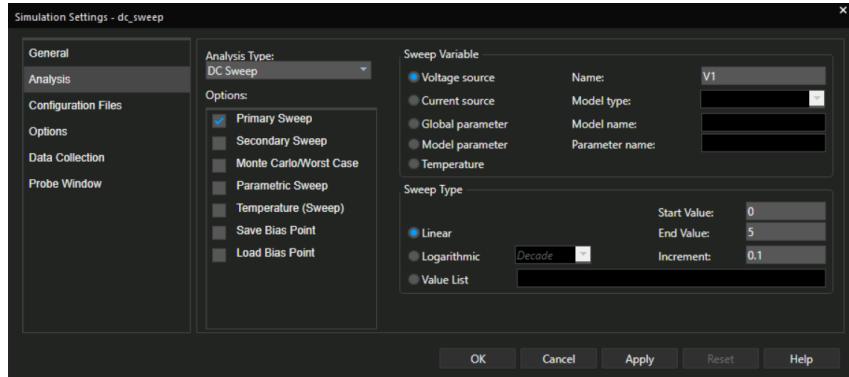


Figure 2.1: DC-Sweep profile for simulation.

Run the simulation and trace for the current  $I_C$  according to the value of V1. Capture your screen and plot it in the report. Please increase the width of the curve.

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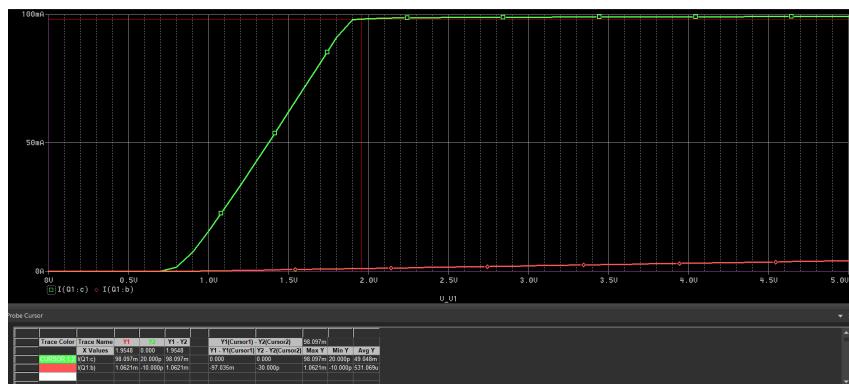


Figure 2.2: DC-Sweep simulation results for  $I_C$ .

When the transistor becomes saturated, the value of V1 is about to 1.95V.  
At this value, the value of  $I_B$  is about to 1.06mA  
And the value of  $I_{C(sat)}$  is about to 98mA

### 3 Exercise 3: BJT used at Switch

For a given BJT circuit, determine  $R_1$  and  $R_2$  so that  $I_C$  is saturated at 50 mA. In this saturation mode  $V_{CE(sat)}$  is 30 mV. Assume that  $V_{BE} = 0.7$  V and the current gain  $\beta = 100$ .

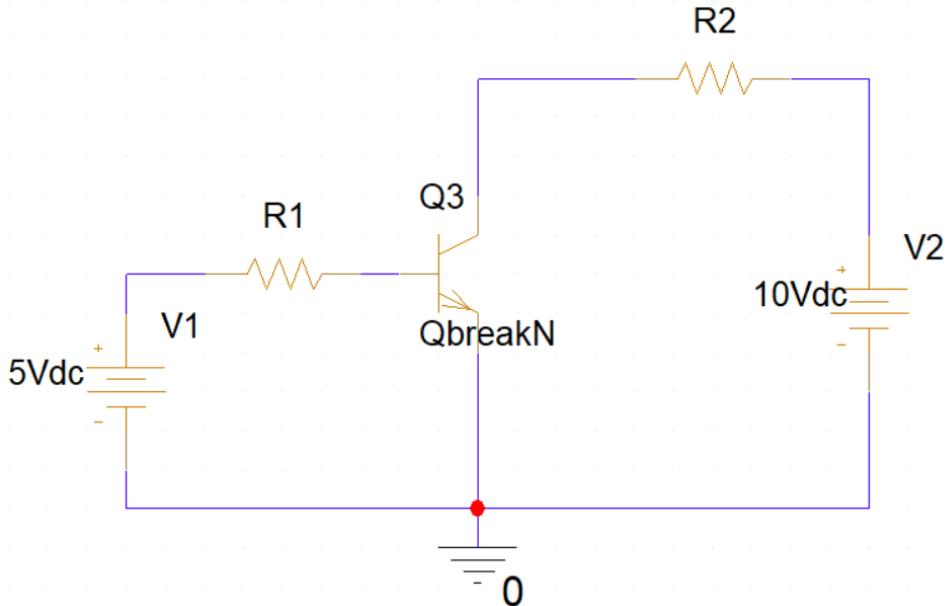


Figure 3.1: BJT used as switch in saturation mode

#### 3.1 Solution

In saturation mode, we have:

$$V_{CE(sat)} = 30 \text{ mV}$$

$$I_C = 50 \text{ mA}$$

$$V_{BE} = 0.7 \text{ V}$$

$$\beta = 100$$

Applying KVL, we have:

$$V_2 = I_C * R_2 + V_{CE(sat)}$$

$$10V = 50 \text{ mA} * R_2 + 30 \text{ mV}$$

$$R_2 = 199,4 \Omega$$



Applying KVL, we have:

$$V_1 = I_B * R_1 + V_{BE}$$

$$I_B = \frac{I_C}{\beta} = \frac{50 \text{ mA}}{100} = 0.5 \text{ mA}$$

$$5V = 0.5 \text{ mA} * R_1 + 0.7 \text{ V}$$

$$R_1 = 8.6 \text{ k}\Omega$$

Thus, we have:

$$R_1 = 8.6 \text{ k}\Omega$$

$$R_2 = 199.4 \text{ }\Omega$$

### 3.2 Simulation

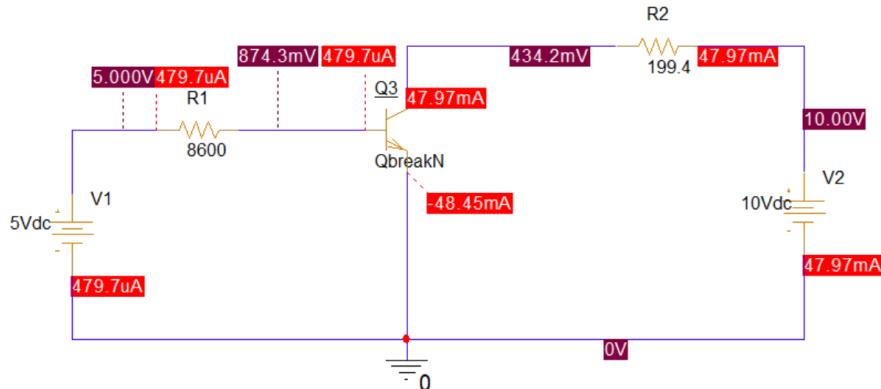


Figure 3.2: Simulation result of Exercise 3

From the simulation result in Figure 3.2, we can see that  $I_C$  is not 50 mA and  $V_{CE}$  is not 30 mV as calculated. Because the real SPICE model does not keep  $V_{BE}$ ,  $\beta$ , or  $V_{CE(\text{sat})}$  fixed as assumed in the hand calculation. The actual base current is not large enough to force saturation, so  $I_C$  and  $V_{CE}$  differ from the calculated values.

## 4 Drive a device with an NPN BJT

This exercise has a 5 V logic output (the  $V_{ter}$  in Figure 4.1) that can source up to 10 mA of current without a severe voltage drop and can withstand a maximum current of 20 mA. If the logic terminal sources a current larger than 20 mA, it would be damaged. If it sources a current larger than 10 mA, the  $V_{ter}$  voltage will drop to less than 4 V; we should avoid this drop in many cases. However, this logic terminal has to be used to drive an electrical component with an equivalent internal resistance of  $5\Omega$  (the LOAD in Figure 1.6) and requires a current of at least 300 mA and not exceeding 500 mA to function normally. Given that we have an NPN transistor with the current gain  $\beta = 100$ , the maximum collector current  $I_C$  is 400 mA, and the barrier potential at the BE junction is  $V_{BE} = 0.7$  V, select a resistor available on the market to replace the resistor  $R_B$  shown in Figure 1.6 to make the circuit function well. After that, perform a simulation to double-check your selection.

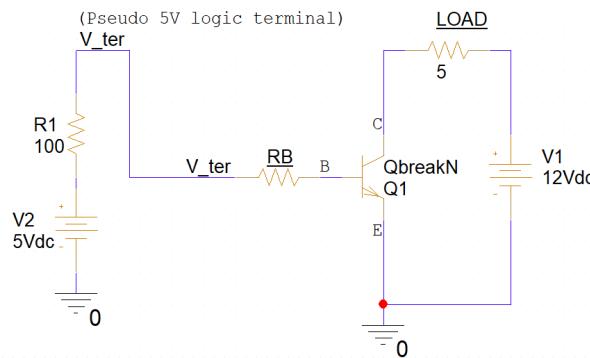


Figure 4.1: Select a resistor available in the market for  $R_B$ .

### 4.1 Theory calculations

#### **Notes:**

*Explanations, formulas, and equations are expected rather than only results.*

The load requires a collector current in the range:

$$300 \text{ mA} < I_L < 500 \text{ mA}$$

However, the transistor used can only provide a maximum collector current of:

$$I_{C(\max)} = 400 \text{ mA}$$



Therefore, the allowable collector-current range is:

$$300 \text{ mA (min)} < I_C < 400 \text{ mA (max)}.$$

With the transistor current gain  $\beta = 100$ , the corresponding base-current range is:

$$\frac{I_{C(\min)}}{\beta} = \frac{300 \text{ mA}}{100} = 3 \text{ mA (min)} < I_B < \frac{I_{C(\max)}}{\beta} = \frac{400 \text{ mA}}{100} = 4 \text{ mA (max)}.$$

According to the circuit in Figure 4.1, the base current is

$$I_B = \frac{V_2 - V_{BE}}{R_1 + R_B} = \frac{5 \text{ V} - 0.7 \text{ V}}{100 \Omega + R_B}.$$

With  $I_{B(\min)} = 3 \text{ mA}$ , we have

$$100 \Omega + R_{B(\max)} = \frac{5 \text{ V} - 0.7 \text{ V}}{3 \text{ mA}} = \frac{4.3 \text{ V}}{3 \text{ mA}} \approx 1433 \Omega,$$

$$R_{B(\max)} \approx 1433 \Omega - 100 \Omega = 1333 \Omega = 1.33 \text{ k}\Omega.$$

With  $I_{B(\max)} = 4 \text{ mA}$ , we have

$$100 \Omega + R_{B(\min)} = \frac{5 \text{ V} - 0.7 \text{ V}}{4 \text{ mA}} = \frac{4.3 \text{ V}}{4 \text{ mA}} = 1075 \Omega,$$

$$R_{B(\min)} = 1075 \Omega - 100 \Omega = 975 \Omega = 0.975 \text{ k}\Omega.$$

Therefore, the base resistor must satisfy:

$$0.975 \text{ k}\Omega (\min) < R_B < 1.33 \text{ k}\Omega (\max).$$

$R_B$  selected is  $1 \text{ k}\Omega$ , which satisfies the above condition.

## 4.2 Simulation

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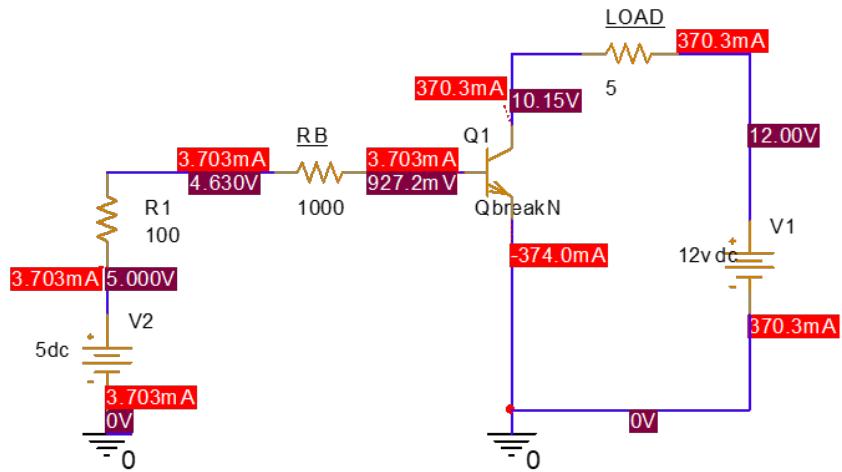


Figure 4.2: Simulation results with  $R_B = 1 \text{ k}\Omega$  (selected).

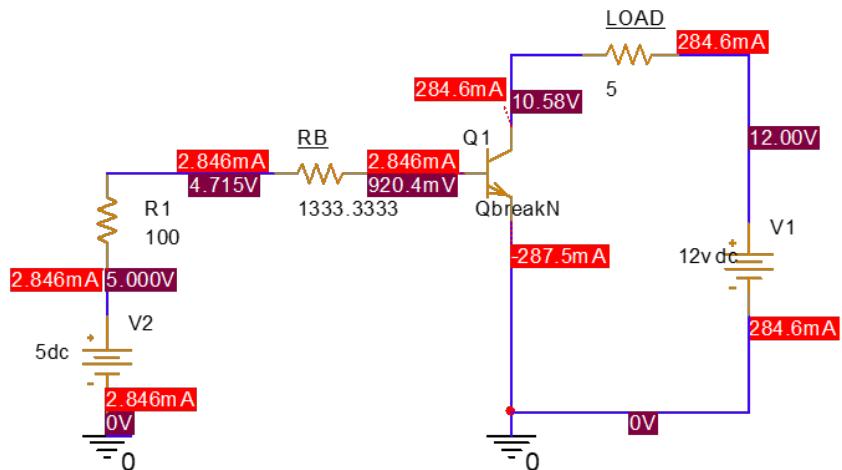


Figure 4.3: Simulation results with  $R_B$  max.

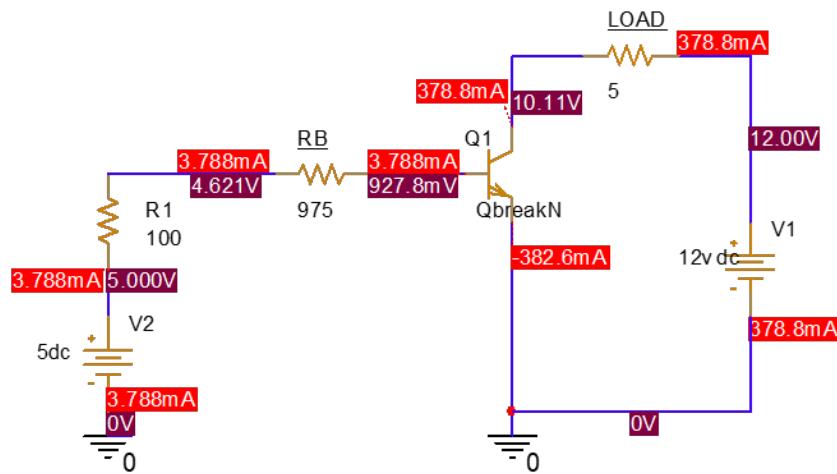


Figure 4.4: Simulation results with  $R_B$  min.

### 4.3 Compare

	Theory				PSpice		
	$R_B$	$V_{BE}$	$I_B$	$I_C$	$V_{BE}$	$I_B$	$I_C$
$R_{B(\min)}$	0.975 k $\Omega$	0.7 V	4.00 mA	400 mA	0.9278 V	3.788 mA	378.8 mA
$R_{B(\max)}$	1.33 k $\Omega$	0.7 V	3.00 mA	300 mA	0.9204 V	2.846 mA	284.6 mA
$R_{B(\text{selected})}$	1.00 k $\Omega$	0.7 V	3.91 mA	391 mA	0.9272 V	3.703 mA	370.3 mA

Table 4.1: Theory and PSpice comparison.

From Table 4.1, we can see that the PSpice simulation results are quite close to the theoretical calculations. The small differences may be due to the non-ideal characteristics of the transistor model used in the simulation.

## 5 Exercise 5: Simple bias configuration

The circuit given in 5.1 is known as a simple kind of NPN bias configuration. First, students simulate the circuit with two values of RC, respectively 10 Ohms and 1k Ohms. Then, give your statement on the change of the current  $I_E$  and explain the phenomena.

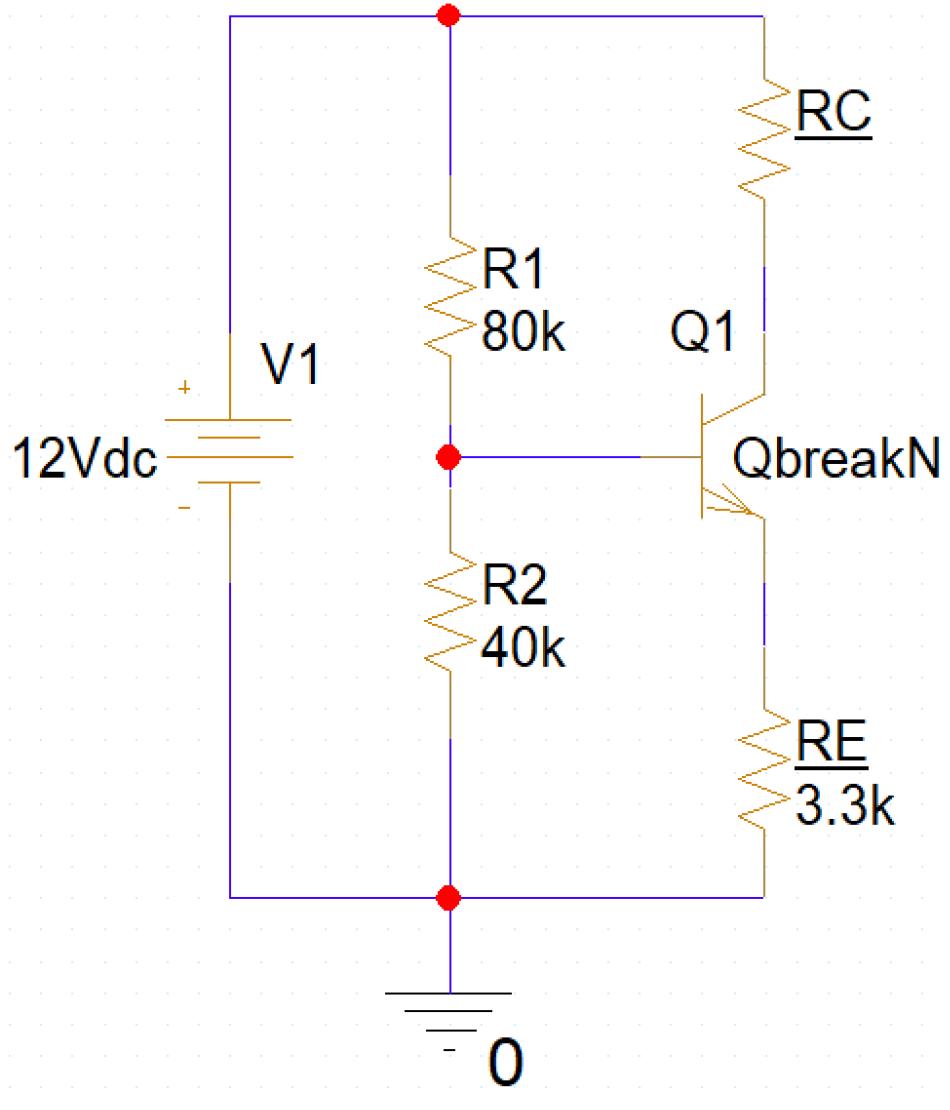


Figure 5.1: Simple bias configuration circuit

### 5.1 Simulation

With  $R_C = 10$  Ohms, the simulation result is shown in Figure 5.2.

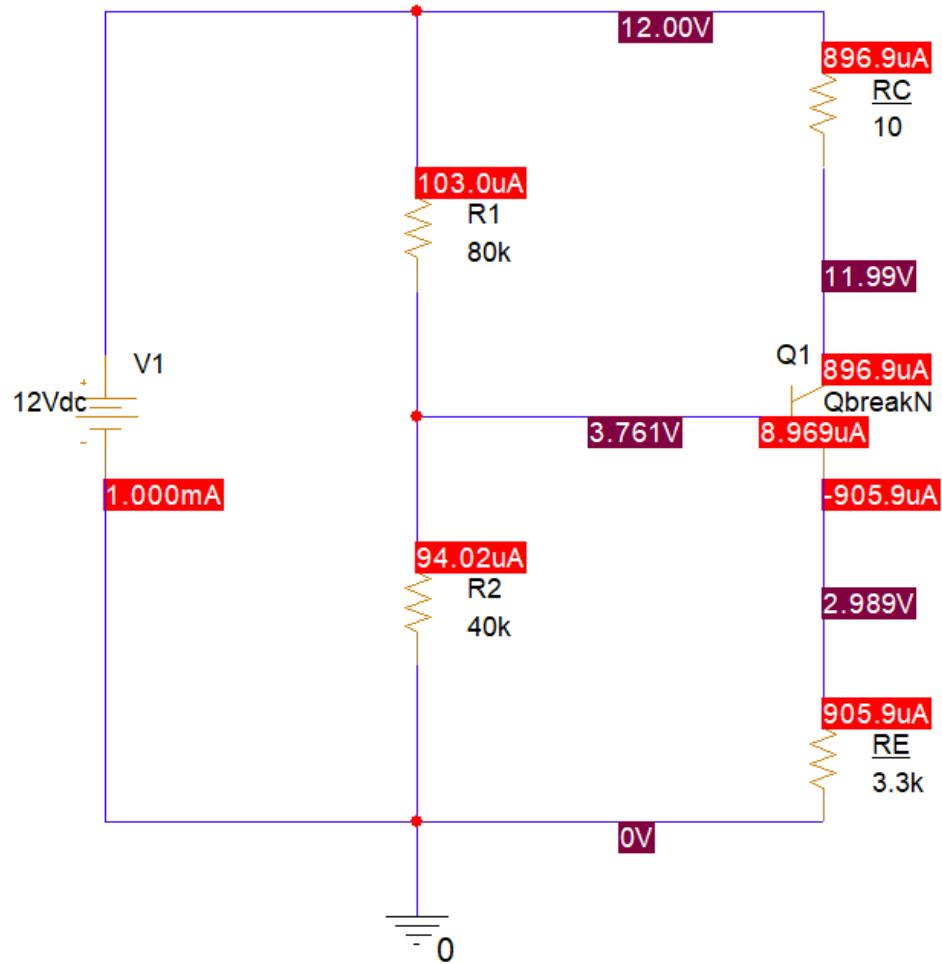


Figure 5.2: Simulation result with  $R_C = 10$  Ohms

With  $R_C = 1k$  Ohms, the simulation result is shown in Figure 5.3.

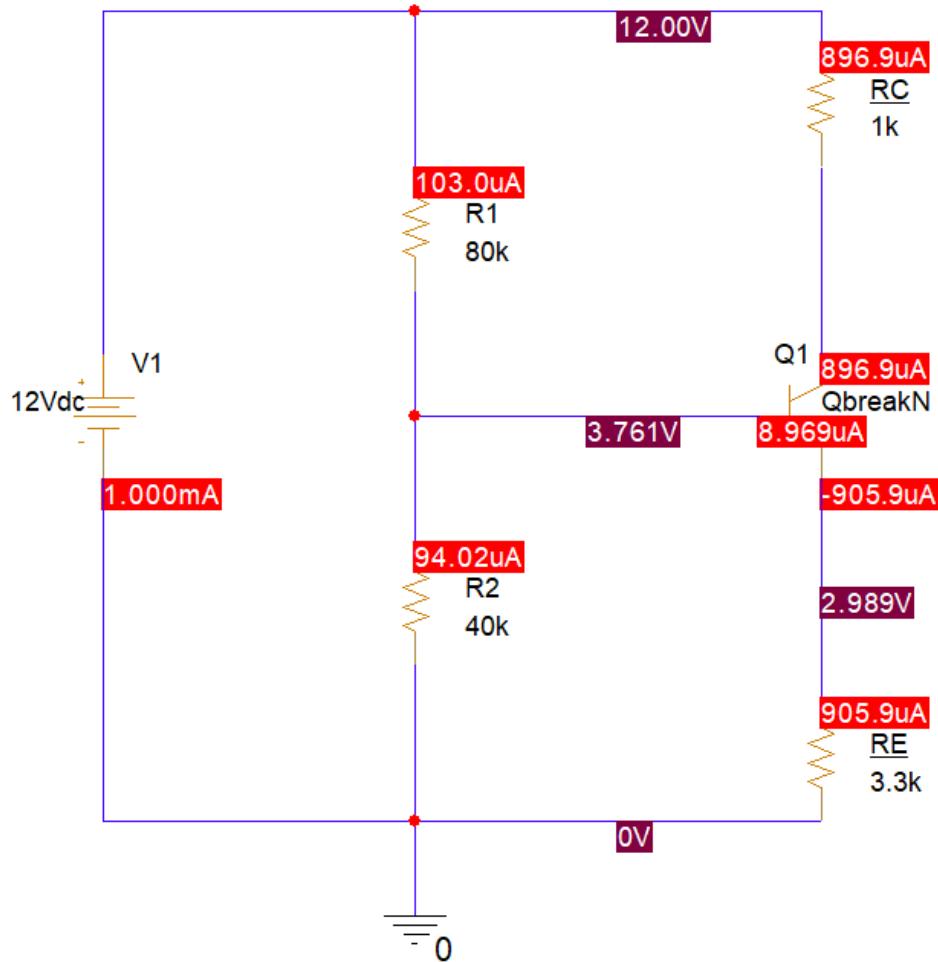


Figure 5.3: Simulation result with  $R_C = 1\text{k}$  Ohms

## 5.2 Circuit analysis

We will redraw the circuit as in Figure 5.4 for easier analysis, using Thevenin's theorem.

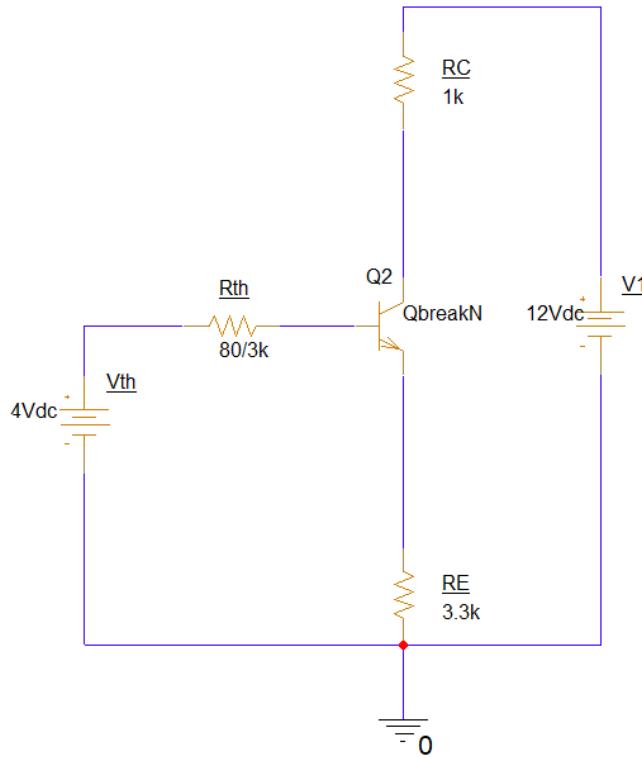


Figure 5.4: Thevenin equivalent circuit

Calculating Thevenin's equivalent voltage and resistance:

$$V_{TH} = V_{CC} * \frac{R_2}{R_1 + R_2} = 12V * \frac{10k\Omega}{80k\Omega + 40k\Omega} = 4V$$

$$R_{TH} = R_1 || R_2 = \frac{R_1 * R_2}{R_1 + R_2} = \frac{80k\Omega * 40k\Omega}{80k\Omega + 40k\Omega} = 26.67k\Omega$$

Applying KVL in the input loop, we have:

$$V_{TH} = I_B * R_{TH} + I_E * R_E + V_{BE}$$

$$I_E = (1 + \beta) * I_B$$

$$V_{TH} = I_B * R_{TH} + (1 + \beta) * I_B * R_E + V_{BE}$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1 + \beta) * R_E} = \frac{4 - 0.7}{26.67k\Omega + (1 + 100) * 3.3k\Omega} = 9.17\mu A$$

$$I_E = I_B * (1 + \beta) = 9.17\mu A * 101 = 0.927mA$$

$$I_C = \beta * I_B = 9.17\mu A * 100 = 0.917mA$$



**When  $R_C = 10 \text{ Ohms}$ :**

The voltage drop across  $R_C$  is  $V_{RC} = I_C * R_C = 0.917mA * 10\Omega = 9.17mV$ .

This voltage drop is very small compared to  $V_{CC}$ , so the collector voltage  $V_C$  remains high, allowing the transistor to operate in the active region.

Therefore, the emitter current  $I_E$  is approximately 0.927 mA.

**When  $R_C = 1k \text{ Ohms}$ :**

The voltage drop across  $R_C$  is  $V_{RC} = I_C * R_C = 0.917mA * 1k\Omega = 0.917V$ .

This voltage drop is significant compared to  $V_{CC}$ , which reduces the collector voltage  $V_C$ . If  $V_C$  drops below the base voltage minus  $V_{BE}$ , the transistor will enter saturation, causing a further increase in  $I_E$ .

However, in this case, the calculated  $I_E$  remains approximately 0.927 mA, but the actual current may be limited by the supply voltage and the saturation of the transistor.

## 6 PNP Circuit

Figure 6.1 shows a very typical PNP transistor circuit. Calculate  $I_B$ ,  $I_E$ , and  $I_C$  then simulate the circuit to double-check your calculation. Assume the current gain  $\beta = 100$ .

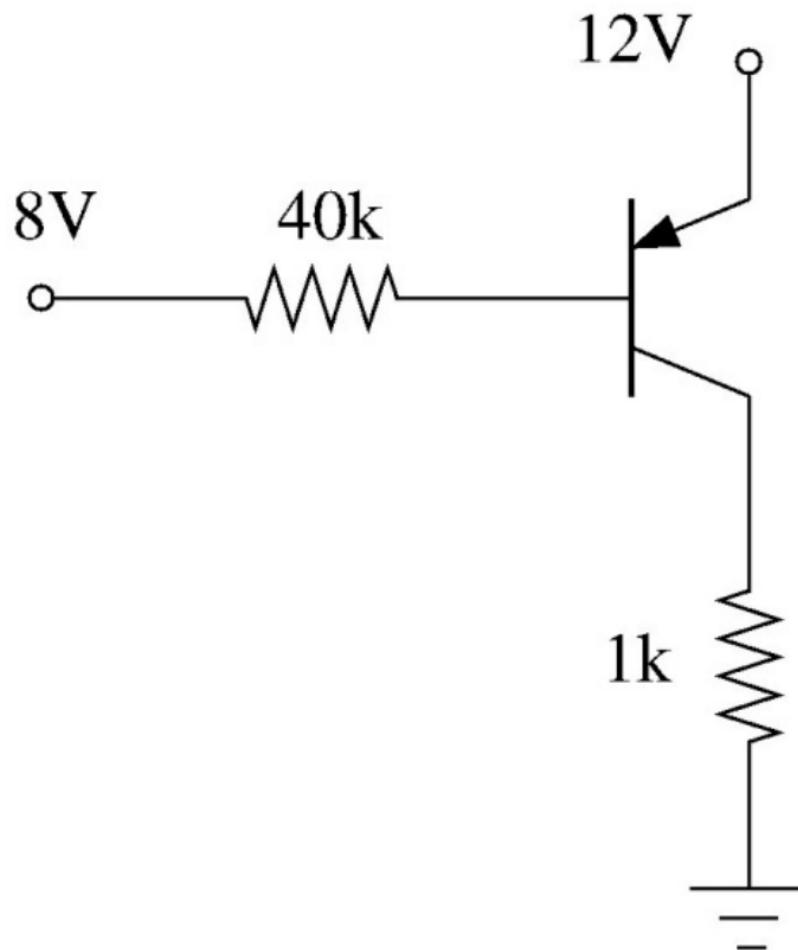


Figure 6.1: A PNP Circuit.

### 6.1 Theoretical Calculation

#### *Notes:*

*Explanations, formulas, and equations are expected rather than only results.*

Because the base-emitter junction of a PNP transistor is forward-biased, the emitter



is approximately 0.7 V higher than the base. Therefore,

$$V_{EB} = 0.7 \text{ V}$$

According to KVL at the base-emitter loop,

$$I_B = \frac{V_{EE} - V_{EB} - V_{BB}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V} - 8 \text{ V}}{40\text{k}\Omega} = 82.5 \mu\text{A}$$

Calculate the collector current  $I_C$ :

$$I_C = \beta \cdot I_B = 100 \cdot 82.5 \mu\text{A} = 8.25 \text{ mA}$$

Calculate the emitter current  $I_E$ :

$$I_E = I_C + I_B = 8.25 \text{ mA} + 0.0825 \text{ mA} = 8.3325 \text{ mA}$$

## 6.2 Simulation

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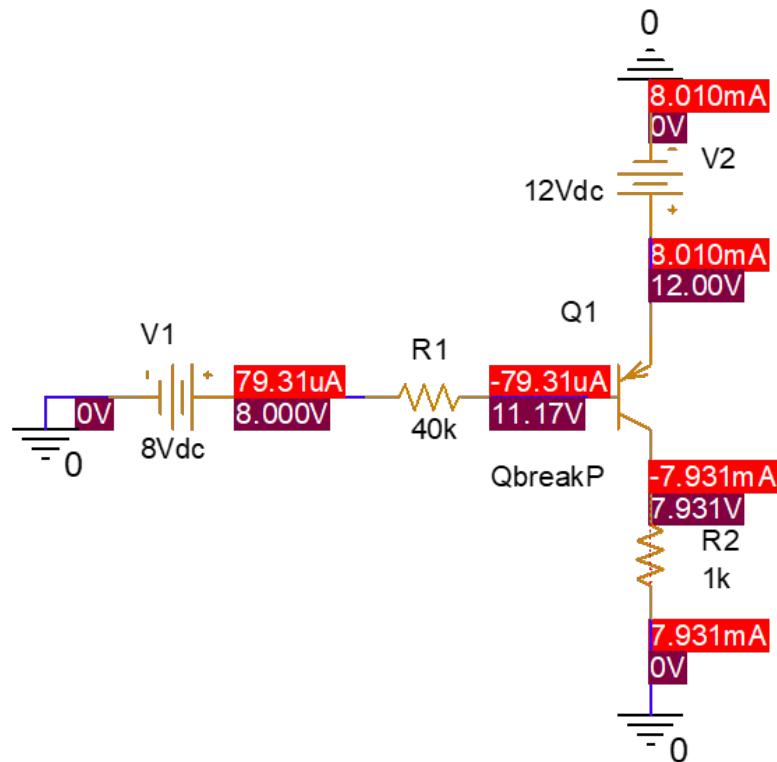


Figure 6.2: Simulation results for the PNP transistor circuit.

### 6.3 Compare

$$I_B(\text{in theory}) = 82.5 \mu\text{A} \quad I_B(\text{simulation}) = 79.31 \mu\text{A}$$

$$I_C(\text{in theory}) = 8.25 \text{ mA} \quad I_C(\text{simulation}) = 7.931 \text{ mA}$$

$$I_E(\text{in theory}) = 8.3325 \text{ mA} \quad I_E(\text{simulation}) = 8.010 \text{ mA}$$

## 7 Circuit with NPN and PNP bipolar junction transistors

Give the circuit in Figure 7.1. Calculate the Voltage at all nodes and the current in all branches. Assume the current gain of both transistors is the same at  $\beta = 100$ . Then perform a simulation and compare the result with the theoretical calculation. form a simulation and compare the result with the theoretical calculation.

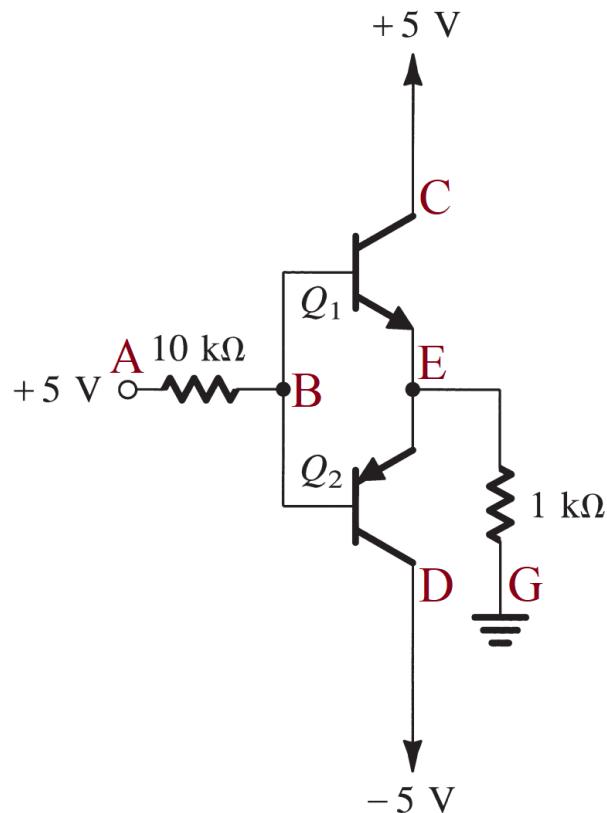


Figure 7.1: Circuit with NPN and PNP bipolar junction transistors

### 7.1 Theoretical calculation

The transistor  $Q_2$  is OFF because  $V_E < V_B$ .

Then, we can calculate the values for transistor  $Q_1$  as follows:



Applying KVL, we have (assuming  $\beta = 100$ ):

$$V_A = I_B * R_B + V_{BE} + I_E * R_E$$

$$I_E = (1 + \beta) * I_B = 101I_B$$

$$V_A = I_B * R_B + V_{BE} + 101I_B * R_E$$

$$I_B = \frac{V_A - V_{BE}}{R_B + 101R_E} = \frac{5V - 0.7V}{10k\Omega + 101 * 1k\Omega} = 38.7\mu A$$

$$I_C = \beta * I_B = 100 * 38.7\mu A = 3.87mA$$

$$I_E = I_C + I_B = 3.87mA + 38.7\mu A = 3.91mA$$

Calculating voltages at all nodes:

$$V_B = V_{BE} + I_E * R_E = 0.7V + 3.91mA * 1k\Omega = 4.61V$$

$$V_E = I_E * R_E = 3.91mA * 1k\Omega = 3.91V$$

## 7.2 Simulation

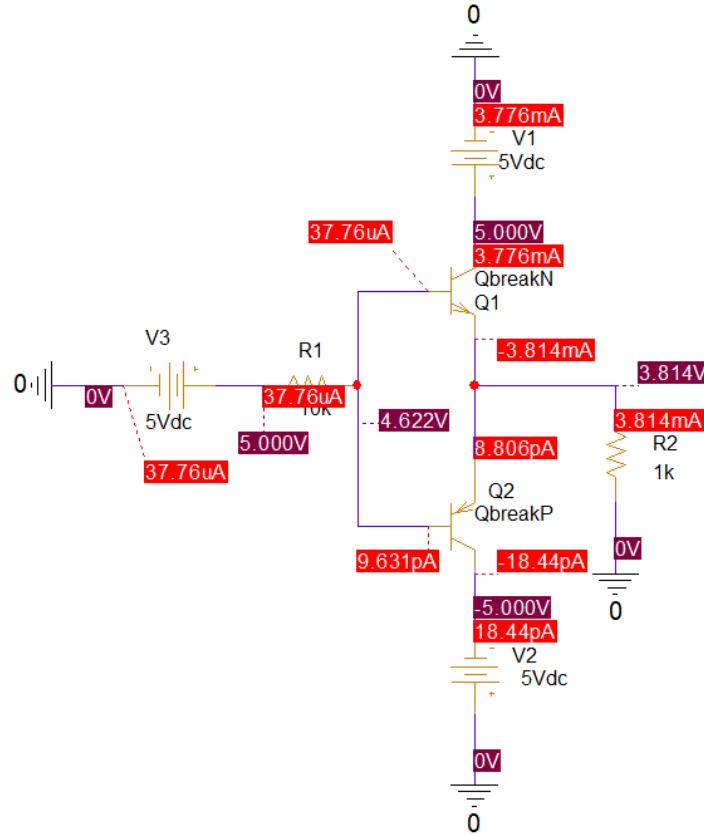


Figure 7.2: Simulation result of Exercise 7

## 7.3 Comparison

Table 7.1: Comparison between theoretical values and PSpice simulation.

Quantity	Theory	Simulation
$I_B$ (mA)	0.03870	0.03776
$I_C$ (mA)	3.8700	3.7760
$I_E$ (mA)	3.9087	3.8140
$V_E$ (V)	3.9087	3.8140
$V_B$ (V)	4.6100	4.6220

## 8 NPN Circuit with E resistance

In Figure 8.1, calculate the values of  $I_B$ ,  $I_C$ ,  $I_E$ ,  $V_E$ , and  $V_C$ . Assume the voltage drop  $V_{BE} = 0.7\text{ V}$  and the transistor current gain coefficient of the transistor is  $\beta = 100$ . Then perform a simulation to double-check your theoretical calculations.

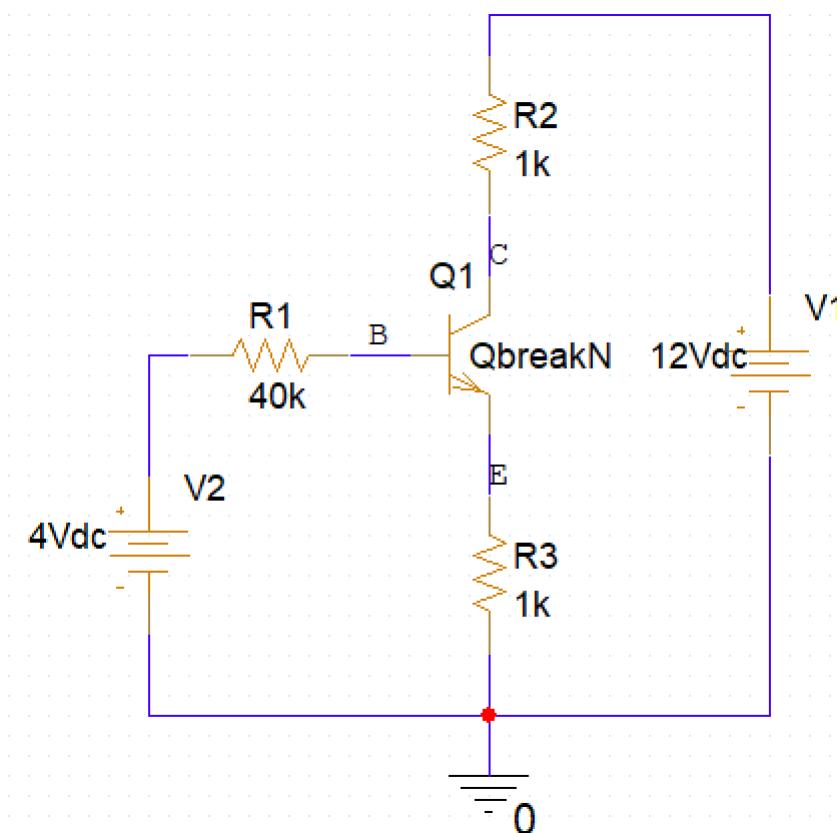


Figure 8.1: NPN Circuit with E resistance

### 8.1 Theoretical calculation

#### *Notes*

*Explanations, formulas, and equations are expected rather than only results.*

According to KVL theorem, we have:

$$V_2 - I_B \cdot R_1 - V_{BE} - I_E \cdot R_3 = 0$$

$$\iff V_2 - I_B \cdot R_1 - V_{BE} - (1 + \beta)I_B \cdot R_3 = 0 \quad (1)$$

Solve equation (1) to find  $I_B$ :

$$I_B = \frac{V_2 - V_{BE}}{R_1 + (1 + \beta)R_3} = \frac{4 \text{ V} - 0.7 \text{ V}}{40 \text{ k}\Omega + (1 + 100) \cdot 1 \text{ k}\Omega} \approx 23.4 \mu\text{A}$$

From that, we can calculate:

- $I_C = \beta \cdot I_B = 100 \cdot 23.4 \mu\text{A} = 2.34 \text{ mA}$
- $I_E = (1 + \beta) \cdot I_B = 101 \cdot 23.4 \mu\text{A} \approx 2.36 \text{ mA}$
- $V_E = I_E \cdot R_3 = 2.36 \text{ mA} \cdot 1 \text{ k}\Omega \approx 2.36 \text{ V}$
- $V_C = V_1 - I_C \cdot R_2 = 12 \text{ V} - 2.34 \text{ mA} \cdot 1 \text{ k}\Omega \approx 9.66 \text{ V}$

## 8.2 Simulation

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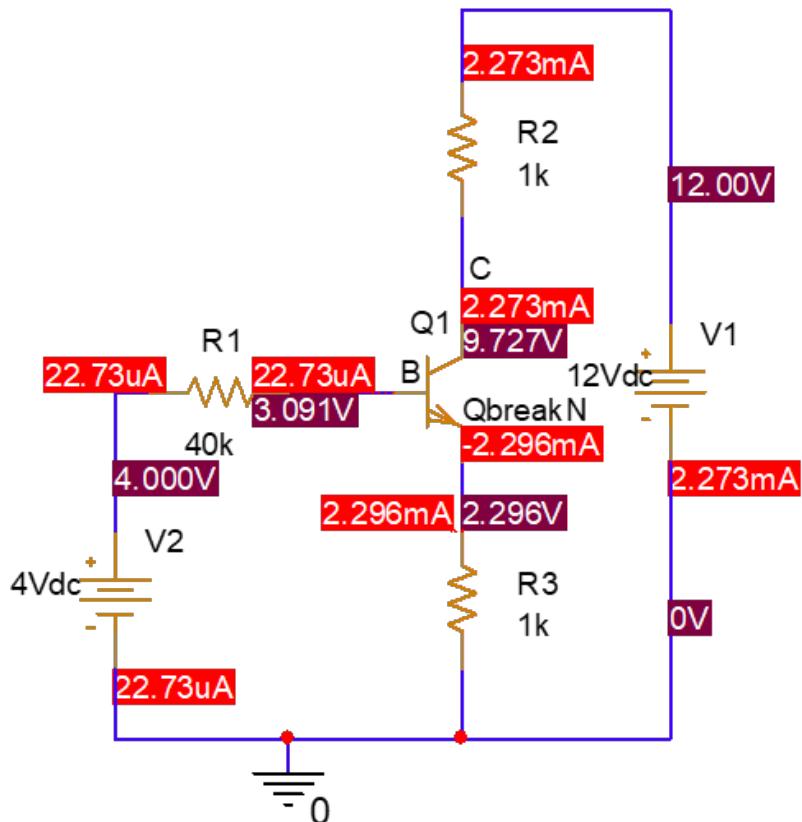


Figure 8.2: Simulation result of NPN Circuit with E resistance

## 9 Darlington circuit

The circuit given in Figure 9.1 is known as a Darlington circuit. Calculate  $I_{BE}$ ,  $I_{AC}$ ,  $I_{AL}$ , and the overall current gain  $\frac{I_{AL}}{I_{BE}}$ . After that, simulate the circuit to double-check your theoretical calculations. Assume both transistors have the same current gain coefficient  $\beta = 100$ .

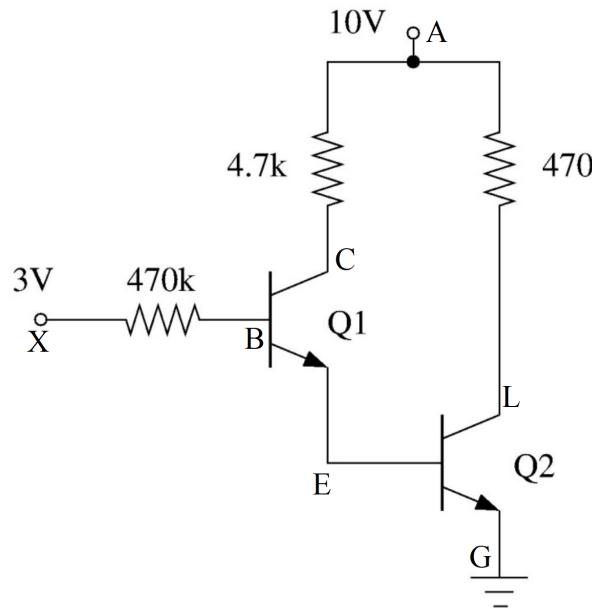


Figure 9.1: Darlington circuit

### 9.1 Theoretical calculation

Applying KVL, we have:

$$\begin{aligned} V_X &= I_{BE} * R_B + V_{BE1} + V_{BE2} \\ 3V &= I_{BE} * 470k\Omega + 0.7V + 0.7V \\ I_{BE} &= \frac{3V - 1.4V}{470k\Omega} = 3.40\mu A \end{aligned}$$



Calculating  $I_{AL}$ :

$$I_{B2} = I_{E1} = (1 + \beta) * I_{BE} = 101 * 3.40\mu A = 0.343mA$$

$$I_{AL} = I_{C2} = \beta * I_{B2} = 100 * 0.343mA = 34.3mA$$

We check if the calculated voltage  $V_L$  is physically valid:

$$V_L = V_{CC} - I_{AL} * R_C = 10V - 34.3mA * 470\Omega = -6.16V$$

Since  $V_L$  is negative, the transistor Q2 is in saturation mode. Therefore, we recalculate  $I_{AL}$  assuming  $V_{CE2(sat)} = 0.2V$ ,  $V_{BE1} = 0.7V$ , and  $V_{BE2} = 0.8V$ :

$$I_{AL} = \frac{V_{CC} - V_{CE2(sat)}}{R_C} = \frac{10V - 0.2V}{470\Omega} = 20.85mA$$

Calculating  $I_{BE}$ :

$$3V = I_{BE} * 470k\Omega + 0.7V + 0.8V$$

$$I_{BE} = \frac{3V - 1.5V}{470k\Omega} = 3.19\mu A$$

Calculating  $I_{AC}$ :

$$I_{AC} = I_{C1} = \beta * I_{BE} = 100 * 3.19\mu A = 0.319mA$$

## 10 Common base

Figure 10.1 shows shows a bias techniques named common base bias. Calculate the values of  $I_E$ ,  $I_B$ ,  $I_C$  and  $V_{CE}$ . Then simulate the circuit to double-check your theoretical calculations. Assume the current gain coefficient  $\beta = 100$ .

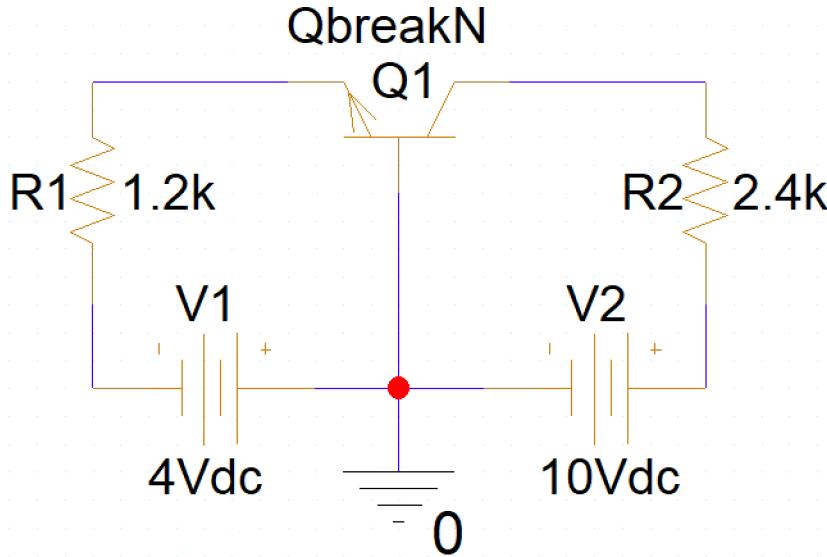


Figure 10.1: Common base

### 10.1 Theoretical calculation

#### *Notes*

*Explanations, formulas, and equations are expected rather than only results.*

Apply KVL for the left loop, we have:

$$-V_1 + I_E \cdot R_1 + V_{BE} = 0$$

$$\Leftrightarrow I_E = \frac{V_1 - V_{BE}}{R_1} = \frac{4 \text{ V} - 0.7 \text{ V}}{1.2 \text{ k}\Omega} = 2.75 \text{ mA}$$

From that, we can calculate:

- $I_B = \frac{I_E}{\beta+1} = \frac{2.75 \text{ mA}}{100+1} \approx 27.2 \mu\text{A}$
- $I_C = \beta \cdot I_B = 100 \cdot 27.2 \mu\text{A} = 2.72 \text{ mA}$

Apply KVL for the right loop, we have:

$$V_2 - I_C \cdot R_2 - V_C = 0$$

$$\iff V_C = V_2 - I_C \cdot R_2 = 10 \text{ V} - 2.72 \text{ mA} \cdot 2.4 \text{ k}\Omega = 3.472 \text{ V}$$

$$\iff V_{CE} = V_C - V_E = 3.472 \text{ V} - (-0.7 \text{ V}) = 4.172 \text{ V}$$

## 10.2 Simulation

Your images goes here

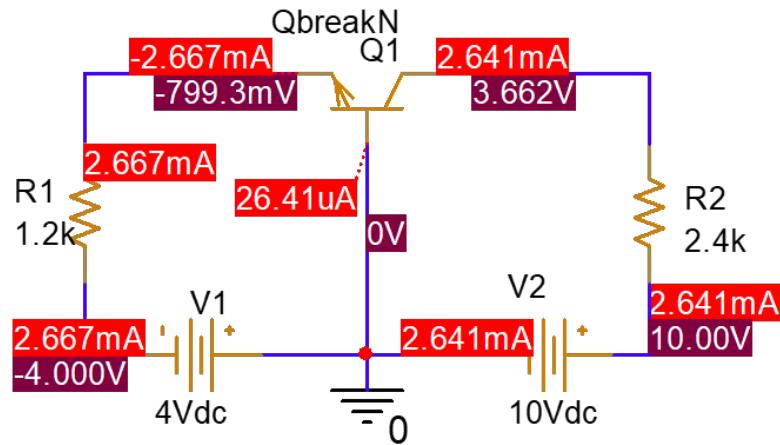


Figure 10.2: Simulation result of Common base

## 11 Current mirror

The circuit shown in Figure 11.1 is known as a current mirror circuit. First, students do some theoretical calculations to get an understanding of it. After that, perform a simulation to double-check its principles and your analysis. Assume that the two transistors Q1 and Q2, are the same type and the current gain  $\beta = 100$ .

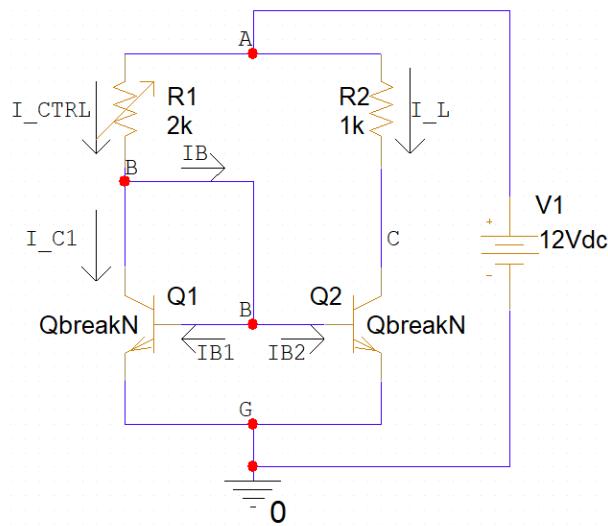


Figure 11.1: Current mirror circuit example

### 11.1 Theoretical calculation

**Case 1:**  $R_1 = 2k\Omega$

According to Ohm's law, we have:

$$I_{CRL} = \frac{V_A - V_B}{R_1} = \frac{12V - 0.7V}{2k\Omega} = 5.65mA$$

Using the KCL at node B, we have:

$$I_{CRL} = I_{C1} + I_{B1} + I_{B2}$$

$$I_{B1} = I_{B2} = \frac{I_{C1}}{100}$$



Therefore:

$$I_{B1} = I_{B2} = \frac{I_{CRL}}{102} = \frac{5.65mA}{102} = 55.4\mu A$$
$$I_L = 100 * I_{B2} = 100 * 55.4\mu A = 5.54mA$$

**Case 2:**  $R_1 = 100\Omega$  According to Ohm's law, we have:

$$I_{CRL} = \frac{V_A - V_B}{R_1} = \frac{12V - 0.7V}{100\Omega} = 113mA$$

Using the KCL at node B, we have:

$$I_{CRL} = I_{C1} + I_{B1} + I_{B2}$$
$$I_{B1} = I_{B2} = \frac{I_{C1}}{100}$$

Therefore:

$$I_{B1} = I_{B2} = \frac{I_{CRL}}{102} = \frac{113mA}{102} = 1.11mA$$
$$I_L = 100 * I_{B2} = 100 * 1.11mA = 111mA$$

## 11.2 Simulation

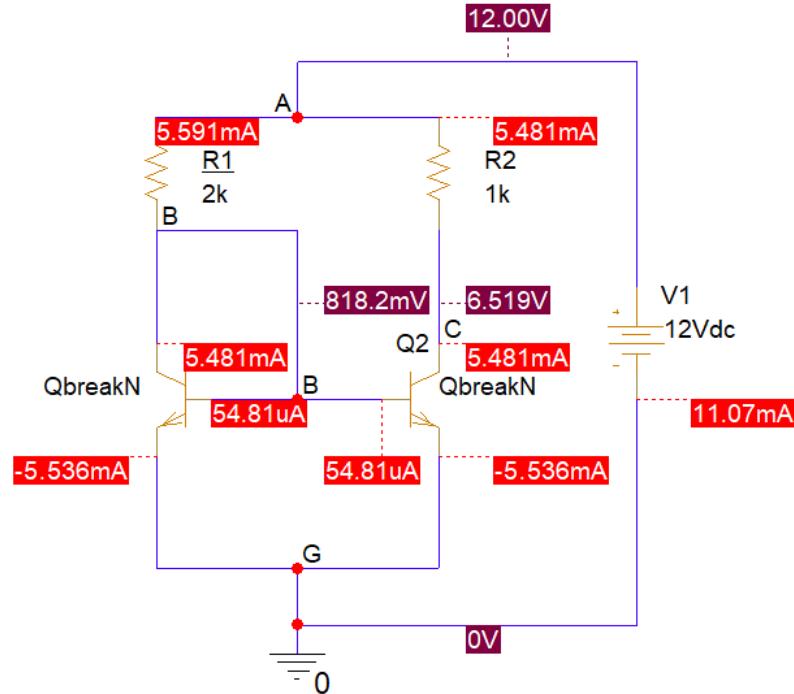


Figure 11.2: Simulation result of current mirror circuit with  $R_1 = 2k\Omega$

The circuit in Figure 11.1 is called circuit mirror because the mirrored current  $I_L$  is approximately equal to the reference current  $I_{CRL}$ . From the simulation result in Figure 11.2, we can see that  $I_{CRL} = 5.481mA$  and  $I_L = 5.481mA$ , which are equal to each other.

Next, we change the value of resistor  $R_1$  to  $100\Omega$  and perform the simulation again.

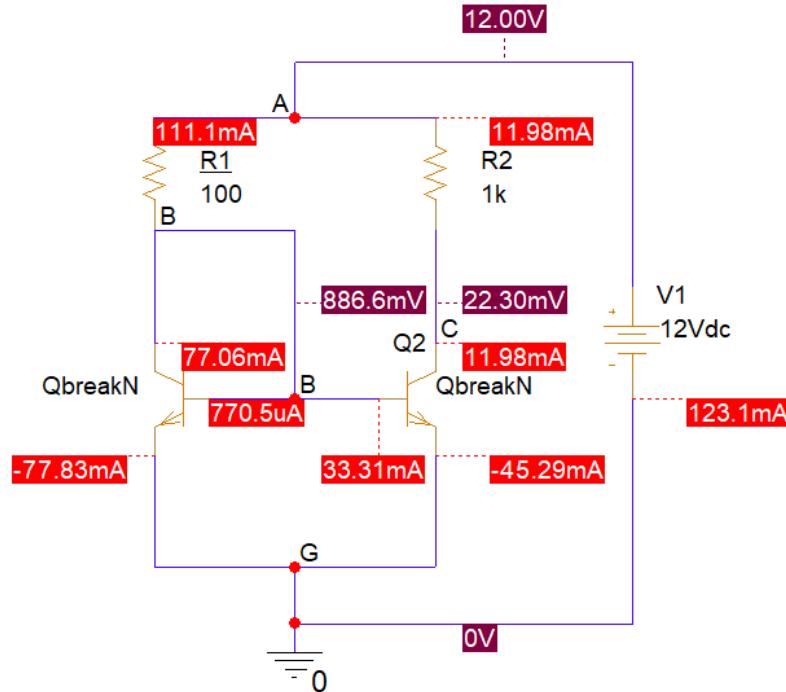


Figure 11.3: Simulation result of current mirror circuit with  $R_1 = 100\Omega$

The phenomena means that  $I_L$  is far from equal to  $I_{CRL}$ .

Since  $R_1$  is too small, then  $I_{CRL}$  is too large, which makes transistor Q2 enter saturation region. Therefore, the current mirror circuit no longer works properly. From the simulation result in Figure 11.3, we can see that  $I_{CRL} = 111mA$  and  $I_L = 11.98mA$ , which are not equal to each other.

## 12 BJT's logic gate application

Figure 12.1 describes a straightforward NOT gate theoretical implementation using an NPN bipolar junction transistor. In the circuit, the NPN junction transistor operates in the saturation mode.

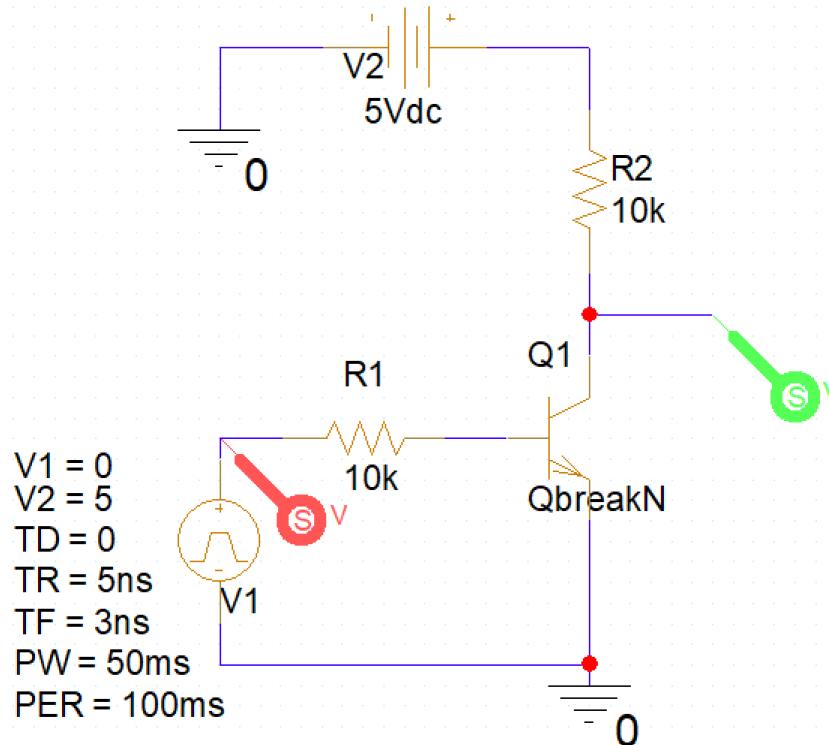


Figure 12.1: NPN theoretical NOT gate

V1 = 0 When the source is off, the voltage would be 0V.

V2 = 5 When the source is on, the voltage would be 5V.

TD = 0 Delay time. This exercise assumes that there is no delay.

TR = 5ns The rise time of the pulse (from off to on stage).

TF = 3ns The fall time of the pulse (from on to off stage).

PW = 50ms Pulse width: The time in which the source keeps on.

PER = 100ms The period of the signal.

### 12.1 Simulation

**Your images goes here**

The red line is the input pulse signal, while the green line is the output pulse signal.

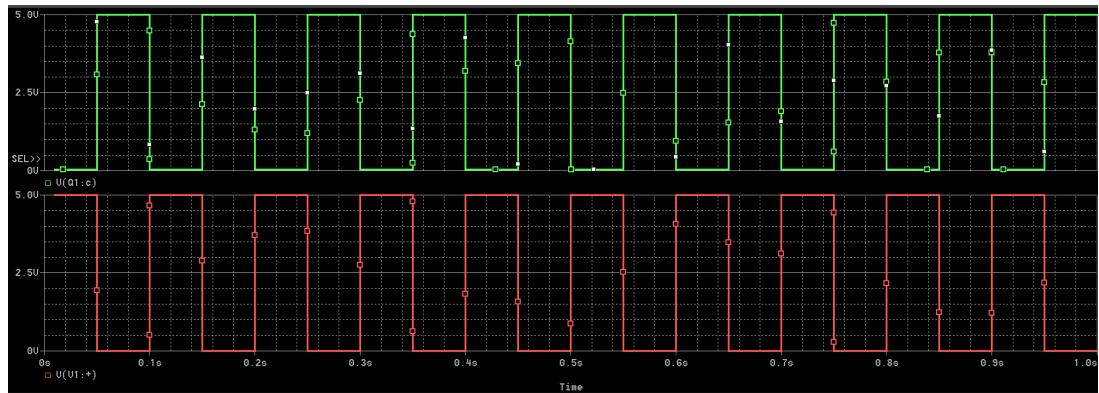


Figure 12.2: Simulation result of NPN theoretical NOT gate

## 13 Opto

The element OK1 in Figure 1.18 is an optocoupler, which includes a light-emitting diode (LED) and a photodiode. The photodiode's conductivity depends on the intensity of the light emitted by the LED and, of course, on the current through the LED. When the voltage across the LED is lower than its barrier potential, the optocoupler is cut off. When there is current through the LED, the optocoupler is in the transfer mode. Like the current gain  $\beta$  of a BJT, the optocoupler also has a current transfer ratio (CTR). Assume the LED has a barrier potential  $V_F = 1.7V$  and the optocoupler has  $CTR = 2$ . Calculate the voltage  $V_{OUT}$  when the switch is closed. Finally, give your idea about what we may use an optocoupler for, and how to use it?

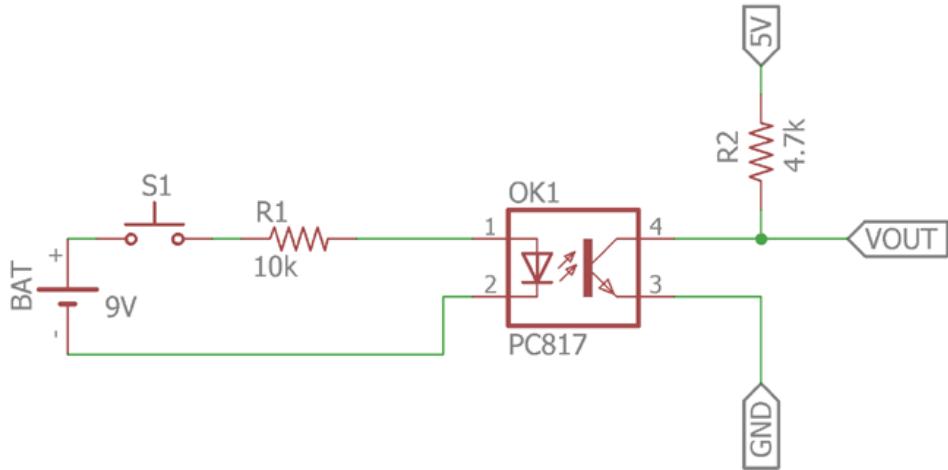


Figure 13.1: Optocoupler circuit

### 13.1 Solution

$$I_F = I_{R1} = \frac{V_{BAT} - V_F}{R_1} = \frac{9V - 1.7V}{10k\Omega} = 0.73mA$$

$$I_{R2} = I_C = CTR * I_F = 2 * 0.73mA = 1.46mA$$

$$V_{OUT} = 5V - (I_C * R_2) = 5V - (1.46mA * 4.7k\Omega) = -1.86V$$

We see that the output voltage  $V_{OUT}$  is negative, which means that the transistor is



in saturation mode. Therefore, we can approximate:

$$V_{OUT} \approx V_{CE(sat)} \approx 0.2V$$

When the switch is opened, there is no current through the LED, and the optocoupler is cut off. Therefore, there is no current through resistor R2, and we have:

$$V_{OUT} = 5V$$

The opto sensor can be used as a non-contact switch or position / speed sensor. It consists of an infrared LED and a phototransistor facing each other. When the light path is not blocked, the phototransistor conducts; when an object interrupts the beam, the collector current decreases and the output voltage changes. In practice, we bias the LED with a current-limiting resistor and connect the phototransistor in a pull-up configuration. By placing a rotating disc or moving object inside the slot, the sensor generates pulses at its output, which can be counted or measured by an oscilloscope or a microcontroller to determine speed or position.