VIETNAM NATIONAL UNIVERSITY HO CHI MINH CITY
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY
FACULTY OF COMPUTER SCIENCE AND ENGINEERING

Electrical Electronic Circuits

Lab Report

Lab 3

Advisor(s):	Phạm Công Thái	
Student(s):	Nguyễn Phúc Vĩnh	2414001
	Trần Văn Minh Triết	2413603

HO CHI MINH CITY, NOVEMBER 2025

Contents

List of Figures

List of Tables

Listings

1 BJT in Saturation Mode

Change the value of R_1 to 1 kΩ and run the simulation again. Capture the simulation results and explain the values of I_B, I_C, and V_{CE}. The default transistor gain is $\beta = 100$, and the saturation voltages are $V_{CE(\text{sat})} = 0.65$ V and $V_{BE} = 0.7$ V.

Your image goes here:

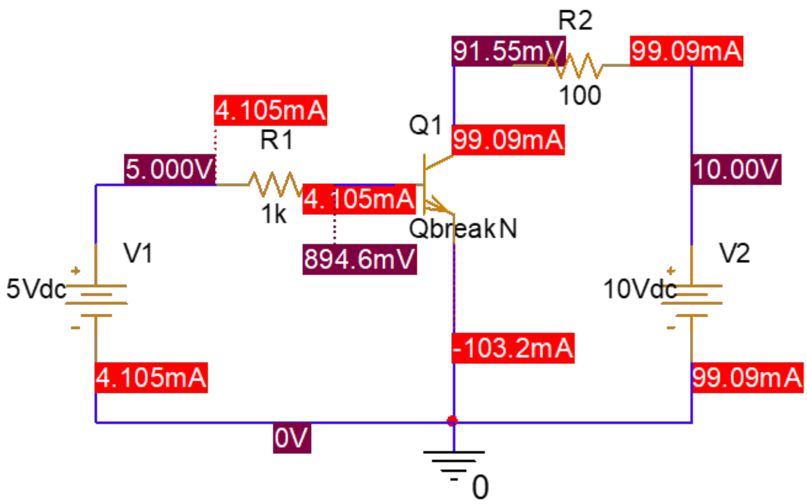

Figure 1.1: Simulation results for the BJT when $R_1 = 1$ kΩ.

The results in PSpice are explained as follows:

- According to Ohm's Law,

$$I_B = \frac{V_{CC} - V_{BE}}{R_1} = \frac{5V - 0.7V}{1k\Omega} = 4.3\text{mA}$$

- It is assumed that the transistor is in linear (or active) mode,

$$I_C = \beta \cdot I_B = 100 \cdot 4.3 \text{ mA} = 430 \text{ mA} = 0.43 \text{ A}$$

- Finally, in order to confirm the assumption above,

$$V_{CE} = V_{CC} - I_C \cdot R_2 = 10\text{V} - 0.43\text{A} \cdot 100\Omega = -33\text{V}$$

Since $V_{CE} < 0$, our assumption is not correct. The transistor stays in saturation mode. Therefore, I_C is determined as follows:

$$I_C = \frac{V_{CC} - V_{CE(\text{sat})}}{R_2} = \frac{10\text{V} - 0.65\text{V}}{100\Omega} = 93.5\text{mA}$$

2 DC Sweep Simulation

The schematic in the first exersice with **R1 = 1k** is re-used in this exercise. However, a DC-Sweep simulation mode is performed with V1 is varied from 0V to 5V (0.1V for the step), as follows:

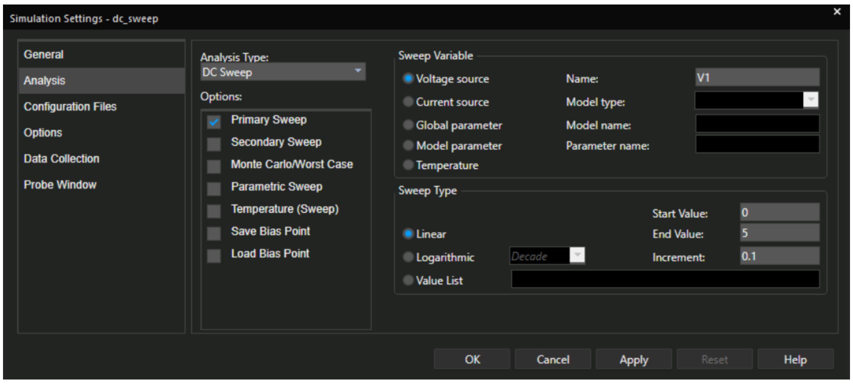

Figure 2.1: DC-Sweep profile for simulation.

Run the simulation and trace for the current I_C according to the value of V1. Capture your screen and plot it in the report. Please increase the width of the curve.

Your image goes here:

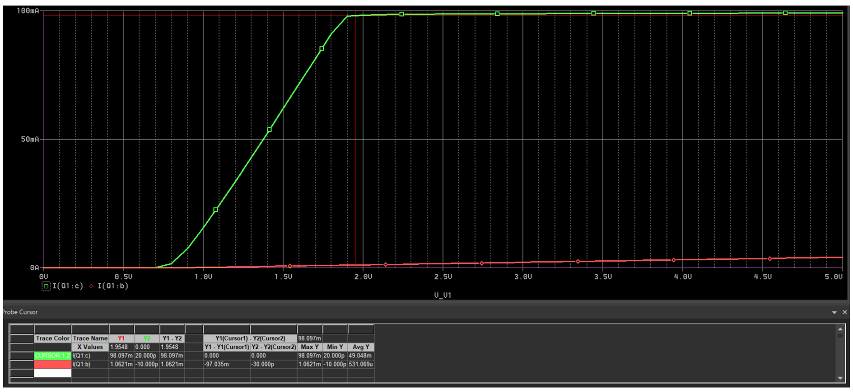

Figure 2.2: DC-Sweep simulation results for I_C.

When the transistor becomes saturated, the value of V1 is about to 1.95V.

At this value, the value of I_B is about to 1.06mA

And the value of $I_{C(sat)}$ is about to 98mA

3 Exercise 3: BJT used at Switch

For a given BJT circuit, determine R_1 and R_2 so that I_C is saturated at 50 mA. In this saturation mode $V_{\text{CE(sat)}}$ is 30 mV. Assume that $V_{BE} = 0.7$ V and the current gain $\beta = 100$.

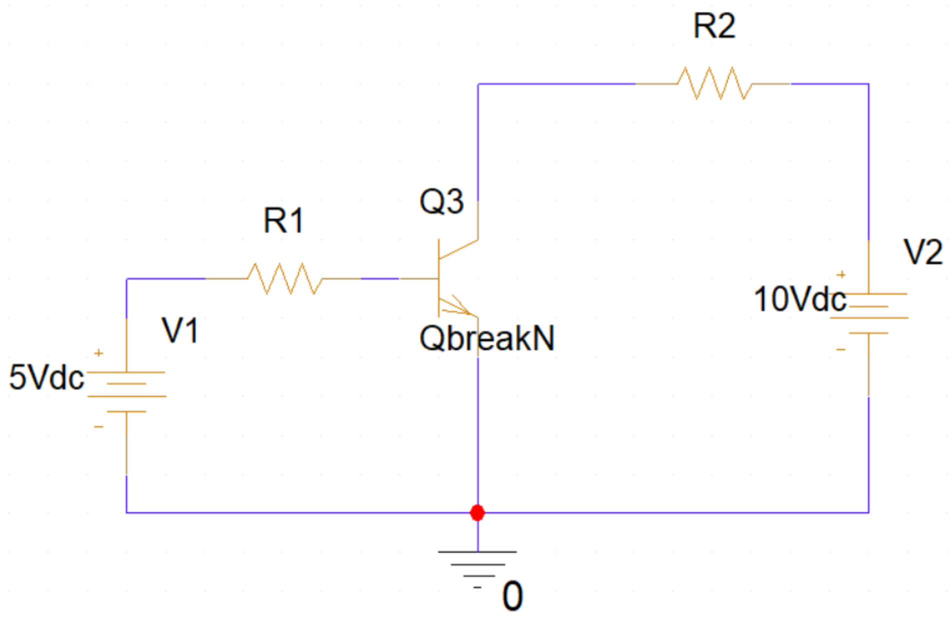

Figure 3.1: BJT used as switch in saturation mode

3.1 Solution

In saturation mode, we have:

$$\begin{aligned} V_{CE(sat)} &= 30 \text{ mV} \\ I_C &= 50 \text{ mA} \\ V_{BE} &= 0.7 \text{ V} \\ \beta &= 100 \end{aligned}$$

Applying KVL, we have:

$$\begin{aligned} V_2 &= I_C * R_2 + V_{CE(sat)} \\ 10V &= 50 \text{ mA} * R_2 + 30 \text{ mV} \\ R_2 &= 199,4\ \Omega \end{aligned}$$

Applying KVL, we have:

$$V_1 = I_B * R_1 + V_{BE}$$
$$I_B = \frac{I_C}{\beta} = \frac{50 \text{ mA}}{100} = 0.5 \text{ mA}$$
$$5V = 0.5 \text{ mA} * R_1 + 0.7 \text{ V}$$
$$R_1 = 8.6 \text{ k}\Omega$$

Thus, we have:

$$R_1 = 8.6 \text{ k}\Omega$$
$$R_2 = 199.4 \ \Omega$$

3.2 Simulation

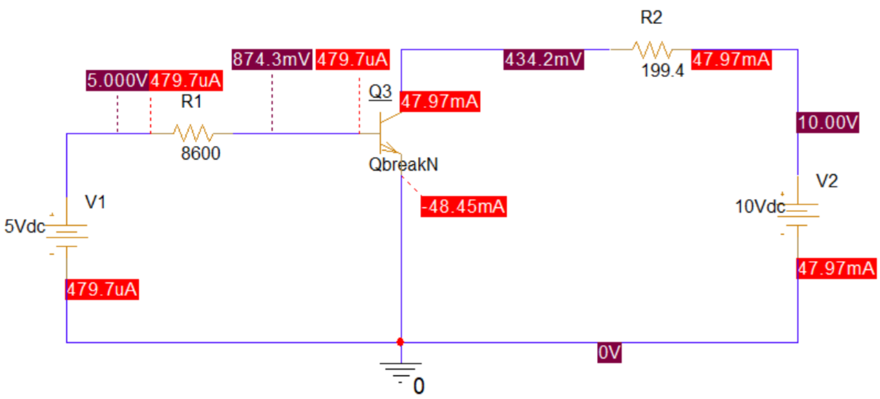

Figure 3.2: Simulation result of Exercise 3

From the simulation result in Figure ??, we can see that I_C is not 50 mA and V_{CE} is not 30 mV as calculated. Because the real SPICE model does not keep V_{BE}, β, or $V_{CE(\text{sat})}$ fixed as assumed in the hand calculation. The actual base current is not large enough to force saturation, so I_C and V_{CE} differ from the calculated values.

4 Drive a device with an NPN BJT

This exercise has a 5 V logic output (the V_{ter} in Figure ??) that can source up to 10 mA of current without a severe voltage drop and can withstand a maximum current of

20 mA. If the logic terminal sources a current larger than 20 mA, it would be damaged. If it sources a current larger than 10 mA, the V_{ter} voltage will drop to less than 4 V; we should avoid this drop in many cases. However, this logic terminal has to be used to drive an electrical component with an equivalent internal resistance of 5 Ω (the LOAD in Figure 1.6) and requires a current of at least 300 mA and not exceeding 500 mA to function normally. Given that we have an NPN transistor with the current gain $\beta = 100$, the maximum collector current I_C is 400 mA, and the barrier potential at the BE junction is $V_{BE} = 0.7\,\text{V}$, select a resistor available on the market to replace the resistor R_B shown in Figure 1.6 to make the circuit function well. After that, perform a simulation to double-check your selection.

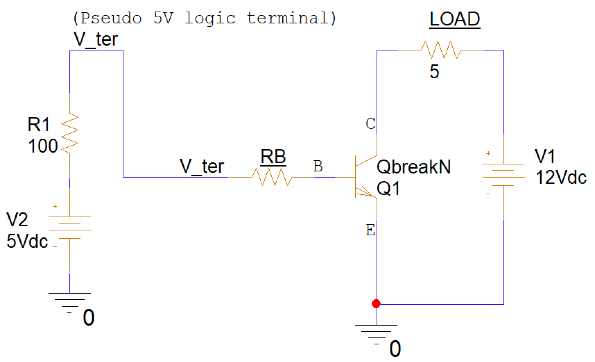

Figure 4.1: Select a resistor available in the market for R_B.

4.1 Theory calculations

Notes:
Explanations, formulas, and equations are expected rather than only results.

The load requires a collector current in the range:

$$300\,\text{mA} < I_L < 500\,\text{mA}$$

However, the transistor used can only provide a maximum collector current of:

$$I_{C(\text{max})} = 400\,\text{mA}$$

Therefore, the allowable collector-current range is:

$$300\,\text{mA (min)} < I_C < 400\,\text{mA (max)}.$$

With the transistor current gain $\beta = 100$, the corresponding base-current range is:

$$\frac{I_{C(\min)}}{\beta} = \frac{300\text{mA}}{100} = 3\text{mA (min)} < I_B < \frac{I_{C(\max)}}{\beta} = \frac{400\text{mA}}{100} = 4\text{mA (max)}.$$

According to the circuit in Figure **??**, the base current is

$$I_B = \frac{V_2 - V_{BE}}{R_1 + R_B} = \frac{5\text{V} - 0.7\text{V}}{100\Omega + R_B}.$$

With $I_{B(\min)} = 3\text{mA}$, we have

$$100\Omega + R_{B(\max)} = \frac{5\text{V} - 0.7\text{V}}{3\text{mA}} = \frac{4.3\text{V}}{3\text{mA}} \approx 1433\Omega,$$

$$R_{B(\max)} \approx 1433\Omega - 100\Omega = 1333\Omega = 1.33\text{k}\Omega.$$

With $I_{B(\max)} = 4\text{mA}$, we have

$$100\Omega + R_{B(\min)} = \frac{5\text{V} - 0.7\text{V}}{4\text{mA}} = \frac{4.3\text{V}}{4\text{mA}} = 1075\Omega,$$

$$R_{B(\min)} = 1075\Omega - 100\Omega = 975\Omega = 0.98\text{k}\Omega.$$

Therefore, the base resistor must satisfy:

$$0.98\text{k}\Omega\ (\text{min}) < R_B < 1.33\text{k}\Omega\ (\text{max}).$$

R_B selected is $1\,\text{k}\Omega$, which satisfies the above condition.

4.2 Simulation

Your image goes here:

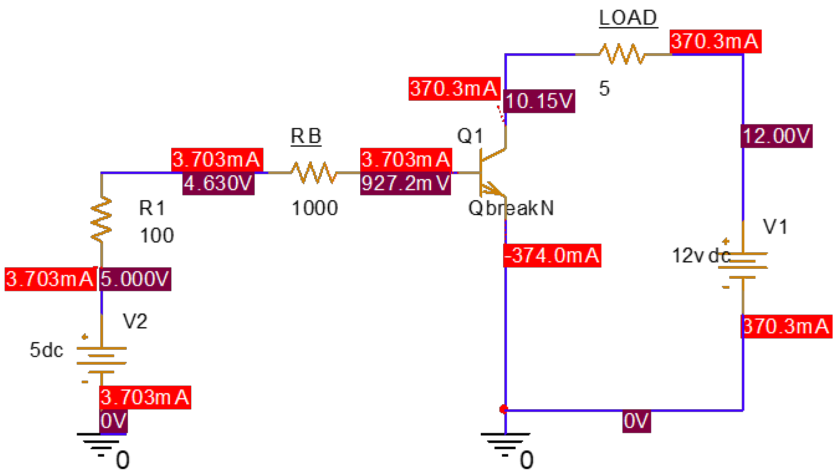

Figure 4.2: Simulation results with $R_B = 1\,\mathrm{k}\Omega$ (selected).

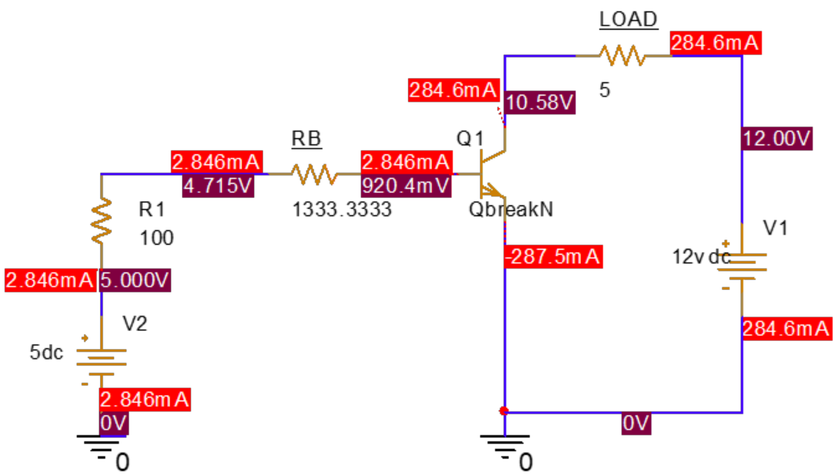

Figure 4.3: Simulation results with R_B max.

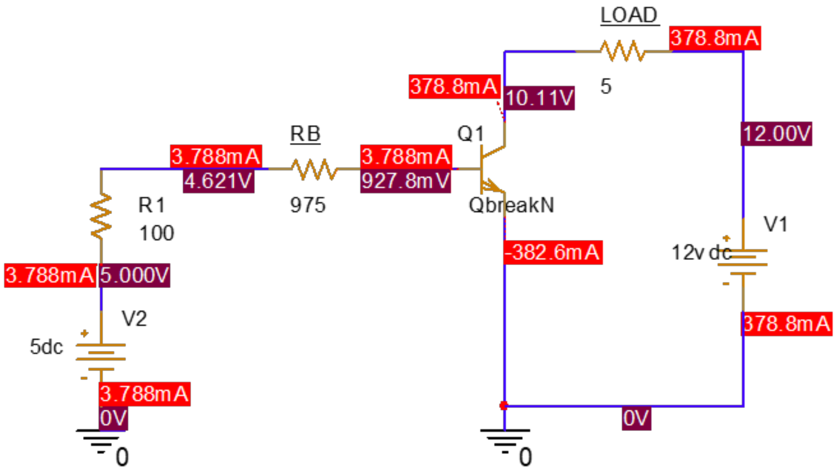

Figure 4.4: Simulation results with R_B min.

4.3 Compare

	Theory				PSpice		
	R_B	V_{BE}	I_B	I_C	V_{BE}	I_B	I_C
$R_{B(\text{min})}$	0.98 kΩ	0.7 V	4.00 mA	400 mA	0.9278 V	3.788 mA	378.8 mA
$R_{B(\text{max})}$	1.33 kΩ	0.7 V	3.00 mA	300 mA	0.9204 V	2.846 mA	284.6 mA
$R_{B(\text{selected})}$	1.00 kΩ	0.7 V	3.91 mA	391 mA	0.9272 V	3.703 mA	370.3 mA

Table 4.1: Theory and PSpice comparison.

From Table **??**, we can see that the PSpice simulation results are quite close to the theoretical calculations. The small differences may be due to the non-ideal characteristics of the transistor model used in the simulation.

5 PNP Circuit

Figure **??** shows a very typical PNP transistor circuit. Calculate I_B , I_E , and I_C then simulate the circuit to double-check your calculation. Assume the current gain $\beta = 100$.

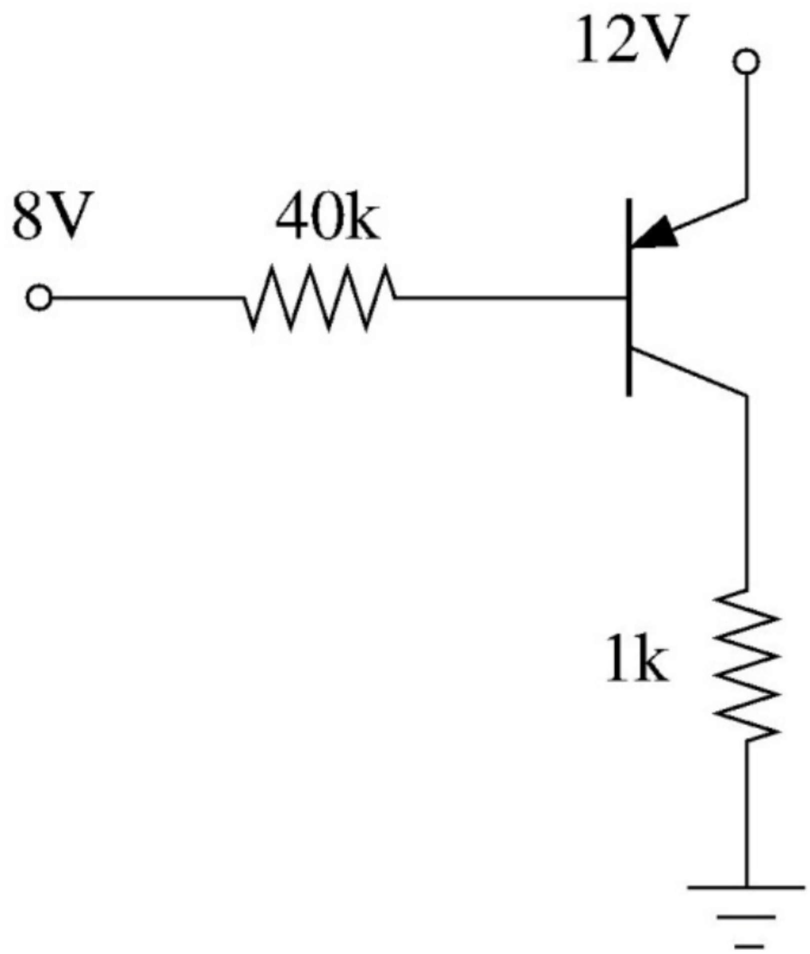

Figure 5.1: A PNP Circuit.

5.1 Theoretical Calculation

Notes:
Explanations, formulas, and equations are expected rather than only results.

Because the base–emitter junction of a PNP transistor is forward-biased, the emitter is approximately 0.7 V higher than the base. Therefore,

$$V_{EB} = 0.7 \text{ V}$$

According to KVL at the base-emitter loop,

$$I_B = \frac{V_{EE} - V_{EB} - V_{BB}}{R_B} = \frac{12\text{ V} - 0.7\text{ V} - 8\text{ V}}{40\text{k}\Omega} = 82.5\ \mu\text{A}$$

Calculate the collector current I_C:

$$I_C = \beta \cdot I_B = 100 \cdot 82.5\ \mu\text{A} = 8.25\text{ mA}$$

Calculate the emitter current I_E:

$$I_E = I_C + I_B = 8.25\text{ mA} + 0.0825\text{ mA} = 8.3325\text{ mA}$$

5.2 Simulation

Your image goes here:

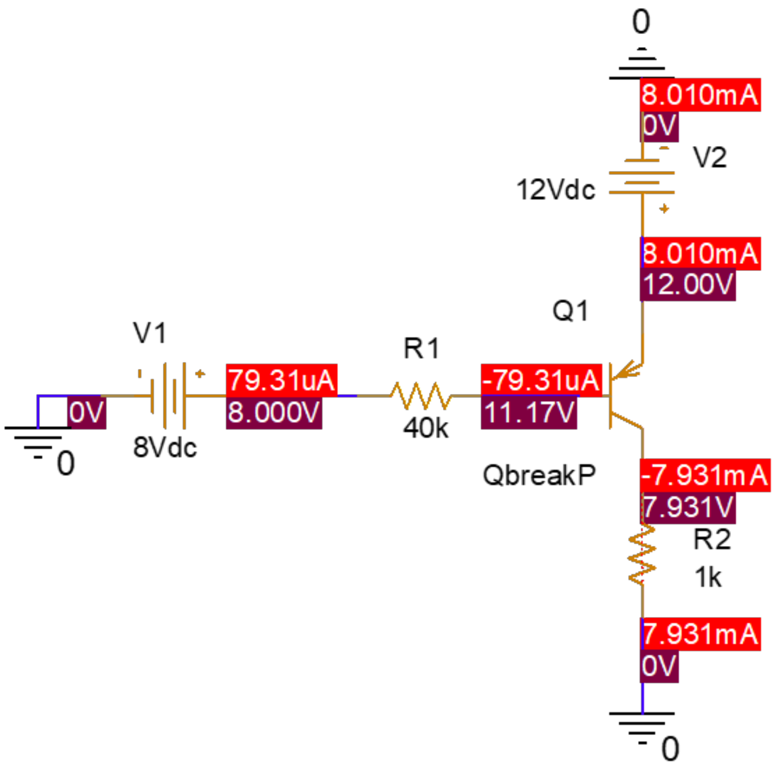

Figure 5.2: Simulation results for the PNP transistor circuit.

5.3 Compare

$$I_B(\text{in theory}) = 82.5\ \mu\text{A} \qquad I_B(\text{simulation}) = 79.31\ \mu\text{A}$$

$$I_C(\text{in theory}) = 8.25\ \text{mA} \qquad I_C(\text{simulation}) = 7.931\ \text{mA}$$

$$I_E(\text{in theory}) = 8.3325\ \text{mA} \qquad I_E(\text{simulation}) = 8.010\ \text{mA}$$

6 NPN Circuit with E resistance

In Figure **??**, calculate the values of I_B, I_C, I_E, V_E, and V_C. Assume the voltage drop $V_{BE} = 0.7\,\text{V}$ and the transistor current gain coefficient of the transistor is $\beta = 100$. Then perform a simulation to double-check your theoretical calculations.

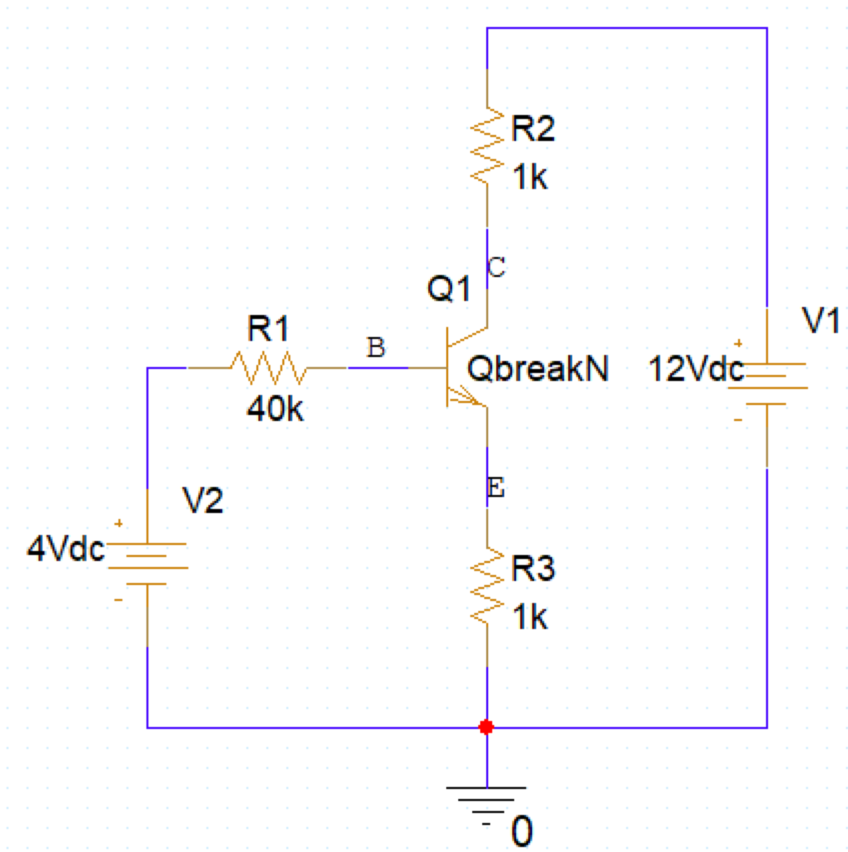

Figure 6.1: NPN Circuit with E resistance

6.1 Theoretical calculation

Notes
Explanations, formulas, and equations are expected rather than only results.

According to KVL theorem, we have:

$$V_2 - I_B \cdot R_1 - V_{BE} - I_E \cdot R_3 = 0$$

$$\iff V_2 - I_B \cdot R_1 - V_{BE} - (1+\beta)I_B \cdot R_3 = 0(1)$$

Solve equation (1) to find I_B:

$$I_B = \frac{V_2 - V_{BE}}{R_1 + (1+\beta)R_3} = \frac{4\text{ V} - 0.7\text{ V}}{40\text{ k}\Omega + (1+100)\cdot 1\text{ k}\Omega} \approx 23.4\ \mu\text{A}$$

From that, we can calculate:

- $I_C = \beta \cdot I_B = 100 \cdot 23.4\ \mu\text{A} = 2.34\text{ mA}$
- $I_E = (1+\beta)\cdot I_B = 101 \cdot 23.4\ \mu\text{A} \approx 2.36\text{ mA}$
- $V_E = I_E \cdot R_3 = 2.36\text{ mA} \cdot 1\text{ k}\Omega \approx 2.36\text{ V}$
- $V_C = V_1 - I_C \cdot R_2 = 12\text{ V} - 2.34\text{ mA} \cdot 1\text{ k}\Omega \approx 9.66\text{ V}$

6.2 Simulation

Your images goes here

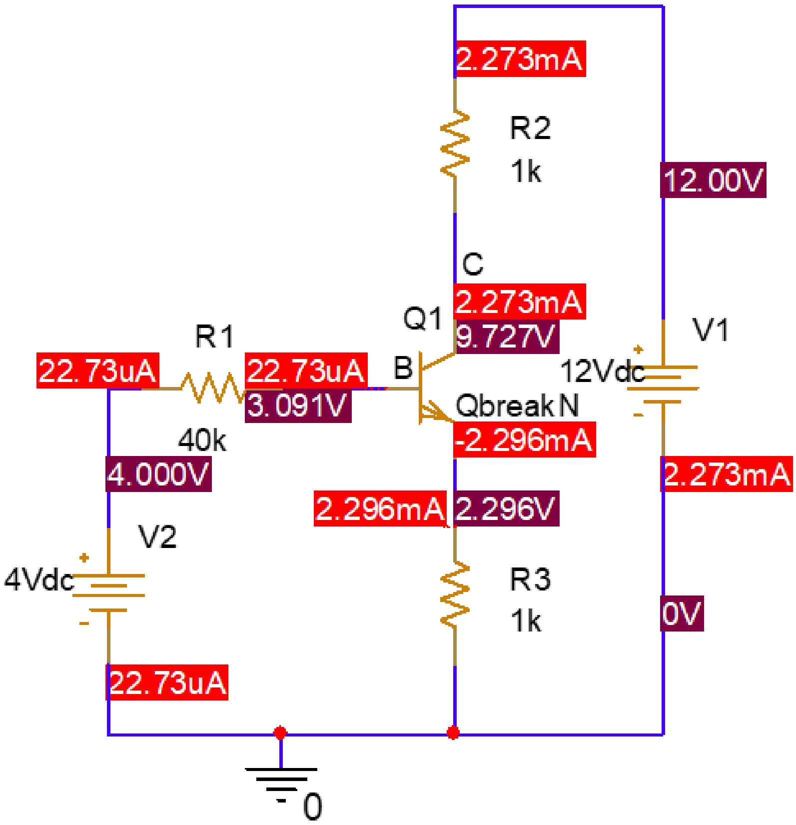

Figure 6.2: Simulation result of NPN Circuit with E resistance

7 Common base

Figure **??** shows shows a bias techniques named common base bias. Calculate the values of I_E, I_B, I_C and V_{CE}. Then simulate the circuit to double-check your theoretical calculations. Assume the current gain coefficient $\beta = 100$.

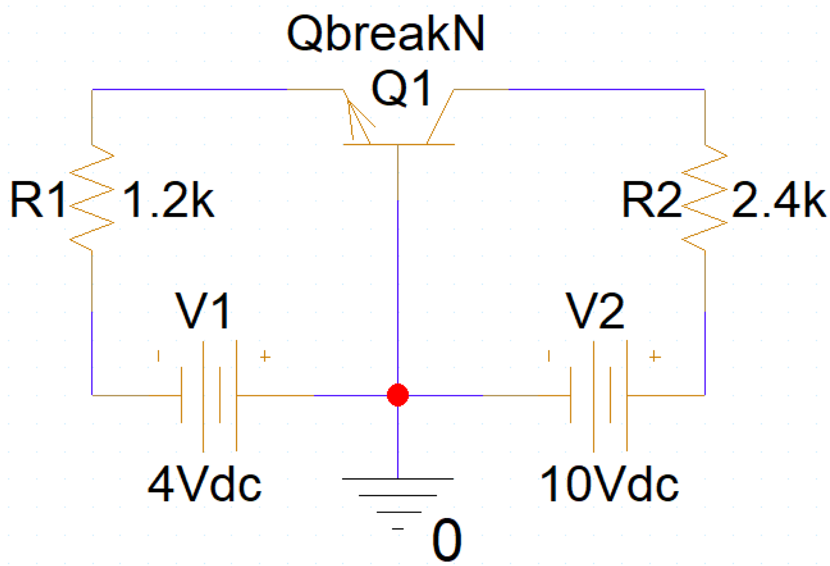

Figure 7.1: Common base

7.1 Theoretical calculation

Notes
Explanations, formulas, and equations are expected rather than only results.

Apply KVL for the left loop, we have:

$$-V_1 + I_E \cdot R_1 + V_{BE} = 0$$

$$\iff I_E = \frac{V_1 - V_{BE}}{R_1} = \frac{4\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega} = 2.75\text{ mA}$$

From that, we can calculate:

- $I_B = \frac{I_E}{\beta+1} = \frac{2.75\text{ mA}}{100+1} \approx 27.2\ \mu\text{A}$
- $I_C = \beta \cdot I_B = 100 \cdot 27.2\ \mu\text{A} = 2.72\text{ mA}$

Apply KVL for the right loop, we have:

$$V_2 - I_C \cdot R_2 - V_C = 0$$

$$\iff V_C = V_2 - I_C \cdot R_2 = 10\text{ V} - 2.72\text{ mA} \cdot 2.4\text{ k}\Omega = 3.472\text{ V}$$

$$\iff V_{CE} = V_C - V_E = 3.472\text{ V} - (-0.7\text{ V}) = 4.172\text{ V}$$

7.2 Simulation

Your images goes here

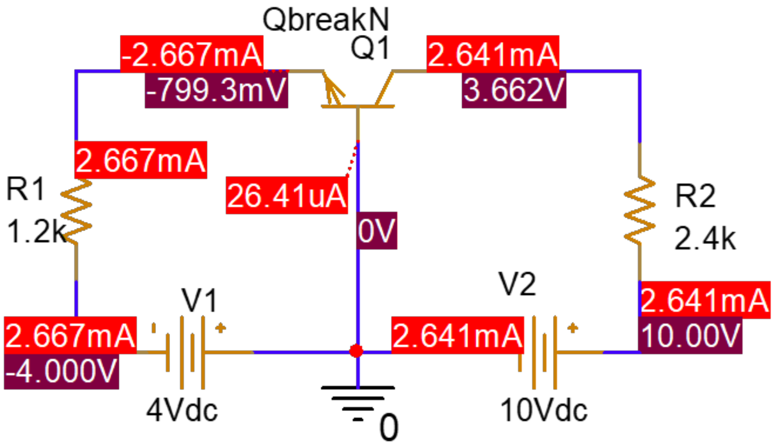

Figure 7.2: Simulation result of Common base

8 BJT's logic gate application

Figure ?? describes a straightforward NOT gate theoretical implementation using an NPN bipolar junction transistor. In the circuit, the NPN junction transistor operates in the saturation mode.

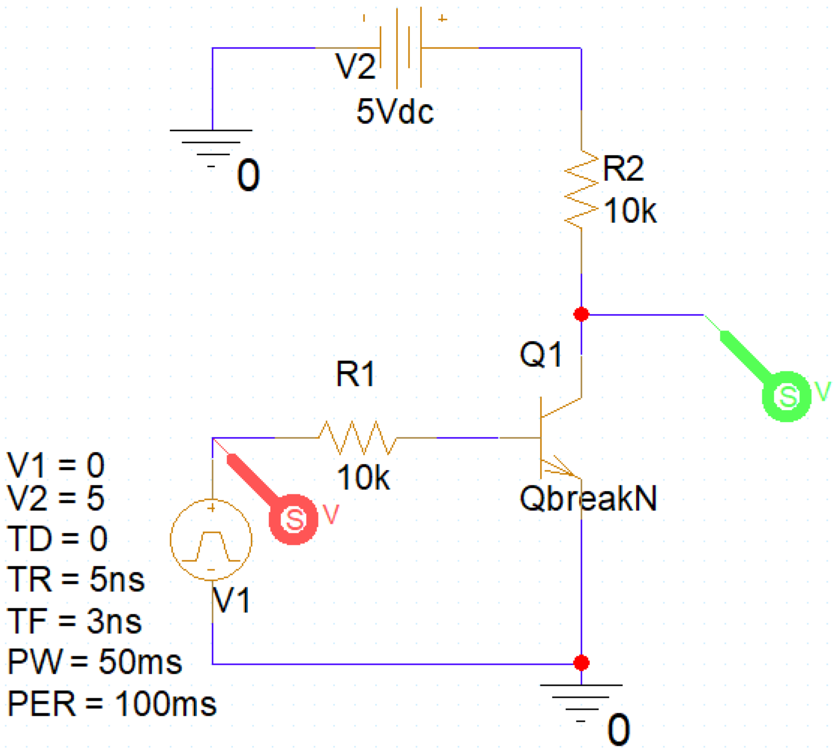

Figure 8.1: NPN theoretical NOT gate

V1 = 0 When the source is off, the voltage would be 0V.

V2 = 5 When the source is on, the voltage would be 5V.

TD = 0 Delay time. This exercise assumes that there is no delay.

TR = 5ns The rise time of the pulse (from off to on stage).

TF = 3ns The fall time of the pulse (from on to off stage).

PW = 50ms Pulse width: The time in which the source keeps on.

PER = 100ms The period of the signal.

8.1 Simulation

Your images goes here

The red line is the input pulse signal, while the green line is the output pulse signal.

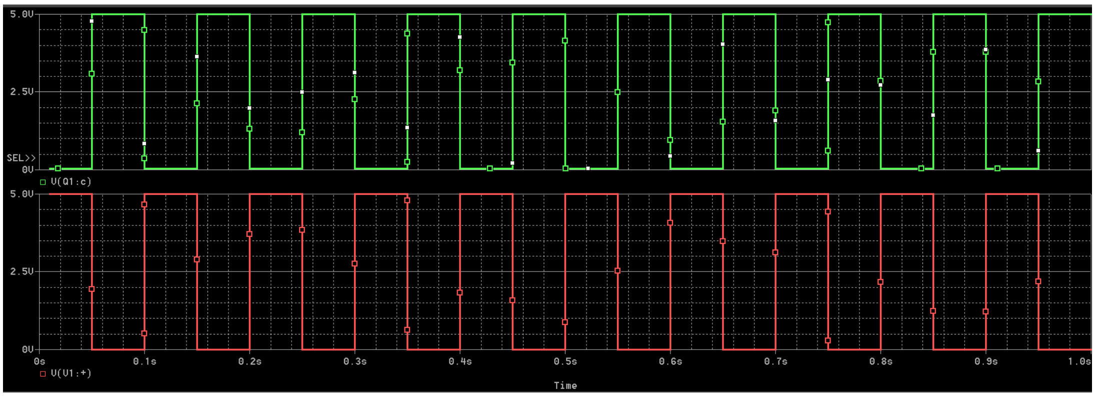

Figure 8.2: Simulation result of NPN theoretical NOT gate