VIETNAM NATIONAL UNIVERSITY HO CHI MINH CITY
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY
FACULTY OF COMPUTER SCIENCE AND ENGINEERING

Electrical Electronic Circuits

Lab Report

Lab 5

Advisor(s): Phạm Công Thái
Student(s): Nguyễn Phúc Vĩnh 2414001
Trần Văn Minh Triết 2413603

HO CHI MINH CITY, DECEMBER 2025

Contents

1 Introduction **1**

2 Closed Loop Operation **1**

2.1 Non inverting configuration 2

2.2 Inverting configuration 2

3 Exercise and Report **3**

3.1 Voltage Follower 3

3.2 High-Current Voltage Follower 6

3.3 Voltage Follower with Gain 7

3.4 Summing Amplifier 10

3.5 Low Pass Filter 12

3.6 High Pass Filter 15

3.7 Comparator with Hysteresis (Schmitt Trigger) 16

4 Altium Designer **19**

4.1 LED driver 19

4.1.1 Schematic design 19

4.1.2 PCB layout 19

4.2 Relay Controller 21

4.2.1 Schematic design 21

4.2.2 PCB layout 21

List of Figures

2.1 Non inverting configuration 2

2.2 Inverting configuration 3

3.1 Opamp follower circuit 4

3.2 Simulation result with R = 1kΩ 4

3.3 Simulation result with R = 2kΩ 5

3.4 Opamp follower circuit 6

3.5 The bias point simulation 7

3.6 Opamp follower with gain for the output 8

3.7 Simulation results with $R_1 = 1K\Omega$ and $R_2 = 2K\Omega$ 8

3.8 Simulation results with $R_1 = 5K\Omega$ and $R_2 = 10K\Omega$ 9

3.9 Non inverse summing using OPAMP 10
3.10 Simulation 10
3.11 Inverse summing using OPAMP 11
3.12 Simulation 11
3.13 Low pass filter principles 12
3.14 Inverting low pass filter 13
3.15 AC Sweep simulation profile 13
3.16 Simulation results 14
3.17 Non-inverting low pass filter 14
3.18 Simulation results of non-inverting low pass filter 15
3.19 Active high pass filter with amplification. 16
3.20 Schmitt Trigger Circuit 17
3.21 Schmitt Trigger Circuit in PSPice 17
3.22 Schmitt trigger in PSPICE 18
3.23 Simulation profile 18
3.24 Schmitt trigger simulation results 18
4.1 Schematic of LED driver 19
4.2 Top layer of LED driver PCB 20
4.3 Bottom layer of LED driver PCB 20
4.4 Schematic of Relay Controller 21
4.5 Top layer of Relay Controller PCB 21
4.6 Bottom layer of Relay Controller PCB 22

List of Tables

Listings

1 Introduction

Operational Amplifiers, also known as Op-amps, are basically a voltage amplifying device designed to be used with components like capacitors and resistors, between its in/out terminals. They are essentially a core part of analog devices. Feedback components like these are used to determine the operation of the amplifier. The amplifier can perform many different operations, giving it the name Operational Amplifier.

One key to the usefulness of these little circuits is in the engineering principle of feedback, particularly negative feedback, which constitutes the foundation of almost all automatic control processes. The principles presented in this section, extend well beyond the immediate scope of electronics. It is well worth the electronics student's time to learn these principles and learn them well.

Operational amplifiers can have either a closed-loop operation or an open-loop operation. The operation (closed-loop or open-loop) is determined by whether or not feedback is used. Without feedback the operational amplifier has an open-loop operation. This open-loop operation is practical only when the operational amplifier is used as a cooperator (a circuit which compares two input signals or compares an input signal to some fixed level of voltage). As an amplifier, the open-loop operation is not practical because the very high gain of the operational amplifier creates poor stability. (Noise and other unwanted signals are amplified so much in open-loop operation that the operational amplifier is usually not used in this way.) Therefore, most operational amplifiers are used with feedback (closed-loop operation).

2 Closed Loop Operation

Operational amplifiers are used with degenerative (or negative) feedback which reduces the gain of the operational amplifier but greatly increases the stability of the circuit. In the closed-loop configuration, the output signal is applied back to one of the input terminals.

This feedback is always degenerative (negative). In other words, the feedback signal always opposes the effects of the original input signal. One result of degenerative feedback is that the inverting and non-inverting inputs to the operational amplifier will be kept at the same potential.

Closed-loop circuits can be of the inverting configuration or non-inverting configuration.

2.1 Non inverting configuration

The typical circuit for this configuration is shown in the figure bellow:

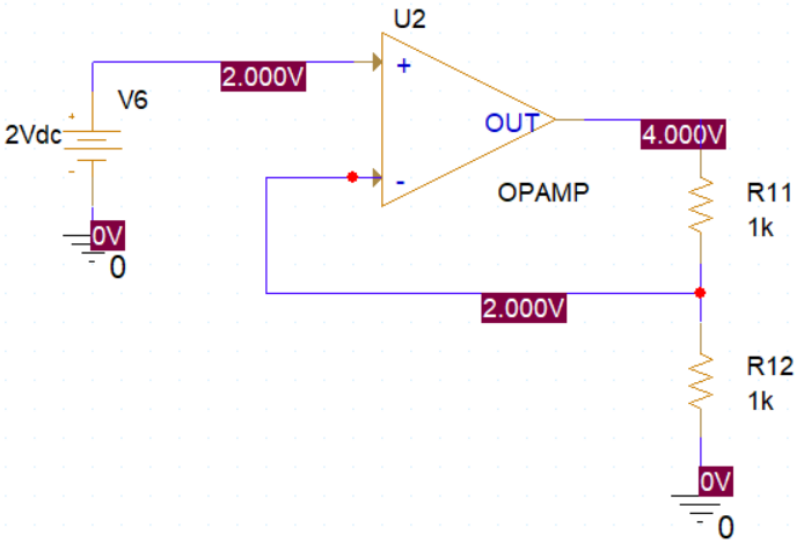

Figure 2.1: Non inverting configuration

The new component, named also OPAMP (Operational Amplifier) is easily found in the favorite list of the PSPICE.

In order to explain the 4V at the ouput, it is obviously that $V(+) = V(-) = 2V$ in a closed loop configuration. Therefore, from a resistor bridge at the output, $V_{out} = 4V$.

2.2 Inverting configuration

In this configuration, the output is connected directly to a pin of the opamp as follow:

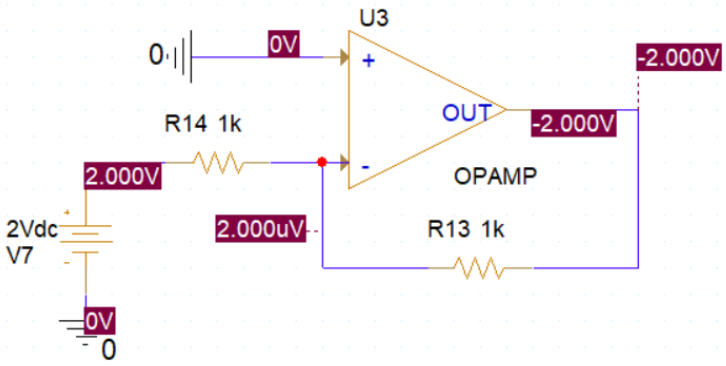

Figure 2.2: Inverting configuration

As the output voltage is negative, which is inverted to the input, the name of this circuit is the invert connection. Students are proposed to perform calculations to confirm the output, which is -2V .

Calculation:

Since the circuit have negative feedback, we have $V(+) = V(-) = 0V$.

Therefore, the current flowing through R_{14} is:

$$I = \frac{V_{in} - V(-)}{R_{14}} = \frac{2 - 0}{1k} = 2\ mA$$

As no current flows into the opamp pin, the same current flows through R_{13}, so the output voltage is:

$$V_{out} = V(-) - I \cdot R_{13} = 0 - 2\ mV \cdot 1k = -2V$$

3 Exercise and Report

3.1 Voltage Follower

Voltage follower is one of the simplest uses of an operational amplifier, where the output voltage is exactly same as the input voltage applied to the circuit. In other words, the gain of a voltage follower circuit is unity. The connections are proposed as follows:

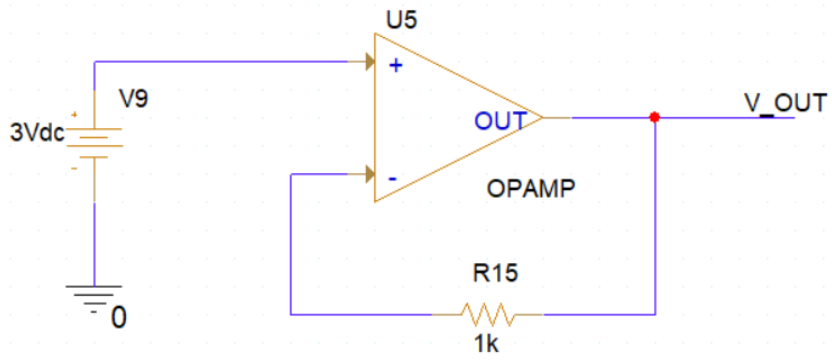

Figure 3.1: Opamp follower circuit

A voltage follower has low output impedance and extremely high input impedance, and this makes it a simple and effective solution to problematic impedance relationships. If a high-output-impedance sub-circuit must transfer a signal to a low-input-impedance sub-circuit, a voltage follower placed between these two sub-circuits will ensure that the full voltage is delivered to the load.

Students are propose to run the simulation with bias mode to confirm that $V_{OUT} = V(+)$. The feedback resistance is also required to change.

Simulation results:

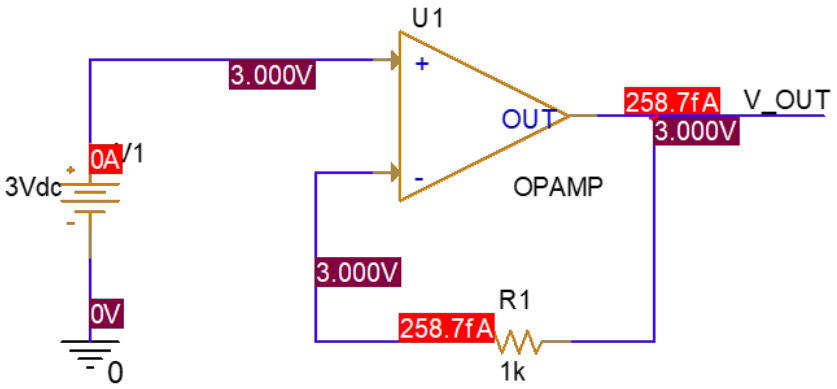

Figure 3.2: Simulation result with R = 1kΩ

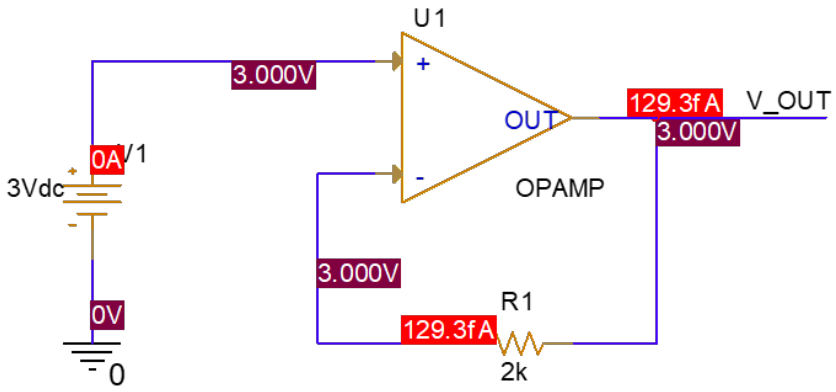

Figure 3.3: Simulation result with R = 2kΩ

Your calculations are presented here to prove $V_{OUT} = V(+)$ with any value of R15.

Solution:

The general voltage gain of a non-inverting operational amplifier is given by:

$$A_v = 1 + \frac{R_f}{R_{in}}$$

For the voltage follower configuration:

- $R_f = 0$ (short-circuited feedback)
- $R_g \to \infty$ (no resistor connected to ground)

Substituting these values into the gain formula:

$$A_v = 1 + \frac{0}{\infty} = 1 + 0 = 1$$

Therefore, we confirm that:

$$V_{OUT} = A_v \cdot V_{IN} = 1 \cdot V_{IN} = V_{IN}$$

3.2 High-Current Voltage Follower

The voltage follower's low output impedance makes it a good circuit for driving current into a low-impedance load, but it's important to remember that most op-amps are not designed to deliver large output currents. The most basic circuit for buffering an op-amp's output current is the following:

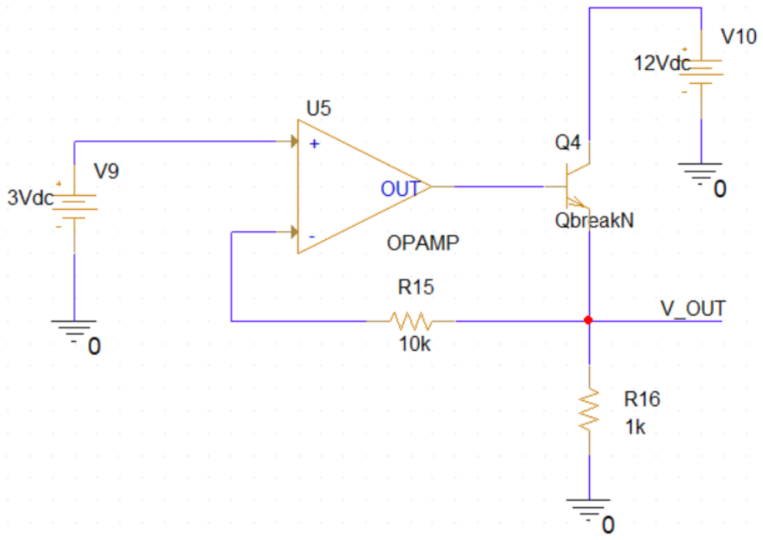

Figure 3.4: Opamp follower circuit

The voltage at the positive pin of the Opamp is copied to V_{OUT}. In this schematic, R16 is used to simulate a load device, which can be a motor or an high power LED. However, in this case, there is a high current can pass the load.
Students are proposed to run the simulation with bias configuration, capture the results and place them in the report.
Finally, your computations go here to explain the results.

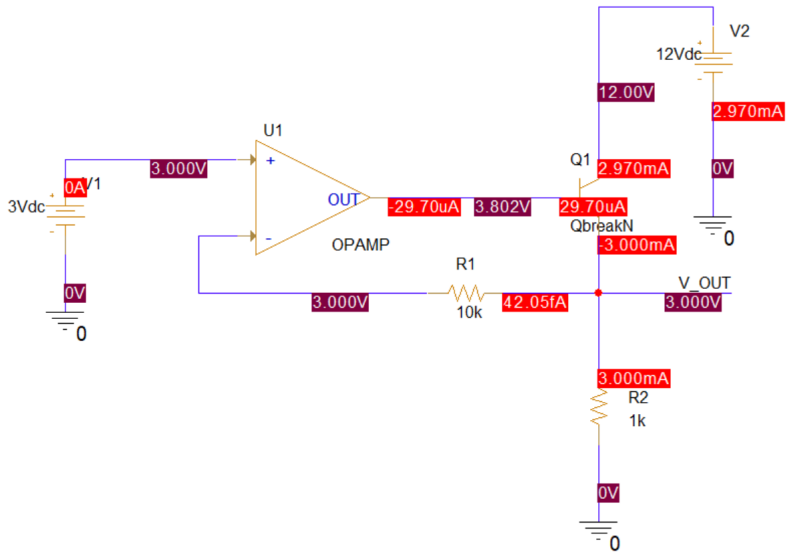

Figure 3.5: The bias point simulation

We have: $V_{(+)} = V_{(-)} = V_E = 3V$

$$I_E = \frac{V_E}{R16} = \frac{3V}{1k\Omega} = 3mA$$

$$I_C = \frac{\beta}{\beta + 1} I_E = \frac{100}{101} \cdot 3mA = 2.97mA$$

$$I_B = I_E - I_C = 3mA - 2.97mA = 0.03mA$$

$$V_B = V_E + 0.7V = 3V + 0.7V = 3.7V$$

3.3 Voltage Follower with Gain

This basic circuit is not limited to the unity-gain configuration. As with a non-buffered op-amp, you can insert resistors into the feedback path to create overall gain from the input to the load voltage. Here is the non-unity-gain version of the circuit:
Students are proposed to implement this circuit on PSPICE with input is 2V and the gain is 3. The voltage supply for the load side is 12VDC. Value of R_{LOAD} is 1K.

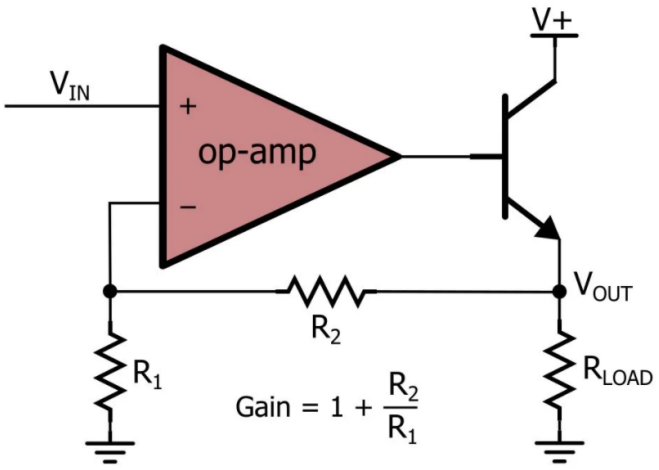

Figure 3.6: Opamp follower with gain for the output

The simulation results in PSPICE (bias configuration) are presented here. Moreover, a short explanations are required in this report to explain the gain of the output follower voltage.

Simulation results:

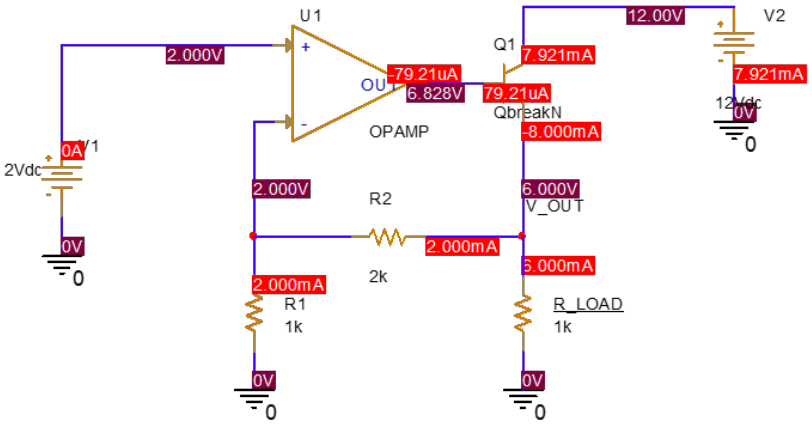

Figure 3.7: Simulation results with $R_1 = 1K\Omega$ and $R_2 = 2K\Omega$

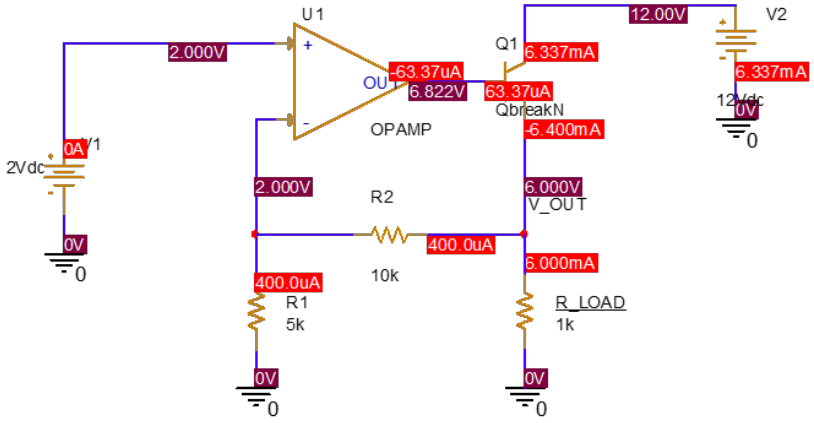

Figure 3.8: Simulation results with $R_1 = 5K\Omega$ and $R_2 = 10K\Omega$

Explanation:

Both simulations use the same input voltage $V_{in} = 2\,V$ and the same resistor ratio $\frac{R_2}{R_1} = 2$. Therefore, the voltage gain is:

$$A_v = 1 + \frac{R_2}{R_1} = 1 + 2 = 3$$

So the output voltage is:

$$V_{out} = A_v \cdot V_{in} = 3 \cdot 2\,V = 6\,V$$

This result is confirmed by both simulations in fig. 3.7 and fig. 3.8.

3.4 Summing Amplifier

Students are proposed to implement following schematic in PSPICE and run the simulation with $R1 = 1K, R2 = 2K, R3 = 5K, Rf = 9K, Ri = 1K$. Their inputs are $V_1 = 1V$, $V_2 = 2V$ and $V_3 = 3V$. This circuit is a non inverting summing configuration using opamp.

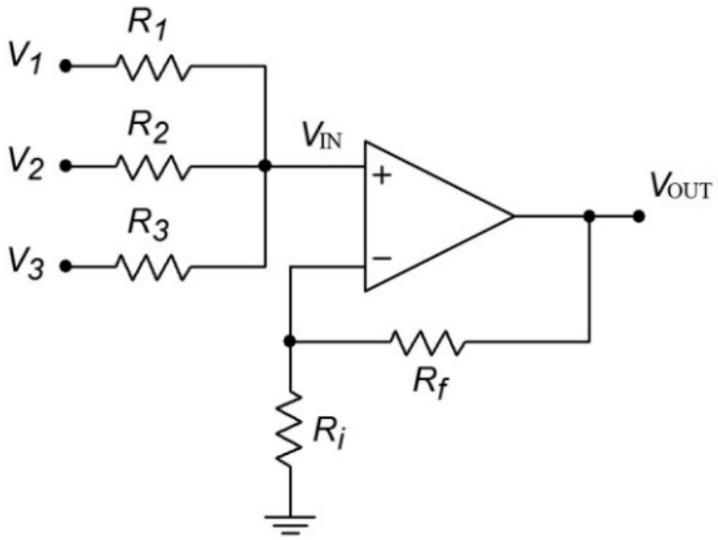

Figure 3.9: Non inverse summing using OPAMP

Students are proposed to design the schematic and place the results in this report.

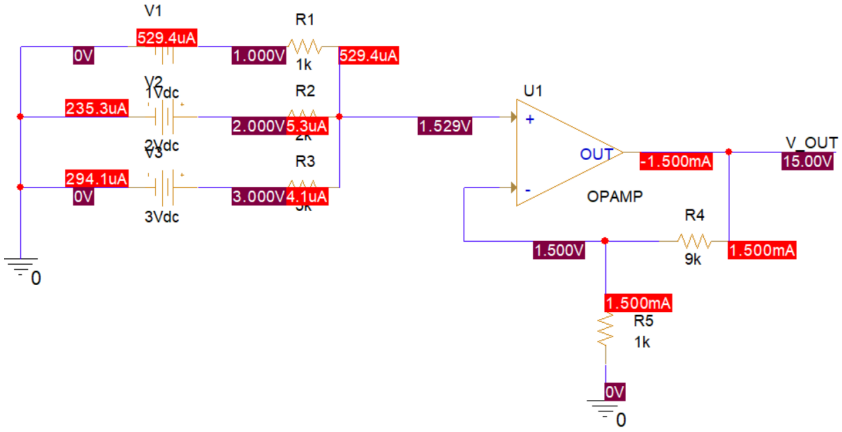

Figure 3.10: Simulation

To prevent saturation at the OpAmp input, we set the input voltage to 0, using KVL:

$$\frac{V_{in}-V_1}{R_1}+\frac{V_{in}-V_2}{R_2}+\frac{V_{in}-V_3}{R_3}=0 \iff \frac{V_{in}-1}{1}+\frac{V_{in}-2}{2}+\frac{V_{in}-3}{5}=0 \Rightarrow V_{in}=1.53 \text{ V}$$

$$A=1+\frac{R_f}{R_i}=1+\frac{9}{1}=10$$

$$V_{out}=A\cdot V_{in}=10\cdot 1.53=15.3 \text{ V}$$

The second type of the summing amplifier is proposed as follows (Inverse Summing):

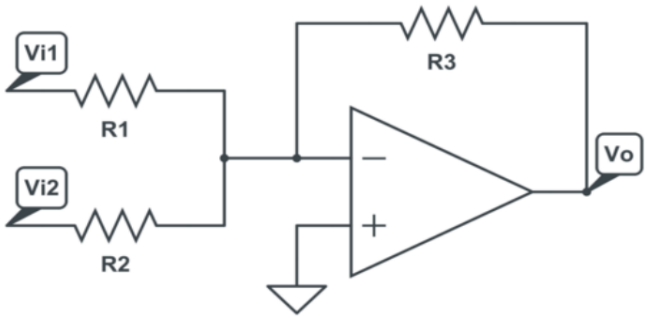

Figure 3.11: Inverse summing using OPAMP

Students are proposed to do the same steps above, with $R_1 = 1K$, $R_2 = 2K$, $R_3 = 10K$ and $V_1 = 1V$, $V_2 = 5V$.

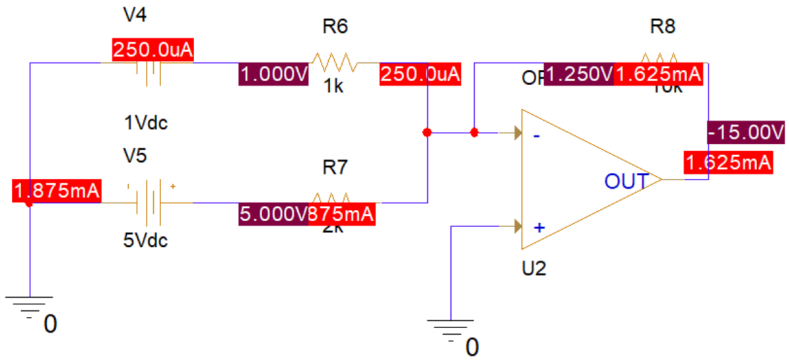

Figure 3.12: Simulation

$$I_1 = \frac{V_1 - V_{in}}{R_1} = \frac{1-0}{1K} = 1mA$$

$$I_2 = \frac{V_2 - V_{in}}{R_2} = \frac{5-0}{2K} = 2.5mA$$

$$V_{OUT} = -R_3 \cdot (I_1 + I_2) = -10K \cdot (1mA + 2.5mA) = -35V$$

3.5 Low Pass Filter

Low pass filter is a filter which passes all frequencies from 0Hz (DC current) to upper cut-off frequency f_H and rejects any signals above this frequency. A picture to demonstrate a low pass filter behavior is shown in the figure bellow:

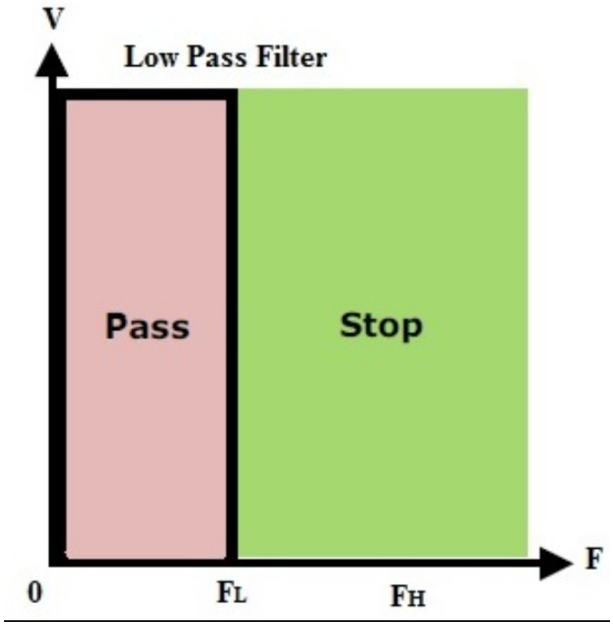

Figure 3.13: Low pass filter principles

Similar to the closed loop configuration, there also 2 types of low pass filter, including the inverting and non-inverting low pass filter. The figure bellow is an inverting low pass filter. The cut-off frequency is determined by this equation:

$$f_H = \frac{1}{2\pi R_2 C}$$

By applying the value of R2 = 10K Ohm and C = 1nF , the cut-off frequency is around 16K Hz. In order to see the results, students are proposed to run the AC Sweep

simulation profile (**Linear Type, Start and Stop frequency are 1Hz and 50kHz, 200 points**), as follows:

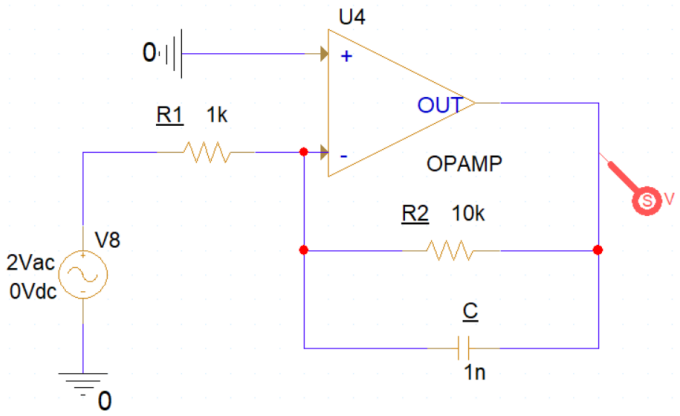

Figure 3.14: Inverting low pass filter

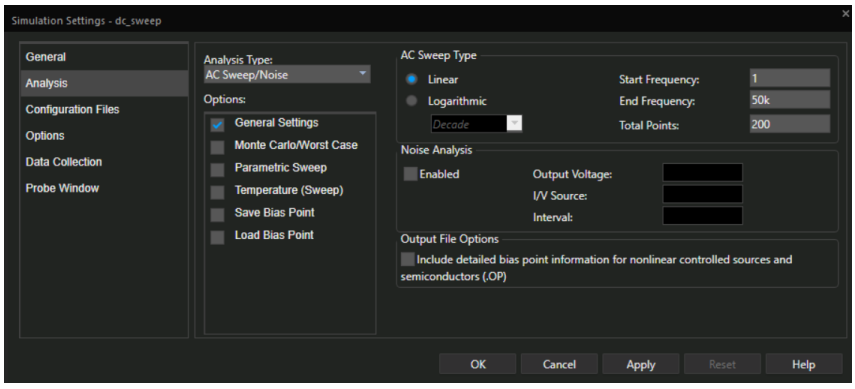

Figure 3.15: AC Sweep simulation profile

The final results can be archived like the figure bellow:

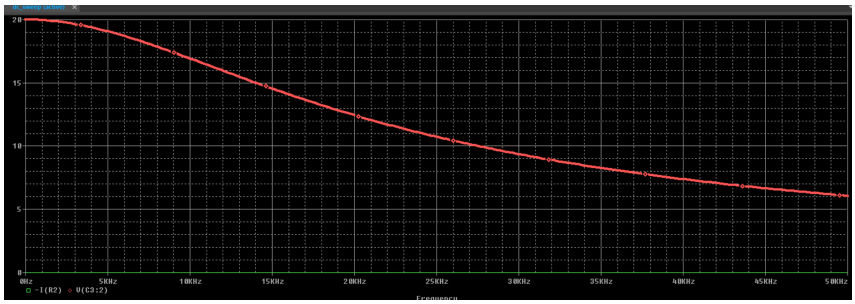

Figure 3.16: Simulation results

It is said that the cut-off frequency point having the gain reduced 3dB. The gain at 0Hz is 10 (input voltage is 2V and output voltage is 20V), or $20\log(10) = 20$ dB, meanwhile, the gain at 16kHz is 7 (input voltage is 2V and output voltage is 14V), or $20\log(7) \approx 16.9$ dB.

The second type of a low pass filter, the non-inverting configuration, is presented as follows:

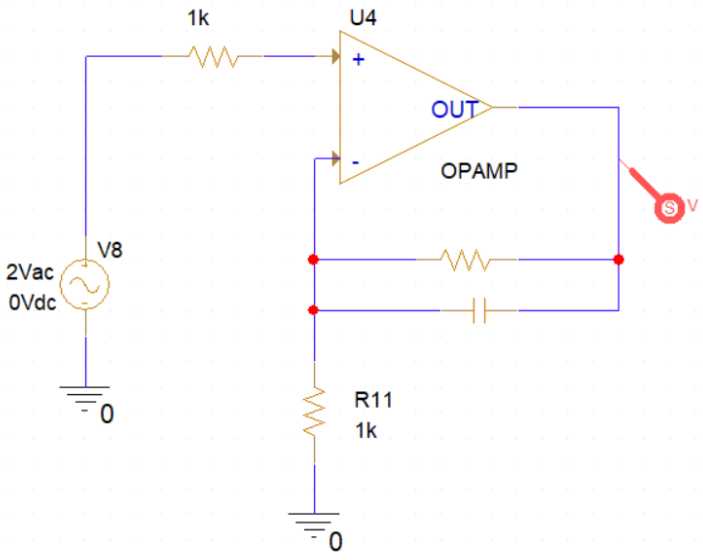

Figure 3.17: Non-inverting low pass filter

Students are proposed to calculate the value of R and C to have the amplifier factor equal to 10 and the cut-off frequency is the same as the previous example. The simulation result with AC Sweep mode is required to plot in this report as well.

Calculation:

To have the amplifier factor equal to 10, the ratio between R2 and R1 is calculated as follows:

$$A_v = 1 + \frac{R_2}{R_3} = 10 \Rightarrow \frac{R_2}{R_3} = 9$$

By choosing $R_2 = 9k\Omega$ and $R_3 = 1k\Omega$, the cut-off frequency is calculated as follows:

$$f_H = \frac{1}{2\pi R_2 C} = 16kHz$$

$$\Longrightarrow C = \frac{1}{2\pi R_2 f_H} = \frac{1}{2\pi \cdot 9k\Omega \cdot 16kHz} \approx 1.1nF$$

The simulation result is presented as follows:

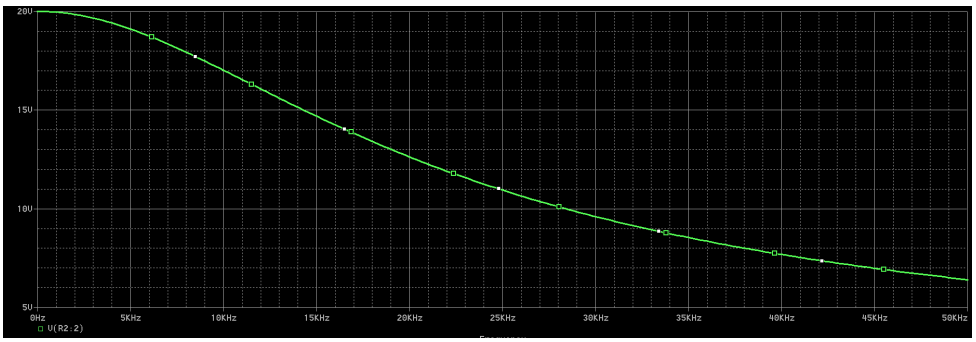

Figure 3.18: Simulation results of non-inverting low pass filter

The gain at 0Hz is 10 (input voltage is 2V and output voltage is 20V), or $20\log(10) = 20$ dB, meanwhile, the gain at 16kHz is 7 (input voltage is 2V and output voltage is 14V), or $20\log(7) \approx 16.9$ dB.

3.6 High Pass Filter

In contrast to the low pass filter, there is a high pass filter, which can be referred from this link: https://www.allaboutcircuits.com/video-tutorials/op-amps-low-pass-and-high-pass

Students are proposed to implement a high pass filter in PSPICE and explain the behaviors of your high pass filter.

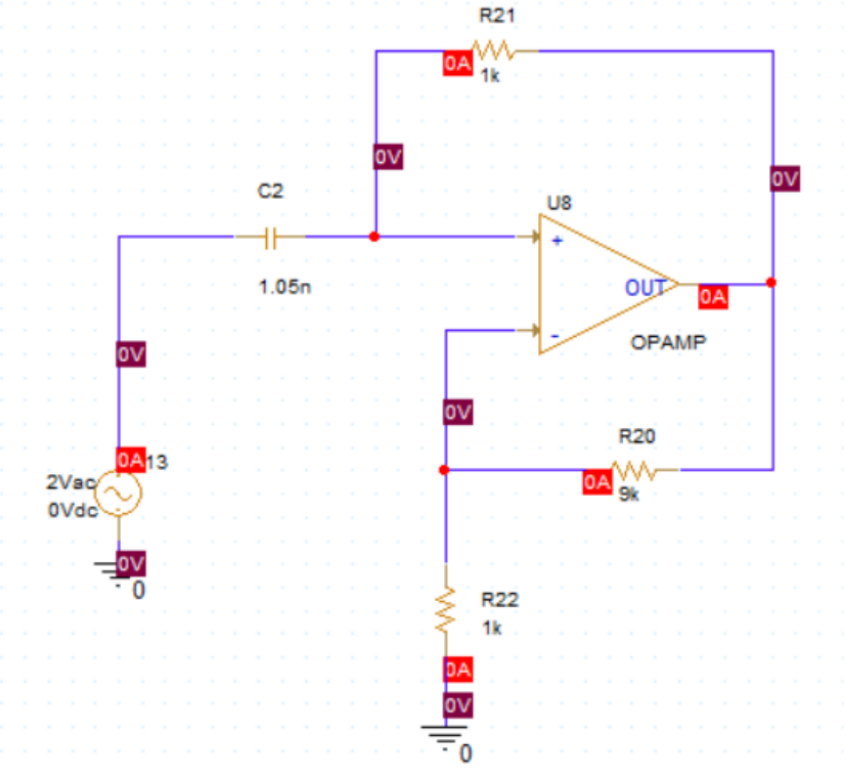

Figure 3.19: Active high pass filter with amplification.

3.7 Comparator with Hysteresis (Schmitt Trigger)

The two resistors R1 and R2 act only as a "pure" attenuator (voltage divider). The input loop acts as a simple series voltage summer that adds a part of the output voltage in series to the circuit input voltage. This series positive feedback creates the needed hysteresis that is controlled by the proportion between the resistances of R1 and the whole resistance (R1 and R2). The effective voltage applied to the op-amp input is floating so the op-amp must have a differential input.

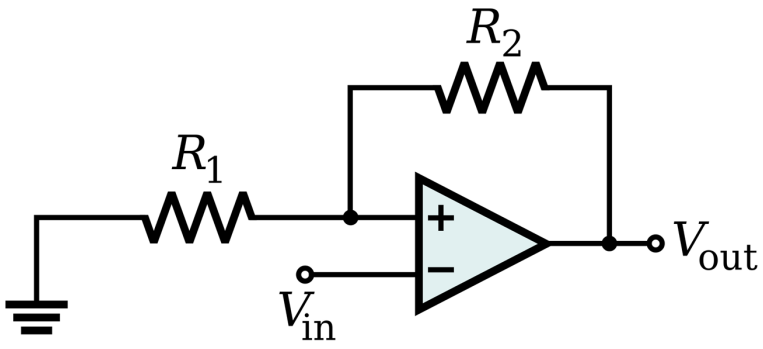

Figure 3.20: Schmitt Trigger Circuit

The circuit is named inverting since the output voltage always has an opposite sign to the input voltage when it is out of the hysteresis cycle (when the input voltage is above the high threshold or below the low threshold). However, if the input voltage is within the hysteresis cycle (between the high and low thresholds), the circuit can be inverting as well as non-inverting. The output voltage is undefined and it depends on the last state so the circuit behaves like an elementary latch.

In PSPice, this trigger is implemented as follows, with 3 voltage markers:

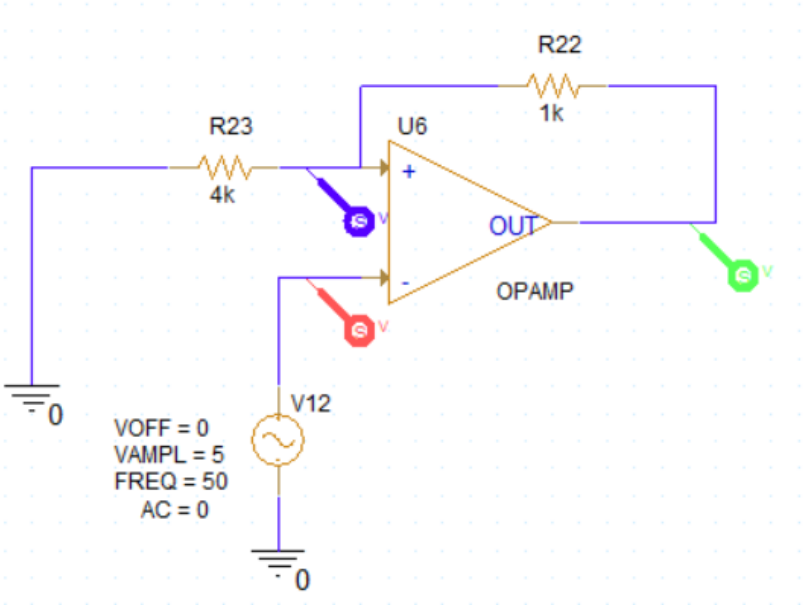

Figure 3.21: Schmitt Trigger Circuit in PSPice

The OPAM device is modified in the Properties windows (right click on the component and chose Edit Properties or double click on the component), in order to set the VPOS

and VNEG to +5V and -5V, as follows:

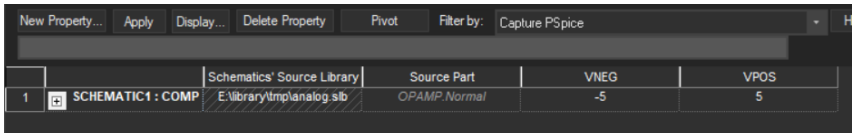

Figure 3.22: Schmitt trigger in PSPICE

The simulation profile in this exercise is the Time Domain, and is configured as follows:

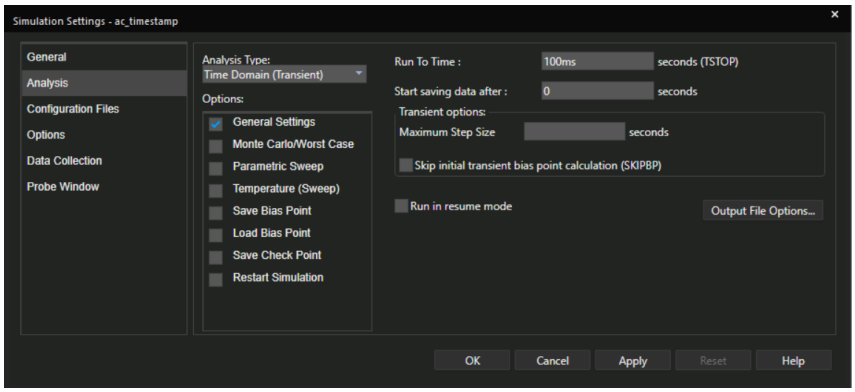

Figure 3.23: Simulation profile

Finally, the simulation results can be archived as follows:

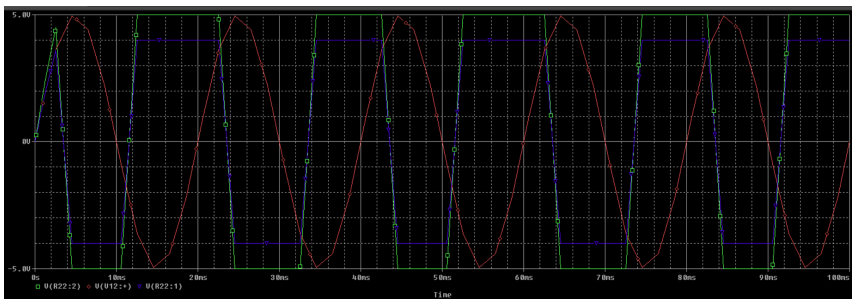

Figure 3.24: Schmitt trigger simulation results

Students are proposed to explain the signal at the output of the opamp. Why the signal is toggled at +4 and -4V.

Explaination:

The output signal is toggled at $+4V$ and $-4V$ due to the positive feedback created by the resistor network R1 and R2. This feedback shifts the switching thresholds of the comparator from 0 V to two distinct values, forming a hysteresis window. When the output

saturates at $+5V$, the feedback sets the upper threshold at $+4V$. Similarly, when the output saturates at $-5V$, the lower threshold becomes $-4V$. As a result, the output changes state only when the input voltage exceeds these thresholds, ensuring stable switching and noise immunity.

4 Altium Designer

4.1 LED driver

In this project, we will show how to build a simple LED driver circuit. A simple driver based on BJT is proposed in this section.

4.1.1 Schematic design

The manual for the schematic is posted in this link:

https://www.youtube.com/watch?v=ftiX8peTsiw

Students are proposed to design the schematic and place the results in this report.
Your image goes here:

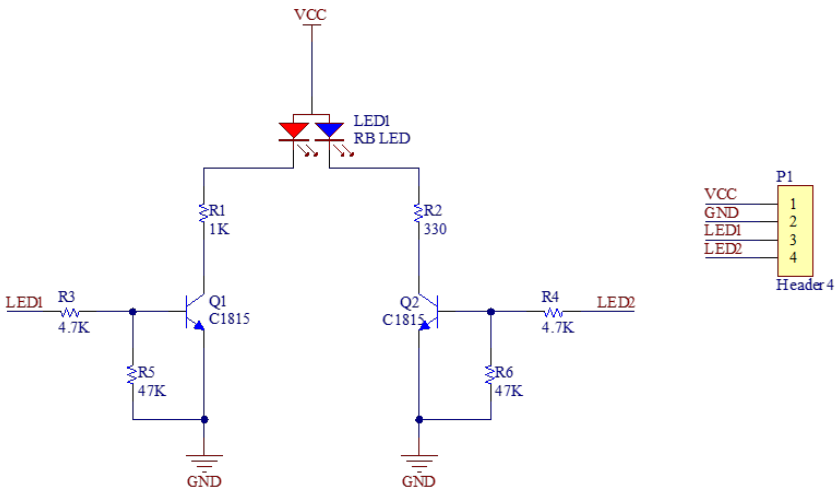

Figure 4.1: Schematic of LED driver

4.1.2 PCB layout

The manual for the PCB layout is posted in this link:

https://www.youtube.com/watch?v=btpAoh3nmBU

Your image goes here:

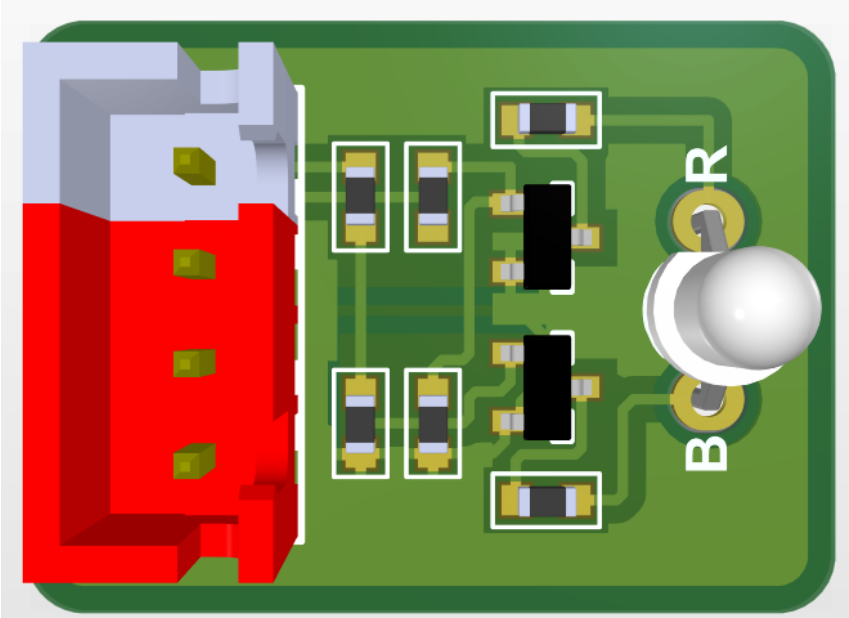

Figure 4.2: Top layer of LED driver PCB

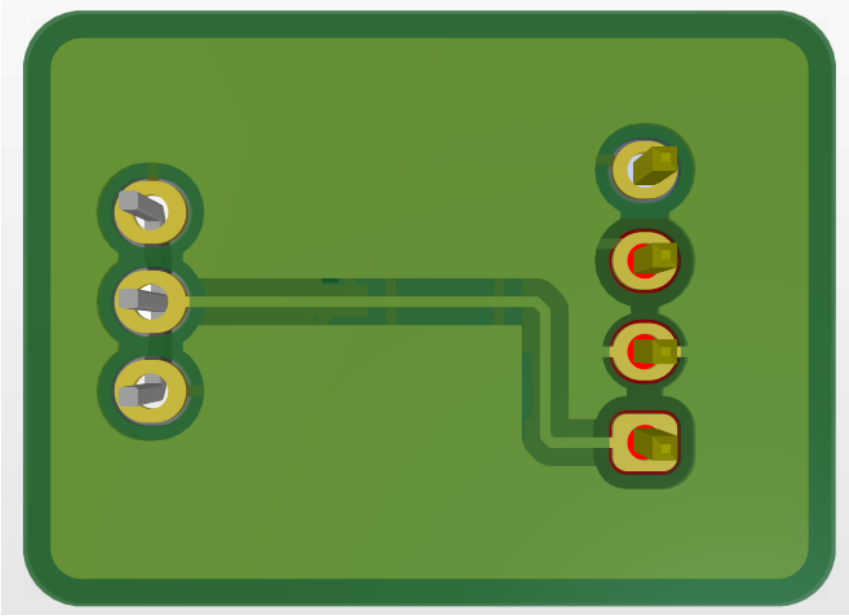

Figure 4.3: Bottom layer of LED driver PCB

4.2 Relay Controller

4.2.1 Schematic design

The manual for the schematic is posted in this link:

https://www.youtube.com/watch?v=VcO_F97ydFM‘

Students are proposed to design the schematic and place the results in this report.
Your image goes here:

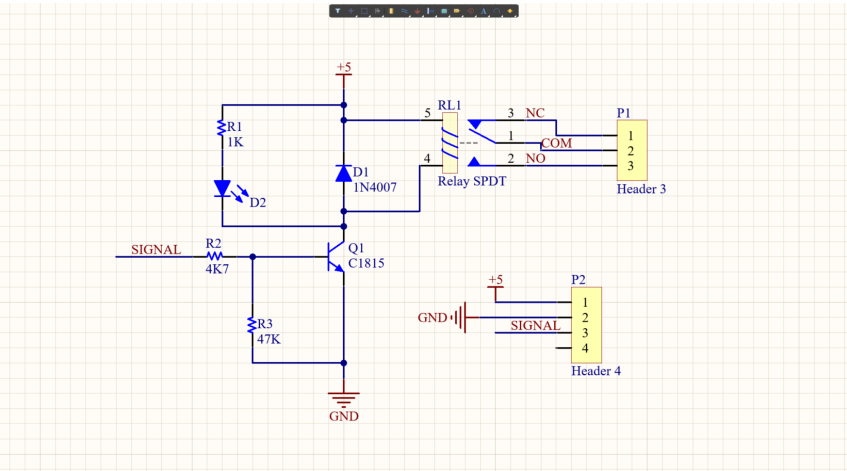

Figure 4.4: Schematic of Relay Controller

4.2.2 PCB layout

The manual for the PCB layout is posted in this link:

https://www.youtube.com/watch?v=DbqcbOzQOE8

Your image goes here:

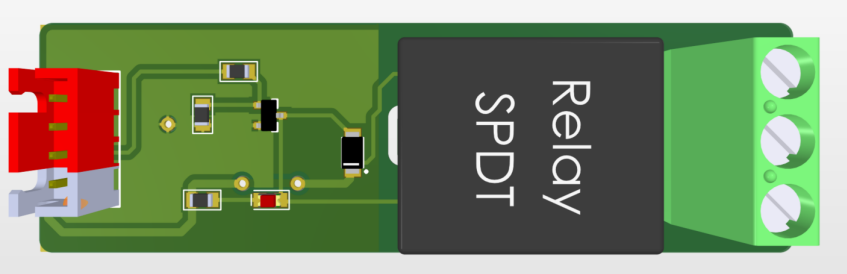

Figure 4.5: Top layer of Relay Controller PCB

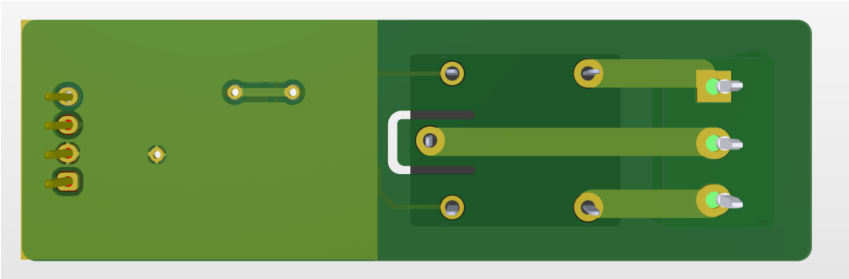

Figure 4.6: Bottom layer of Relay Controller PCB