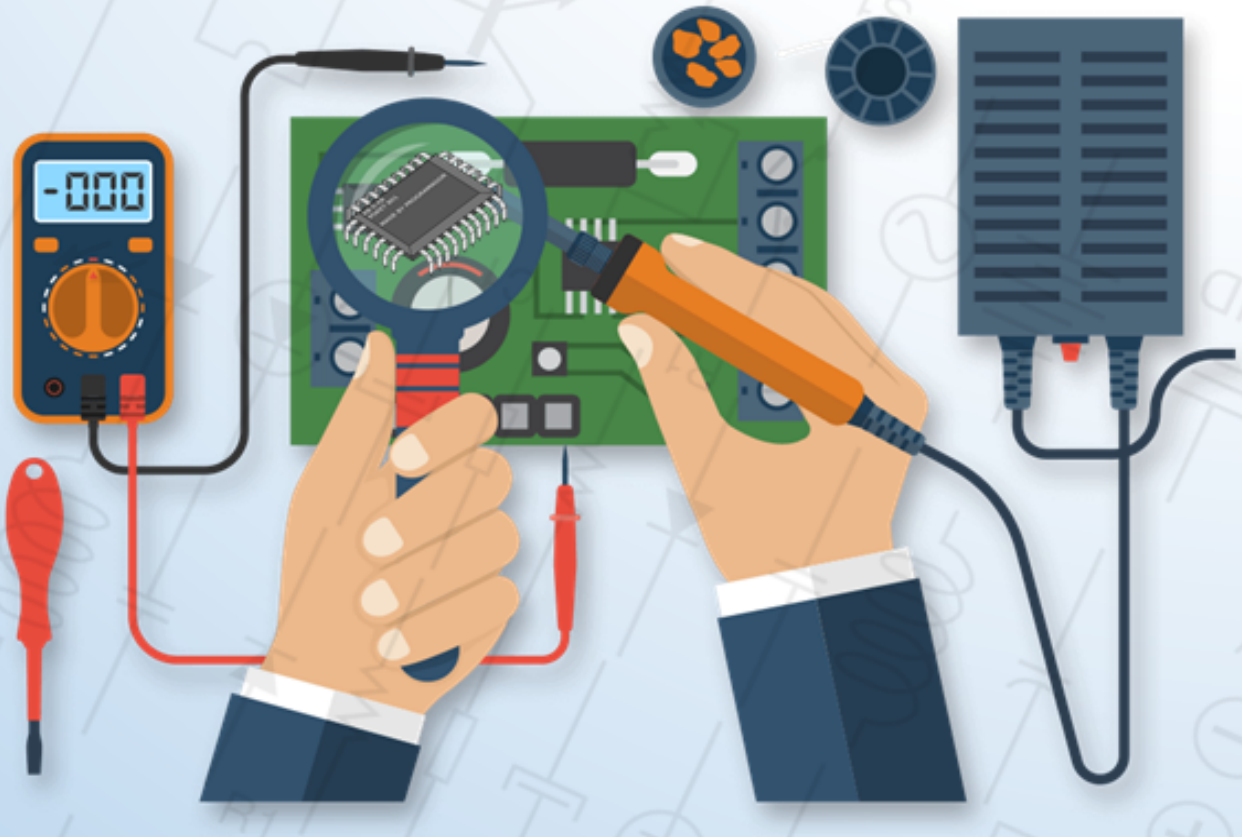
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY
COMPUTER ENGINEERING

Electronic Device Component



Dr. Le Trong Nhan

Contents

CHAPTER 1

Operational Amplifier - OPAMP

1 Introduction

Operational Amplifiers, also known as Op-amps, are basically a voltage amplifying device designed to be used with components like capacitors and resistors, between its in/out terminals. They are essentially a core part of analog devices. Feedback components like these are used to determine the operation of the amplifier. The amplifier can perform many different operations, giving it the name Operational Amplifier.

One key to the usefulness of these little circuits is in the engineering principle of feedback, particularly negative feedback, which constitutes the foundation of almost all automatic control processes. The principles presented in this section, extend well beyond the immediate scope of electronics. It is well worth the electronics student's time to learn these principles and learn them well.

Operational amplifiers can have either a closed-loop operation or an open-loop operation. The operation (closed-loop or open-loop) is determined by whether or not feedback is used. Without feedback the operational amplifier has an open-loop operation. This open-loop operation is practical only when the operational amplifier is used as a cooperator (a circuit which compares two input signals or compares an input signal to some fixed level of voltage). As an amplifier, the open-loop operation is not practical because the very high gain of the operational amplifier creates poor stability. (Noise and other unwanted signals are amplified so much in open-loop operation that the operational amplifier is usually not used in this way.) Therefore, most operational amplifiers are used with feedback (closed-loop operation).

2 Closed Loop Operation

Operational amplifiers are used with degenerative (or negative) feedback which reduces the gain of the operational amplifier but greatly increases the stability of the circuit. In the closed-loop configuration, the output signal is applied back to one of the input terminals. This feedback is always degenerative (negative). In other words, the feedback signal always opposes the effects of the original input signal. One result of degenerative feedback is that the inverting and non-inverting inputs to the operational amplifier will be kept at the same potential.

Closed-loop circuits can be of the inverting configuration or non-inverting configuration.

2.1 Non inverting configuration

The typical circuit for this configuration is shown in the figure bellow:

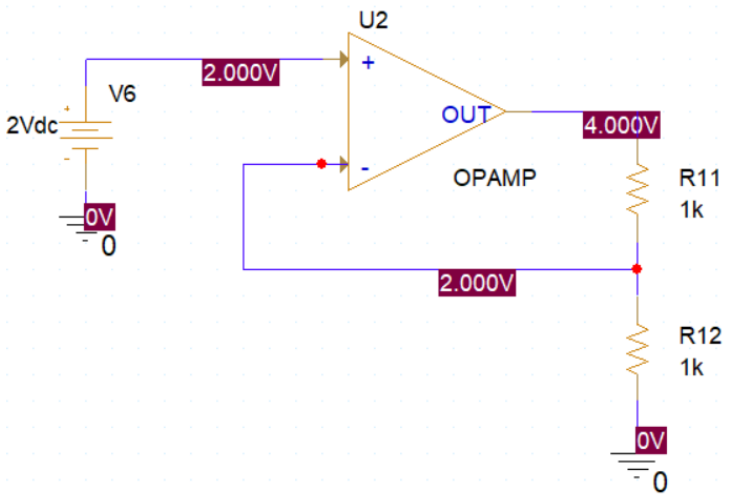


Figure 1.1: Non inverting configuration

The new component, named also OPAMP (Operational Amplifier) is easily found in the favorite list of the PSPICE.

In order to explain the 4V at the ouput, it is obviously that $V(+) = V(-) = 2V$ in a closed loop configuration. Therefore, from a resistor bridge at the output, $V_{OUT} = 4V$.

2.2 Inverting configuration

In this configuration, the output is connected directly to a pin of the opamp as follow:

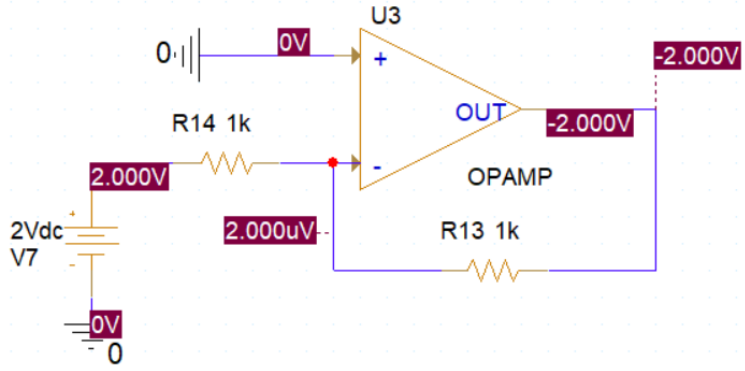


Figure 1.2: Inverting configuration

As the output voltage is negative, which is inverted to the input, the name of this circuit is the invert connection. Students are proposed to perform calculations to confirm the output, which is $-2V$.

3 Exercise and Report

3.1 Voltage Follower

Voltage follower is one of the simplest uses of an operational amplifier, where the output voltage is exactly same as the input voltage applied to the circuit. In other words, the gain of a voltage follower circuit is unity. The connections are proposed as follows:

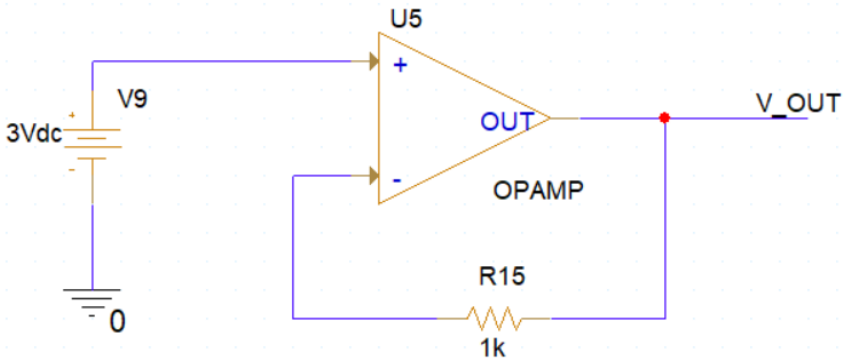


Figure 1.3: Opamp follower circuit

A voltage follower has low output impedance and extremely high input impedance, and this makes it a simple and effective solution to problematic impedance relationships. If a high-output-impedance sub-circuit must transfer a signal to a low-input-impedance sub-circuit, a voltage follower placed between these two sub-circuits will ensure that the full voltage is delivered to the load.

Students are propose to run the simulation with bias mode to confirm that $V_{OUT} = V(+)$. The feedback resistance is also required to change.

Your calculations are presented here to prove $V_{OUT} = V(+)$ with any value of R15.

3.2 High-Current Voltage Follower

The voltage follower's low output impedance makes it a good circuit for driving current into a low-impedance load, but it's important to remember that most op-amps are not designed to deliver large output currents. The most basic circuit for buffering an op-amp's output current is the following:

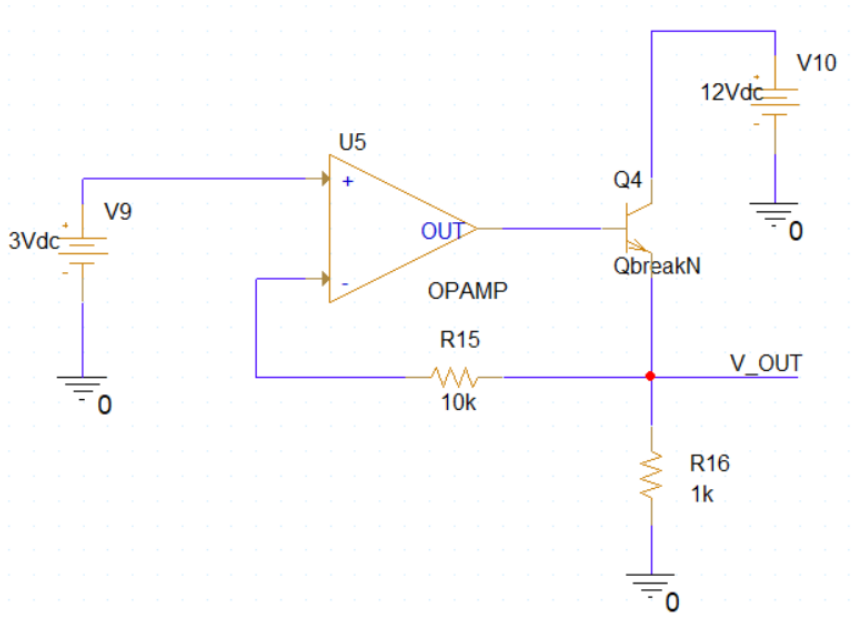


Figure 1.4: Opamp follower circuit

The voltage at the positive pin of the Opamp is copied to V_{OUT}. In this schematic, R16 is used to simulate a load device, which can be a motor or an high power LED. However, in this case, there is a high current can pass the load.

Students are proposed to run the simulation with bias configuration, capture the results and place them in the report.

Finally, your computations go here to explain the results.

3.3 Voltage Follower with Gain

This basic circuit is not limited to the unity-gain configuration. As with a non-buffered op-amp, you can insert resistors into the feedback path to create overall gain from the input to the load voltage. Here is the non-unity-gain version of the circuit:
Students are proposed to implement this circuit on PSPICE with input is 2V and the gain is 3. The voltage supply for the load side is 12VDC. Value of R_{LOAD} is 1K.

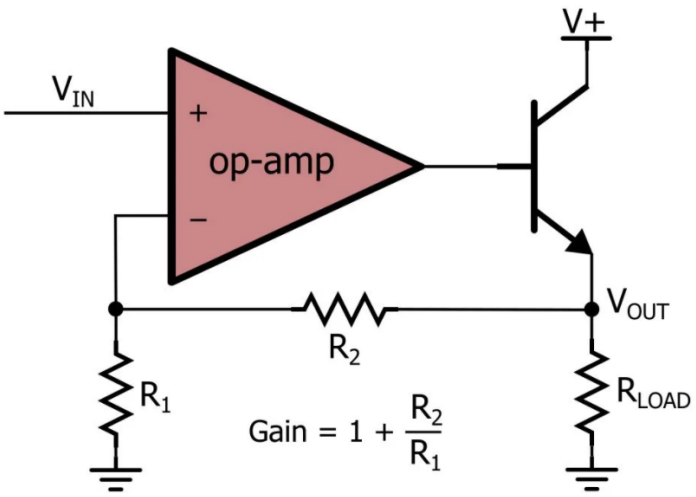


Figure 1.5: Opamp follower with gain for the output

The simulation results in PSPICE (bias configuration) are presented here. Moreover, a short explanations are required in this report to explain the gain of the output follower voltage.

3.4 Summing Amplifier

Students are proposed to implement following schematic in PSPICE and run the simulation with R1 = 1K, R2 = 2K, R3 = 5K, Rf = 9K, Ri = 1K. There inputs are V1 = 1V, V2 = 2V and V3 = 3V. This circuit is a non inverting summing configuration using opamp.

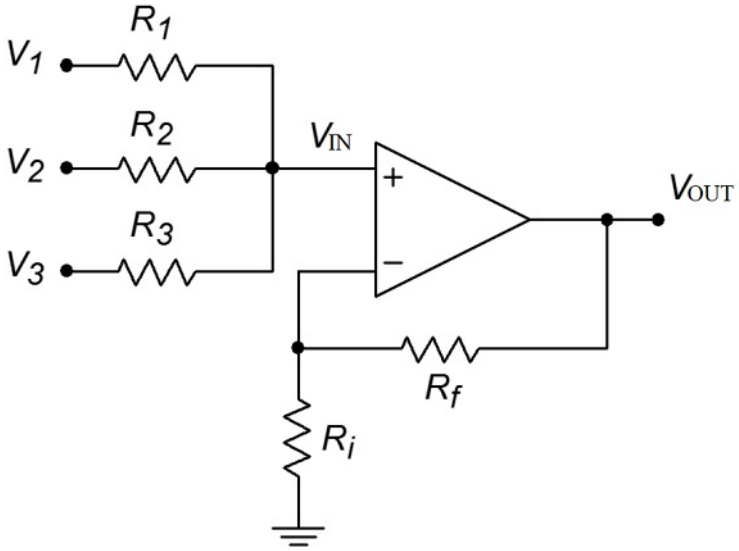


Figure 1.6: Non inverse summing using OPAMP

Students are proposed to design the schematic and place the results in this report.

Your image goes here
Your calculations go here to explain the value of V_{OUT}

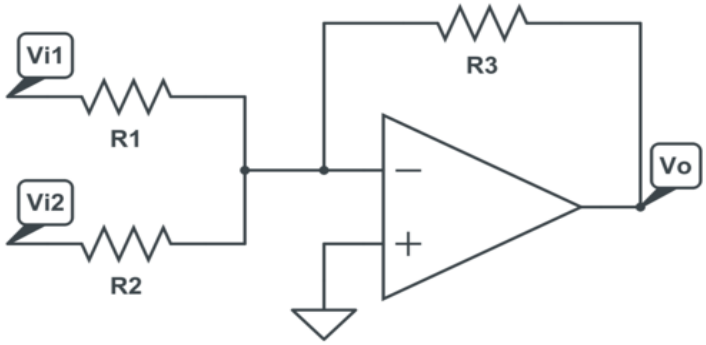


Figure 1.7: Inverse summing using OPAMP

The second type of the summing amplifier is proposed as follows:
Students are proposed to do the same steps above, with R1 = 1K, R2 = 2K, R3 = 10K and V1 = 1V, V2 = 5V.

3.5 Low Pass Filter

Low pass filter is a filter which passes all frequencies from 0Hz (DC current) to upper cut-off frequency f_H and rejects any signals above this frequency. A picture to demonstrate a low pass filter behavior is shown in the figure bellow:

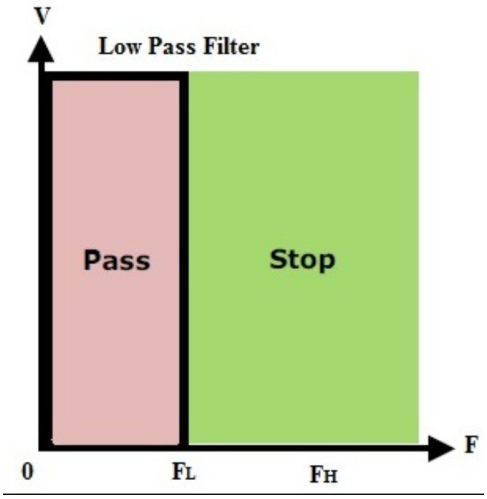


Figure 1.8: Low pass filter principles

Similar to the closed loop configuration, there also 2 types of low pass filter, including the inverting and non-inverting low pass filter. The figure bellow is an inverting low pass filter. The cut-off frequency is determined by this equation:

$$f_H = \frac{1}{2\pi R_2 C}$$

By applying the value of $R2 = 10KOhm$ and $C = 1nF$, the cut-off frequency is around $16KHz$. In order to see the results, students are proposed to run the AC Sweep simulation profile (**Linear Type, Start and Stop frequency are 1Hz and 50kHz, 200 points**), as follows:

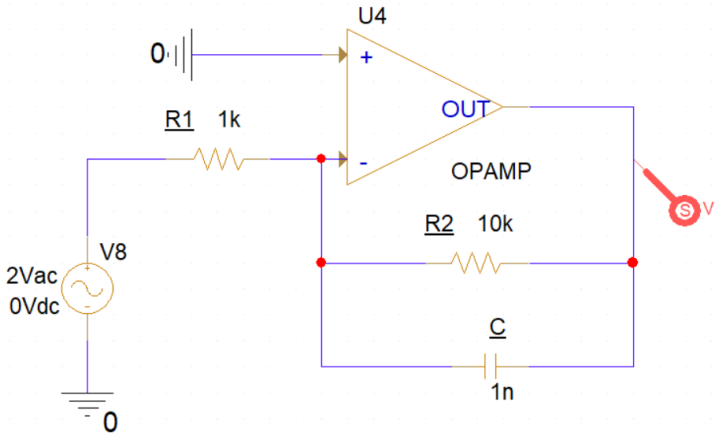


Figure 1.9: Inverting low pass filter

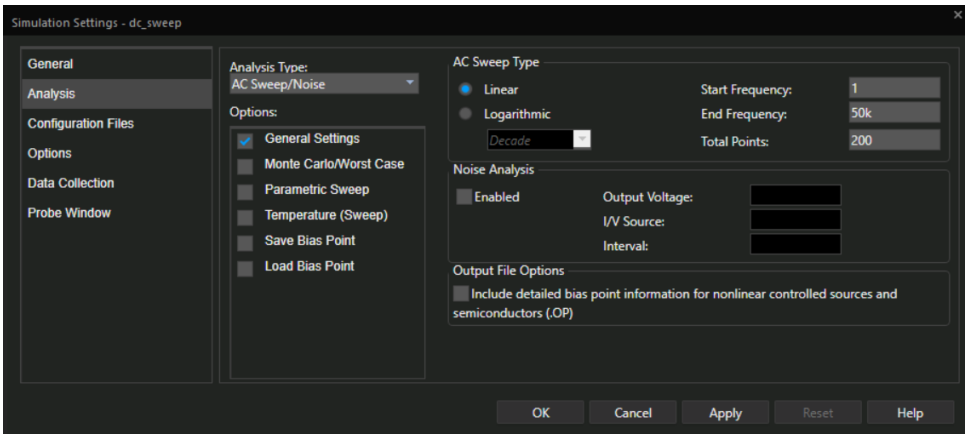


Figure 1.10: AC Sweep simulation profile

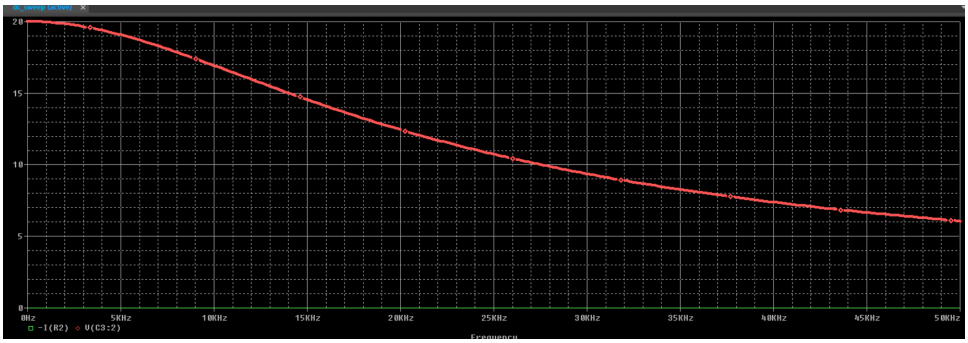


Figure 1.11: Simulation results

The final results can be archived like the figure bellow:
It is said that the cut-off frequency point having the gain reduced 3dB. The gain at 0Hz is 10 (input voltage is 2V and output voltage is 20V), or $20log(10) = 20dB$, meanwhile, the gain at 16kHz is 7 (input voltage is 2V and output voltage is 14V), or $20log(7) = 16.9$.

The second type of a low pass filter, the non-inverting configuration, is presented as follows:

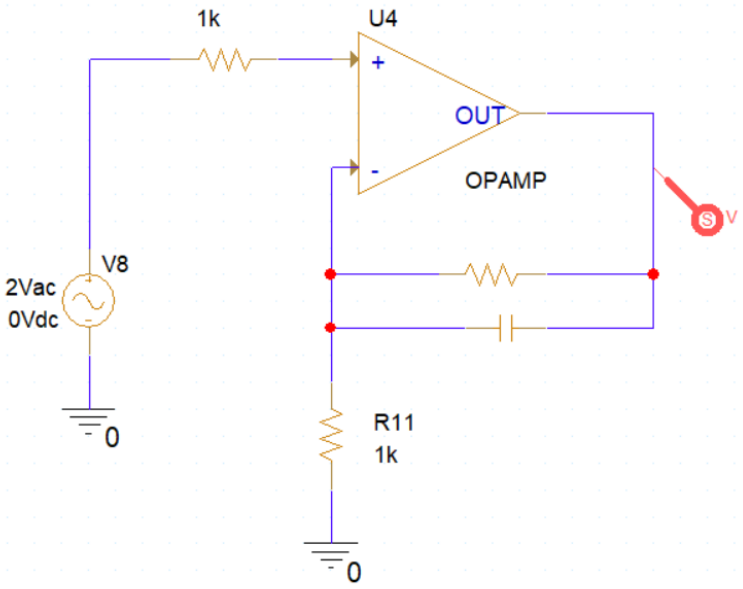


Figure 1.12: Non-inverting low pass filter

Students are proposed to calculate the value of R and C to have the amplifier factor equal to 10 and the cut-off frequency is the same as the previous example. The simulation result with AC Sweep mode is required to plot in this report as well.

3.6 High Pass Filter

In contrast to the low pass filter, there is a high pass filter, which can be referred from this link:

https://www.allaboutcircuits.com/video-tutorials/op-amps-low-pass-and-high-pass-active-filters/

Students are proposed to implement a high pass filter in PSPICE and explain the behaviors of your high pass filter.

3.7 Comparator with Hysteresis (Schmitt Trigger)

The two resistors R1 and R2 act only as a "pure" attenuator (voltage divider). The input loop acts as a simple series voltage summer that adds a part of the output voltage in series to the circuit input voltage. This series positive feedback creates the needed hysteresis that is controlled by the proportion between the resistances of R1 and the whole resistance (R1 and R2). The effective voltage applied to the op-amp input is floating so the

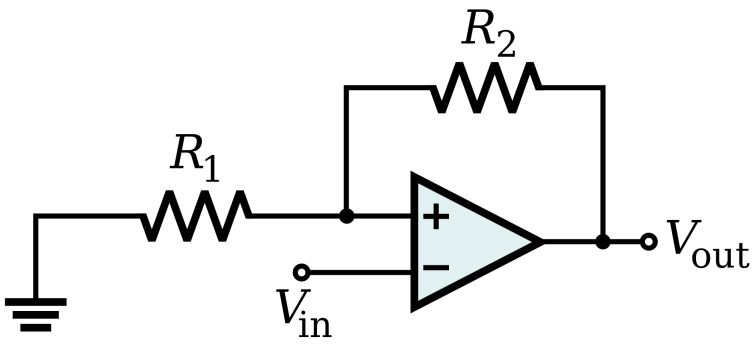


Figure 1.13: Inverting Schmitt trigger

op-amp must have a differential input.

The circuit is named inverting since the output voltage always has an opposite sign to the input voltage when it is out of the hysteresis cycle (when the input voltage is above the high threshold or below the low threshold). However, if the input voltage is within the hysteresis cycle (between the high and low thresholds), the circuit can be inverting as well as non-inverting. The output voltage is undefined and it depends on the last state so the circuit behaves like an elementary latch.

In PSPice, this trigger is implemented as follows, with 3 voltage markers:

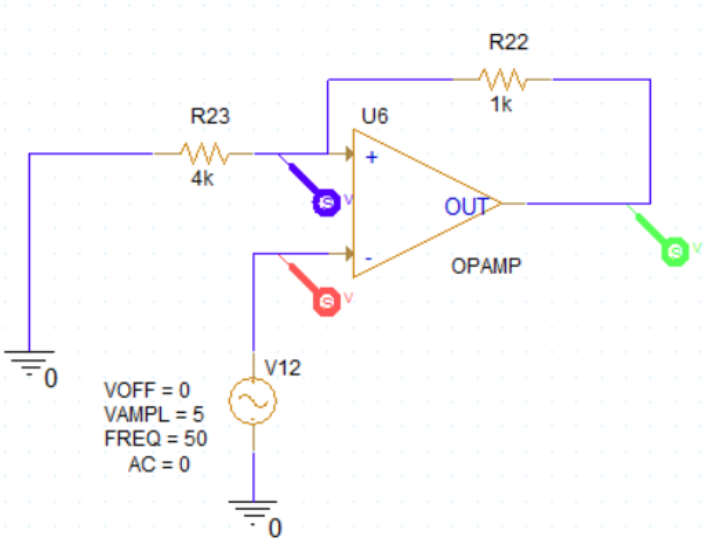


Figure 1.14: Schmitt trigger in PSPICE

The OPAMP device is modified in the **Properties** windows (right click on the component and chose Edit Properties or double click on the component), in order to set the VPOS and VNEG to +5V and -5V, as follows:
The simulation profile in this exercise is the **Time Domain**, and is configured as follows:
Finally, the simulation results can be archived as follows:
Students are proposed to explain the signal at the output of the opamp. Why the signal is toggled at +4V and -4V.

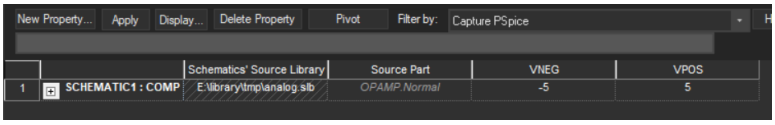


Figure 1.15: Schmitt trigger in PSPICE

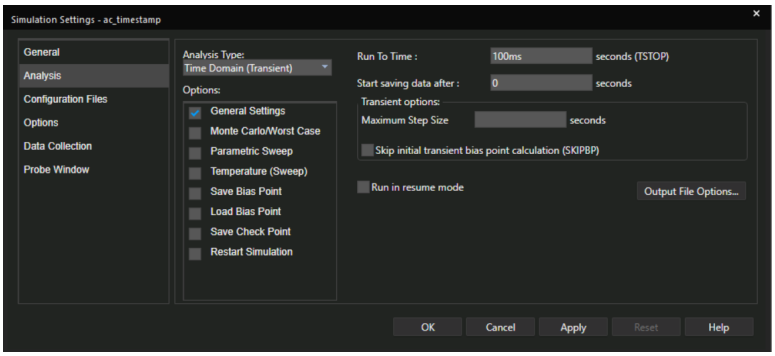


Figure 1.16: Simulation profile

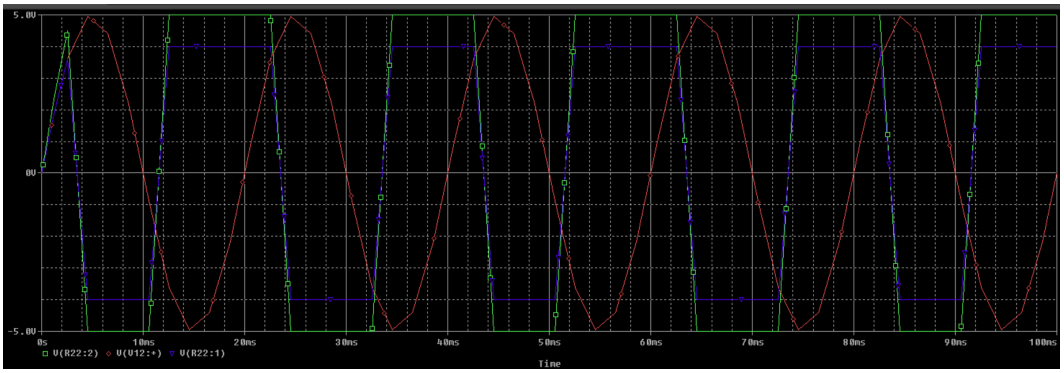


Figure 1.17: Schmitt trigger simulation results

4 Altium Designer

4.1 LED Driver

In this project, we will show how to build a simple LED driver circuit. A simple driver based on BJT is proposed in this section.

4.1.1 Schematic design

The manual for the schematic is posted in this link:

https://www.youtube.com/watch?v=ftiX8peTsiw

Students are proposed to design the schematic and place the results in this report.

Your image goes here

4.1.2 PCB layout

The manual for PCB layout is posted in this link:

https://www.youtube.com/watch?v=btpAoh3nmBU

Your image goes here

4.2 Relay Controller

4.2.1 Schematic design

The manual for the schematic is posted in this link:

https://www.youtube.com/watch?v=VcO_F97ydFM

Students are proposed to design the schematic and place the results in this report.

Your image goes here

4.2.2 PCB layout

The manual for PCB layout is posted in this link:

https://www.youtube.com/watch?v=Dbqcb0zQ0E8

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CHAPTER 2

Chapter 6: Field Effect Transistor (FET)

1 Introduction

In the Bipolar Junction Transistor tutorials, we saw that the output Collector current of the transistor is proportional to input current flowing into the Base terminal of the device, thereby making the bipolar transistor a **CURRENT** operated device (Beta model) as a smaller current can be used to switch a larger load current.

The Field Effect Transistor, or simply FET however, uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the Field Effect Transistor a **VOLTAGE** operated device.

The Field Effect Transistor has one major advantage over its standard bipolar transistor cousins, in that their input impedance, (Rin) is very high, (thousands of Ohms), while the BJT is comparatively low. This very high input impedance makes them very sensitive to input voltage signals, but the price of this high sensitivity also means that they can be easily damaged by static electricity.

2 Junction Field Effect Transistor

We saw previously that a bipolar junction transistor is constructed using two PN-junctions in the main current carrying path between the Emitter and the Collector terminals. The Junction Field Effect Transistor (JUGFET or JFET) has no PN-junctions but instead has a narrow piece of high resistant semiconductor material forming a “Channel” of either N-type or P-type silicon for the majority carriers to flow through with two ohmic electrical connections at either end commonly called the Drain and the Source, respectively.

Before analysing the circuit using JFET, students are proposed to characterize the I-V curve of a JFET in PSPICE (named JbreakN in the Favourite list), to determine IDSS and VP, which are two parameters for a JFET. The circuit bellow is required to implement in PSPICE:

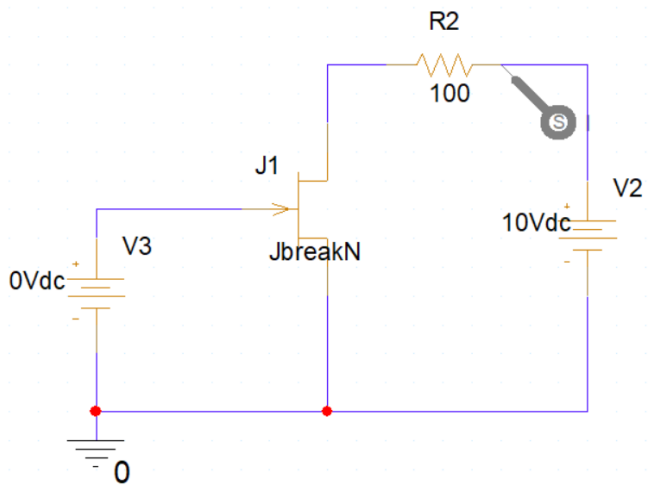

Figure 2.1: JFET circuit in PSPICE

2.1 DC Sweep simulation

In the first simulation, a DC sweep for input source V3 is perform, varying from -3V to 0V to verify the **active region**. The simulation profile is suggested as follows:

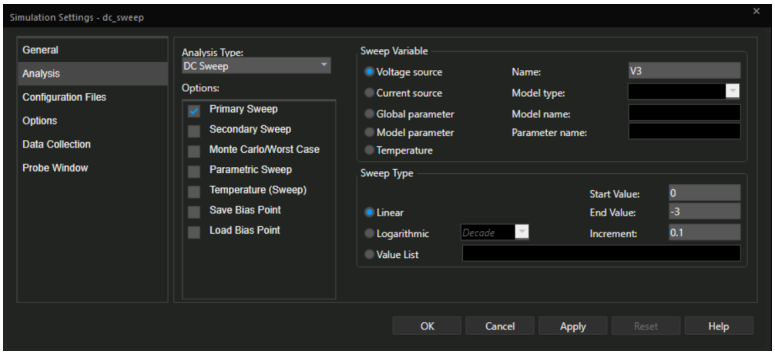

Figure 2.2: DC Sweep simulation profile

The simulation results are presented in the following figure:

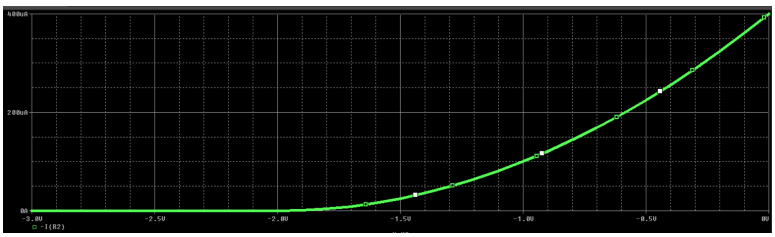

Figure 2.3: Simulation results for sweeping V3 from -3V to 0V

The simulation results confirm that **IDSS = 400mA** and **VP = -2V** for a typical JFET device in PSPICE.

2.2 Nested DC Sweep simulation

In this simulation, more details for the I-V characteristics are performed. Instead of varying the source V3, V2 can be also varied in a nested DC Sweep simulation.

Firstly, for the primary DC sweep source, which is set to V2, is configured as follows:

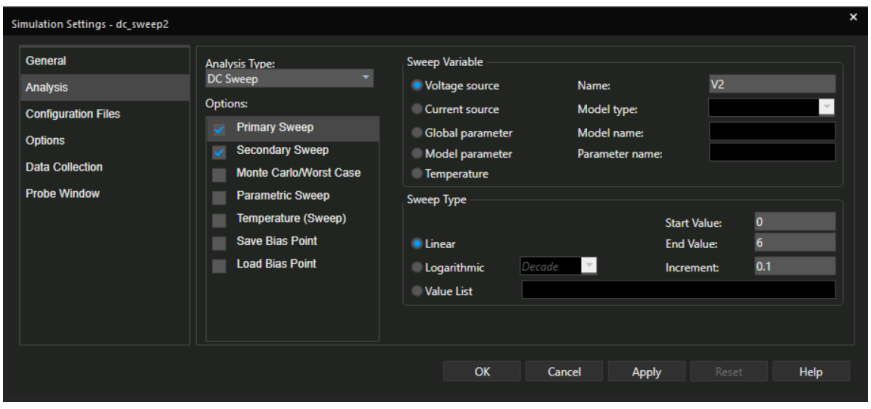

Figure 2.4: Primary dc sweep source V2

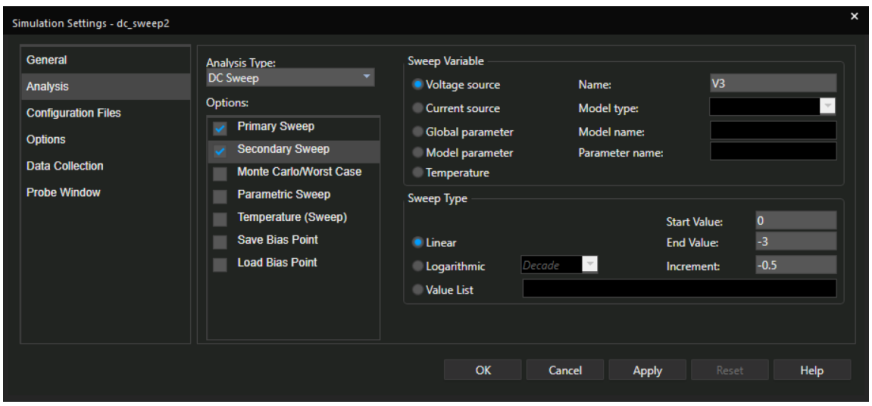

Figure 2.5: Primary dc sweep source V3

Secondly, the secondary DC sweep source, which is set to V3, is configured as follows: The simulation results are shown as the figure bellow:

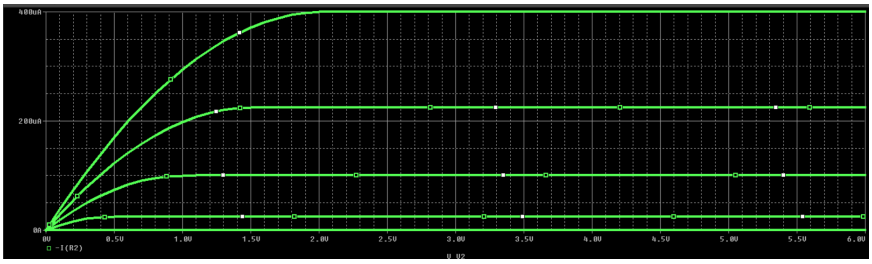

Figure 2.6: Simulation results with JFET

This figure also confirm that IDSS = 400mA and VP = -2V (the lowest curve is -1.9V). In this simulation, the ohmic region and saturation region are indicated better.

2.3 Exercises

2.3.1 Self bias configuration

This is the first configuration for a JFET, when the Gate pin is connected to the Ground. A typical circuit is presented as follows:

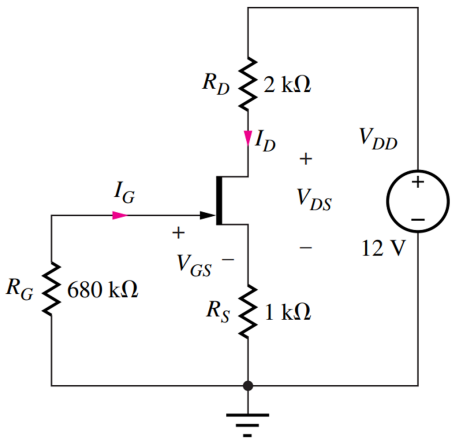

Figure 2.7: Self bias configuration

Students are proposed to implement this circuit in PSPICE with the JFET is JbreakN. The simulation results in PSPICE (**bias configuration**) are presented here. Moreover, a short explanations are required in this report to explain the value of ID and VGS.

2.3.2 Voltage divider configuration

The proposed schematic for this configuration is presented as follows:

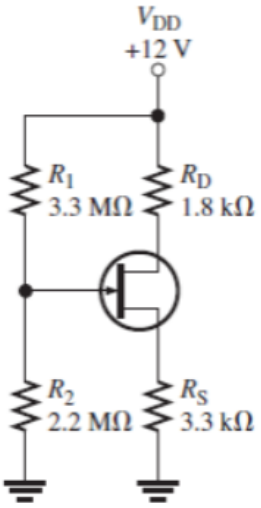

Figure 2.8: Voltage divider configuration

Students are proposed to implement this circuit in PSPICE with the JFET is JbreakN. The simulation results in PSPICE (**bias configuration**) are presented here. Moreover, a short explanations are required in this report to explain the value of ID and VGS.

3 Metal Oxide Semiconductor FET

As well as the Junction Field Effect Transistor (JFET), there is another type of Field Effect Transistor available whose Gate input is electrically insulated from the main current carrying channel and is therefore called an Insulated Gate Field Effect Transistor.

The most common type of insulated gate FET which is used in many different types of electronic circuits is called the Metal Oxide Semiconductor Field Effect Transistor or MOSFET for short.

The IGFET or MOSFET is a voltage controlled field effect transistor that differs from a JFET in that it has a “Metal Oxide” Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass.

3.1 Depletion-mode MOSFET

The Depletion-mode MOSFET, which is less common than the enhancement mode types. This device is very similar to JFET, except that the maximum current saturation is obtained at VGS > 0. The circuit used to verify IDSS and VP for DFET is presented as follows:

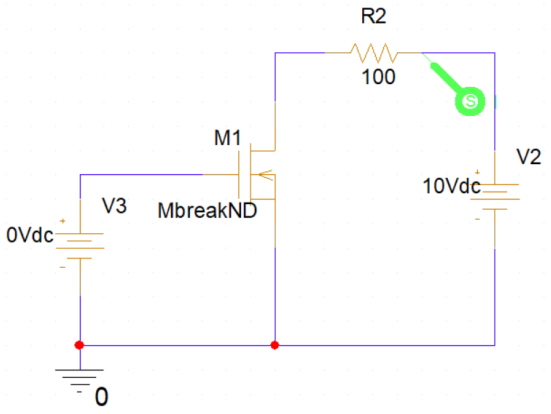

Figure 2.9: DFET verification in PSPICE

The device for a common DFET is MbreakND. After a dc sweep simulation when V3 varies from -5V to 0V, the results are shown bellow:

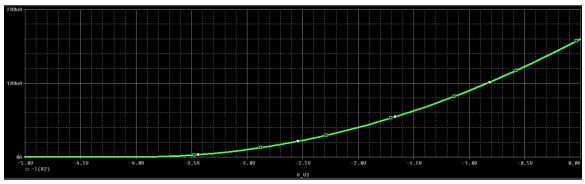

Figure 2.10: Simulation results with DFET

From this simulation results, it is confirmed that IDSS = 160mA and VP = -4V for DFET.

Students are proposed to implement the circuit bellow:

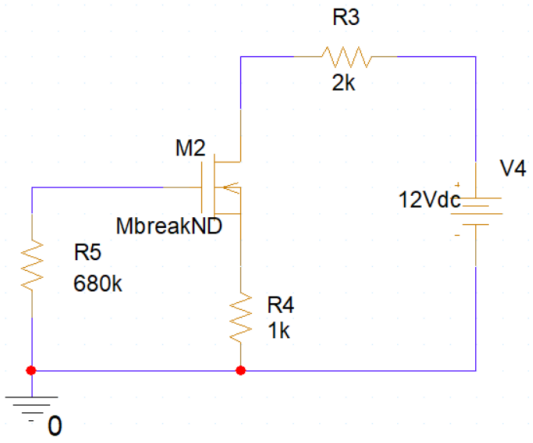

Figure 2.11: Self bias configuration for DFET

Only the bias configuration is required to executed. Please capture the simulation results with current and voltage information on the circuit. Finally, explain these values by theory calculations.

3.2 Enhancement-mode MOSFET

The more common Enhancement-mode MOSFET or eMOSFET. The device is normally "OFF" (non-conducting) when the gate bias voltage, VGS is equal to zero. For the n-channel enhancement MOS transistor a drain current will only flow when a gate voltage (VGS) is applied to the gate terminal greater than the threshold voltage (VTH) level in which conductance takes place making it a transconductance device. In other words, for an n-channel enhancement mode MOSFET: +VGS turns the transistor "ON", while a zero or -VGS turns the transistor "OFF". Thus the enhancement-mode MOSFET is equivalent to a "normally-open" switch.

The reverse is true for the p-channel enhancement MOS transistor. When VGS = 0 the device is "OFF" and the channel is open. The application of a negative (-ve) gate voltage to the p-type eMOSFET enhances the channels conductivity turning it "ON". Then for an p-channel enhancement mode MOSFET: +VGS turns the transistor "OFF", while -VGS turns the transistor "ON".

The validation of an EFET in PSPICE is presented bellow. The typical EFET in PSPICE is **MbreakN** device.

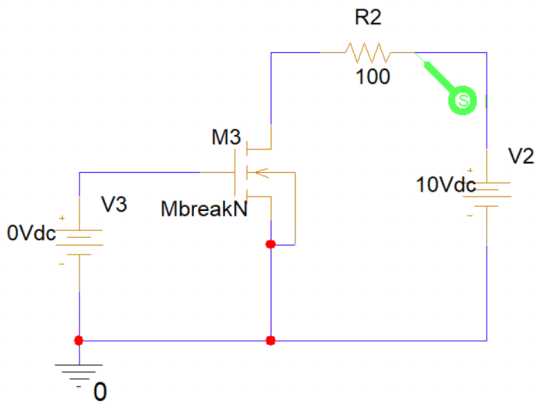

Figure 2.12: EFET validation

A dc sweep simulation with V3 can be performed. The simulation results with V3 varies from -1V to 5V are presented as following:

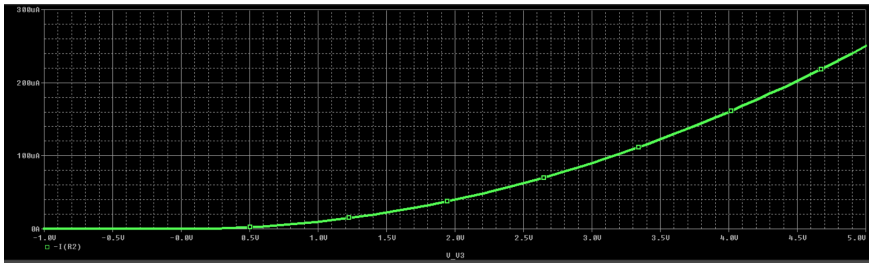

Figure 2.13: Simulation results with EFET

4 MOSFET Applications

This part presents some applications using MOSFETs and most of them are EFETs. Students are proposed to implement the schematic and then, validate in PSPICE.

4.1 MOSFET as a switch

In this circuit arrangement an Enhancement-mode N-channel MOSFET is being used to switch a simple lamp “ON” and “OFF” (**could be replace by an resistor to simulate in PSPICE**).

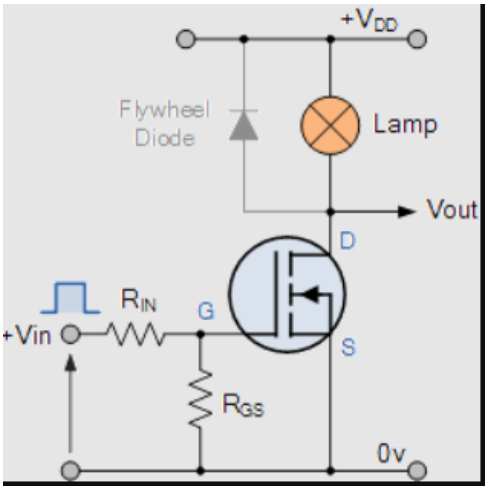

Figure 2.14: EFET is used as a switch

The gate input voltage VGS is taken to an appropriate positive voltage level to turn the device and therefore the lamp load either “ON”, (VGS = +ve) or at a zero voltage level that turns the device “OFF”, (VGS = 0V).

If the resistive load of the lamp was to be replaced by an inductive load such as **a coil, solenoid or relay** a “flywheel diode” would be required in parallel with the load to protect the MOSFET from any self generated back-emf.

Students are proposed to simulation this circuit with RIN = 4.7k and RGS = 47k and VIN is the TTL level (0V and 5V). The power supply for VDD can be set to 12V or 24V. Shortly explain the current passing through the load (a resistance 100Ohm replaced for the Lamp in the circuit).

4.2 MOSFET Motor Controller [Optional]

As the motor load is inductive, a simple flywheel diode is connected across the inductive load to dissipate any back emf generated by the motor when the MOSFET turns it “OFF”. A clamping network formed by a zener diode in series with the diode can also be used to allow for faster switching and better control of the peak reverse voltage and drop-out time.

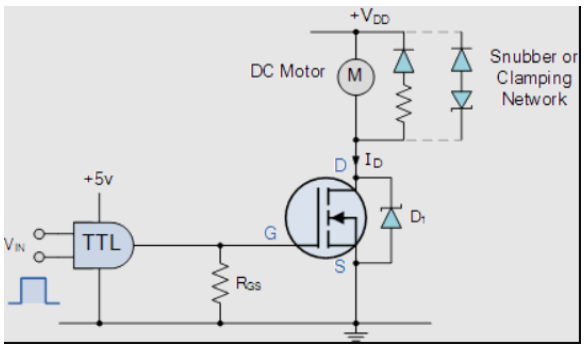

Figure 2.15: Simple motor controller using EFET

For added security an additional silicon or zener diode D1 can also be placed across the channel of a MOSFET switch when using inductive loads, such as motors, relays, solenoids, etc, for suppressing over voltage switching transients and noise giving extra protection to the MOSFET switch if required. Resistor RGS is used as a pull-down resistor to help pull the TTL output voltage down to 0V when the MOSFET is switched "OFF".
This exercise is optional in this lab.

4.3 Complementary MOSFET Motor Controller [Optinal]

The two MOSFETs are configured to produce a bi-directional switch from a dual supply with the motor connected between the common drain connection and ground reference. When the input is LOW the P-channel MOSFET is switched-ON as its gate-source junction is negatively biased so the motor rotates in one direction. Only the positive +VDD supply rail is used to drive the motor.

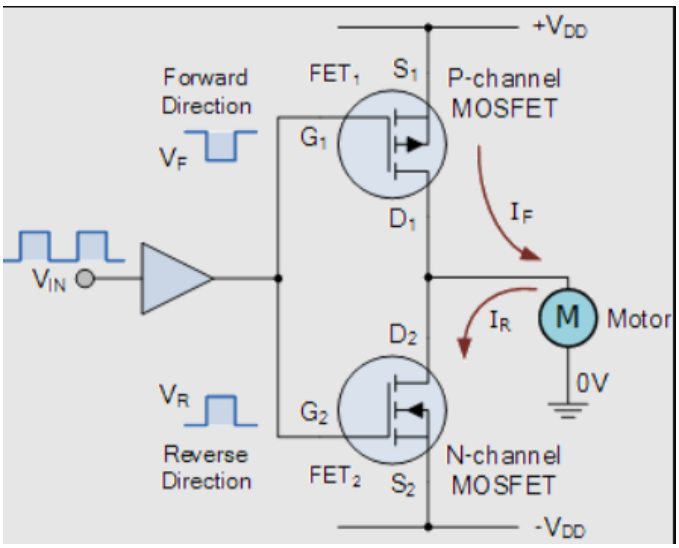

Figure 2.16: Full Motor controller with N and P channel EFET

When the input is HIGH, the P-channel device switches-OFF and the N-channel device switches-ON as its gate-source junction is positively biased. The motor now rotates in the opposite direction because the motors terminal voltage has been reversed as it is now supplied by the negative -VDD supply rail.

Then the P-channel MOSFET is used to switch the positive supply to the motor for forward direction (high-side switching) while the N-channel MOSFET is used to switch the negative supply to the motor for reverse direction (low-side switching).

This exercise is also optional in this lab.

5 Altium Designer

5.1 Button Input

Pushbuttons or switches connect two points in a circuit when you press them. In a system, button is a traditional input method. The figure bellow is an example of a simple button, which is the target of this exercise:

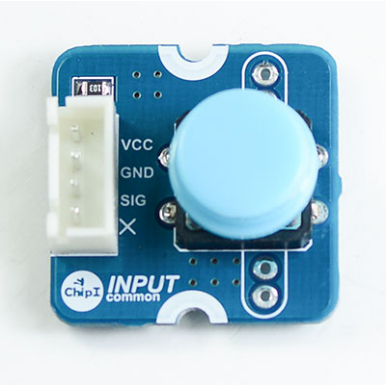

Figure 2.17: An example of a button

The schematic of this circuit is proposed as follows:

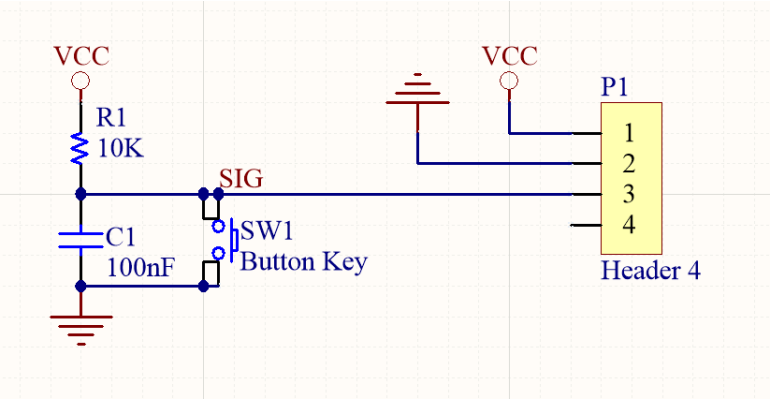

Figure 2.18: Button schematic in Altium

Students are proposed to implement the circuit in Altium Designer. The manual can be found in the same playlist with other manual videos. Please capture the screen to present the schematic as well as the layout of your PCB.

5.2 ADC Input

The second type of the input signal is the ADC input value, which is a kind of sensing device. In this sensor part, we use two opamps which are packed in one IC LM358. IC LM358

includes two opamps. A photoresistor (also known as a light-dependent resistor, LDR, or photo-conductive cell) is use to measure the light intensitive. It is a passive component that decreases resistance with respect to receiving luminosity (light) on the component's sensitive surface. An example of this module can be found in the figure bellow:

Figure 2.19: An example of a light sensor

The schematic of this circuit is proposed as follows, which is based on a voltage follower circuit:

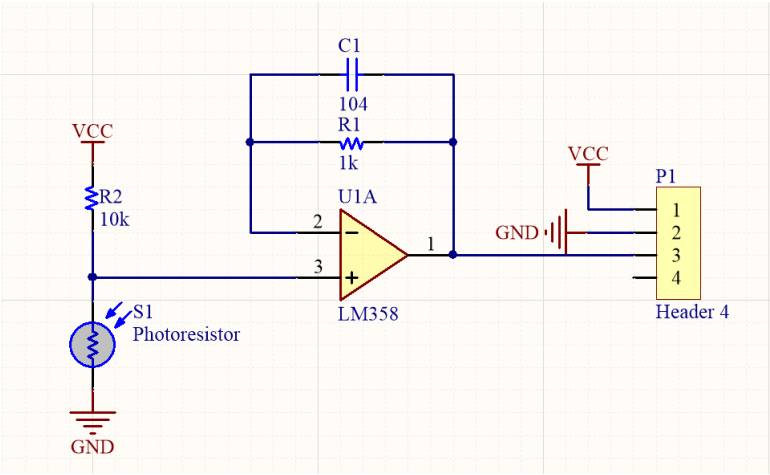

Figure 2.20: Light sensor schematic in Altium

Students are proposed to implement the circuit in Altium Designer. The manual can be found in the same playlist with other manual videos. Please capture the screen to present the schematic as well as the layout of your PCB.