LU Dongzhuyuan

Email: d72lu@uwaterloo.ca
Website: https://tim-lu-cuhksz.github.io/

EDUCATION

University of Waterloo *September 2024 - Present*
M.Eng., Electrical and Computer Engineering

The Chinese University of Hong Kong, Shenzhen *September 2019 - July 2023*
B.Eng., Electronic Information Engineering, Stream: Computer Engineering
CGPA: 3.628/4, **MGPA:** 3.668/4
Degree: *B.Eng. with Honours, First Class*
Honors & Awards: *Dean's List Award of AY2022-23, AY2021-22* and *AY2020-21*

EXPERIENCE

The Chinese University of Hong Kong, Shenzhen *December 2023 - June 2024*
Research Assistant for Prof. Zhen Li

- Built a navigation module on the habitat-sim virtual environment which integrates a top-down 2D semantic map (based on home-robot) and a Multimodal LLM (e.g. LISA) to segment and project a short-term navigation goal captured in a RGB image to a pixel coordinate on the 2D semantic map

The Chinese University of Hong Kong, Shenzhen *September - December 2022*
Student Help Room Preceptor, School of Science and Engineering

- Provided academic assistance to undergraduate students enrolling in *MAT3007 Optimization*

KUKA Robotics (China), Midea Group *May - July 2022*
Software Development Intern, Department of Logistic Automation

- Developed the Pacecat lidar interface (specifically, ros2-based publisher node and subscriber node to process the lidar data) of the 600ic-ul Autonomous Mobile Robot (AMR)
- Designed basic high-level robot task diagrams based on Kuka Studio and Kuka RCS system and conducted tests including auto-charging, auto-lifting of the shelves, and auto-navigation

PROJECTS

Comparative Anime Recommendation System Exploration with DualTaste Recommender
January - May 2023

- Perform meticulous data pre-processing techniques (*Adaboost* algorithm combined with Support Vector Regressor) on the dataset to fill in the unknown fields
- Verify the performance of two collaborative-filtering methods: Alternating Least Squares (ALS) and Neural Collaborative Filtering (NCF)
- Propose a novel content-based method (DualTaste Anime Recommender-DTAR), in which the user's specific preference and the general trends (calculated via Bayesian rating) are taken into consideration. We devise a special weight parameter to aggregate the two components together
- *Adaboost.SVR* is applied to address the cold-start problem and attains relatively good performance
- By applying Borda-count voting method, we combine the results of the three algorithms (ALS, NCF, DTAR) into a hybrid answer

Self-Supervised Federated Learning on Non-iid Data *September - December 2022*

Final Year Project, Supervised by Prof. Xiaoying Tang

- Apply contrastive self-supervised learning technique including SimCLR, BYOL, and SimSiam to perform image classification task on CIFAR-10 and CIFAR-100 in a federated-learning setting with Dirichlet sampling
- Conduct experiments on personalized self-supervised federated learning method by introducing an additional l_2 loss function to each client with a regularizer to minimize the distance between the global model and local model

Database Management System Implementation *October - December 2022*

- Collaboratively implemented a miniature relational database management system (DBMS) that stores tables of data, where a table consists of some number of labeled columns of information
- Our system uses very restricted dialect of Structured Query Language (SQL) and accepts a sequence of commands from the standard input in the terminal for data insertion and extraction. The functionalities we support include create, load, insert, select from multiple tables with conditions, order by columns, case insensitivity, syntax and syntactic errors recognition, etc.

Simplified Virtual Memory and File System *September - December 2021*

- Implemented a virtual memory system including an inverted page table and least recently used (LRU) page replacement algorithm. CPU physical memory and disk storage were simulated by CUDA GPU shared memory and global memory respectively
- Built a file system via contiguous allocation including a volume control block, a single-root directory, and a file control block. Constructed a device (n-th prime number calculator) under /dev with file operations (e.g., ioctl that changes device configurations) implemented in kernel module

MIPS Assembler and 5-Pipelined CPU *January - May 2021*

- Built up a 5-pipelined CPU that interprets machine code, performs arithmetic operations, and stores and loads data in Verilog in the main memory. The CPU mainly consists of an arithmetic logic unit (ALU), a control unit and a main memory
- Devised a virtual MIPS instruction set architecture (ISA) assembler and simulator which “translate” assembly language into machine codes and execute them in C