



Universität des Saarlandes Lehrstuhl für Mikroelektronik Prof. Dr.-Ing. Chihao Xu

DEF - ABC

Entwicklung eines FPGA-basierten Dimming-Algorithmus zur Senkung des Energiebedarfs eines LC-Displays

Left section:

Some Text

Gebäude A5.1

Raum 0.29

Right section:

Some Text More Text another line

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1 Basics

Text can be **bold**, *italic*, <u>underlined</u> or <u>everything together</u>. Inline code is possible too. Another sentence.

Text indents automatically if you leaves one row empty. Lorem ipsum dolor sit amet, consetetur sadipscing elitr, sed diam nonumy eirmod tempor invidunt ut labore et dolore magna aliquyam erat, sed diam voluptua. At vero eos et accusam et justo duo dolores et ea rebum. Stet clita kasd gubergren, no sea takimata sanctus est Lorem ipsum dolor sit amet. Lorem ipsum dolor sit amet, consetetur sadipscing elitr, sed diam nonumy eirmod tempor invidunt ut labore et dolore magna aliquyam erat, sed diam voluptua. At vero eos et accusam et justo duo dolores et ea rebum. Stet clita kasd gubergren, no sea takimata sanctus est Lorem ipsum dolor sit amet. [1]

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1.1 Item list

- item 1
 - subitem 1
 - subitem 2
- item 2

1.2 Numbered List

- 1. numbered item 1
- 2. numbered item 2

1.3 Table

	Item 1	Item 2
1	С	d
2	e	f

Tab. 1: Title......

1.4 Math

Inline Math looks like this x = y + z.

$$x = y + z \tag{1}$$

$$v + b = 4 (2)$$

$$x = y + z$$

$$v + b = 4$$



 $\mbox{Abb.}$ 1: Basys 2 Board mit angeschlossenem Display an einem PMOD.

2 Layer 1

asdf

2.1 Layer 2

asdf

2.1.1 Layer 3

asdf

Layer 4 asdf

Layer 5 asdf

3 Code

Reference to Listing 3.

```
module Addiererzelle (
      input [5:0] A,
      input [5:0] B,
3
                             // Carry In (Uebertragseingang)
      input C_IN,
4
      output reg[5:0] S,
                             // Summe
5
      output reg C_OUT
                             // Carry Out (Uebertragsausgang)
6
  );
  //something happens here
  endmodule
```

Listing 1: Beispiel einer Portliste mit Register-/Wirearrays

```
module Addiererzelle #(parameter WIDTH=10) (
17
       input [WIDTH-1:0] A,
18
       input [WIDTH-1:0] B,
19
                                   // Carry In (Uebertragseingang)
       input C_IN,
20
       output reg[WIDTH-1:0] S, // Summe
21
       output reg C_OUT
                                   // Carry Out (Uebertragsausgang)
   );
23
24
   //something happens here
25
26
   endmodule
27
28
29
30
   parameter ADD1_WIDTH = 6;
31
32
   Addierzelle #(.WIDTH(ADD1_WIDTH)) add1 (
33
        . A
               (A),
34
       .В
               (B),
35
       .C_IN
               (C_IN),
36
       .S
               (S),
37
        .C_OUT (C_OUT)
38
   );
39
```

Listing 2: Beispiel einer Portliste mit Register-/Wirearrays

3.1 Hidden subsection

I'm hidden in the ToC! [1]

Hidden subsection without a number

I'm hidden too! [4]

Literatur

- [1] Marc Albrecht. Sorted Sector Covering mit Bildkondensierung Eine universelle Methode zur effizienten Berechnung von Local Dimming LED Backlight. PhD thesis, Saarland University, 2010.
- [2] Niklas Claesson Alexander Aulin. Tools in CMOS design. https://www.eit.lth.se/fileadmin/eit/courses/eti135/slides/AlexanderNiklas.pdf. [letzter Zugriff am 6.07.2018; Online].
- [3] Tom Ashe. Color Management and Quality Output: Working with Color from Camera to Display to Print. Focal Press, 2012. ISBN: 0240821114 9780240821115.
- [4] Marc Albrecht, Andreas Karrenbauer, Tobias Jung, and Chihao Xu. Sorted sector covering combined with image condensation: an efficient method for local dimming of direct-lit and edge-lit LCDs. *IEICE Transactions on Electronics*, E93-C(11):1556–1563, 2010.