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LEHRSTUHL FÜR MIKROELEKTRONIK
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DEF - ABC

Entwicklung eines FPGA-basierten Dimming-Algorithmus zur Senkung des Energiebedarfs eines LC-Displays

Left section:

Some Text
Gebäude A5.1
Raum 0.29

Right section:

Some Text
More Text
another line

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1 Basics

Text can be **bold**, *italic*, underlined or *everything together*. Inline code is possible too. Another sentence.

Text indents automatically if you leaves one row empty. Lorem ipsum dolor sit amet, consetetur sadipscing elitr, sed diam nonumy eirmod tempor invidunt ut labore et dolore magna aliquyam erat, sed diam voluptua. At vero eos et accusam et justo duo dolores et ea rebum. Stet clita kasd gubergren, no sea takimata sanctus est Lorem ipsum dolor sit amet. Lorem ipsum dolor sit amet, consetetur sadipscing elitr, sed diam nonumy eirmod tempor invidunt ut labore et dolore magna aliquyam erat, sed diam voluptua. At vero eos et accusam et justo duo dolores et ea rebum. Stet clita kasd gubergren, no sea takimata sanctus est Lorem ipsum dolor sit amet. [1]

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1.1 Item list

- item 1
 - subitem 1
 - subitem 2
- item 2

1.2 Numbered List

1. numbered item 1
2. numbered item 2

1.3 Table

	Item 1	Item 2
1	c	d
2	e	f

Tab. 1: Title.....

1.4 Math

Inline Math looks like this $x = y + z$.

$$\begin{aligned}x &= y + z & (1) \\v + b &= 4 & (2)\end{aligned}$$

$$\begin{aligned}x &= y + z \\v + b &= 4\end{aligned}$$

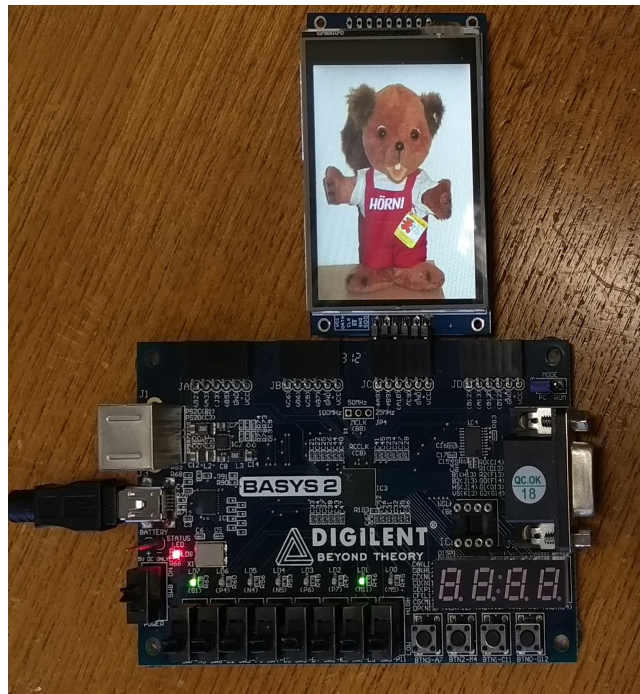


Abb. 1: Basys 2 Board mit angeschlossenem Display an einem PMOD.

2 Layer 1

asdf

2.1 Layer 2

asdf

2.1.1 Layer 3

asdf

Layer 4 asdf

Layer 5 asdf

3 Code

Reference to Listing 3.

```
1 module Addiererzelle (  
2     input [5:0] A,  
3     input [5:0] B,  
4     input C_IN,           // Carry In (Uebertragseingang)  
5     output reg[5:0] S,    // Summe  
6     output reg C_OUT      // Carry Out (Uebertragsausgang)  
7 );  
8 //something happens here  
9 endmodule
```

Listing 1: Beispiel einer Portliste mit Register-/Wirearrays

```
17 module Addiererzelle #(parameter WIDTH=10) (  
18     input [WIDTH-1:0] A,  
19     input [WIDTH-1:0] B,  
20     input C_IN,           // Carry In (Uebertragseingang)  
21     output reg[WIDTH-1:0] S, // Summe  
22     output reg C_OUT      // Carry Out (Uebertragsausgang)  
23 );  
24  
25 //something happens here  
26  
27 endmodule  
28  
29 /******  
30  
31 parameter ADD1_WIDTH = 6;  
32  
33 Addiererzelle #(.WIDTH(ADD1_WIDTH)) add1 (  
34     .A      (A),  
35     .B      (B),  
36     .C_IN   (C_IN),  
37     .S      (S),  
38     .C_OUT  (C_OUT)  
39 );
```

Listing 2: Beispiel einer Portliste mit Register-/Wirearrays

3.1 Hidden subsection

I'm hidden in the ToC! [1]

Hidden subsection without a number

I'm hidden too! [4]

Literatur

- [1] Marc Albrecht. *Sorted Sector Covering mit Bildkondensierung - Eine universelle Methode zur effizienten Berechnung von Local Dimming LED Backlight*. PhD thesis, Saarland University, 2010.
- [2] Niklas Claesson Alexander Aulin. Tools in CMOS design. <https://www.eit.lth.se/fileadmin/eit/courses/eti135/slides/AlexanderNiklas.pdf>. [letzter Zugriff am 6.07.2018; Online].
- [3] Tom Ashe. *Color Management and Quality Output: Working with Color from Camera to Display to Print*. Focal Press, 2012. ISBN: 0240821114 9780240821115.
- [4] Marc Albrecht, Andreas Karrenbauer, Tobias Jung, and Chihao Xu. Sorted sector covering combined with image condensation : an efficient method for local dimming of direct-lit and edge-lit LCDs. *IEICE Transactions on Electronics*, E93-C(11):1556–1563, 2010.