Pipeline Buffers

COEN 122 Lab 4

Grading

- Lab 1-4 (10% each) 40%
- Final Project 60%

Office Hours

- TA office hours:
  - Tianxin Zhou (Wednesday Lab): Friday 10am to 12pm
  - Brandon Quant (Tuesday Lab): Tuesday 10am to 12pm

- TA emails:
  - tzhou@scu.edu
  - bquant@scu.edu

Late Policy

- Late submissions submitted within 24 hours after the deadline receive 50% credit. After 24 hours, no credit is given.

Demo

- Labs submitted with no demo will receive no credit. Please demo to me before the lab is due.
- You can demo in either TAs Office Hours

Lab 4 Overview

- Objective: Implement a buffer for a CPU pipeline in Verilog using Vivado
  - Only one example is required, but we recommend implementing all buffers: IF/ID, ID/EX, EX/WB (or EX/MEM and MEM/WB)
- Due: Week 6 @ 2:14 PM on your lab day
- For the first 4 labs, you will be working individually, but will be working in teams for the project

Helpful website: http://www.asic-world.com/verilog/veritut.html

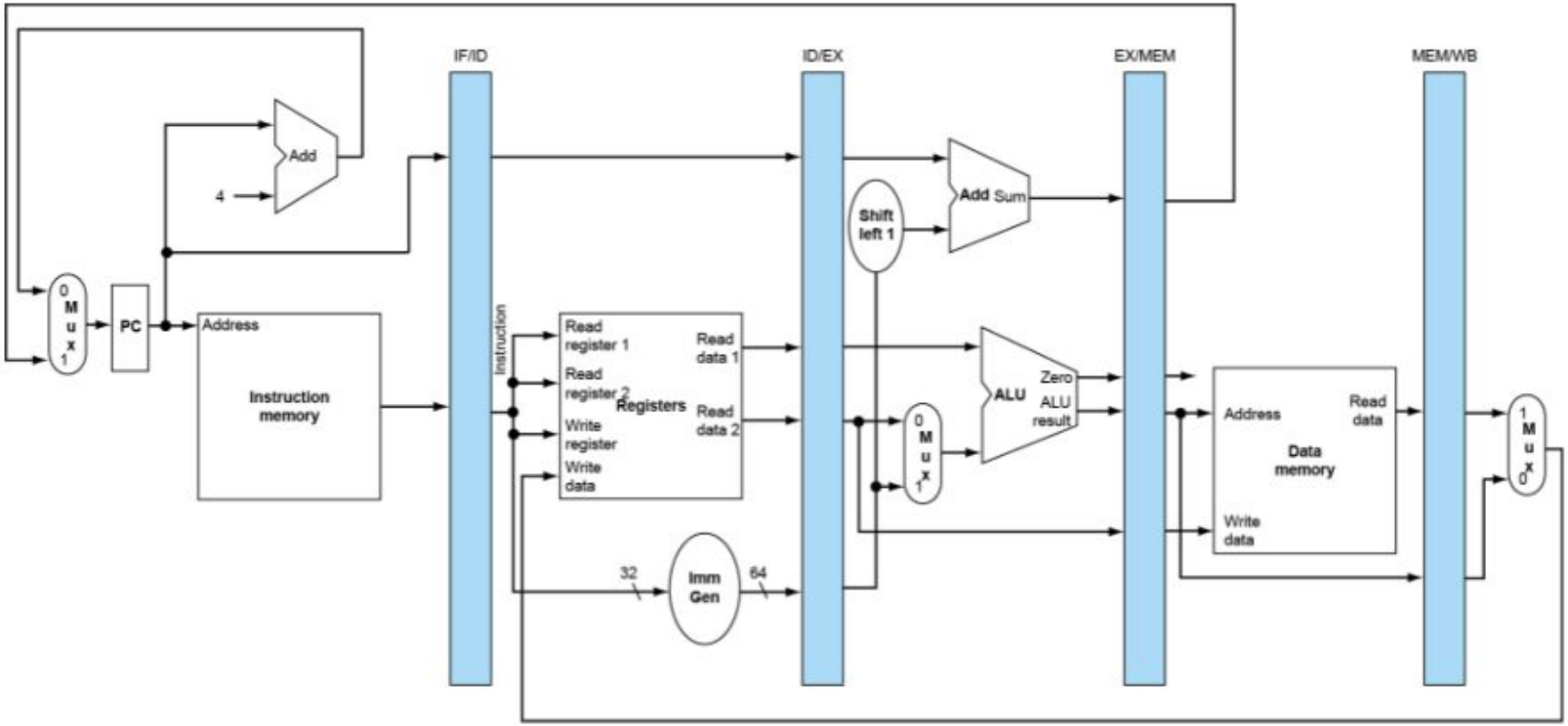
Design Flow

- Write code for logic block (e.g. IF/ID, ID/EX, EX/WB)
- Write test bench to verify proper function of logic block
- Run Synthesis
- Run Simulation
- View waveform, verify results

Pipeline buffers

- Buffers serve as a way to synchronize the pipeline across its multiples stages
- Each buffer is responsible for taking the data from the preceding stage and, on each clock cycle, transferring it into the following stage.

Simple Datapath for Single Cycle



Recommendation

- We know you are still covering the topic of pipelines in lecture, but implement your buffers with your final project in mind. You will be designing and implementing a datapath for your final project and doing some of the work now will make your life easier

- Hint: you've already implemented some of the modules, so think about how they would be connected through the buffers. Also take a look at the lecture slides for more sample pipelines.