

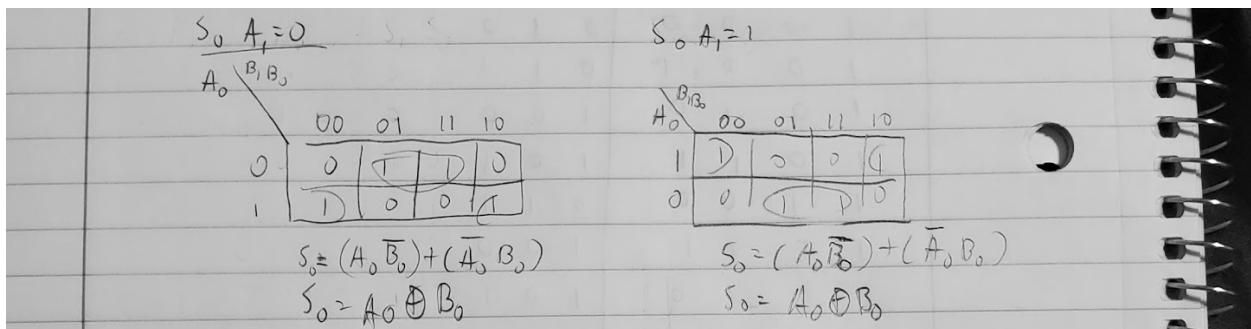
## Lab 4 Report

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### Introduction:

In this lab, we used Shannon's expansion to design the circuit and the outputs. Each of S1, S1, and S0 outputs will be created by designing two functions of three variables and using the fourth variable to select one of the two functions using a 2:1 multiplexer.

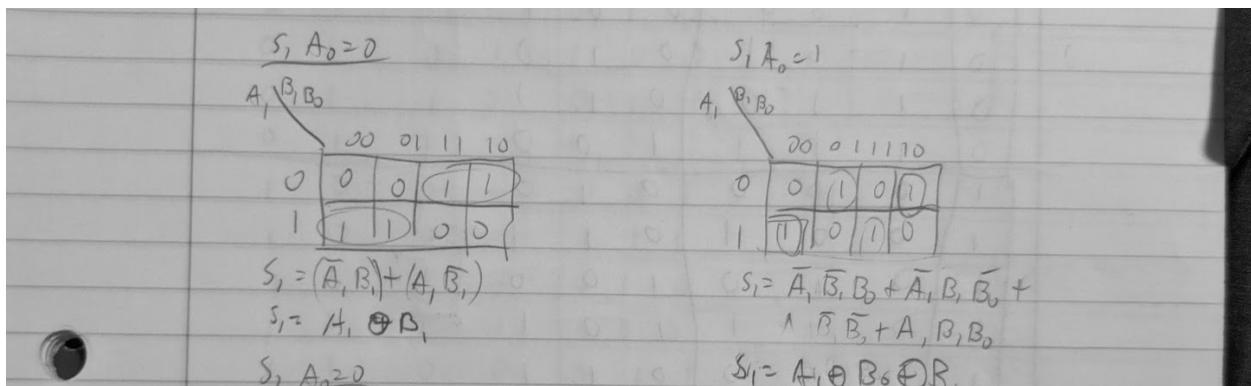
### Include the K-maps and the logic expressions for the functions you used.



$$S_0 = (A_0 \bar{B}_0) + (\bar{A}_0 B_0)$$

$$S_0 = (A_0 \bar{B}_0) + (\bar{A}_0 B_0)$$

$$S_0 = A_0 \oplus B_0$$



$$S_1 = (\bar{A}_1 B_1) + (A_1 \bar{B}_1)$$

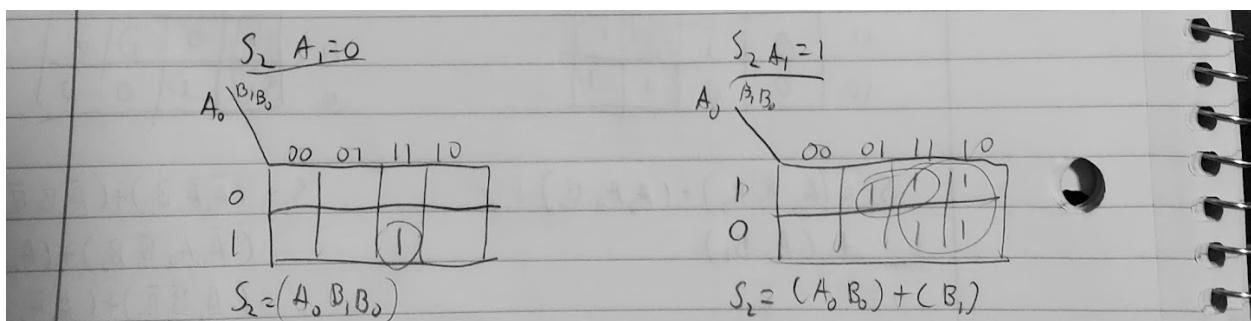
$$S_1 = A_1 \oplus B_1$$

$$S_2 \mid A_0 = 0$$

$$S_1 = \bar{A}_1 \bar{B}_1 B_0 + \bar{A}_1 B_1 \bar{B}_0 +$$

$$A_1 \bar{B}_1 \bar{B}_0 + A_1 B_1 B_0$$

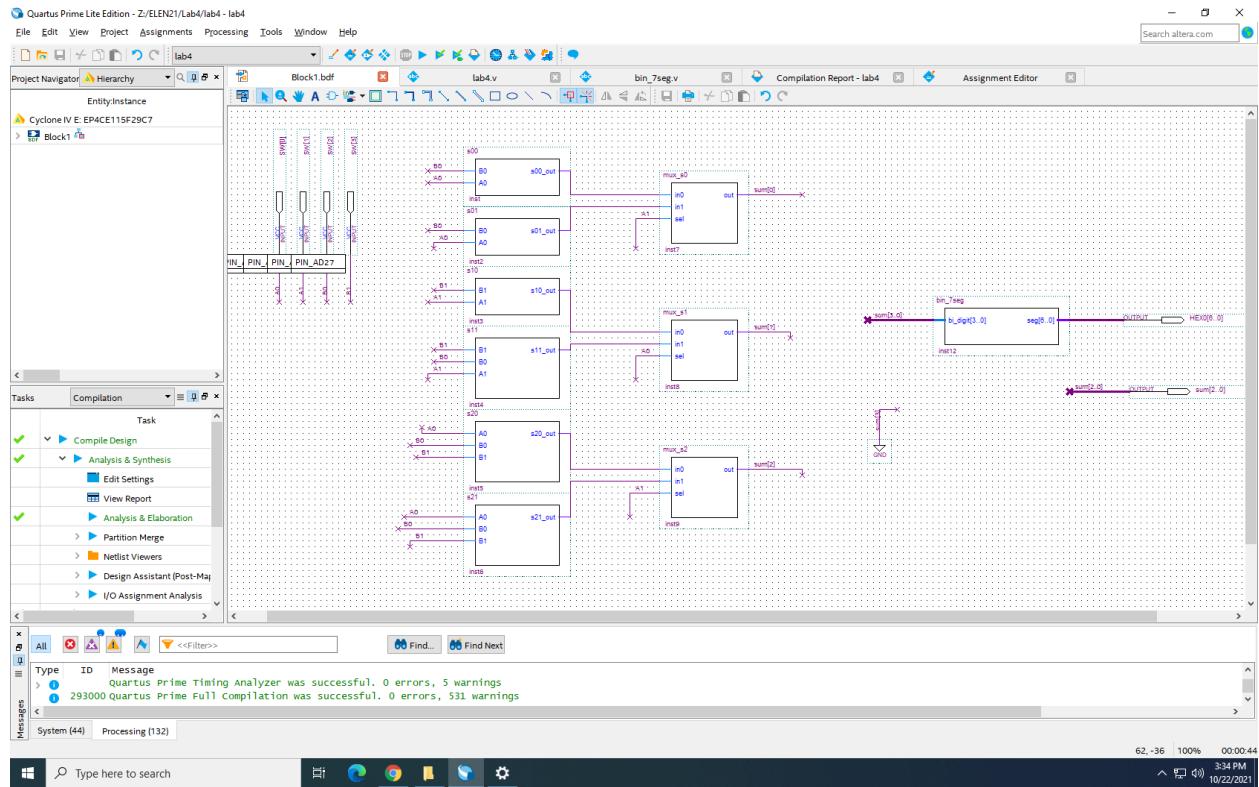
$$S_1 = A_1 \oplus B_0 \oplus B_1$$



$$S_2 = (A_0 B_1 B_0)$$

$$S_2 = (A_0 B_1 B_0) + (B_1)$$

Include your final schematics, your final Verilog code, and proof of successful download and functioning on the FPGA.



Quartus Prime Edition - Z/ELEN21/Lab4/lab4 - lab4

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Project Navigator Hierarchy Block1.bdf lab4.v bin\_7seg.v Compilation Report - lab4 Assignment Editor

```

module s10(input B1, A1, output s10_out);
  xor($10_out, B1, A1);
endmodule

module s11(input B1, B0, A1, output s11_out);
  xor($11_out, B1, B0, A1);
endmodule

module s00(input B0, A0, output s00_out);
  assign s00_out = A0 ^ B0;
endmodule

module s01(input B0, A0, output s01_out);
  assign s01_out = A0 ^ B0;
endmodule

module mux_s1(input in0, in1, sel, output out);
  wire x,y;
  and(x, in0, ~sel);
  and(y, in1, sel);
  or(out, x, y);
endmodule

module mux_s0(input in0, in1, sel, output out);
  assign out = (sel) ? in1 : in0;
endmodule

module s20(input A0, B0, B1, output s20_out);
  and($20_out, A0, B0, B1);
endmodule

module s21(input A0, B0, B1, output s21_out);
  assign s21_out = (A0 & B0) | B1;
endmodule

module mux_s2(input in0, in1, sel, output out);
  if (out = ($sel)) ? in1 : in0;
endmodule

```

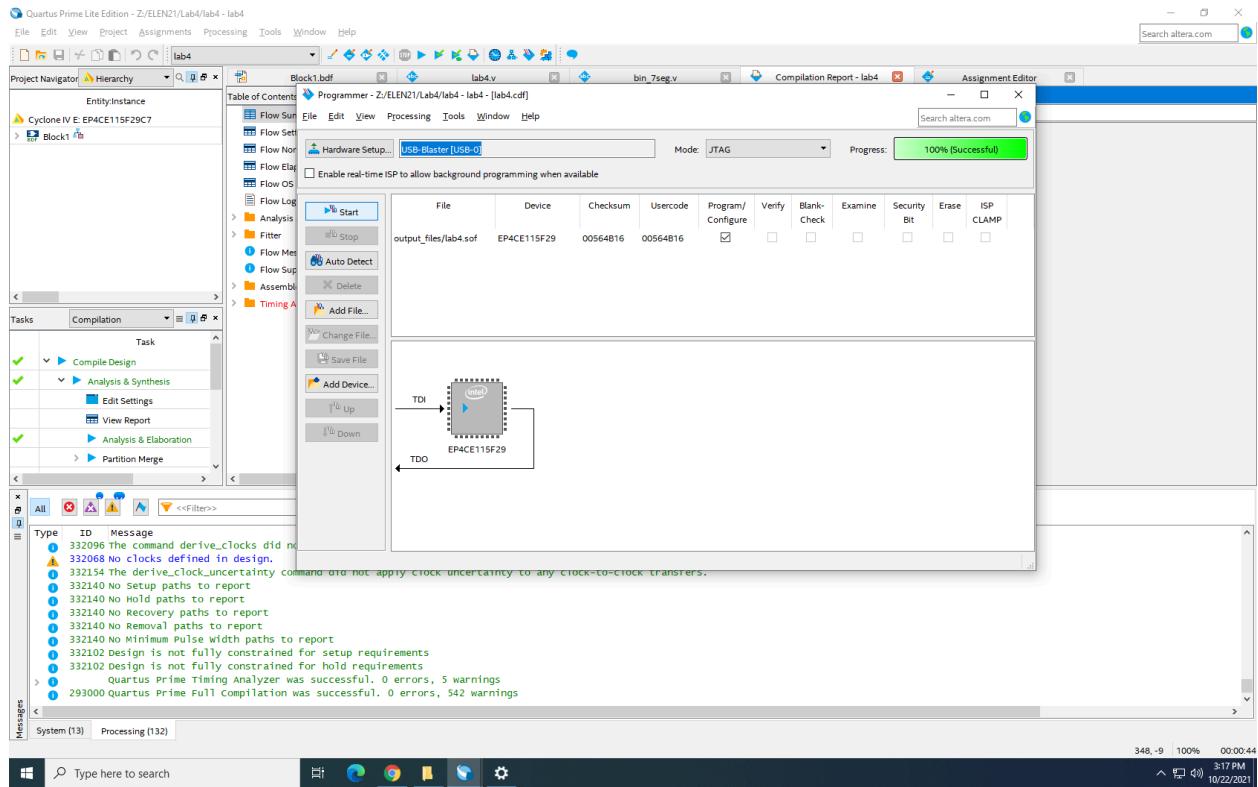
Tasks Compilation

- Compile Design
- Analysis & Synthesis
  - Edit Settings
  - View Report
- Analysis & Elaboration
- Partition Merge
- Netlist Viewers
- Design Assistant (Post-Match)
- I/O Assignment Analysis

Messages

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**Explain the advantages and disadvantages of the alternate choice of MUX select input and the different implementation methodologies, from your perspective. Consider both ease and efficiency of design and ease and efficiency of making modifications.**

The advantage of implementing MUX select input is that we could have a better sight with the schematic, because it will make the schematic more clear. Also, it would highly increase the efficiency of design because we don't need to draw out the same circuit several times. The disadvantage of using MUX select input is that if we have the wrong verilog code, this will eventually affect the inputs and outputs. In this case, we won't be able to have the result we want.

**Do you think we made the right choice to implement our 2-bit adder using the A1-based synthesis for output bits S2 and S0, and using the A0-based synthesis for output bit S1? Explain.**

No, I do not think it was the right choice to implement output bit S0 using A1-based synthesis. Using A0-based synthesis for S0 would require only one input B0 rather than two as well as would use fewer gates.

**If you found problems with the circuit that required correction and a new download, explain what you observed that demonstrated the problem and describe determined the cause of the problem and how you fixed it.**

When we originally tested the circuit, we noticed that the second 7-segment display was displaying strange characters and knew that there must be an issue with the output pin. We looked at our two output pins and realized that it was unnecessary to have the HEX1 to display a digit. We renamed it to sum[2..0] which corrected the issue.

### **Conclusion:**

In this lab, we learned how to use Shannon's expansion to synthesize a logic function. We also learned how to design circuit components by using verilog code and implementing it in the schematic. One of the challenges we faced during the lab is when we were compiling the schematic and an error with the schematic occurred. We solved the issue by changing the output of sum[2..0] from HEX1[2..0] to sum[2..0] in the schematic. Other small issues included proper naming of files and making sure that each wire was fully connected to each module.