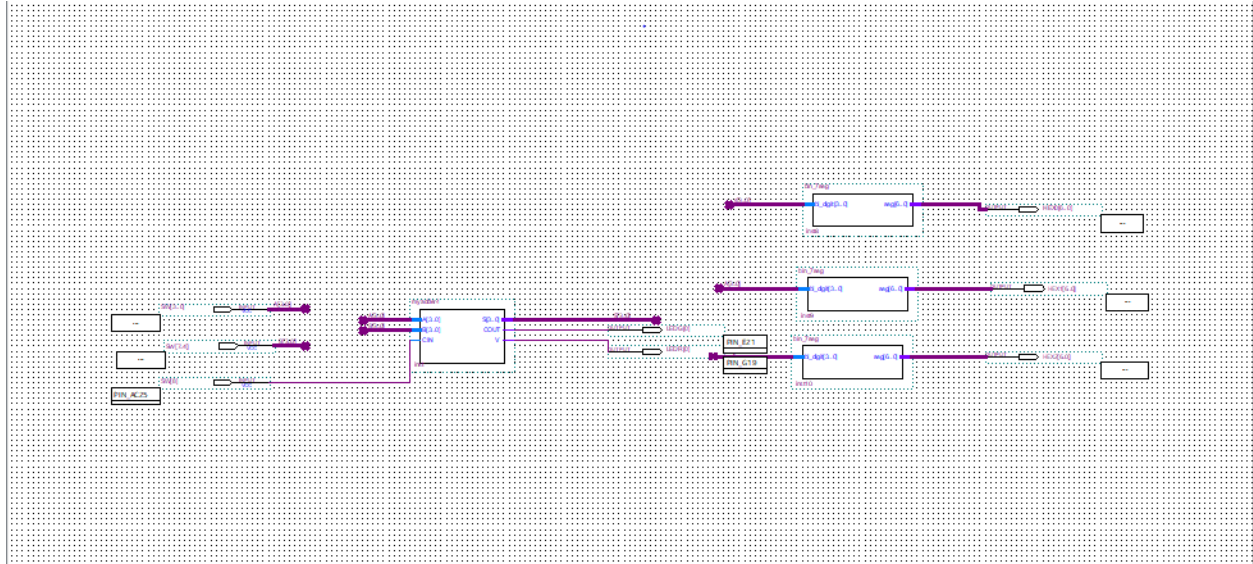


=Lab 5: Yen-Jung (Tim), Kulsoom Sabit, Eric Hicks

For your lab report, include the schematics, Verilog, and simulation waveforms of all the components you designed. In addition, include answers to the following questions.

Schematics:

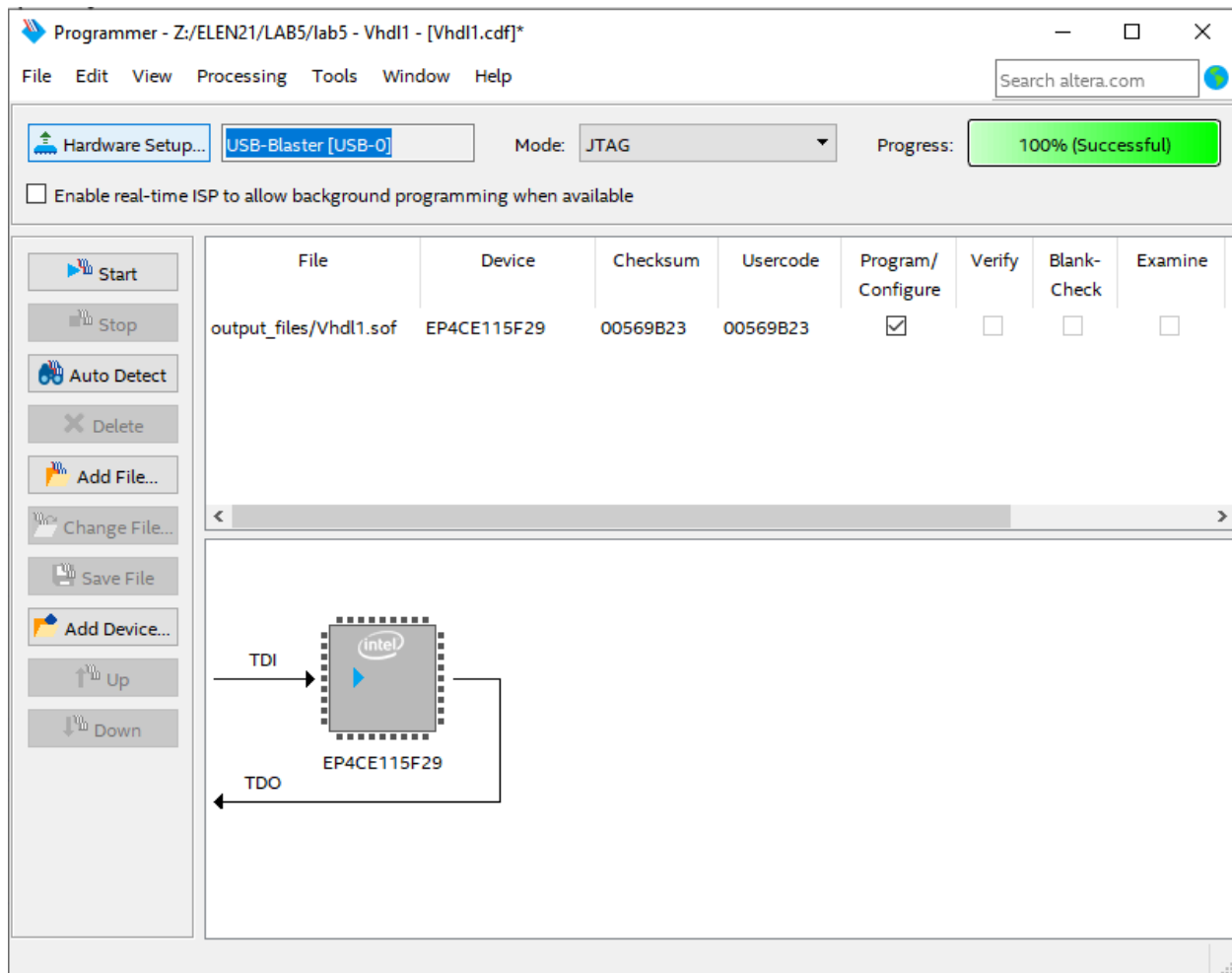


Verilog:

```
1 module myfulladder(S, COUT, A, B, CIN);
2     output S, COUT;
3     input A, B, CIN;
4
5     assign S = (A^B)^CIN;
6     assign COUT = (A&B)|(CIN&A)|(B&CIN);
7 endmodule
8
```

```
1 module myadder4 (S, COUT,V, A, B, CIN);
2     output [3:0] S;
3     output COUT,V;
4     input [3:0] A, B;
5     input CIN;
6     wire [2:0] C;
7
8     myfulladder stage0(S[0], C[0], A[0], B[0], CIN);
9     myfulladder stage1(S[1], C[1], A[1], B[1], C[0]);
10    myfulladder stage2(S[2], C[2], A[2], B[2], C[1]);
11    myfulladder stage3(S[3], COUT, A[3], B[3], C[2]);
12
13    assign V = COUT ^ C[2];
14
15 endmodule
16
```

## Programmer



- Find one pair of X and Y inputs (with C0=0) that would result in the following:
  - o C4 = 0 and V = 0  
X = 0000, Y = 0000
  - o C4 = 0 and V = 1  
X = 0100, Y = 0100
  - o C4 = 1 and V = 0  
X = 1100, Y = 1100
  - o C4 = 1 and V = 1  
X = 1000, Y = 1000
- If you had to make an 8-bit adder, show how would you do it using only instances of the 4-bit module you have built in this lab? Specifically show how you would create the C8 output and the V output.

```

module myadder8(S, C8, V, A, B, C0);
    output [7:0]S;
    output C8, V;
    input [7:0]A, B;
    input C0;
    wire C4, V0;

    myadder4 low(S[3:0], C4, V0, A[3:0], B[3:0], C0);
    myadder4 high(S[7:4], C8, V, A[7:4], B[7:4], C4);
endmodule

```

- Discussion of testing procedures and results.

- o Initial implementation: Did the initial testing of your circuit (i.e., before Section 5) go smoothly or did you encounter incorrect results? If the latter, describe how you determined what was wrong.

During our initial testing, we encountered errors with the design we had for the full adder. This, in turn, impacted the rest of the 4 bit adder circuit. In order to fix this issue, we tested our full adder and found that the issue was with the carry bit.

- o Testing Challenge: In Section 5 you tested a circuit to detect an error. Summarize what the steps you followed to identify the problem. Discuss whether you could have followed a shorter set of tests to identify the Problem.

During our testing challenge, we were able to identify the issue by using the expected values and comparing them to our actual values. Doing so we were able to pinpoint that there was an issue with two of our bits on our adder.

- If the circuit were completely correct except that  $X[1]$  and  $Y[1]$  were interchanged in a full adder input, would you be able to detect this based on observing outputs during testing? Why or why not?

It would be impossible to observe this issue through the output. This is because the sum and carry values would be the same since  $X[1] + Y[1] = Y[1] + X[1]$ . In order to observe this error, we would need to know the values of the inputs  $X$  and  $Y$  to see if they are returning their expected values.