6.117 Final Project: Receiver

Overview

The receiver portion of the project comprises a 4-bit digital lock, a discrete, 3-transistor Class AB audio amplifier, and a 38 kHz infrared receiver. The receiver is powered through an unregulated DC input ranging from 12 -- 16V. Either two screw terminals or a 2.1mm ID / 5.0mm OD barrel jack may be used for power input. A 3.5mm jack is used for stereo audio input, and two screw terminals are used for audio output into a 16 ohm nominal load.

Table of Contents

Sheet: Amplifier

Audio amplifier. Accepts a 5V-compatible active-high logic input from the lock section. Connects amplifier input with a relay. Frequency response is approximately linear from 20 Hz to 20 kHz.

File: amplifier.sch

Sheet: Lock

Digital lock. Input may come from PCB-mounted switches or from IR receiver section, depending on jumper settings. Passcode is hardwired by user by soldering jumper links.

File: lock.sch

Sheet: IR Receiver

Infrared receiver. Contains photodiode input, IR processing blocks and output level conversion. Produces two 5V-compatible outputs for use by digital lock portion.

File: ir_receiver.sch

Sheet: Power

Power supply and regulation. Contains power input, protection diode, op-amp supply splitter circuit, regulated 5V power supply and bulk capacitance.

File: power.sch

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Sheet: /
File: receiver.sch

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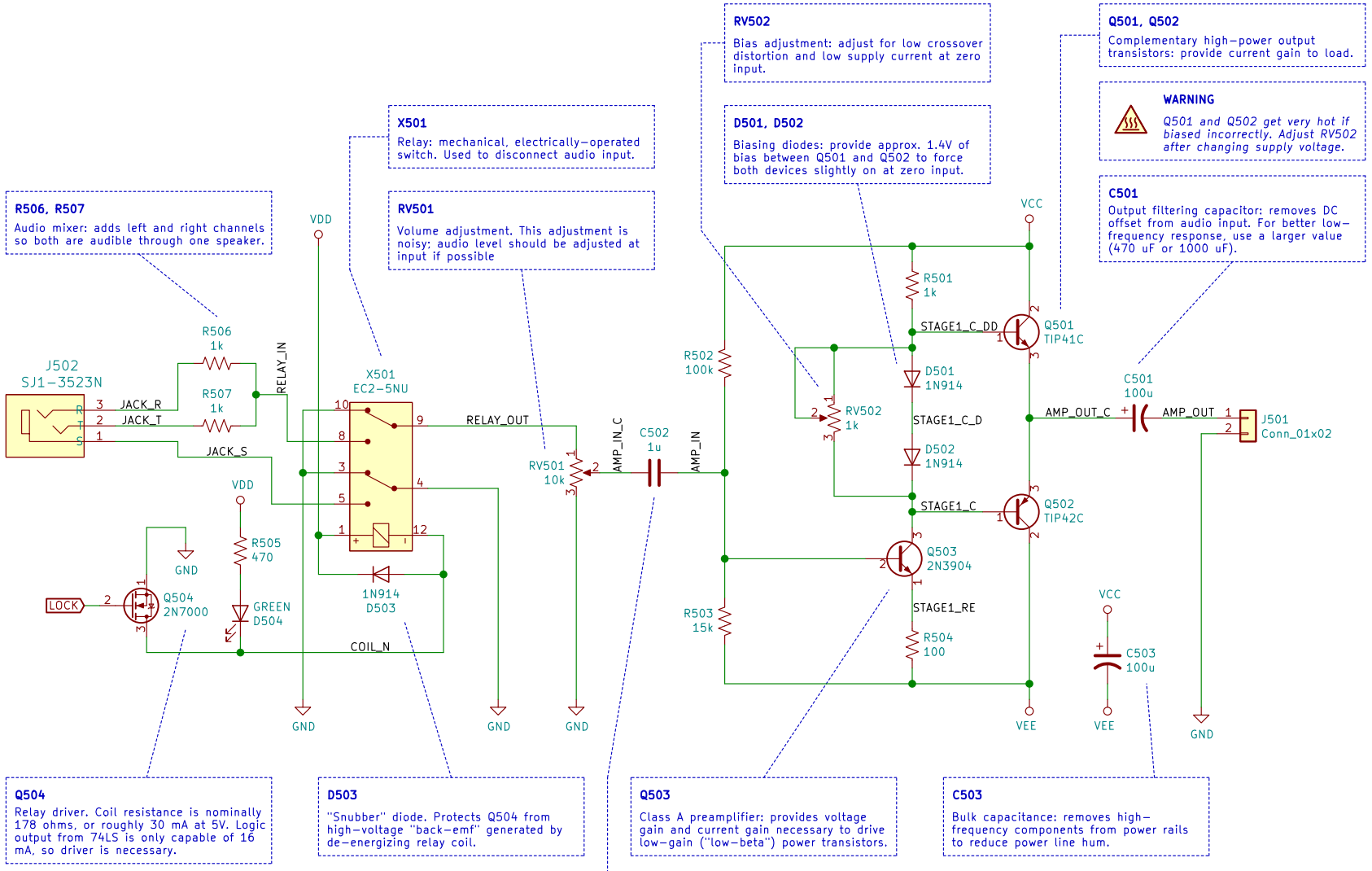

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Sheet: /Amplifier/

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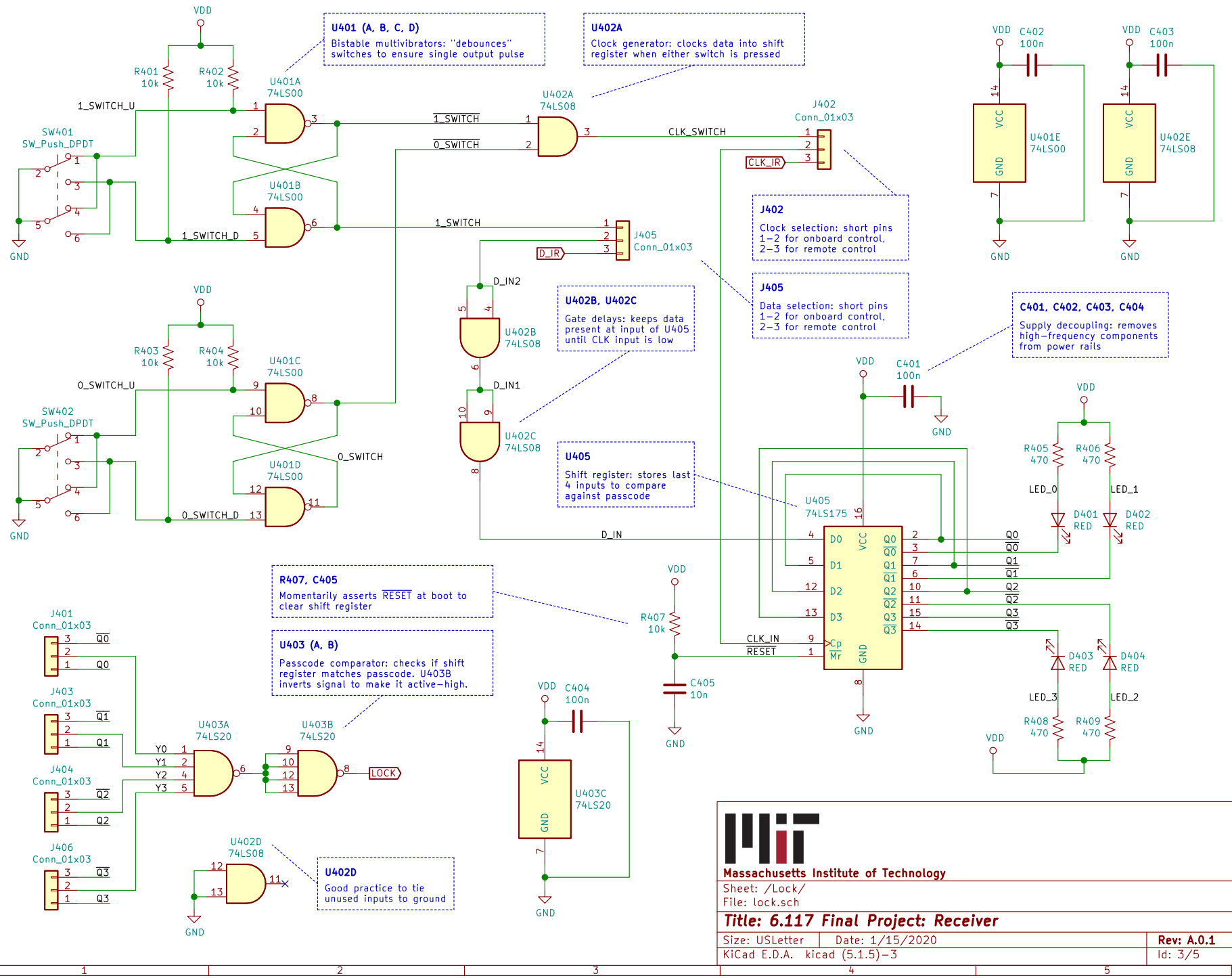
U401 (A, B, C, D)
Bistable multivibrators: "debounces" switches to ensure single output pulse
U402A
Clock generator: clocks data into shift register when either switch is pressed
J402
Clock selection: short pins 1–2 for onboard control, 2–3 for remote control
J405
Data selection: short pins 1–2 for onboard control, 2–3 for remote control
U402B, U402C
Gate delays: keeps data present at input of U405 until CLK input is low
C401, C402, C403, C404
Supply decoupling: removes high–frequency components from power rails
U405
Shift register: stores last 4 inputs to compare against passcode
R407, C405
Momentarily asserts RESET at boot to clear shift register
U403 (A, B)
Passcode comparator: checks if shift register matches passcode. U403B inverts signal to make it active–high.
U402D
Good practice to tie unused inputs to ground
VDD
GND
R401 10k
R402 10k
R403 10k
R404 10k
R405 470
R406 470
R407 10k
R408 470
R409 470
C401 100n
C402 100n
C403 100n
C404 100n
C405 10n
SW401 SW_Push_DPDT
SW402 SW_Push_DPDT
U401A 74LS00
U401B 74LS00
U401C 74LS00
U401D 74LS00
U401E 74LS00
U402A 74LS08
U402B 74LS08
U402C 74LS08
U402D 74LS08
U402E 74LS08
U403A 74LS20
U403B 74LS20
U403C 74LS20
U405 74LS175
1_SWITCH_U
0_SWITCH_U
1_SWITCH_D
0_SWITCH_D
1_SWITCH
0_SWITCH
CLK_SWITCH
D_IR
CLK_IR
D_IN2
D_IN1
D_IN
CLK_IN
RESET
LED_0
LED_1
LED_2
LED_3
D401 RED
D402 RED
D403 RED
D404 RED
J401 Conn_01x03
J403 Conn_01x03
J404 Conn_01x03
J405 Conn_01x03
J406 Conn_01x03
J402 Conn_01x03
Q0
Q1
Q2
Q3
LOCK
Y0
Y1
Y2
Y3
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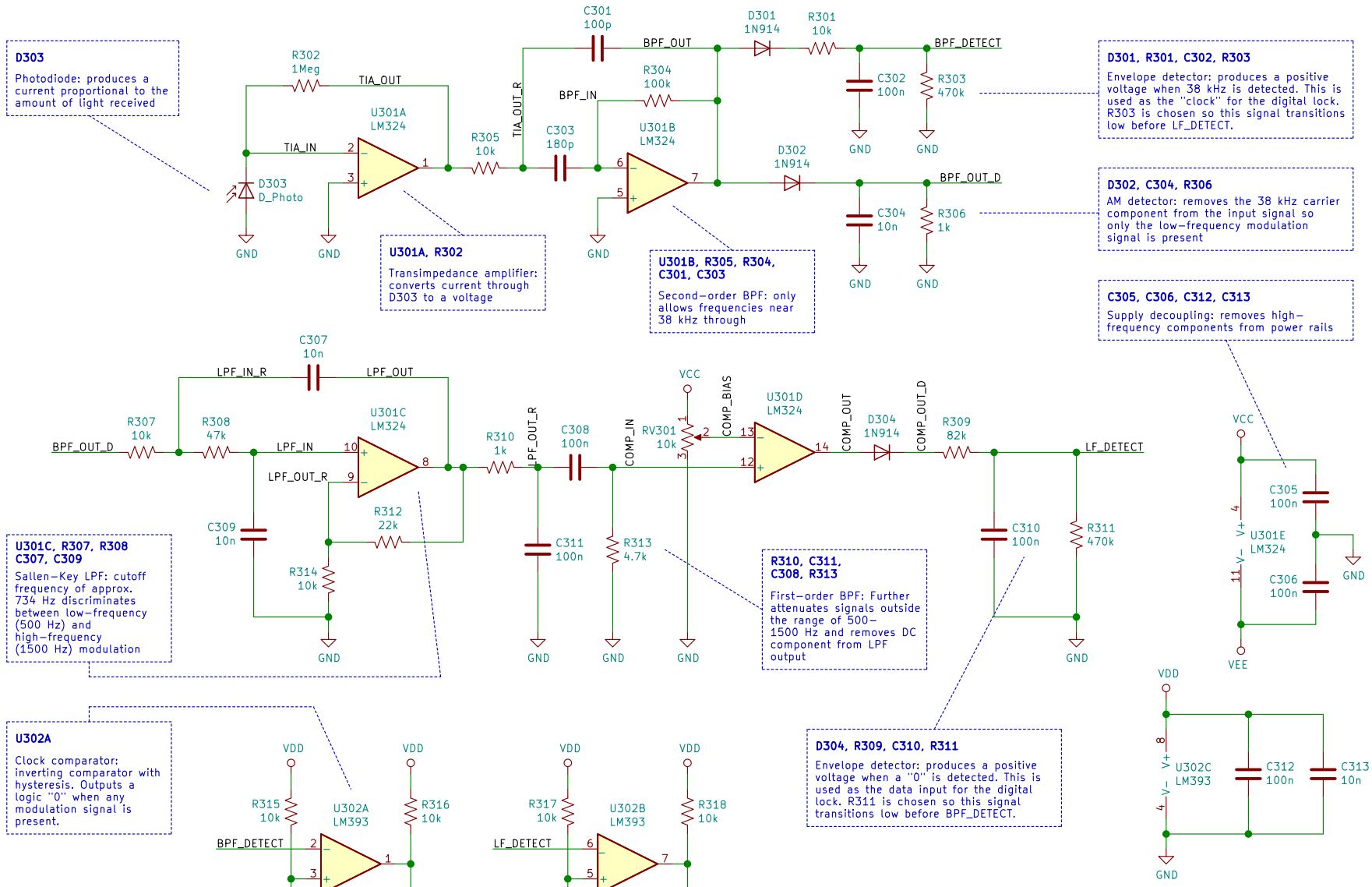
D303
Photodiode: produces a current proportional to the amount of light received
R302
1Meg
TIA_OUT
U301A
LM324
TIA_IN
D303
D_Photo
GND
C301
100p
BPF_OUT
D301
1N914
R301
10k
BPF_DETECT
R304
100k
BPF_IN
C302
100n
R303
470k
R305
10k
TIA_OUT_R
C303
180p
U301B
LM324
D302
1N914
BPF_OUT_D
C304
10n
R306
1k
U301A, R302
Transimpedance amplifier: converts current through D303 to a voltage
U301B, R305, R304, C301, C303
Second-order BPF: only allows frequencies near 38 kHz through
D301, R301, C302, R303
Envelope detector: produces a positive voltage when 38 kHz is detected. This is used as the "clock" for the digital lock. R303 is chosen so this signal transitions low before LF_DETECT.
D302, C304, R306
AM detector: removes the 38 kHz carrier component from the input signal so only the low-frequency modulation signal is present
C305, C306, C312, C313
Supply decoupling: removes high-frequency components from power rails
C307
10n
LPF_IN_R
LPF_OUT
R307
10k
R308
47k
U301C
LM324
BPF_OUT_D
LPF_IN
LPF_OUT_R
C309
10n
R312
22k
R314
10k
R310
1k
LPF_OUT_R
C308
100n
COMP_IN
VCC
RV301
10k
COMP_BIAS
U301D
LM324
COMP_OUT
D304
1N914
COMP_OUT_D
R309
82k
LF_DETECT
C311
100n
R313
4.7k
C310
100n
R311
470k
U301C, R307, R308 C307, C309
Sallen-Key LPF: cutoff frequency of approx. 734 Hz discriminates between low-frequency (500 Hz) and high-frequency (1500 Hz) modulation
R310, C311, C308, R313
First-order BPF: Further attenuates signals outside the range of 500-1500 Hz and removes DC component from LPF output
D304, R309, C310, R311
Envelope detector: produces a positive voltage when a "0" is detected. This is used as the data input for the digital lock. R311 is chosen so this signal transitions low before BPF_DETECT.
VCC
U301E
LM324
C305
100n
C306
100n
VEE
VDD
U302C
LM393
C312
100n
C313
10n
U302A
U302A
LM393
R315
10k
R316
10k
BPF_DETECT
R319
56k
CLK_IR
R321
3.3k
U302B
U302B
LM393
R317
10k
R318
10k
LF_DETECT
R320
56k
D_IR
R322
10k
U302A
Clock comparator: inverting comparator with hysteresis. Outputs a logic "0" when any modulation signal is present.
U302B
Data comparator: inverting comparator with hysteresis. Outputs a logic "1" when a "1" is received by the photodiode.
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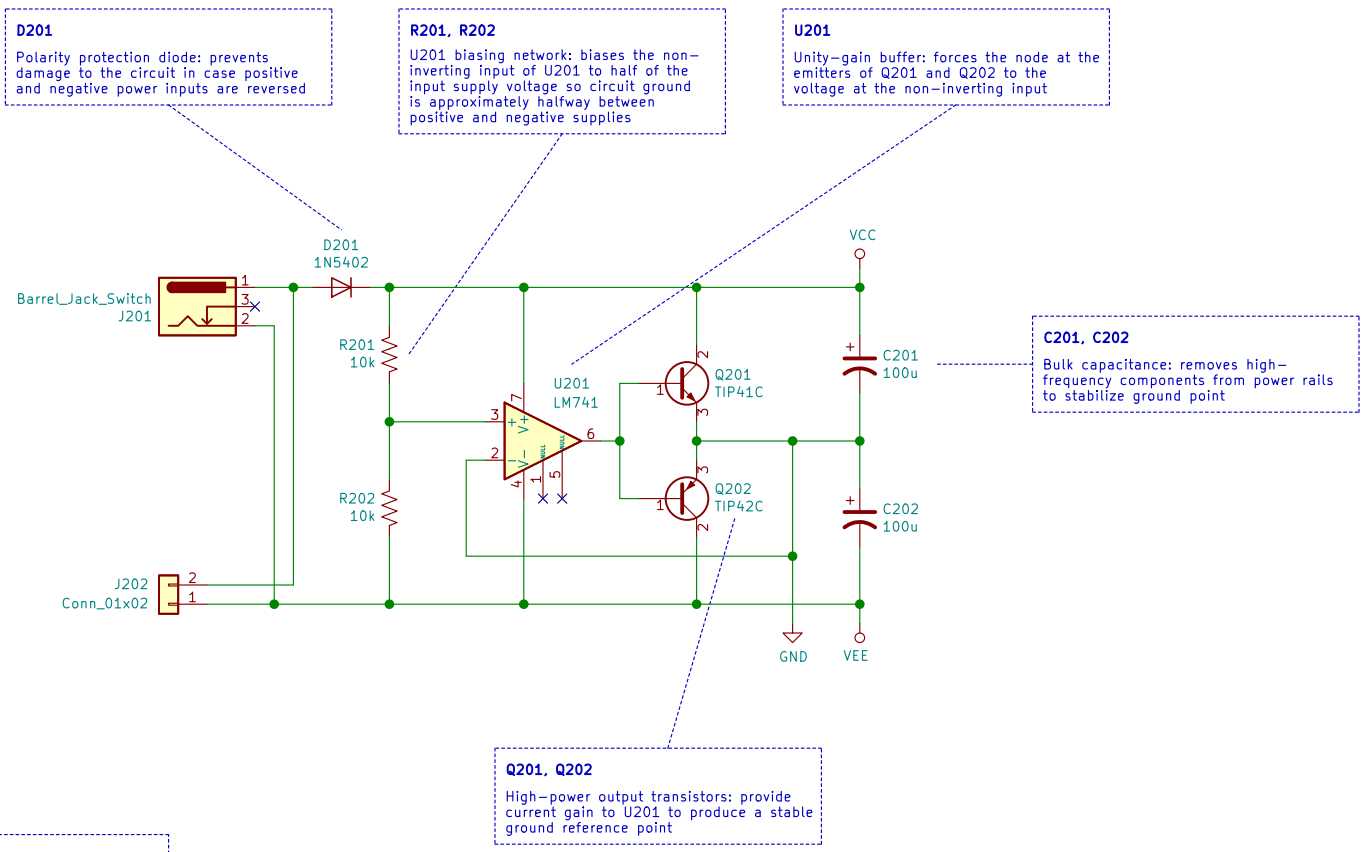

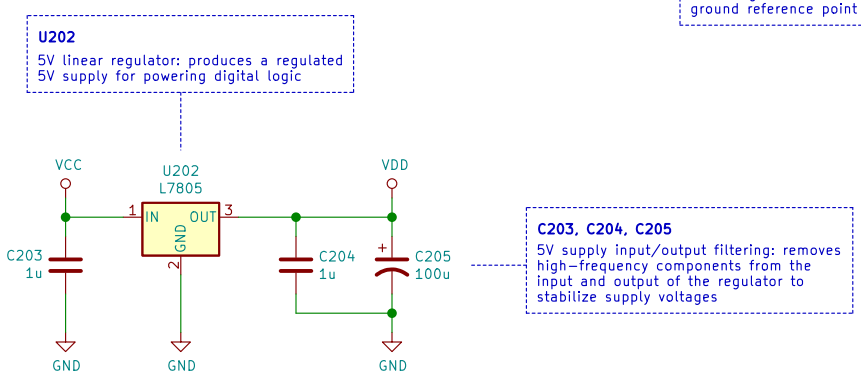

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