

# TM124GU8A

## 1 048 576-WORD BY 8-BIT DYNAMIC RANDOM-ACCESS MEMORY MODULE

SMMS181A—JANUARY 1991—REVISED JANUARY 1993

- Organization . . . 1 048 576 × 8
- Single 5-V Power Supply (±10% Tolerance)
- 30-Pin Single In-Line Memory Module (SIMM)
- TM124GU8A Utilizes Two 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)
- Long Refresh Period . . . 16 ms (1024 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS TIME (t <sub>RAC</sub> )	ACCESS TIME (t <sub>AA</sub> )	READ OR WRITE CYCLE (MIN)
	(MAX)	(MAX)	
TM124GU8A-60	60 ns	30 ns	110 ns
TM124GU8A-70	70 ns	35 ns	130 ns
TM124GU8A-80	80 ns	40 ns	150 ns

- Low Power Dissipation
- Operating Free-Air Temperature Range 0°C to 70°C

### description

The TM124GU8A is a dynamic random-access memory module organized as 1 048 576 × 8 in a 30-pin leadless single in-line memory module (SIMM).

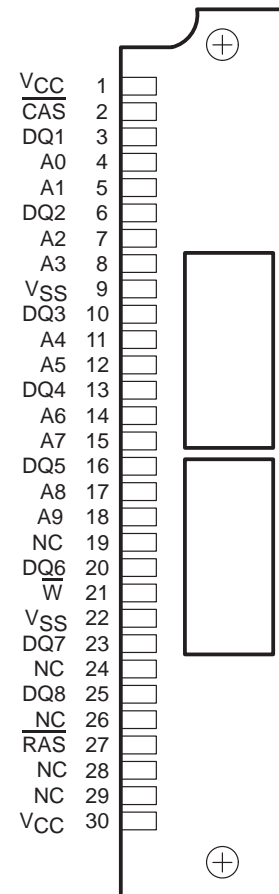
The TM124GU8A is composed of two TMS44400, 1 048 576 × 4 bit dynamic RAMs in 20/26-lead plastic small-outline J-lead packages (SOJs).

The TM124GU8A is mounted on a substrate with decoupling capacitors. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated through-holes, a cost savings can be realized.

The TM124GU8A features  $\overline{\text{RAS}}$  access times of 60 ns, 70 ns, and 80 ns. All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM124GU8A is characterized for operation from 0°C to 70°C.

SINGLE IN-LINE  
MODULE  
(TOP VIEW)



PIN NOMENCLATURE

A0–A9	Address Inputs
CAS	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
NC	No Internal Connect
RAS	Row-Address Strobe
VCC	5-V Supply
VSS	Ground

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### operation

The TM124GU8A operates as two TMS44400s connected as shown in the functional block diagram. The common I/O features of the TM124GU8A dictates the use of early write cycles to prevent contention on the DQ lines.

### specifications

Refresh period is extended to 16 milliseconds and, during this period, each of the 1024 rows must be strobed with  $\overline{\text{RAS}}$  in order to retain data.  $\overline{\text{CAS}}$  can remain high during the refresh sequence to conserve power.

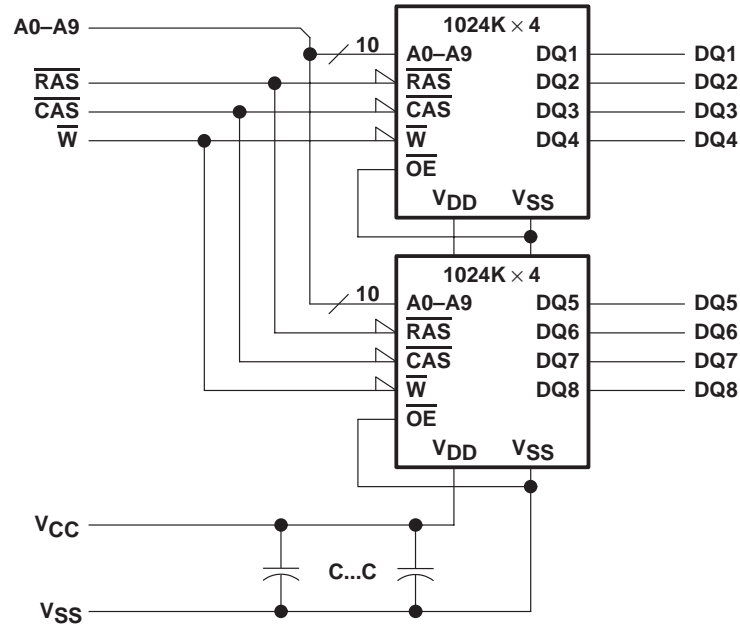
### single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness on contact area

Bypass capacitors: Multilayer ceramic

Contact area for socketable devices: Nickel plate and solder plate over copper

**functional block diagram**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range on any pin (see Note 1)	– 1 V to 7 V
Voltage range on V <sub>CC</sub>	– 1 V to 7 V
Short circuit output current	50 mA
Power dissipation	2 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	– 55°C to 125°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V<sub>SS</sub>.

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### recommended operating conditions

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2.4		6.5	V
$V_{IL}$ Low-level input voltage (see Note 2)	– 1		0.8	V
$T_A$ Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

### electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TM124GU8A-60		TM124GU8A-70		TM124GU8A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$ High-level output voltage	$I_{OH} = -5$ mA	2.4		2.4		2.4		V
$V_{OL}$ Low-level output voltage	$I_{OL} = 4.2$ mA		0.4		0.4		0.4	V
$I_I$ Input current (leakage)	$V_I = 0$ to 6.5 V, $V_{CC} = 5.5$ V, All other pins = 0 V to $V_{CC}$		$\pm 10$		$\pm 10$		$\pm 10$	$\mu$ A
$I_O$ Output current (leakage)	$V_O = 0$ to $V_{CC}$ , $V_{CC} = 5.5$ V, $CAS$ high		$\pm 10$		$\pm 10$		$\pm 10$	$\mu$ A
$I_{CC1}$ Read or write cycle current (see Note 3)	Minimum cycle, $V_{CC} = 5.5$ V		210		180		160	mA
$I_{CC2}$ Standby Current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, $V_{IH} = 2.4$ V (TTL)		4		4		4	mA
	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, $V_{IH} = V_{CC} - 0.2$ V (CMOS)		2		2		2	mA
$I_{CC3}$ Average refresh current (see Note 3)	Minimum cycle, $V_{CC} = 5.5$ V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		210		180		160	mA
$I_{CC4}$ Average page current (see Note 4)	$t_{C(P)} = \text{minimum}$ , $V_{CC} = 5.5$ V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		180		160		140	mA

NOTES: 3. Measured with a maximum of one address change while  $\overline{RAS} = V_{IL}$ .

4. Measured with a maximum of one address change while  $\overline{CAS} = V_{IH}$ .

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## 1 048 576-WORD BY 8-BIT DYNAMIC RANDOM-ACCESS MEMORY MODULE

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capacitance over recommended ranges of supply voltage and operating free-air temperature,  $f = 1 \text{ MHz}$

PARAMETER		MIN	MAX	UNIT
$C_i(A)$	Input capacitance, address inputs		10	pF
$C_i(DQ)$	Input capacitance, data inputs/outputs		7	pF
$C_i(RC)$	Input capacitance, strobe inputs		14	pF
$C_i(W)$	Input capacitance, $\overline{W}$ input		14	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TM124GU8A-60		TM124GU8A-70		TM124GU8A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{AA}$	Access time from column-address		30		35		40	ns
$t_{CAC}$	Access time from $\overline{CAS}$ low		15		18		20	ns
$t_{CPA}$	Access time from column precharge		35		40		45	ns
$t_{RAC}$	Access time from $\overline{RAS}$ low		60		70		80	ns
$t_{CLZ}$	$\overline{CAS}$ to output in low Z	0		0		0		ns
$t_{OFF}$	Output disable time after $\overline{CAS}$ high (see Note 5)	0	15	0	18	0	20	ns

NOTE 5:  $t_{OFF}$  is specified when the output is no longer driven.

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### timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TM124GU8A-60		TM124GU8A-70		TM124GU8A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Random read or write cycle (see Note 6)	110		130		150		ns
t <sub>PC</sub>	Page-mode read or write cycle time (see Note 7)	40		45		50		ns
t <sub>RASP</sub>	Page-mode pulse duration, $\overline{\text{RAS}}$ low	60	100 000	70	100 000	80	100 000	ns
t <sub>RAS</sub>	Non-page-mode pulse duration, $\overline{\text{RAS}}$ low	60	10 000	70	10 000	80	10 000	ns
t <sub>CAS</sub>	Pulse duration, $\overline{\text{CAS}}$ low	15	10 000	18	10 000	20	10 000	ns
t <sub>CP</sub>	Pulse duration, $\overline{\text{CAS}}$ high	10		10		10		ns
t <sub>RP</sub>	Pulse duration, $\overline{\text{RAS}}$ high (precharge)	40		50		60		ns
t <sub>WP</sub>	Write pulse duration	15		15		15		ns
t <sub>ASC</sub>	Column-address setup time before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>ASR</sub>	Row-address setup time before $\overline{\text{RAS}}$ low	0		0		0		ns
t <sub>DS</sub>	Data setup time	0		0		0		ns
t <sub>RCS</sub>	Read setup time before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>CWL</sub>	$\overline{\text{W}}$ low setup time before $\overline{\text{CAS}}$ high	15		18		20		ns
t <sub>RWL</sub>	$\overline{\text{W}}$ low setup time before $\overline{\text{RAS}}$ high	15		18		20		ns
t <sub>WCS</sub>	$\overline{\text{W}}$ low setup time before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>WSR</sub>	$\overline{\text{W}}$ high setup time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh only)	10		10		10		ns
t <sub>WTS</sub>	$\overline{\text{W}}$ low setup time (test mode only)	10		10		10		ns
t <sub>CAH</sub>	Column-address hold time after $\overline{\text{CAS}}$ low	10		15		15		ns
t <sub>DHR</sub>	Data hold time after $\overline{\text{RAS}}$ low (see Note 8)	50		55		60		ns
t <sub>DH</sub>	Data hold time	10		15		15		ns
t <sub>AR</sub>	Column-address hold time after $\overline{\text{RAS}}$ low (see Note 8)	50		55		60		ns
t <sub>RAH</sub>	Row-address hold time after $\overline{\text{RAS}}$ low	10		10		10		ns
t <sub>RCH</sub>	Read hold time after $\overline{\text{CAS}}$ high (see Note 9)	0		0		0		ns
t <sub>RRH</sub>	Read hold time after $\overline{\text{RAS}}$ high (see Note 9)	0		0		0		ns
t <sub>WCH</sub>	Write hold time after $\overline{\text{CAS}}$ low	15		15		15		ns
t <sub>WCR</sub>	Write hold time after $\overline{\text{RAS}}$ low (see Note 8)	50		55		60		ns
t <sub>WHR</sub>	$\overline{\text{W}}$ high hold time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh only)	10		10		10		ns
t <sub>WTH</sub>	$\overline{\text{W}}$ low hold time (test mode only)	10		10		10		ns

Continued next page.

NOTES: 6. All cycle times assume  $t_T = 5$  ns.

7. To assure  $t_{PC}$  min,  $t_{ASC}$  should be greater than or equal to 5 ns.

8. The minimum value is measured when  $t_{RCD}$  is set to  $t_{RCD}$  min as a reference.

9. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.

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**timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)**

		TM124GU8A-60		TM124GU8A-70		TM124GU8A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CHR</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high (CAS-before-RAS refresh only)	15		15		20		ns
t <sub>CRP</sub>	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	0		0		0		ns
t <sub>CSH</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	60		70		80		ns
t <sub>CSR</sub>	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low (CAS-before-RAS refresh only)	10		10		10		ns
t <sub>RAD</sub>	Delay time, $\overline{\text{RAS}}$ low to column-address (see Note 10)	15	30	15	35	15	40	ns
t <sub>RAL</sub>	Delay time, column-address to $\overline{\text{RAS}}$ high	30		35		40		ns
t <sub>CAL</sub>	Delay time, column-address to $\overline{\text{CAS}}$ high	30		35		40		ns
t <sub>RCD</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (see Note 10)	20	45	20	52	20	60	ns
t <sub>RPC</sub>	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low (CBR only)	0		0		0		ns
t <sub>RSH</sub>	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	15		18		20		ns
t <sub>TAA</sub>	Access time from address (test mode)	35		40		45		ns
t <sub>TCPA</sub>	Access time from column precharge (test mode)	40		45		50		ns
t <sub>TRAC</sub>	Access time from $\overline{\text{RAS}}$ (test mode)	65		75		85		ns
t <sub>REF</sub>	Refresh time interval		16		16		16	ms
t <sub>T</sub>	Transition time	2	50	2	50	2	50	ns

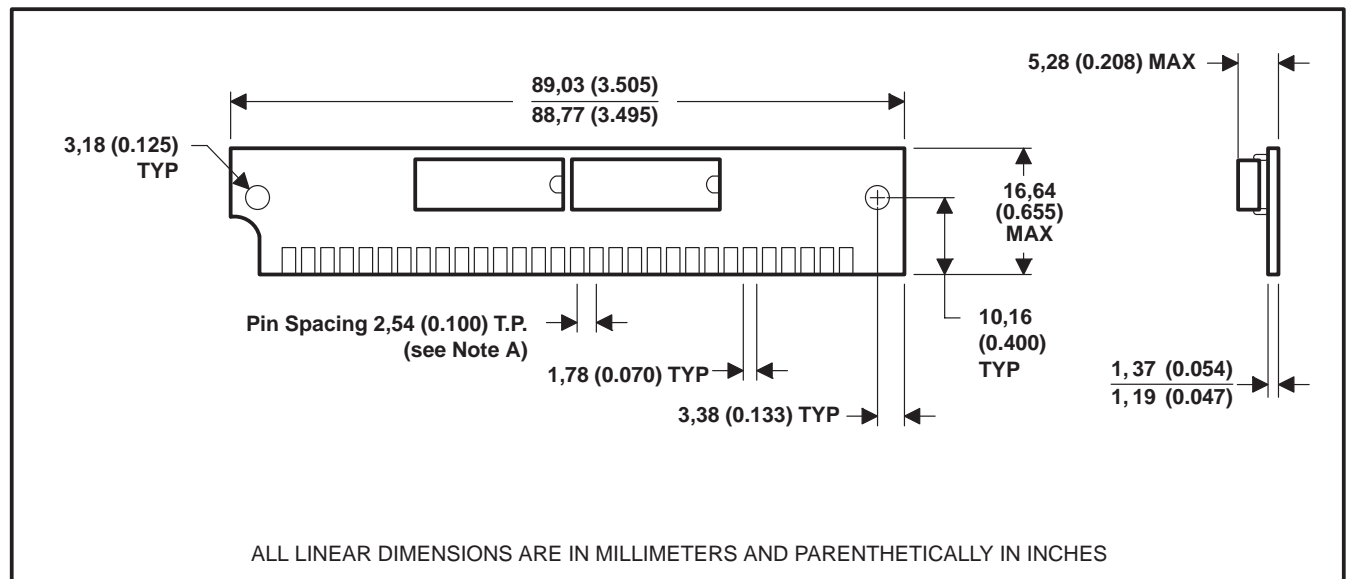
NOTE 10: The maximum value is specified only to assure access time.

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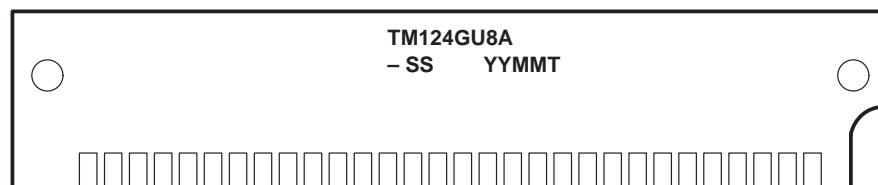
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### 30-pin U-A single in-line memory module



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

### device symbolization



YY = Year Code  
MM = Month Code  
T = Assembly Site Code  
-SS = Speed

NOTE: The location of the part number may vary.



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