FAST CMOS 16-BIT BUS TRANSCEIVER/ REGISTER (3-STATE)

IDT74FCT162646AT/CT

FEATURES:
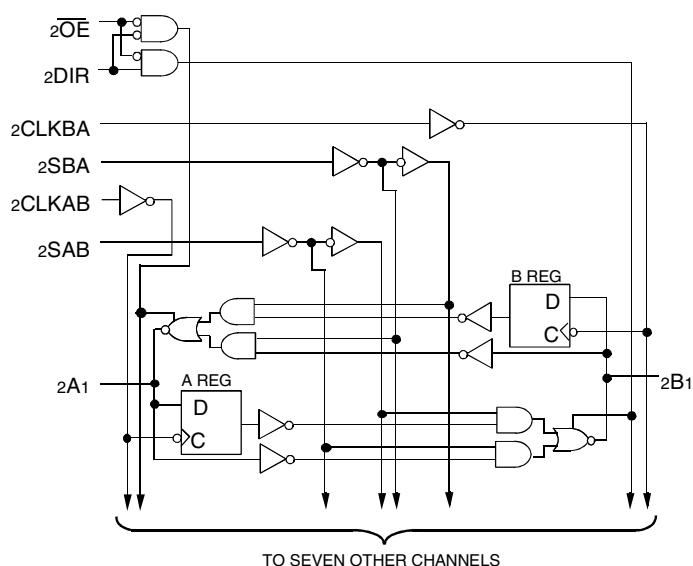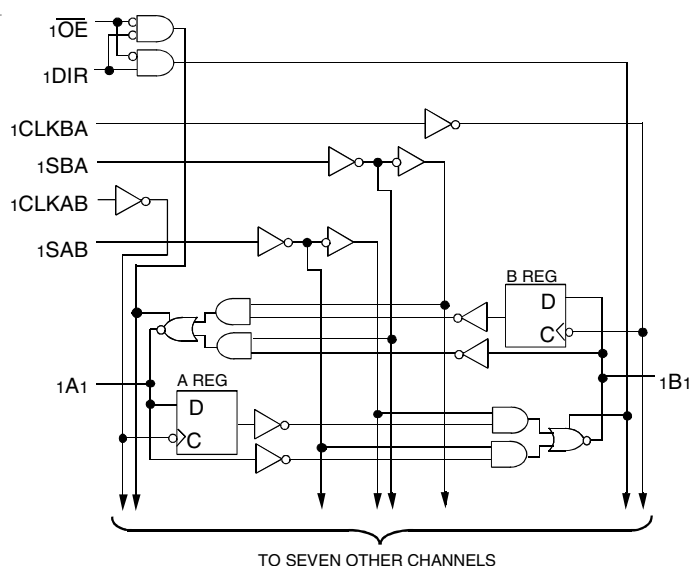
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{SK(o)}$ (Output Skew) < 250ps
- Low input and output leakage –1µA (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- V_{CC} = 5V ±10%
- Balanced Output Drivers (±24mA)
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 1V at V_{CC} = 5V, T_A = 25°C
- Available in SSOP, TSSOP, and TVSOP packages

DESCRIPTION:

The FCT162646T 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. The control circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (xDIR), over-riding Output Enable control (xOE) and Select lines (xSAB and xSBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the low-to-high transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162646T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162646T is a plug-in replacement for the FCT16646T and ABT16646 for on-board bus interface applications.
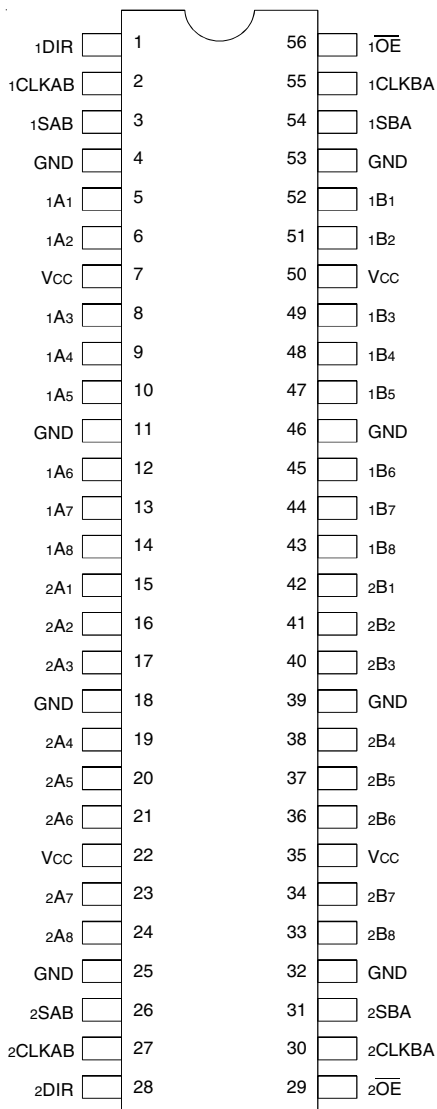
FUNCTIONAL BLOCK DIAGRAM

TO SEVEN OTHER CHANNELS

TO SEVEN OTHER CHANNELS

INDUSTRIAL TEMPERATURE RANGE

APRIL 2002

DSC-5449/2

PIN CONFIGURATION

1DIR	1		56	1$\overline{OE}$
1CLKAB	2		55	1CLKBA
1SAB	3		54	1SBA
GND	4		53	GND
1A1	5		52	1B1
1A2	6		51	1B2
VCC	7		50	VCC
1A3	8		49	1B3
1A4	9		48	1B4
1A5	10		47	1B5
GND	11		46	GND
1A6	12		45	1B6
1A7	13		44	1B7
1A8	14		43	1B8
2A1	15		42	2B1
2A2	16		41	2B2
2A3	17		40	2B3
GND	18		39	GND
2A4	19		38	2B4
2A5	20		37	2B5
2A6	21		36	2B6
VCC	22		35	VCC
2A7	23		34	2B7
2A8	24		33	2B8
GND	25		32	GND
2SAB	26		31	2SBA
2CLKAB	27		30	2CLKBA
2DIR	28		29	2$\overline{OE}$

SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to 7	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX Output and I/O terminals.
3. Output and I/O terminals for FCT162XXX.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
x A x	Data Register A Inputs
	Data Register B Outputs
x B x	Data Register B Inputs
	Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xDIR, x$\overline{OE}$	Output Enable Inputs

FUNCTION TABLE[2]

| Inputs						Data I/O[1]		Operation or Function
x$\overline{OE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

NOTES:
1. The data output functions may be enabled or disabled by various signals at the x$\overline{OE}$ or xDIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
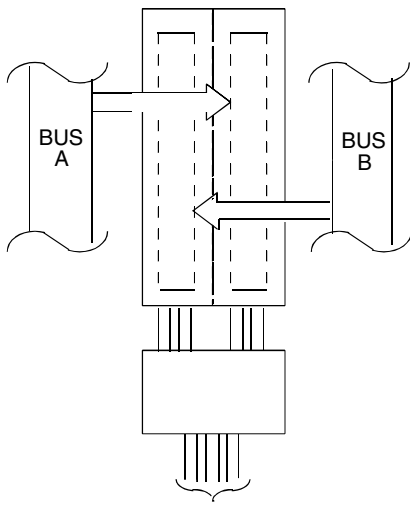   X = Don't Care
   ↑ = LOW-to-HIGH Transition
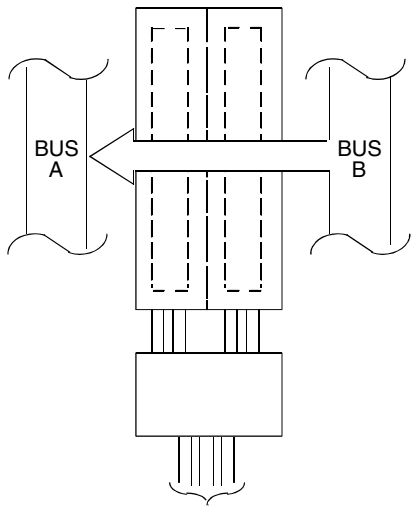
xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

Real-Time Transfer Bus B to A
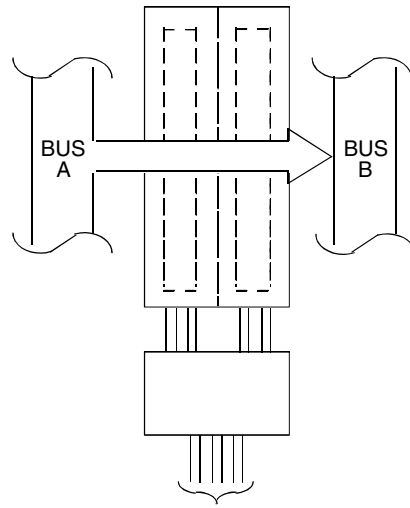
xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

Real-Time Transfer Bus A to B

xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

Storage From A and/or B
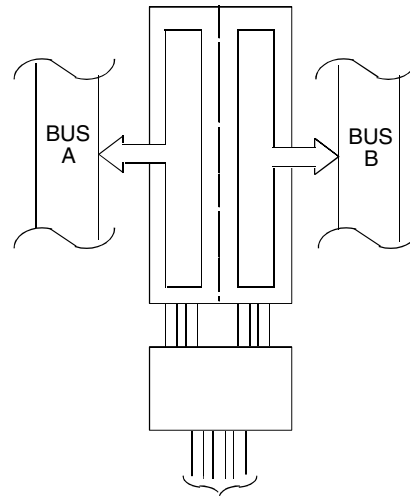
xDIR[1]	xOE	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

Transfer Stored Data to A and/or B

NOTE:
1. Cannot transfer data to A bus and B bus simultaneously.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[4]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[4]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[4]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[4]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	5	500	µA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24mA	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.55	V

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xDIR = xOE = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
		xDIR = xOE = GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
		xDIR = xOE = GND Sixteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	8.3	20[5]	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
 N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol	Parameter	Condition[1]	FCT162646AT		FCT162646CT		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2	6.3	1.5	4.3	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR or x$\overline{OE}$ to Bus		2	9.8	1.5	4.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR or x$\overline{OE}$ to Bus		2	6.3	1.5	4.3	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2	6.3	1.5	3.8	ns
t_{PLH} t_{PHL}	Propagation Delay xSBA or xSAB to Bus		2	7.7	1.5	4.2	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		2	—	2	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		1.5	—	0	—	ns
t_W	Clock Pulse Width HIGH or LOW		5	—	3	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
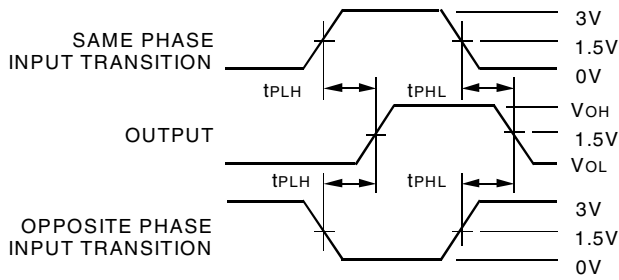
TEST CIRCUITS AND WAVEFORMS
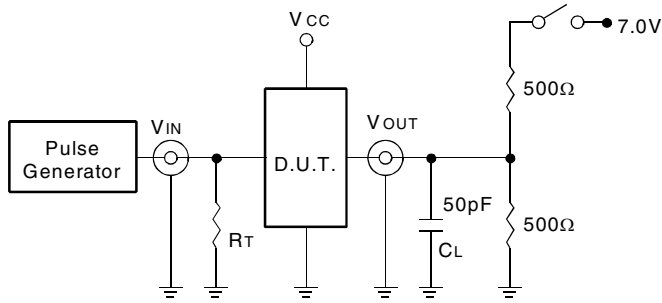
Test Circuits for All Outputs
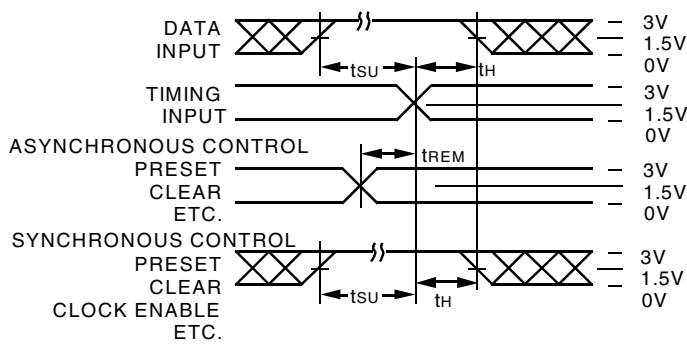
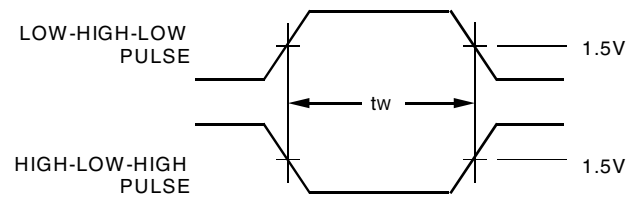*Set-up, Hold, and Release Times*

Propagation Delay

SWITCH POSITION

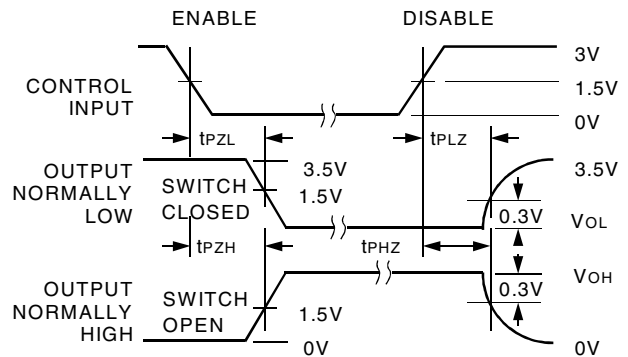| Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
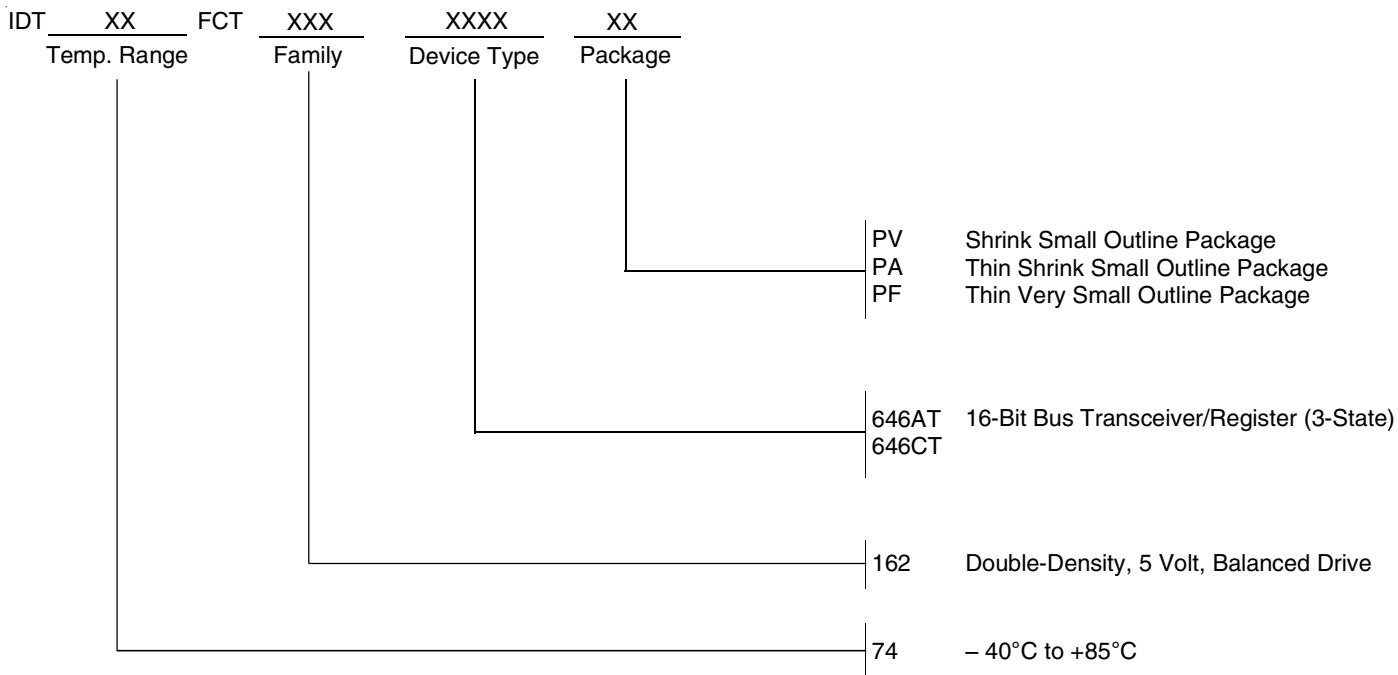

Pulse Width

Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq$ 1.0MHz; $t_F \leq$ 2.5ns; $t_R \leq$ 2.5ns.

ORDERING INFORMATION

```
IDT ___XX___ FCT ___XXX___ ___XXXX___ ___XX___
    Temp. Range    Family    Device Type   Package
```

PV	Shrink Small Outline Package
PA	Thin Shrink Small Outline Package
PF	Thin Very Small Outline Package

646AT	16-Bit Bus Transceiver/Register (3-State)
646CT	

162	Double-Density, 5 Volt, Balanced Drive

74	– 40°C to +85°C

DATA SHEET DOCUMENT HISTORY

1/21/2002 Removed Military temp grade

3/28/2002 Removed standard speed grade