

Institute for Hadronic Structure and Fundamental Symmetries
School of Natural Sciences
Technical University of Munich

Development of FPGA frontend electronics of the scintillating fiber hodoscope of AMBER at CERN

Tim Maehrholz

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Supervisor:

Prof. Dr.

Chair of

Second Examiner:

PD Dr.

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Abstract

The proton radius measurement (PRM) experiment at AMBER at CERN aims to measure the proton radius by scattering muons on protons. The scintillating fiber hodoscope (SFH) is a key component of the PRM experiment, providing essential time measurements of the incoming and scattered muons. In this thesis, the development of the FPGA-driven frontend electronics of the SFH is presented, focusing on the development of the FPGA firmware required for the control and provisional readout of the Citiroc1A ASIC, a crucial part of the readout and trigger electronics.

We conclude that the developed firmware is capable of controlling and reading out the signals from the Citiroc1A ASIC, but that the frontend electronics are currently not performing as desired. We propose further research and steps to investigate and understand the behaviour of the frontend electronics of the scintillating fiber hodoscope and complete its development.

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CHAPTER 1

Introduction

”What we observe is not nature itself, but nature exposed to our method of questioning.”[Werner Heisenberg][9]

Progress in particle physics has always been driven by the desire to understand the fundamental building blocks of our universe.

Our current best theory for the innnerworkings of our world, the standart model of particle physics tells us, that the matter we see around us is mostly made up of down and up quarks and electrons. Combinations of these quarks, held together by the strong nuclear force form the proton and neutron, the nuclei of the atoms that make up the matter of the everyday world.[15] Even though the proton was discovered over a century ago by Ernest Rutherford[13], it still holds several mysteries that continue to puzzle physicists. One of these mysteries is the size of the proton.

The semantic meaning of size in the realm of particle physics is not as straight forward as in the macroscopic world. An answer to the question, what is the size of the proton can be given by looking at the charge radius of the proton, first measured in 1956 by E. E. Chambers and R. Hofstadter.[4]

The radius of the proton has been measured several times more since then, with different methods, such as electron-proton scattering experiments and the lamb shift in muonic and ordinary hydrogen. The results of these measurements differ by five standard deviations, giving rise to the so called proton radius puzzle.[1]

The proton radius measurement (PRM) experiment at AMBER at CERN aims to help resolve this puzzle by measuring the proton radius with a new method, the elastic scattering of muons on protons.

To achieve this, the PRM experiment will measure the cross section of this scattering process and from this extract the form factors of the proton, which in turn allows for the calculation of the proton radius.

The scintillating fiber hodoscope (SFH) is a key component of the PRM experiment, as it provides essential time measurements of the incoming and scattered muons, needed for the measurement of the proton radius.[\[1\]](#)

This thesis will focus on the development of the FPGA driven frontend electronics of the scintillating fiber hodoscope (SFH), developed at the Technical University of Munich by the Physics Department E18 for the proton radius measurement at AMBER at CERN, especially on the development of the FPGA firmware required for the control and readout of the Citroc1A ASIC, a crucial part of the readout and trigger electronics.

The framework of this thesis is structured in order to provide the necessary background information for the development of the frontend electronics of the SFH.

The next chapter will give a general overview of the PRM experiment and the theoretical background of the proton radius measurement.

In chapter 3 the frontend electronics of the SFH, with a focus on the functionality and behaviour of Citroc1A ASIC will be described.

Chapter 4 will explain the developed FPGA firmware for the control and readout of the Citroc1A ASIC, as well as give a short overview of the setup that was used for testing the developed firmware.

Chapter 5 will present the results of the testing of the developed firmware and the performance of the frontend electronics of the SFH.

In chapter 6 these results will be analyzed and discussed.

The final chapter of this thesis will give a short summary of the results and an outlook on the future development of the frontend electronics of the SFH, necessary for it to successfully contribute to the resolution of the proton radius puzzle.

CHAPTER 2

Theoretical Concepts and Overview of AMBER

2.1. Measurment of the Charge Radius of the Proton (PRM)

The proton is a baryon, a composite particle made up of one down quark and two up quarks. From this follows that the proton is not a point particle, but has an internal structure.[\[15\]](#)

The internal structure can be described by the structure functions of the proton, the electric and magnetic form factors G_E and G_M .[\[1\]](#)

2.1.1. Previous Measurements of the Proton Radius

The charge radius of the proton has been measured several times before with different methods. The two premier methods are electron proton scattering experiments and the Lamb shift in muonic and ordinary hydrogen. The results of these measurements differ by five standard deviations as shown in Figure 2.1, this has given rise to the so called proton radius puzzle.[\[1\]](#)

2.1.2. Elastic Scattering of Muons on Protons

The AMBER PRM experiment at CERN aims to help reslove the proton radius puzzle, by measuring the elastic scattering of muons on protons. The first order cross section,

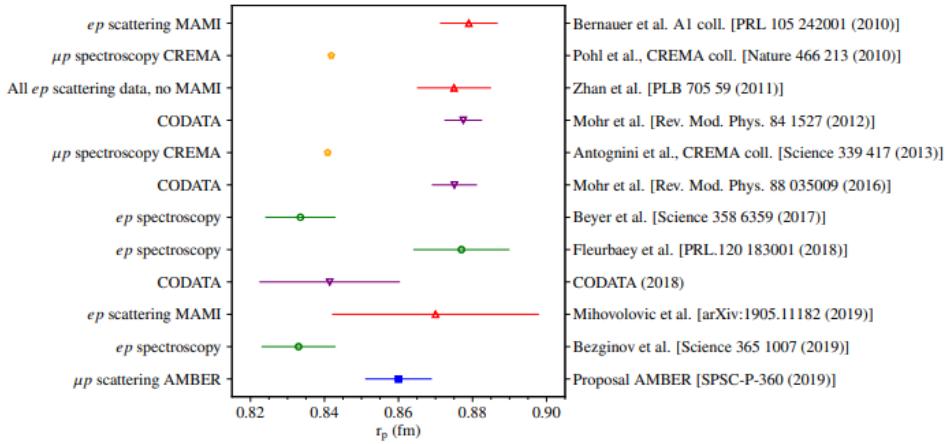


Figure 2.1.: Previous measurements of the proton radius from electron proton scattering experiments and the Lamb shift in muonic and ordinary hydrogen, the measurements differ from each other by five standard deviations. An arbitrary result for the proton radius by the PRM experiment, with the expected uncertainty is included.[1]

taking into account only interactions where one virtual photon was exchanged, for the elastic scattering of muons on a proton target is

$$\frac{d\sigma}{dQ^2} = \frac{\pi\alpha^2}{Q^4 m_p^2 p_\mu^2} \left[(G_E^2 + \tau G_M^2) \frac{4E_\mu^2 m_p^2 - Q^2(s - m_\mu^2)}{1 + \tau} - G_M^2 \frac{2m_\mu^2 Q^2 - Q^4}{2} \right] \quad (2.1)$$

with $Q^2 = -q^2$ the squared transferred four-momentum, $\tau = Q^2/4m_p^2$, $s = (p_\mu + p_p)^2$, G_E the electric form factor of the proton, G_M the magnetic form factor of the proton and α the fine structure constant.[2] Through determining the form factor G_E for small Q^2 , the charge radius of the Proton can be claculated with the following equation[2]

$$r_p^2 = -6 \frac{dG_E}{dQ^2} \Big|_{Q^2=0} \quad (2.2)$$

Since the cross section can not be measured at $Q^2 = 0$, the form factors G_E and G_M have to be extrapolated to $Q^2 = 0$. This is done by fitting the form factors to the experimental data and then extrapolating to $Q^2 = 0$.[2]

2.2. General Setup for PRM at AMBER.

2.2.1. Detectors for PRM

To determine the magentic G_M and electric form G_E factors of the proton and thus the charge radius of the Proton, the experimental cross section of the elastic scattering of

2.2. General Setup for PRM at AMBER.

muons on protons has to be measured. The general setup of the PRM experiment, with focus on the new detectors needed for the proton radius measurement, is shown in Figure 2.2.

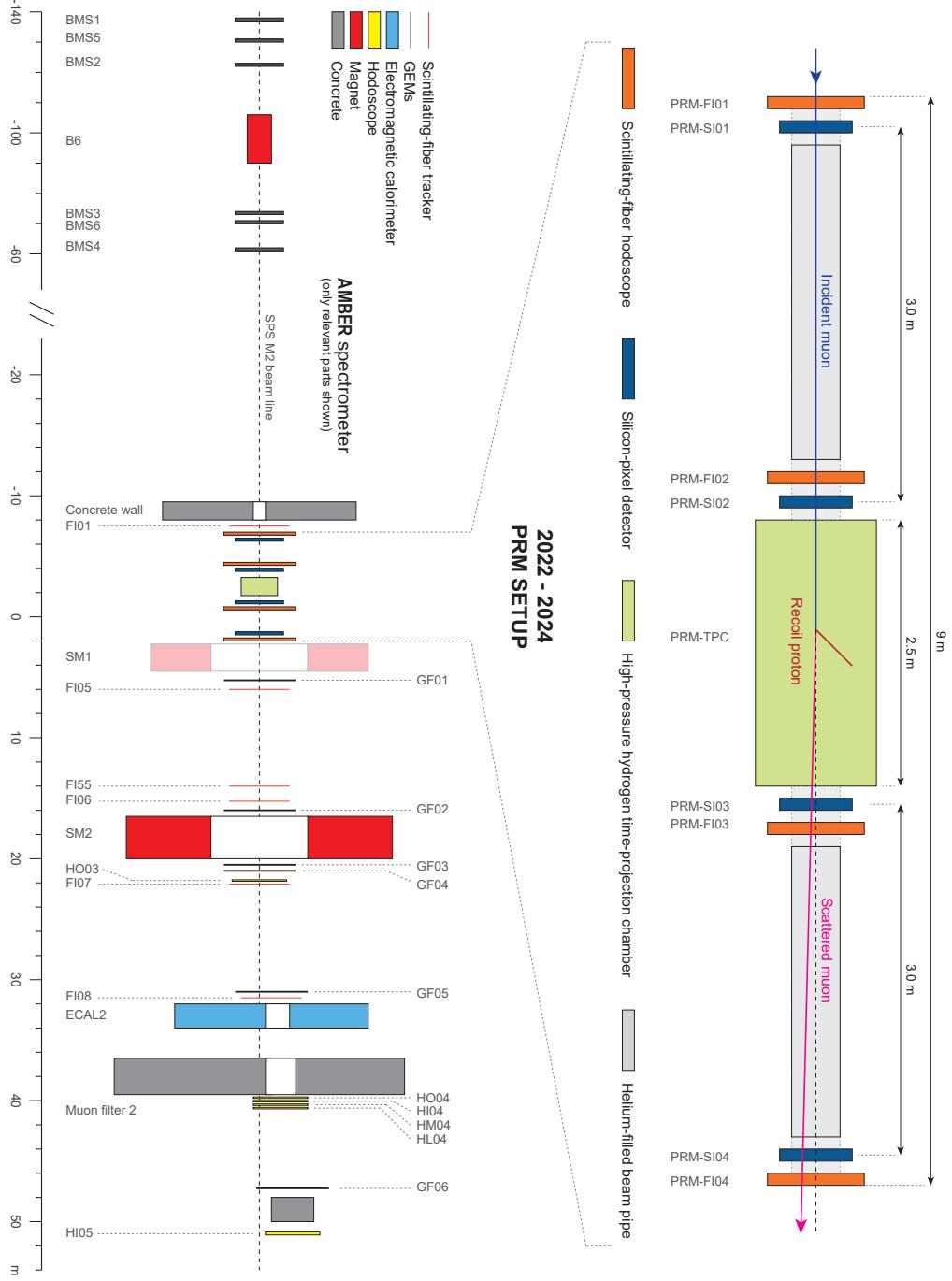


Figure 2.2.: General setup of the Amber experiment with new detectors for PRM.[7]

The incoming muon beam with an energy of 100 GeV[1] and an beam rate of 2×10^6 [3] particles per second is scattered on a pressurized hydrogen gas target, located in the

Time Projection Chamber (TPC), which also acts as the detector for the recoil path of the scattered proton.

The reconstruction of the path of the muon is achieved through the usage of two detector types, combined into one unified tracking station (UTS) as shown in Figure 2.3.

Each UTS consists of three layers of pixilated silicon detectors (ALPIDEs), for precise positional measurements (spacial resolution of about $8 \mu\text{m}$ ^[8]) of the incoming and scattered muons, but they lack, with their time uncertainty of $5 \mu\text{s}$ ^[8] the required time resolution for the PRM experiment. For this reason each UTS includes a scintillating fiber hodoscope (SFH), the detector of interest for this thesis, which provides the time precision(300 ps ^[8]) for the measurement.

Four of these unified tracking stations, two before and two after the active target, are placed in the beamline as shown in Figure 2.2. The measurement of the momentum of the scattered muon is done by existing COMPASS detectors located after the, for the PRM newly included, detectors^[1].

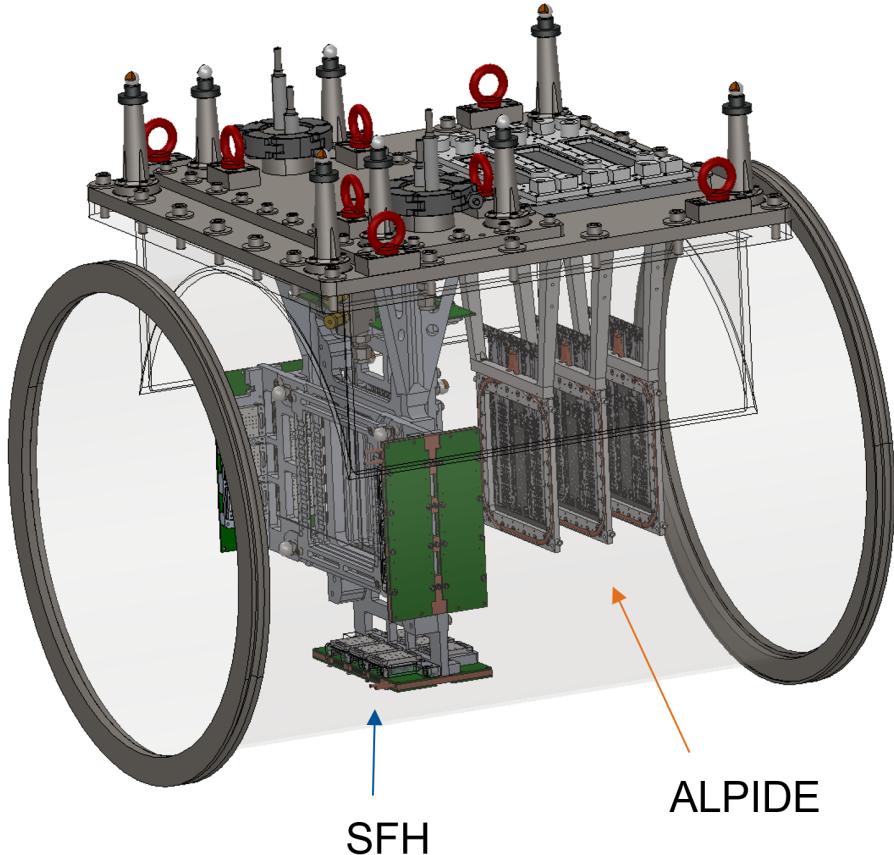


Figure 2.3.: Unified tracking station (UTS) with three layers of pixilated silicon detectors (ALPIDEs) and the scintillating fiber hodoscope (SFH).^[7]

2.2.2. Scintillating Fiber Hodoscope(SFH)

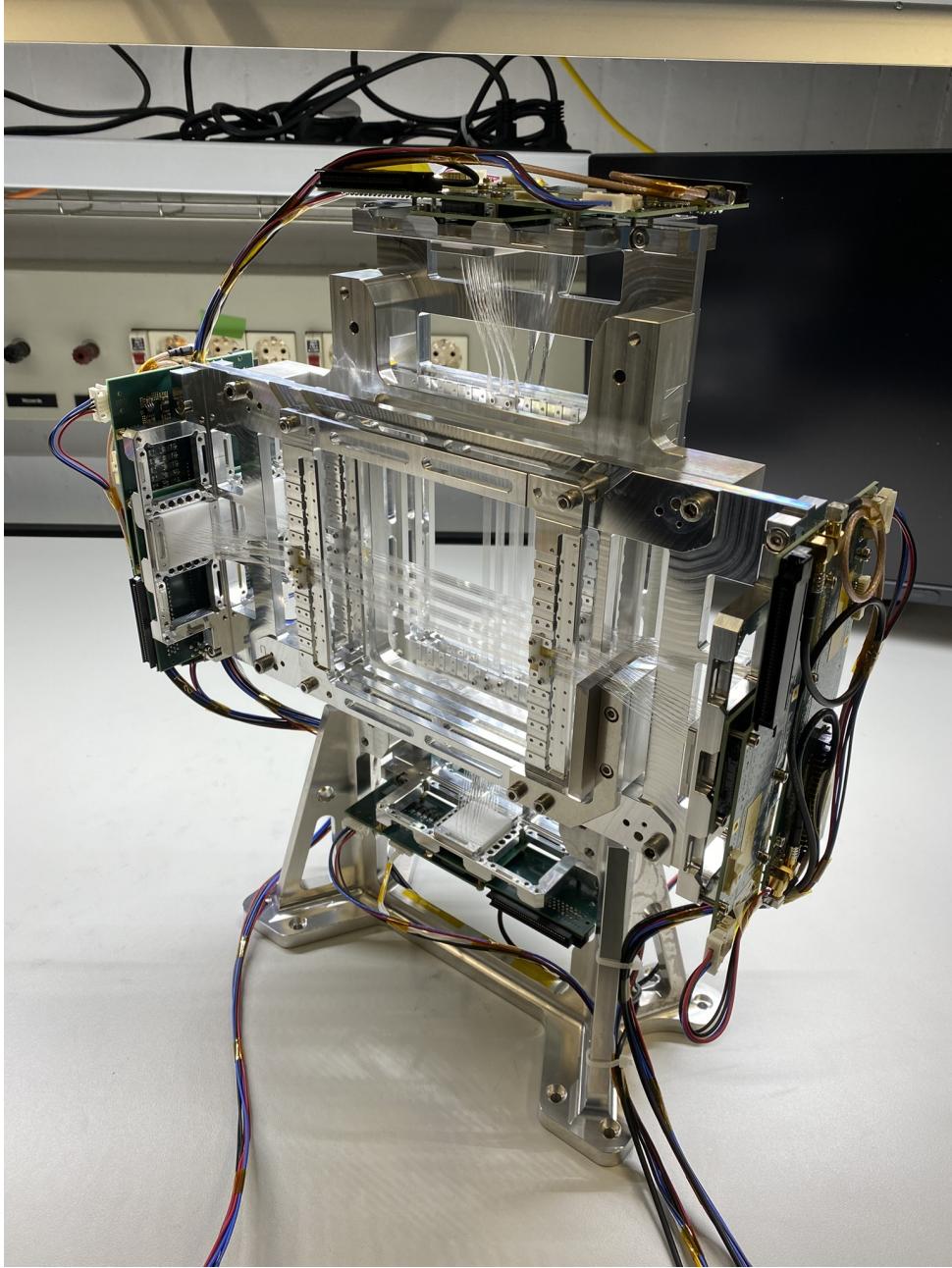


Figure 2.4.: Scintillating fiber hodoscope (SFH) with two of the four layers of scintillating fibers installed. The frontend electronics are not attached.[7]

The scintillating fiber hodoscope shown in Figure 2.4, the detector for which the FPGA driven frontend electronics are developed in this thesis, is used to measure the precise timing(300 ps[8]) of the incoming and scattered muons. Every SFH contains four layers of scintillating fibers, two in x and two in y direction. Each layer is made up of 192[8], 500 μm thick[5] fibers, in total 768[8] fibers per SFH. When charged particles, muons in

this case, pass through a scintillating fiber they excite the scintillating material, which then emits photons. Both ends of every fiber are connected to a silicon photomultiplier (SiPM) which converts the photons into an electrical signal, that is then proccesed by the frontend electronics. To minimize cost and the amount of data that has to be processed, a mirrored readout is planned, where only one end is connected to the SiPM array and the other end is mirrored.[\[7\]](#)

2.3. Field Programmable Gate Arrays (FPGA)

Field Programmable Gate Arrays (FPGAs) are integrated circuits that can be programmed after manufacturing. FPGA are made up of a grid of programmable logic blocks (PLBs) and programmable interconnects. They posses the advantage of beeing flexible, reconfigurable and beeing able to process large amounts of data in parallel. The frontend electronics for the SFH require large amounts of data to be processed in real time, which makes FPGAs with their large data throughput and parallel processing capabilities ideal for this task.[\[6\]](#)

The FPGA used in the frontend electronics for the scintillating fiber hodoscope is part of the Xilinx Artix-7 family.[\[11\]](#)

CHAPTER 3

Frontend Electronic of the Scintillating Fiber Hodoscope

3.1. Overview of the Frontend Electronics

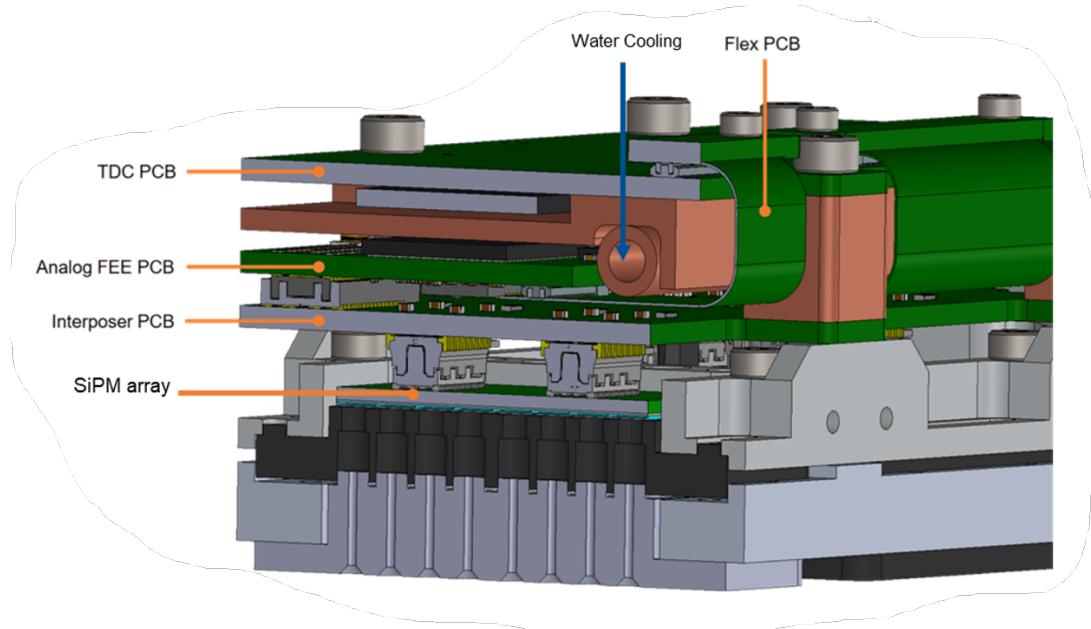


Figure 3.1.: Sideview of the frontend electronics that will be attached on the sides of the SFH, the fiber holders will be attached to the fibers.[7]

3.1.1. Proccesing of the SFH Signal

The frontend electronics of the scintillating fiber hodoscope process the signals from the scintillating fibers. They can be attached on all four sides of the SFH, as can be seen in

Figure 2.4. The fibers are connected to the fiber holders on both ends as shown in Figure 3.1. There are in total 768[8] fibers per SFH. Since both ends produce an electric signal, a total of 1546 signals have to be proccesed. This would require a total of 48 Citiroc1A ASICs, spread over 8 frontend electronics units. To mitigate the cost of the frontend electronics, as well as limit the amount of data that has to be processed, a mirrored setup is planed. In this setup only one end of the fibers is connected to the SiPM array, while the other end is mirrored. This would reduce the amount of required frontend electronics units to 4.[7]

The incoming photons are transformed into electric signals by the SiPM arrays. The SiPM signals are then transmitted to the analog frontend electronics (FEE) PCB by the interposer PCB also shown in Figure 3.1.

The FEE PCB and the iFTDC are the two main components of the frontend electronics, as shown in Figure 3.1, and are connected over three flex PCBs as well as plug connectors. The whole setup is cooled by a water cooling system and is designed in a way that minimizes its size in order to reduce the amount of material in the beamline.[7]

3.1.2. The Analog Frontend Electronics (FEE) PCB



Figure 3.2.: The analog frontend electronics (FEE) PCB with the six Citiroc1A ASICs, on the left side the power supply and on the right side ADCs for temporary readout, in order to test the SFH. The output of the Citiroc1A ASICs is transmitted to the iFTDC over three flex PCBs.[7]

The analog frontend electronics (FEE) PCB, shown in Figure 3.2, together with the iFTDC forms the heart of the frontend electronics. The FEE PCB incorporates six Citiroc1A ASICs, which are designed to amplify and process the signals from the SiPM arrays. Each Citiroc1A ASIC handles 32 signals. The output of the ASICs is then transmitted to the iFTDC over three flex PCBs. Two Citirroc1A ASICs are each controlled by one Artix-7 FPGA located on the iFTDC.[11]

Currently, for prototype testing the SFH is read out by the ADCs on the FEE PCB, as is illustrated on the right side of the FEE PCB in Figure 3.2, but the final setup will use the iFTDC for the readout of the SFH.[7]

3.1.3. The iFTDC



Figure 3.3.: The iFTDC with three Artix-7 FPGA, the three flex PCBs that connect the iFTDC with the FEE PCB and the connected power suply.

The iFTDC, depicted in Figure 3.3 is a FPGA based time-to-digital converter. It consists of three Artix-7 FPGA, who each control two Citiroc1A ASICs. The FPGA handels the readout as well as the configuration of the Citiroc1A ASICs[11].

The FPGAs are programmed via jtag and connected to the controlling computer via ethernet.

3.2. The Citiroc1A ASIC

The Citiroc1A ASIC is a frontend application-specific integrated circuit developed by Weeroc for the readout of SiPM detectors. It allows for the readout of 32 channels and is sensitive to $\frac{1}{3}$ of a photoelectron.[14]

The Citiroc1A ASIC is controlled and readout by the Artix-7 FPGAs on the iFTDC, each FPGA controlling two Citiroc1A ASICs.[11] The focus of this thesis is the development of the FPGA firmware for the control of the Citiroc1A ASICs, but a provisional readout firmware for testing the configuration of the Citiroc1A will also be developed.

3.2.1. Signal Processing of the Citiroc1A

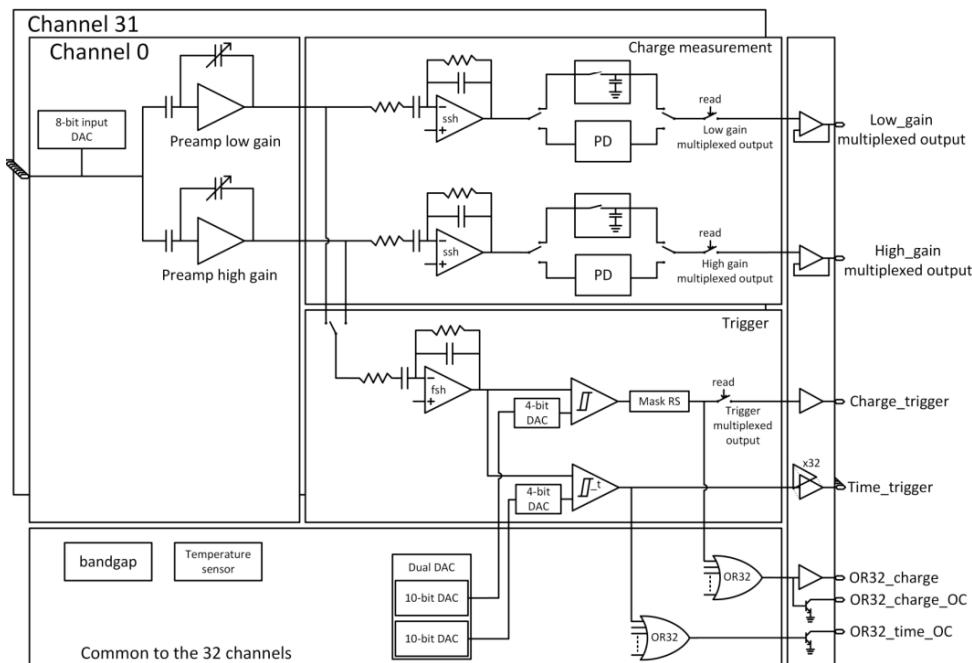


Figure 3.4.: General ASIC block scheme of the Citiroc1A.[14]

The general block scheme of the Citiroc1A is shown in Figure 3.4.

The Citiroc1A allows for the fine tuning of the SiPM bias voltage for each channel via the 8-bit input DAC.

The input signals are amplified with a variable high or low gain, configurable for every channel as depicted in Figure 3.5. The PRM experiment requires the maximal high gain of 62.[11]

The amplified signals are then shaped by either the slow (ssh) or fast shaper (fsh) as shown in Figure 3.4. The fast shaper is used for the PRM experiment, since it has a 15 ns peaking time and a better time resolution, which is necessary for the time precision of

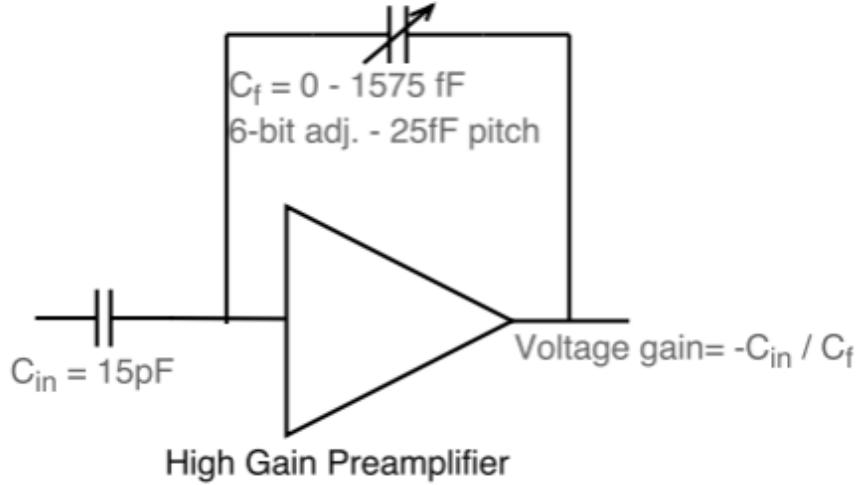


Figure 3.5.: High gain amplification of the Citiroc1A. The gain is adjustable from 0 to 1575 fF in 25 fF steps.[14]

the SFH.[14]

The ASIC has two discriminators, the charge discriminator and the time discriminator. In this thesis we will only look at the time discriminator, since it provides the time information. The time discriminator threshold is adjustable via a 10 bit dac for all channels and an additional 4 bit dac for every individual channel as shown in Figure 3.4[14].

3.3. Configuration of the Citiroc1A

The configuration of the Citiroc1A is achieved by the FPGA via the five signals shown in Figure 3.6. The **Select** signal allows the choice between configuring the slow control, for **Select** = 1 or the probe register, for **Select** = 0.[14]

3.3.1. The Slow Control Register

The slow control register is used to set values for internal variables like the high gain for a channel or the time discriminator threshold. It also allows for the FPGA to turn off specific stages of the Citiroc1A, such as the slow shaper or the time discriminator. The register is 1144 bits long. A full list of all the register that can be set is shown in Table A.1 in Appendix A.

The process of writing the bitstream into the slow control register by the FPGA is illustrated in Figure 3.7.

The **Rstb_sr** signal is an asynchronous active-high reset for the serial register, applying to

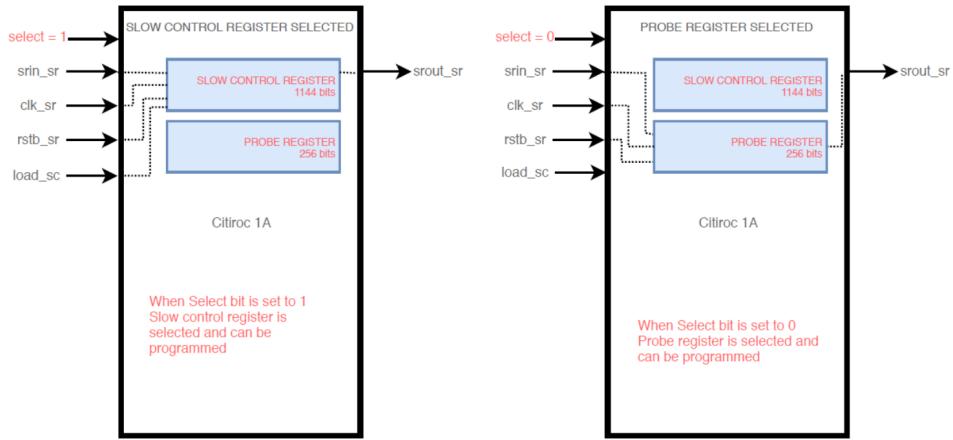


Figure 3.6.: The two configurable registers of the Citiroc1A are selected using the **Select** signal. The FPGA communicates with the Citiroc1A through the signals **Clk_sr**, **Rstb_sr**, **Srin_sr**, and **Load_sc**, while the **Srout** signal is sent back from the Citiroc1A to the FPGA for verification.[14]

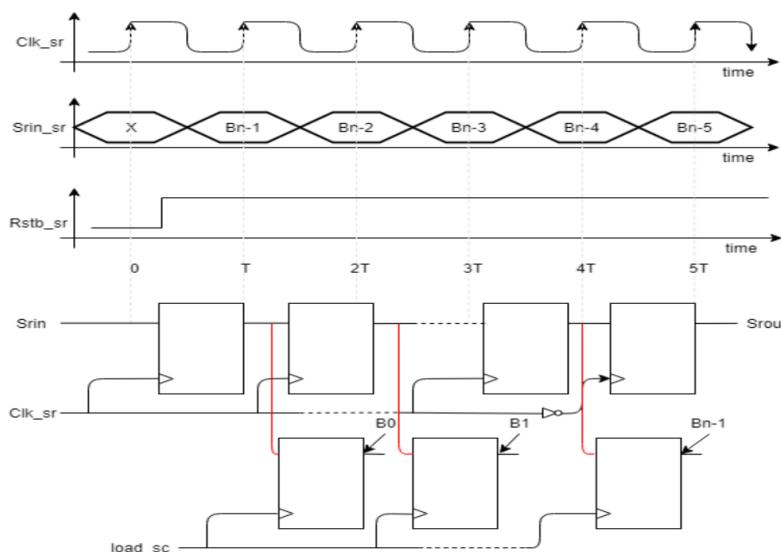


Figure 3.7.: The slow control chronogram, depicting the bitstream writing process controlled by **Clk_sr** the clock signal and **Srin_sr** the data signal. A rising edge of **Load_sc** is required, after successful verification with the **Srout** signal to load the slow control register.[14]

both the slow control and probe register.

The FPGA processes the bitstream sequentially, starting with the least significant bit (LSB). The first bit of the bitstream to enter the serial register will be the last bit of the slow control register. Each bit is sent on the **Srin_sr** signal in coordination with a rising edge of the **Clk_sr** clock signal.

The **Load_sc** signal is used to load the bitstream into the slow control register. After all

bits have been sent to the Citiroc1A, a rising edge on **Load_sr** is required to load the slow control register.

The **Srou** signal is sent back from the Citiroc1A to the FPGA for bitstream verification. Only after the FPGA has sent the full bitstream twice, does the **Srou** signal take on the value of the bitstream, since the **Srou** signal is shifted by the length of the bitstream.[14] One should only set the rising edge of the **Load_sr** signal after verifying that the **Srou** signal takes on the correct values.

3.3.2. The Probe Register

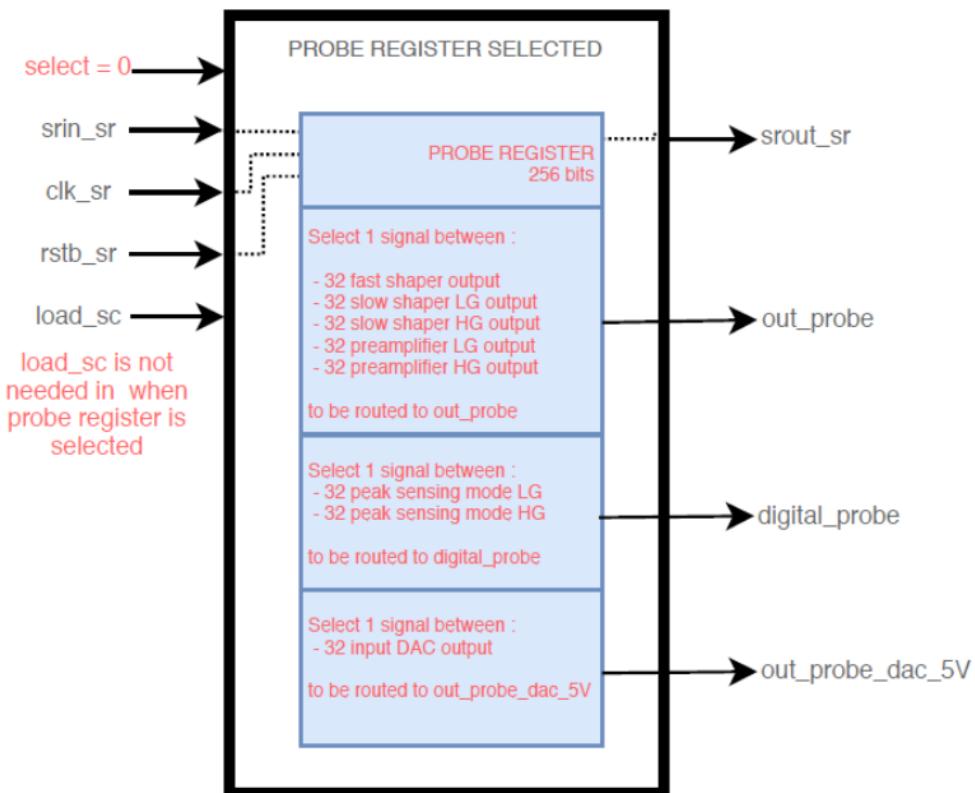


Figure 3.8.: Scheme block of internal probing system, allowing the routing of internal signals to probe pins for debugging purposes. It is configured via the probe register.[14]

The probe register is used for routing internal signals to several output pins for debugging purposes. Its functionality is illustrated in Figure 3.8. The register consists of 256 bits and is written the same way as the slow control register, with the difference that the bits are directly written into the Citiroc1A without requiring a rising edge on **Load_sc**.[14]

The full list of all the register that can be set in the probe register is shown in Table A.2 in Appendix A.

The internal signals for each channel that can be routed to the output pins are shown in Table 3.1.

Signal Source	Description	Output Pin
High and low gain preamplifier, slow and fast shapers	Outputs of preamplifiers and shapers	<code>out_probe</code>
<code>PeakSensing_modeb_LG</code>	Internal peak-sensing signal for low gain	<code>digital_probe</code>
<code>PeakSensing_modeb_HG</code>	Internal peak-sensing signal for high gain	-
Output of input DAC	DAC output voltage (5 V)	<code>out_probe_dac_5_V</code>

Table 3.1.: Internal signal routing to output pins for each channel.

Only one signal can be routed to each output pin at a time, without potentially causing a short circuit.[[14](#)]

CHAPTER 4

Development of the FPGA Firmware for the SFH

4.1. Overview of the Firmware

The firmware in this thesis was developed for only two of three Artix-7 FPGAs integrated into the iFTDC, as detailed in Section 3.1.3. The third FPGA was excluded due to the incomplete development of its Ethernet connection.

The firmware of the different FPGAs differs only by their port assignment but are otherwise identical.

The firmware must perform several functionalities.

The main tasks of the firmware are to configure the Citiroc1A ASICs, explained in Section 3.3, communication with the controlling computer via ethernet and the IPBUS protocol and a provisional readout of the time triggerd data from the Citiroc1A ASICs.

The firmware is written in VHSIC Hardware Description Language (VHDL) and is synthesized and implemented using Xilinx Vivado. Several IP-cores, provided by Xilinx, are used to simplfy the development of the firmware for several tasks like the implementation of the configuration memory.

4.1.1. The IPBUS Protocol

The IPBUS protocol used for the communication between the FPGA and the controlling computer is a simple protocol for controlling IP-aware hardware devices with a 32 bit read and write bus using UDP as the transport protocol.[\[12\]](#)

The IPBUS protocol defines a read and write command enabling successful write and read operations of a 32 bit register, with a 32 bit address in the FPGA.

The commands can be issued on the controlling computer with the μ HAL library, which allows the user to issue read and write commands using a python script and an XML file defining the addresses of the registers.[\[12\]](#)

The address space inside the FPGA is defined in the firmware. The address space is divided into separate address spaces for each of the slaves by the leading bits of the address. For some slaves, the address space is further divided into subspaces for the different registers of the slave.

4.1.2. The Firmware Structure

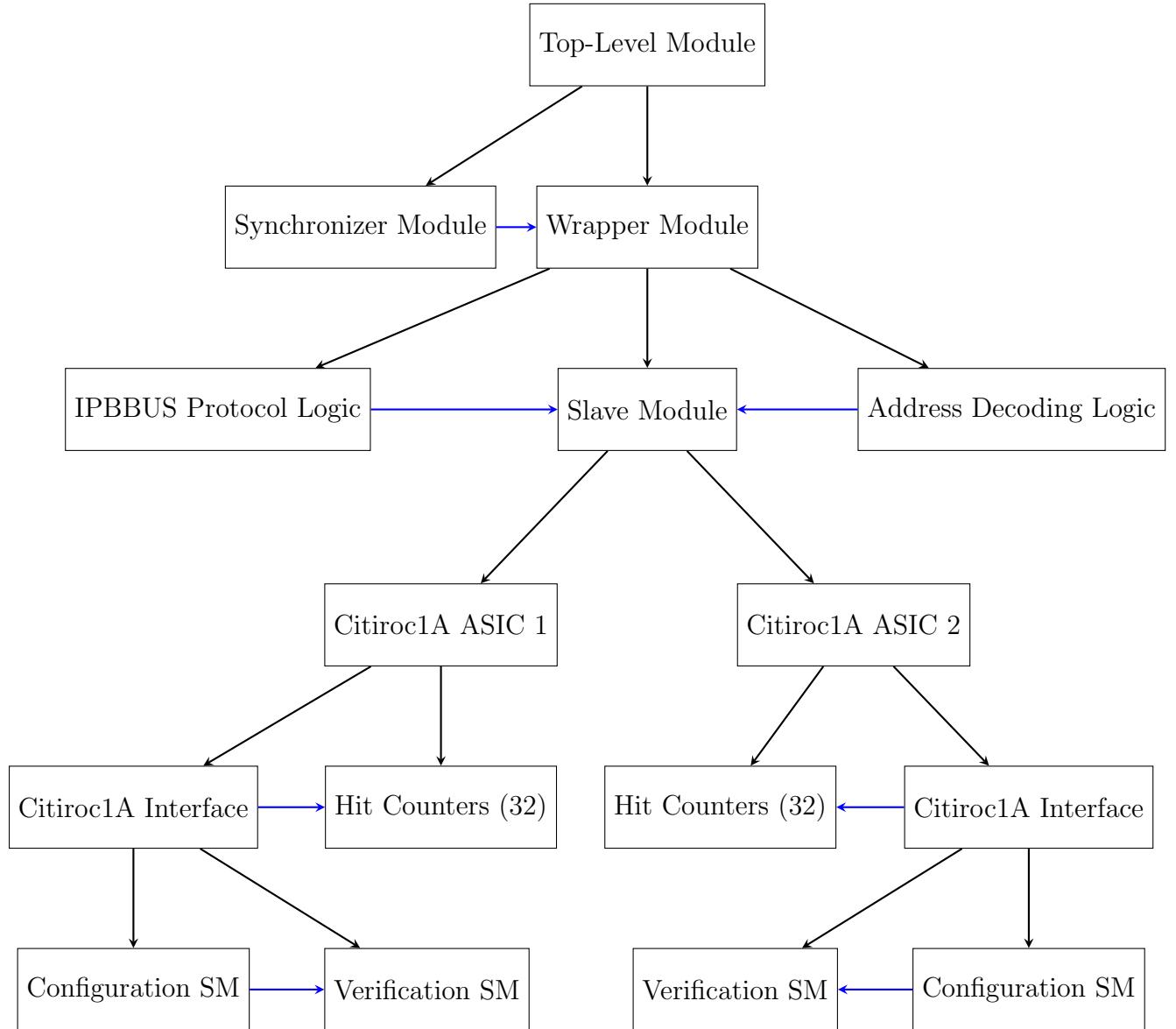


Figure 4.1.: Structure of the firmware developed for this thesis. The black arrows represent the true hierarchical connections between the modules, while the blue arrows indicate connections that are semantically correct but are routed through higher-level modules.

The firmware has a hierarchical structure illustrated in Figure 4.1.

The top level modul of the firmware contains the outgoing and incoming signals of the FPGA.

The top level modul instantiates a wrapper modul for the IPBUS protocol and the slave entities in addition to a synchronizer modul for the incoming time triggered Citiroc1A signals.

Bit	Description
bit 0	Selects between slow control (1) and probe register (0)
bit 1	Loads the configuration into the serial register
bit 2	Resets the Configuration and Verification SM and the Configuration RAM
bit 3	Resets the Citiroc1A serial register
bit 4	Loads the configuration into the slow control register
bit 5	Resets the hitcounters associated with the Citiroc1A
bit 6	Enables the hitcounters associated with the Citiroc1A

Figure 4.2.: Structure of the status and control register of the Citiroc1A interface. The specified commands are executed when the bits are set to 1.

The wrapper modul contains the IPBUS protocol logic and the address decoding logic as well as a modul containing the slaves.

The slave modul contains several slaves for the different tasks of the firmware. For each of the Citiroc1A ASICs, a Citiroc1A interface is instantiated for the configuration and verification of the ASIC, along with 32 hitcounters for the 32 channels of the Citiroc1A ASIC.

4.2. Configuration of the Citiroc1A ASIC

The configuration of the slow control and probe registers of the Citiroc1A ASIC, along with the verification of this configuration, is handled by two finite state machines.

Each state machine controls a random access memory (RAM) with a depth of 64 addresses, with each address storing 32 bits of data.

The state machiens in turn are controlled by the status and control register of the corresponding Citiroc1A Interface, which can be written by the controlling computer via the IPBUS protocol.

4.2.1. Status and Control Register

Each Citiroc1A interface has a 32 bit status and control register, but only the first 7 bits are used. It is responsible for the control of the configuration and verification state machines as well as the hitcounters. The bits of the status and control register, with the exception of bit 1, which is set to 0 by the FPGA after the configuration is loaded into the serial register, do not reset themselves after being set to 1 and have to be deaserted by the controlling computer.

Its structure is shown in Table 4.2.

4.2.2. Configuration State Machine

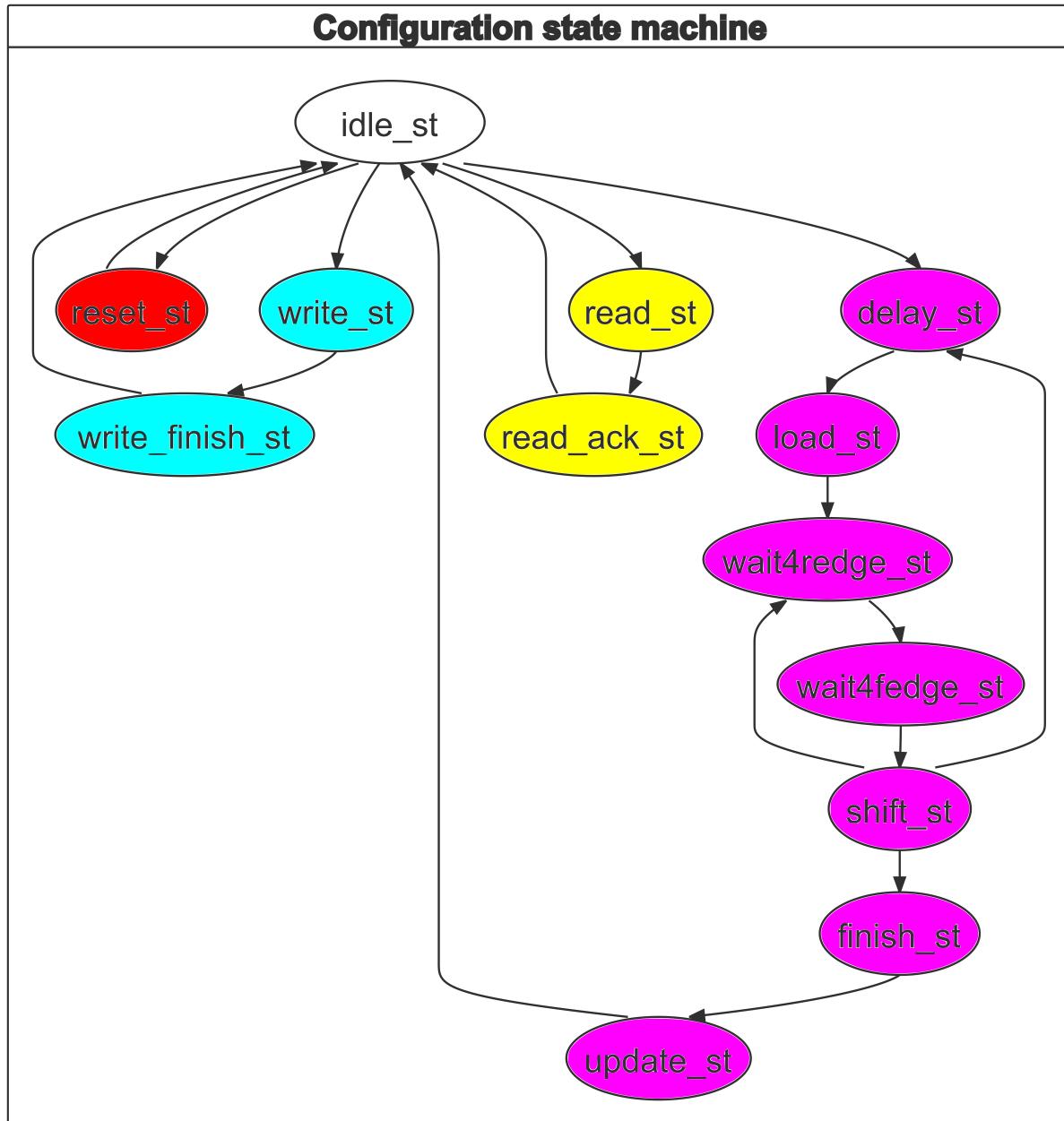


Figure 4.3.: Finite state machine for configuring the Citiroc1A ASIC. States associated with the same processes are highlighted using the same color.

The Configuration state machine, embedded in the firmware as shown in Figure 4.1, is responsible for configuring the slow control and probe registers of the Citiroc1A ASIC. The state machine is controlled by the status and control register, which is written by the controlling computer via the IPBUS protocol. It has four processes, whose states are shown in different colors in Figure 4.3.

The [write](#) process is responsible for writing the configuration data to the configuration

RAM. 32 bits can be written to a specified address in the configuration ram at a time by the controlling computer.

The `read` process allows the controlling computer to read the content of the configuration RAM at the specified address.

The `reset` process resets the configuration RAM and the Configuration state machine and is initiated by setting bit 2 of the status and control register to 1.

The `load` process loads the configuration data from the configuration RAM into the serial register of the Citiroc1A ASIC. The first 1144/256 bits of the configuration RAM are shifted into the serial register of the Citiroc1A ASIC, depending on the selected register. Each bit is shifted in by setting the data line `Srin.sr` and clock `clk` as described in Section 3.3. Since as described in Section 3.3 the first bit written to the serial register is the last bit of the configuration, the controlling computer has to write the bitstream in reverse order to the configuration RAM.

The `clk` clock signal for the ASIC's serial register is generated by the FPGA with a frequency of 1 MHz. The `load` process modulates this clock signal to control the operation of the serial register.

The process is repeated until all the data is shifted in and the configuration is loaded. It can be initiated by the controlling computer by setting bit 1 of the status and control register to 1 and is only interruptible by the `reset` process.

In order to load the configuration into the slow control register from the serial register, bit 4 of the status and control register must be set to 1, this is not necessary for the probe register.

4.2.3. Verification State Machine

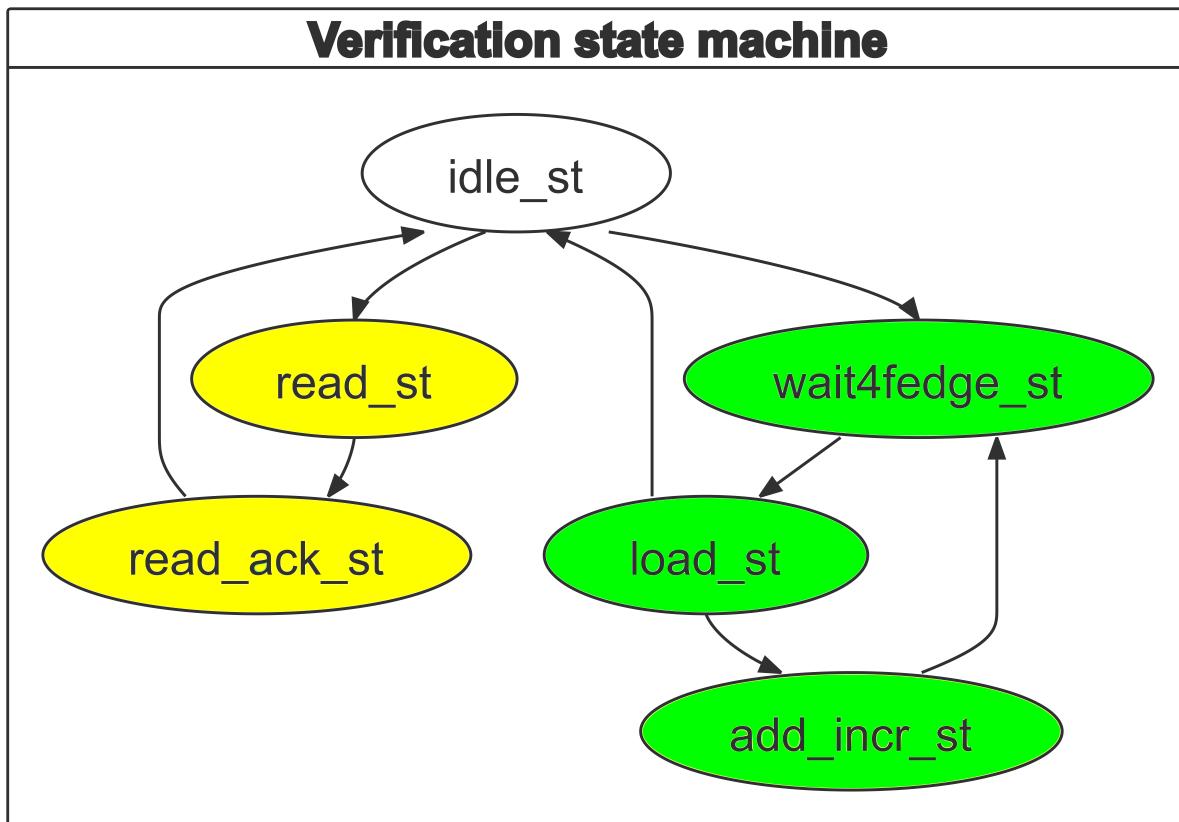


Figure 4.4.: Finite state machine for verifying the configuration of the Citiroc1A ASIC.
States belonging to the same processes are represented with the same color.

The Verification state machine, illustrated in Figure 4.4 is responsible for verifying the configuration of the Citiroc1A ASIC. It is incorporated into the firmware, as shown in Figure 4.1.

It can be reset by the controlling computer by setting bit 2 of the status and control register to 1.

If bits are shifted into the serial register of the Citiroc1A ASIC, the **verification** process is automatically started. The **sroute** signal coming back from the ASIC, explained in Section 3.3, is used to read back the shifted bits from the serial register of the Citiroc1A ASIC. The bits arrive at the FPGA in the same order as they were loaded in, but shifted by the length of the bitstream(1144/256). To compare the read back bits with the the loaded bits the bitstream has to be loaded twice.

The readback bits are stored in the verification RAM by the **verification** process and can be read by the controlling computer via the **read** process. This allows the controlling computer to compare the loaded bits with the read back bits and ensure that the configuration was loaded correctly into the serial register of the Citiroc1A ASIC.

4.3. The Provisional Readout

In addition to the configuration and verification of the configuration of Citroc1A ASIC, the firmware also provides a provisional readout in form of hitcounters and timecounters. The hitcounters are used to count the number of hits on each channel of the Citroc1A ASIC.

They are limited to a minimal time between hits of two periods of the synchronization clock. In this case a 325 MHz clock is used, which corresponds to a minimal time between hits of 6.16 ns.

Each Citroc1A has 32 hitcounters, one for each channel. The 32 bit hitcounters are enabled by setting bit 6 of the status and control register of the corresponding Citroc1A Interface to 1. This also enables the timecounter, which counts the number of clock cycles since it was last reset.

The hitcounters and timecounters are reset by setting bit 5 of the status and control register of the corresponding Citroc1A Interface to 1.

To read the hit and time counters, the controlling computer first has to disable the hitcounters by setting bit 6 of the status and control register to 0, in order to avoid metastability issues arising from the clock domain crossing. The hitcounters can then be read by the controlling computer via the IPBUS protocol.

The combination of the hitcounters and the timecounter allows the controlling computer to determine the number of hits per second on each channel of the Citroc1A ASIC.

4.4. Testing the Firmware

4.4.1. Setup for the Threshold Scan

The firmware will be evaluated through a threshold scan of the frontend electronics of the scintillating fiber hodoscope. This threshold scan will be performed with the SiPMs disconnected from the frontend electronics. The experimental setup is illustrated in Figure 4.5.

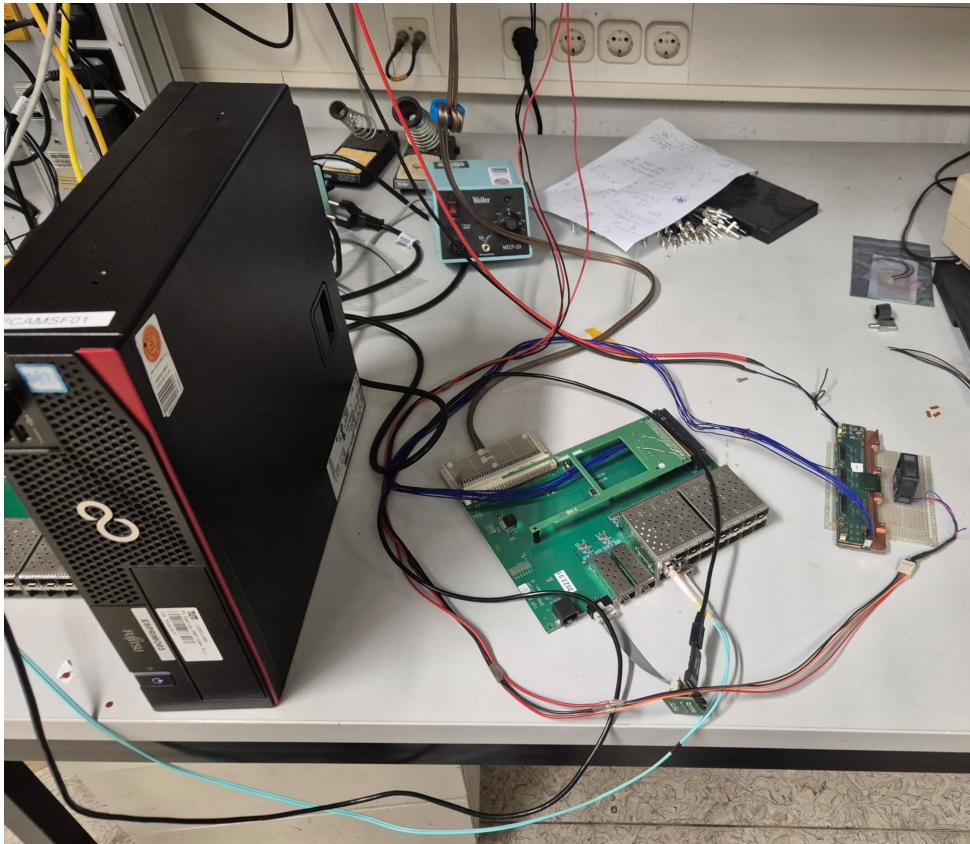


Figure 4.5.: Experimental setup for the threshold scan of the frontend electronics of the scintillating fiber hodoscope.

The scan will be performed by the controlling computer, which will scan through a range of thresholds of the time discriminator of the Citiroc1A ASIC and record the number of hits per second on each channel with an integration time of 400 ms. This scan will be performed for several different high gains near the maximum value of 62.

For comparison, the threshold scan will also be performed with the same configuration of the Citiroc1A ASICs on a testboard provided by Weeroc, with the setup shown in Figure 4.6.

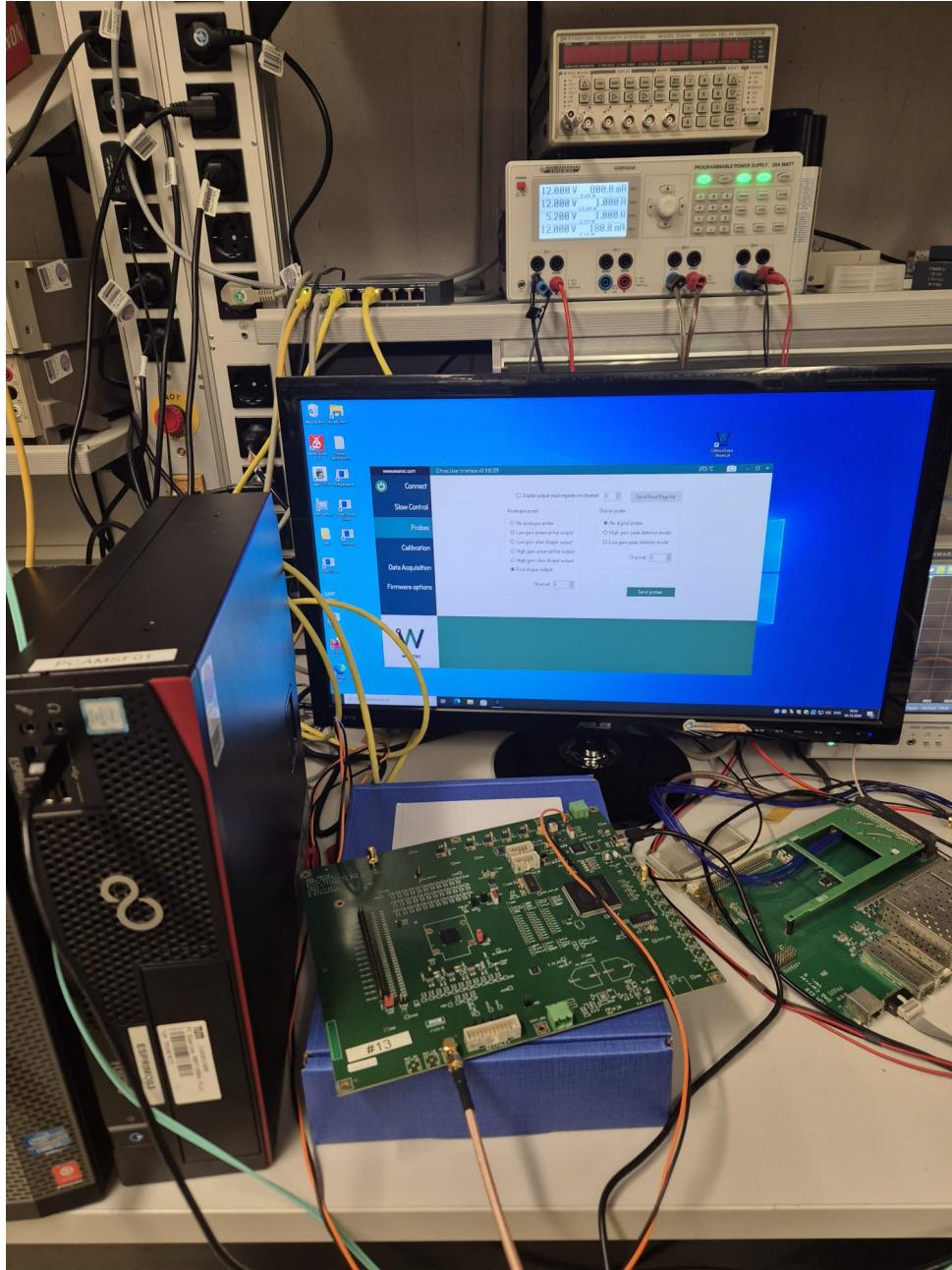


Figure 4.6.: Experimental setup for the threshold scan with a testboard provided by Weeroc.

4.4.2. Theoretical Background for the Threshold Scan

The noise on the unconnected frontend electronics is assumed to be of gaussian distribution,

$$P(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \quad (4.1)$$

where μ is the mean and σ the standard deviation of the noise.[10]

The number of hits per second on each channel of the Citiroc1A ASIC is assumed to be proportional to the number of noise events above the threshold of the time discriminator, but limited by the maximal trigger rate of the fast shaper Citiroc1A ASICs and thus only approximately proportional to the integral of the noise distribution above the threshold.[10]

The number of hits per second vs the threshold of the time discriminator is expected to follow an S-curve, which can be described by a modified error function,

$$N = \frac{A}{2} \left(1 - \operatorname{erf} \left(\frac{x - \mu}{\sqrt{2}\sigma} \right) \right) \quad (4.2)$$

where N is the number of hits per second, x the threshold of the time discriminator and A an renormalization factor.[10]

CHAPTER 5

Results

5.1. Threshold Scan Results

For the threshold scan, the threshold was scanned in steps of 1 for a range of high gains, starting with gain 58 and ending with the maximum gain of 62.

The number of hits was measured for each of the 32 channels of the Citiroc1A ASICs with an integration time of 400 ms. The threshold scan was performed for both the Citiroc1A ASICs of FPGA 1 and 2.

The results of the threshold scan are shown for the Citiroc1A ASICs of FPGA 1 and 2 for gains 58 to 62 in Figures 5.1, 5.2, 5.3, 5.4 and 5.5 respectively.

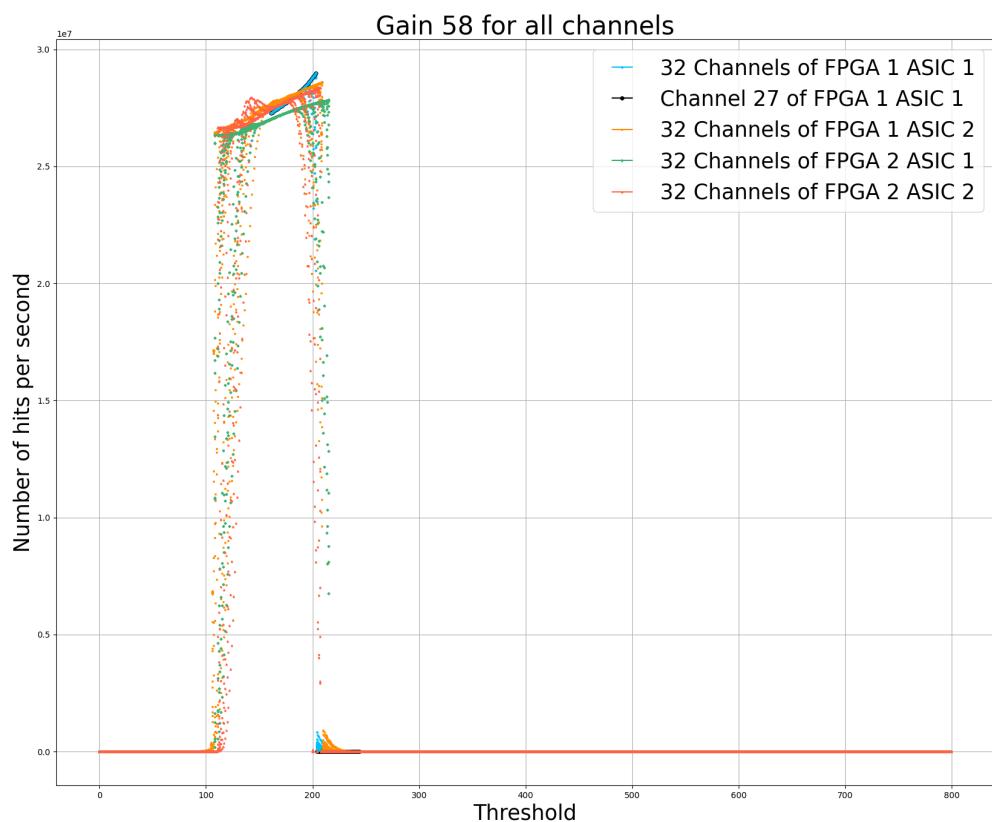


Figure 5.1.: Threshold scan of the Citiroc1A ASICs of FPGA 1 and 2 for gain 58 from threshold 0 to 800.

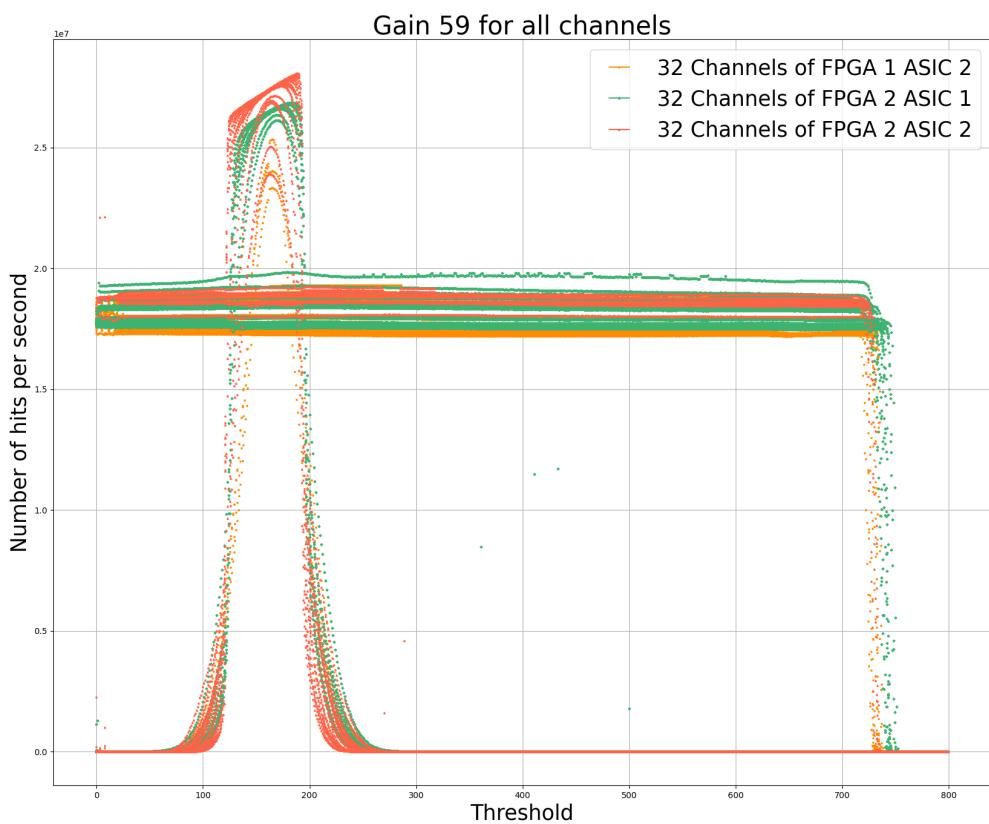


Figure 5.2.: Threshold scan of the Citiroc1A ASICs of FPGA 1 and 2 for gain 59 from threshold 0 to 800.

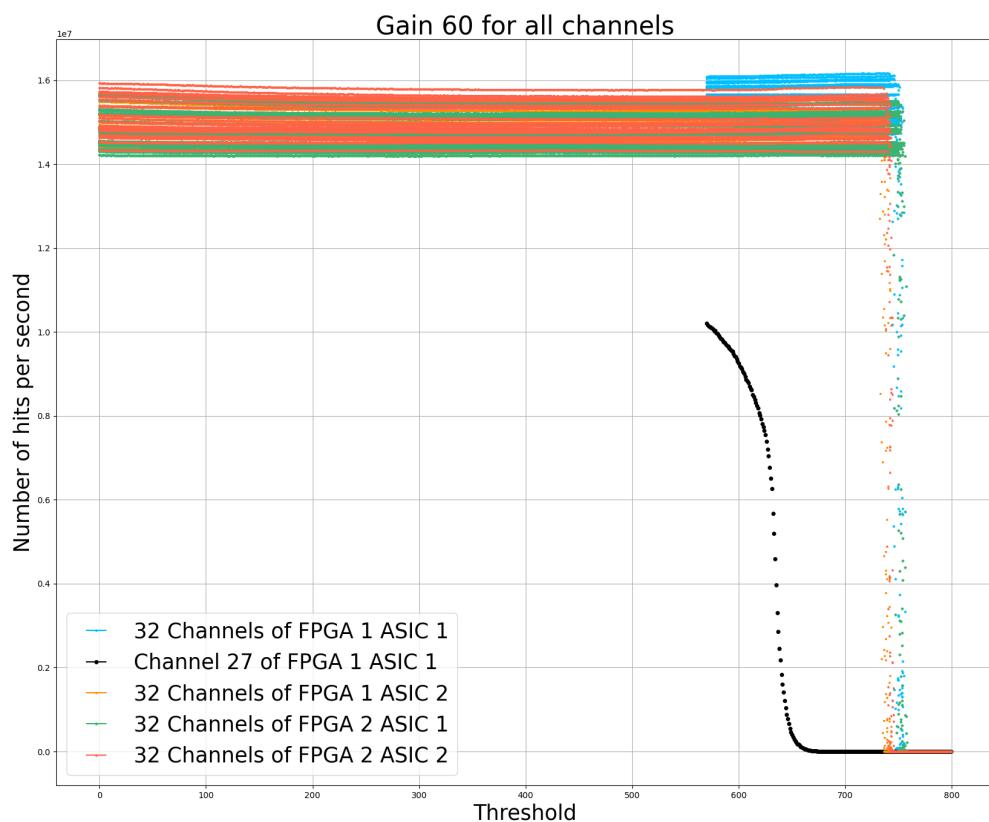


Figure 5.3.: Threshold scan of the Citiroc1A ASICs of FPGA 1 and 2 for gain 60 from threshold 0 to 800.

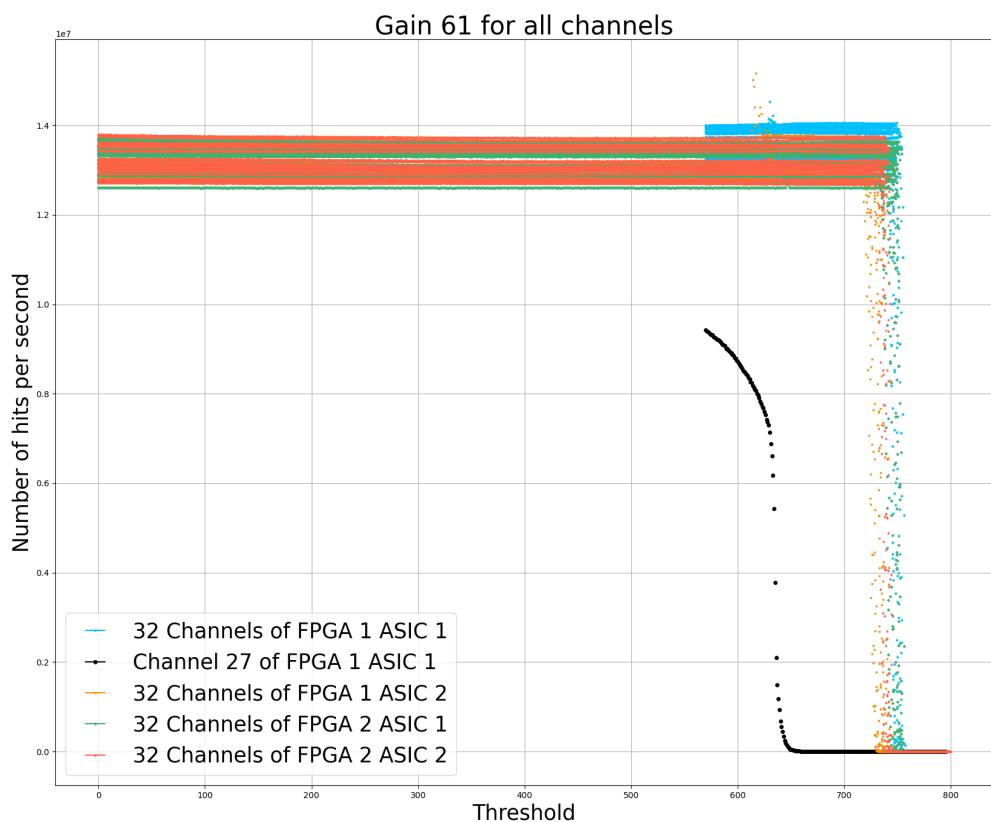


Figure 5.4.: Threshold scan of the Citiroc1A ASICs of FPGA 1 and 2 for gain 61 from threshold 0 to 800.

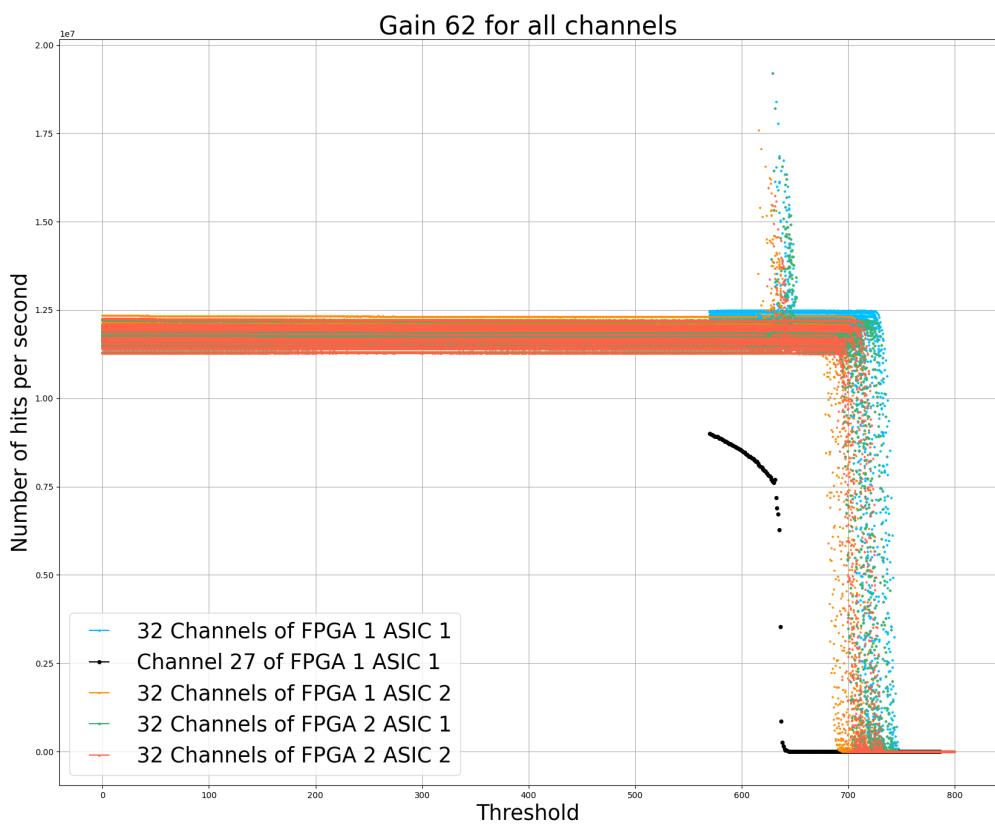


Figure 5.5.: Threshold scan of the Citiroc1A ASICs of FPGA 1 and 2 for gain 62 from threshold 0 to 800.

CHAPTER 6

Discussion

6.1. Firmware Evaluation

The threshold scan confirms that the firmware allows for the configuration of the Citiroc1A ASICs.

Furthermore, several tests were performed to verify successful configuration of the Citiroc1A ASICs by the FPGAs, such as disabling specific stages of the ASICs and routing probe signals using the probe register, as detailed in Section 3.3.2.

6.2. Frontend Electronics Characterization

6.2.1. Comparison with Testboard Measurements

A comparison of the threshold scan to one performed with the same configuration of the Citiroc1A ASIC on a by Weeroc provided testboard with gain 58 is shown in Figure 6.1.

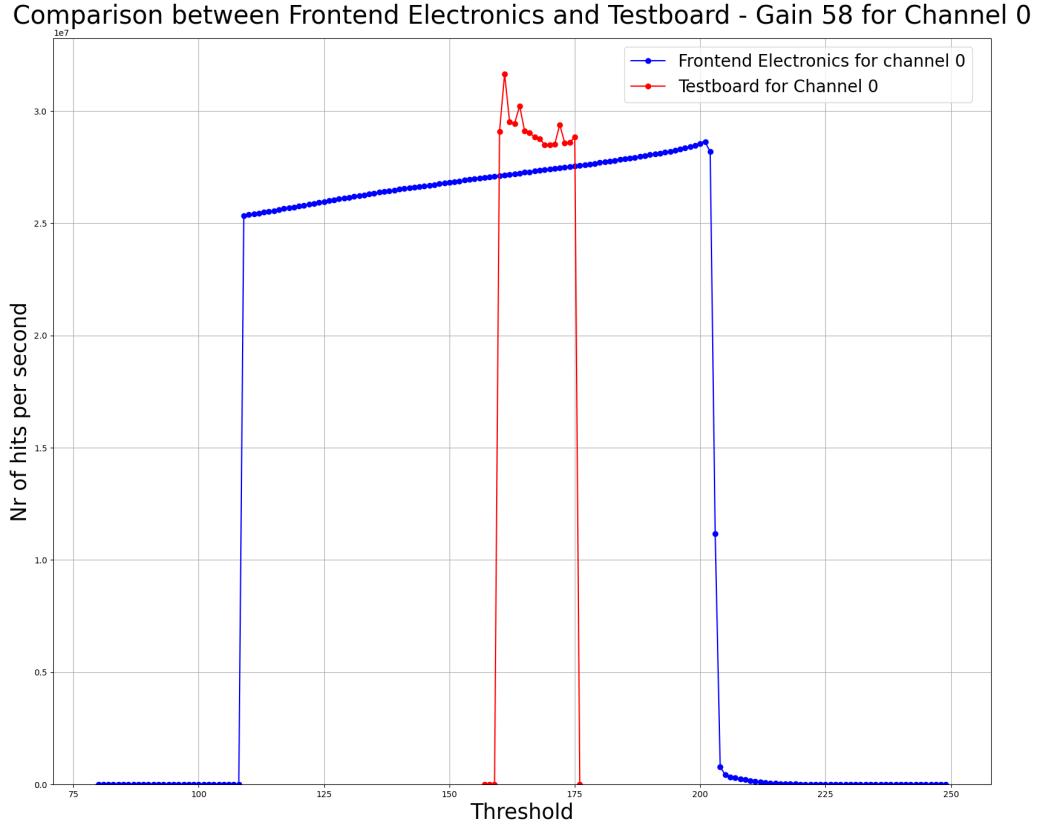


Figure 6.1.: Comparison of the threshold scan of the frontend electronics to the threshold scan performed on a by Weeroc provided testboard with a gain of 58.

The pedestal of the threshold scan performed with the frontend electronics is far larger than the pedestal of the threshold scan performed with the by testboard. This difference in the observed behavior of the frontend electronics can currently not be explained. The possibility of the Citiroc1A being wrongly configured was investigated and ruled out by testing for specific behaviors. Further tests with an oscilloscope probe showed significant high frequency noise on the input signals of the Citiroc1A ASICs, which could be the cause of the observed behaviour, but further investigation is required.(Old noise explanation new explanation needed)

6.2.2. S-curve Analysis

In order to determine the optimal threshold and characterize the noise of the Citiroc1A ASICs of FPGA 1 and 2, an S-curve analysis was performed.

The falling edge of the pedestal was fitted with the S-curve described in Section 4.4.2

6.2. Frontend Electronics Characterization

The results of the S-curve analysis are shown exemplary for channel 0 of Citiroc1A 1 of FPGA 1 with gain 60,61 and 62 in Figures 6.2, 6.3 and 6.4.

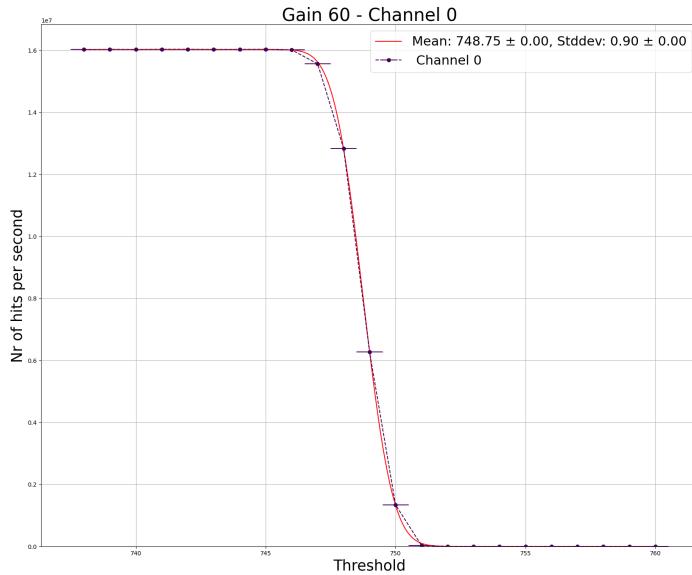


Figure 6.2.: Results of the S-curve analysis for channel 0 of Citiroc1A 1 of FPGA 1 with gain 60.

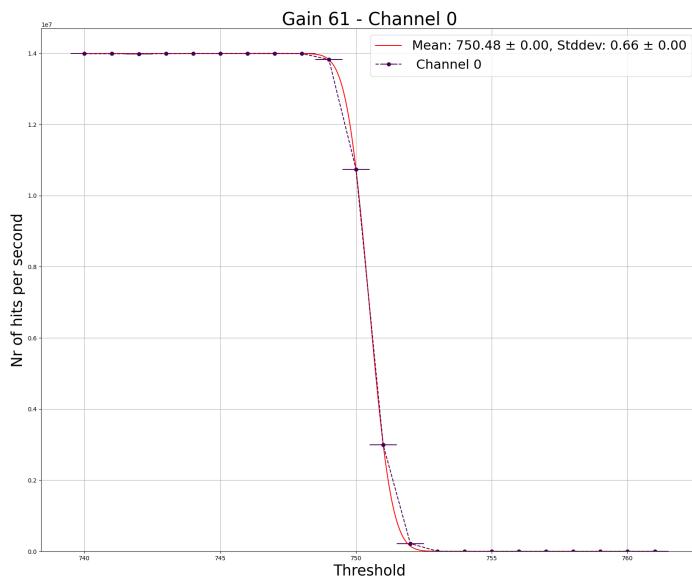


Figure 6.3.: Results of the S-curve analysis for channel 0 of Citiroc1A 1 of FPGA 1 with gain 61.

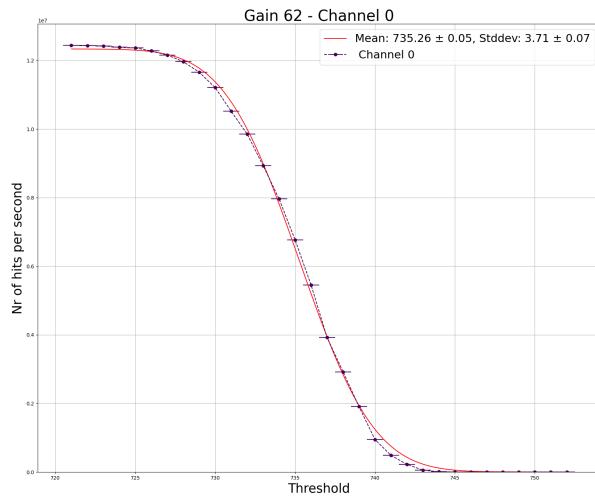


Figure 6.4.: Results of the S-curve analysis for channel 0 of Citiroc1A 1 of FPGA 1 with gain 62.

The S-curve fit, for all channels, for the high gain of 62 needed for the PRM experiment is shown in Figure 6.5.

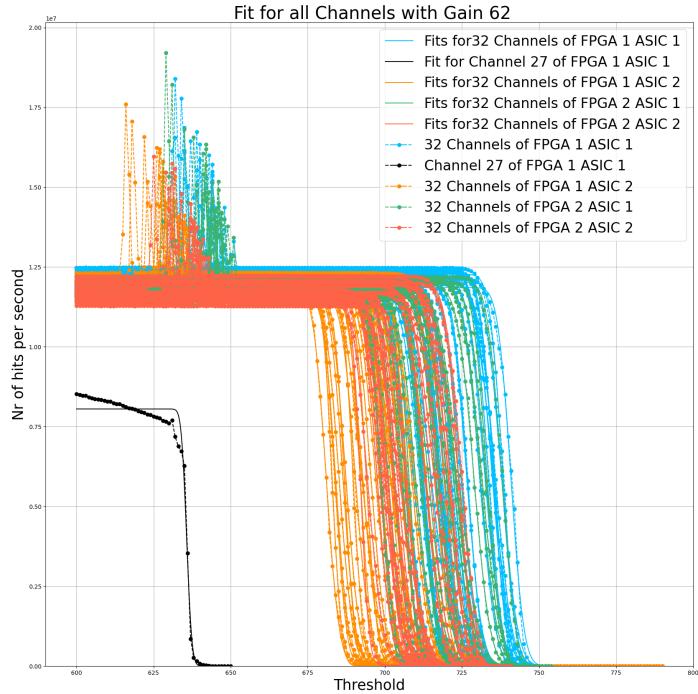


Figure 6.5.: Results of the S-curve analysis for all channels of the Citiroc1A ASICs of FPGA 1 and 2 with gain 62.

The mean μ and the standard deviation σ of the noise distribution that were determined from the S-curve fits are plotted against the gain for all channels in Figure 6.6.

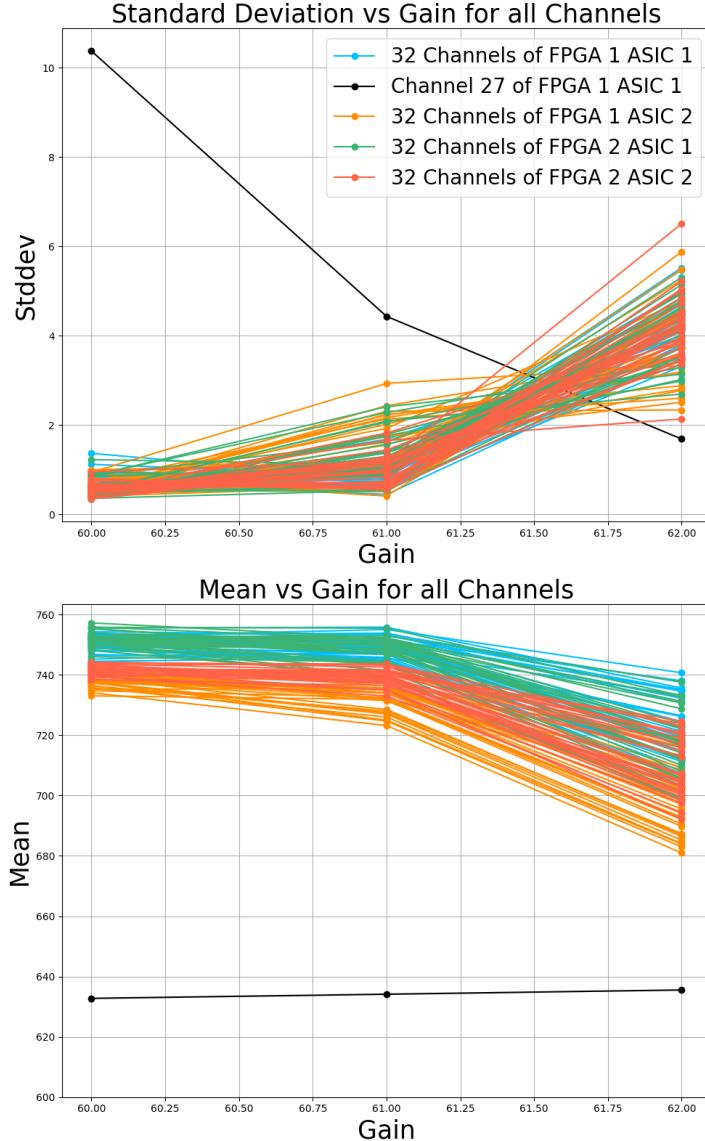


Figure 6.6.: Mean μ and standard deviation σ determined from the S-curve fits for all channels of the Citiroc1A ASICs of FPGA 1 and 2 plotted vs the gain.

6.2.3. Behaviour at different Gain Setting

The threshold scan of the Citiroc1A ASICs in the frontend electronics shows different behaviour for gain ranges of 0 to 58 (5.1) and 60 to 62 (5.3, 5.4 and 5.5), with the threshold scan at gain 59 showing a transition between the two behaviours depicted in Figure 5.2. This difference is also currently not understood and is suspected to have the same cause as the difference in the threshold scan compared to the testboard measurements.

A general trend of the standard deviation σ of the S-curve increasing and the mean μ decreasing with higher gain is observed.

6.2.4. Channel Behaviour Analysis

From the S-curve analysis it can be observed that the channels of the Citiroc1A ASICs show different behaviour in the threshold scan.

Especially channel 27 of Citiroc1A 1 of FPGA 1 shows a significantly different behaviour compared to the other channels, as can be seen in Figure 6.6 and in the results of the threshold scan shown in the Figures 5.3, 5.4 and 5.5.

Furthermore, for the threshold scan with gain 59 depicted in Figure 5.2 , all the channels show diverging behavior, this is also suspected to be because of the transition between the two gain regions.

The behavior of channel 27 of Citiroc1A 1 of FPGA 1 seems to have a different cause than the gain transition and needs further investigation. This could be investigated by performing a threshold scan with another FEE PCB and comparing the results.

6.2.5. Summary of the Characterisation

The threshold scan and the S-curve analysis show that the frontend electronics of the SFH are not performing as desired. Due to this, a calibration of the individual channels of the frontend electronics is not yet possible. The cause of the observed behaviour is currently not understood and further investigation is required, but a possible cause could be high frequency noise on the input signals of the Citiroc1A ASICs causing some unknown behaviour of the ASIC. Furthermore, the behaviour of channel 27 of Citiroc1A 1 of FPGA 1 seems to have a different cause than the gain transition and also needs further investigation.

CHAPTER 7

Conclusion and Outlook

7.1. Conclusion

In this thesis, the firmware for two of the three FPGAs of the frontend electronics of the scintillating fiber hodoscope (SFH) responsible for the control and provisional readout of the Citroc1A ASICs was developed and tested. For this, the firmware was hierarchically structured into different modules, responsible for the configuration of the Citroc1A ASICs, communication with the controlling computer and the readout of the ASICs and developed in VHDL using Xilinx Vivado. The firmware was tested by characterizing the frontend electronics with a threshold scan and an S-curve analysis. The threshold scan shows that the Citroc1A ASICs can be successfully configured, but that the frontend electronics show abnormal behaviour. This could be due to high frequency noise causing some unexpected behavior in the Citroc1A ASICs, but this has to be investigated further. We conclude that the developed firmware allows for the configuration and provisional readout of the Citroc1A ASICs, but that the frontend electronics of the SFH are not performing as desired.

7.2. Outlook

The next steps in the development of the frontend electronics for the SFH are, the development of the firmware for the third FPGA, the integration of this part of the firmware with the rest of the frontend electronics and the final readout of the SFH. Moreover, additional investigation into the abnormal behaviour of the frontend electronics observed during the threshold scan is required.

Chapter 7. Conclusion and Outlook

This could be accomplished using the internal probing capabilities of the Citiroc1A ASICs. Furthermore more tests with different FEE PCBs could be performed to investigate the origin of the observed behaviour.

By conducting these proposed steps and completing the development of the frontend electronics, the scintillating fiber hodoscope will be one step closer to being fully operational and performing its role in the PRM experiment and solving the proton radius puzzle.

APPENDIX A

Configurable registers of the Citiroc1A ASIC

Table A.1.: Configurable registers of the slow control register[7]

Field	Bits	Default	Position	Description
Register:channel_thr_time				
ch_0	4	0	0	Channel-dependent 4-bit threshold for time discriminator.
:				
ch_31	4	0	-	-
Register:channel_thr_charge				
ch_0	4	0	128	Channel-dependent 4-bit threshold for charge discriminator.
:				
ch_31	4	0	-	-
Register:discriminator_power				
discriminator_charge_en	1	0	256	Enable charge discriminator.
discriminator_charge_pp	1	0	-	Power pulse for charge discriminator.
discriminator_latched_output	1	0	-	1: latched, 0: direct output.

Configurable registers of the slow control register continued on next page

Appendix A. Configurable registers of the Citiroc1A ASIC

Field	Bits	Default	Position	Description
discriminator_time_en	1	1	-	Enable time discriminator.
discriminator_time_pp	1	1	-	Power pulse for time discriminator.
4bit_dac_charge_en	1	0	261	Enable 4-bit charge DAC.
4bit_dac_charge_pp	1	0	-	Power pulse for 4-bit charge DAC.
4bit_dac_time_en	1	1	-	Enable 4-bit time DAC.
4bit_dac_time_pp	1	1	-	Power pulse for 4-bit time DAC.
ch_0	1	1	265	0: masked, 1: unmasked.
:				
ch_31	1	1	-	-
Register:track_and_hold_power				
high_gain_pp	1	0	297	Enable high gain.
high_gain_en	1	0	-	-
low_gain_pp	1	0	-	Power pulse for low gain.
low_gain_en	1	0	-	Enable low gain.
weak_bias	1	0	-	1: weak bias (600kHz max), 0: high bias (5MHz max).
Register:peak_detector_power				
high_gain_pp	1	0	302	Enable high gain for peak detector.
high_gain_en	1	0	-	-
low_gain_pp	1	0	-	Power pulse for low gain.
low_gain_en	1	0	-	Enable low gain for peak detector.
Register:select_peak_sensing				
high_gain_th	1	0	306	0: peak detector, 1: track and hold.
low_gain_th	1	0	-	-
peak_sensing_cell_bypass	1	0	-	0: cell active, 1: bypass peak sensing cell.
peak_sensing_external_trigger	1	0	-	0: internal trigger, 1: external trigger.

Configurable registers of the slow control register continued on next page

Field	Bits	Default	Position	Description
Register:shaper				
fast_shaper_follower_pp	1	0	310	Power pulse for fast shaper follower.
fast_shaper_en	1	1	-	Enable fast shaper.
fast_shaper_pp	1	1	-	Power pulse for fast shaper.
low_gain_slow_shaper_pp	1	0	-	Power pulse for low gain slow shaper.
low_gain_slow_shaper_en	1	0	-	Enable low gain slow shaper.
low_gain_slow_shaper_time_const	3	0	-	See the table above for values.
high_gain_slow_shaper_pp	1	0	-	Power pulse for high gain slow shaper.
high_gain_slow_shaper_en	1	0	-	Enable high gain slow shaper.
high_gain_slow_shaper_time_const	3	0	-	See the table above for values.
Register:pre_amp_power				
low_gain_weak_bias	1	0	323	0: normal bias, 1: weak bias.
high_gain_pp	1	1	-	Power pulse for high gain preamp.
high_gain_en	1	1	-	Enable high gain preamp.
low_gain_pp	1	0	-	Power pulse for low gain preamp.
low_gain_en	1	0	-	Enable low gain preamp.
fast_shaper_low_gain	1	0	-	0: fast shaper on high gain.
Register:input_dac				
dac_en	1	1	329	Input DAC for bias correction.
dac_ref	1	1	-	Voltage ref: 1 = internal 4.5V, 0 = internal 2.5V, depends on vdd_dac.

Configurable registers of the slow control register continued on next page

Appendix A. Configurable registers of the Citiroc1A ASIC

Field	Bits	Default	Position	Description
ch_0	8	255	-	VSipm = V_HV - V_DAC (check what makes sense here).
ch_0_en	1	1	-	Enable channel 0 input DAC.
:				
ch_31	8	255	-	Same as ch_0 for channel 31.
ch_31_en	1	1	-	Enable channel 31 input DAC.
Register:channel_preamp				
ch_0_hg	6	62	619	High gain preamp setting.
ch_0_lg	6	0	-	Low gain preamp setting.
ch_0_ctest_hg	1	0	-	1: Connect injection capacitance for test signal.
ch_0_ctest_lg	1	0	-	1: Connect low gain injection capacitance.
ch_0_disable	1	0	-	1 disables preamp for channel 0.
:				
ch_31_hg	6	62	-	High gain preamp setting.
ch_31_lg	6	0	-	Low gain preamp setting.
ch_31_ctest_hg	1	0	-	1: Connect injection capacitance for test signal.
ch_31_ctest_lg	1	0	-	1: Connect low gain injection capacitance.
ch_31_disable	1	0	-	1 disables preamp for channel 0.
Register:service_blocks				
temp_pp	1	1	999	Enable power pulse for temperature monitoring.
temp_en	1	1	-	Enable temperature monitoring.
band_gap_pp	1	1	-	Enable power pulse for band gap reference.

Configurable registers of the slow control register continued on next page

Field	Bits	Default	Position	Description
band_gap_en	1	1	-	Enable band gap reference.
Register:threshold_dac				
charge_dac_en	1	0	1103	Enable charge threshold DAC.
charge_dac_pp	1	0	-	Power pulse for charge threshold DAC.
time_dac_en	1	1	-	Enable time threshold DAC.
time_dac_pp	1	1	-	Power pulse for time threshold DAC.
charge_threshold	10	0	-	Charge threshold value.
time_threshold	10	-	-	Time threshold value (e.g., 200 for 1 cell min, 250 for 2 cells).
Register:otaq_power				
high_gain_en	1	1	1127	Enable high gain for OTAQ.
high_gain_pp	1	1	-	Power pulse for high gain OTAQ.
low_gain_en	1	0	-	Enable low gain for OTAQ.
low_gain_pp	1	0	-	Power pulse for low gain OTAQ.
debug_probe_en	1	1	-	Enable debug probe.
debug_probe_pp	1	1	-	Power pulse for debug probe.
Register:input_output				
output_buffer_bias	1	0	1133	Output OTA buffer bias: 0 = auto bias, 1 = force on.
val_event_receiver_en	1	1	-	Enable validation event receiver.
val_event_receiver_pp	1	1	-	Power pulse for validation event receiver.
raz_chn_en	1	1	-	Enable RAZ channel.
raz_chn_pp	1	1	-	Power pulse for RAZ channel.

Configurable registers of the slow control register continued on next page

Appendix A. Configurable registers of the Citiroc1A ASIC

Field	Bits	Default	Position	Description
digital_output_en	1	1	-	Enable digital multiplexed output.
or32_output_en	1	1	-	Enable OR32 output.
or32_oc_output_en	1	1	-	Enable OR32 over-current output.
trigger_polarity	1	0	-	Trigger polarity: 0 = positive (rising edge), 1 = negative (falling edge).
or32_t_oc_en	1	1	-	Enable OR32 timeout over-current.
32_triggers_en	1	1	1143	Enable 32 triggers.

Table A.2.: Configurable registers of the probe register[7]

Register	Field	Bits	Position	Type
out_probe_fast_shaper	ch_0 ⋮ ch_31	1 ⋮ 1	0 ⋮ 31	Analog - Out_probe
out_probe_slow_shaper_lg	ch_0 ⋮ ch_31	1 ⋮ 1	32 ⋮ 63	Analog - Out_probe
digital_probe_peak_sense_lg	ch_0 ⋮ ch_31	1 ⋮ 1	64 ⋮ 95	Digital - Digital_probe
out_probe_slow_shaper_hg	ch_0 ⋮ ch_31	1 ⋮ 1	96 ⋮ 127	Analog - Out_probe
digital_probe_peak_sense_hg	ch_0 ⋮ ch_31	1 ⋮ 1	128 ⋮ 159	Digital - Digital_probe
out_probe_preamp_hg	ch_0 ⋮ ch_31	1 ⋮ 1	160 ⋮ 191	Analog - Out_probe
out_probe_preamp_lg	ch_0 ⋮ ch_31	1 ⋮ 1	192 ⋮ 223	Analog - Out_probe
input_dac_probe	ch_0 ⋮ ch_31	1 ⋮ 1	224 ⋮ 255	Analog - Out_probe_dac_5V

APPENDIX B

Fit parameters of the S-curve analysis

gain	FPGA 1	FPGA 2	Citiroc1A	Channel	μ	σ	FPGA 1	FPGA 2	Citiroc1A	Channel	μ	σ
60	ch_0	NAN	NAN	ch_0	NAN	NAN	ch_0	NAN	NAN	ch_0	NAN	NAN
	ch_1	NAN	NAN	ch_1	NAN	NAN	ch_1	NAN	NAN	ch_1	NAN	NAN
	ch_2	NAN	NAN	ch_2	NAN	NAN	ch_2	NAN	NAN	ch_2	NAN	NAN
	ch_3	NAN	NAN	ch_3	NAN	NAN	ch_3	NAN	NAN	ch_3	NAN	NAN
	ch_4	NAN	NAN	ch_4	NAN	NAN	ch_4	NAN	NAN	ch_4	NAN	NAN
	ch_5	NAN	NAN	ch_5	NAN	NAN	ch_5	NAN	NAN	ch_5	NAN	NAN
	ch_6	NAN	NAN	ch_6	NAN	NAN	ch_6	NAN	NAN	ch_6	NAN	NAN
	ch_7	NAN	NAN	ch_7	NAN	NAN	ch_7	NAN	NAN	ch_7	NAN	NAN
	ch_8	NAN	NAN	ch_8	NAN	NAN	ch_8	NAN	NAN	ch_8	NAN	NAN
	ch_9	NAN	NAN	ch_9	NAN	NAN	ch_9	NAN	NAN	ch_9	NAN	NAN
	ch_10	NAN	NAN	ch_10	NAN	NAN	ch_10	NAN	NAN	ch_10	NAN	NAN
	ch_11	NAN	NAN	ch_11	NAN	NAN	ch_11	NAN	NAN	ch_11	NAN	NAN
	ch_12	NAN	NAN	ch_12	NAN	NAN	ch_12	NAN	NAN	ch_12	NAN	NAN
	ch_13	NAN	NAN	ch_13	NAN	NAN	ch_13	NAN	NAN	ch_13	NAN	NAN
	ch_14	NAN	NAN	ch_14	NAN	NAN	ch_14	NAN	NAN	ch_14	NAN	NAN
	ch_15	NAN	NAN	ch_15	NAN	NAN	ch_15	NAN	NAN	ch_15	NAN	NAN
	ch_16	NAN	NAN	ch_16	NAN	NAN	ch_16	NAN	NAN	ch_16	NAN	NAN
	ch_17	NAN	NAN	ch_17	NAN	NAN	ch_17	NAN	NAN	ch_17	NAN	NAN
	ch_18	NAN	NAN	ch_18	NAN	NAN	ch_18	NAN	NAN	ch_18	NAN	NAN
	ch_19	NAN	NAN	ch_19	NAN	NAN	ch_19	NAN	NAN	ch_19	NAN	NAN
	ch_20	NAN	NAN	ch_20	NAN	NAN	ch_20	NAN	NAN	ch_20	NAN	NAN
	ch_21	NAN	NAN	ch_21	NAN	NAN	ch_21	NAN	NAN	ch_21	NAN	NAN
	ch_22	NAN	NAN	ch_22	NAN	NAN	ch_22	NAN	NAN	ch_22	NAN	NAN
	ch_23	NAN	NAN	ch_23	NAN	NAN	ch_23	NAN	NAN	ch_23	NAN	NAN
	ch_24	NAN	NAN	ch_24	NAN	NAN	ch_24	NAN	NAN	ch_24	NAN	NAN
	ch_25	NAN	NAN	ch_25	NAN	NAN	ch_25	NAN	NAN	ch_25	NAN	NAN
	ch_26	NAN	NAN	ch_26	NAN	NAN	ch_26	NAN	NAN	ch_26	NAN	NAN
	ch_27	NAN	NAN	ch_27	NAN	NAN	ch_27	NAN	NAN	ch_27	NAN	NAN
	ch_28	NAN	NAN	ch_28	NAN	NAN	ch_28	NAN	NAN	ch_28	NAN	NAN
	ch_29	NAN	NAN	ch_29	NAN	NAN	ch_29	NAN	NAN	ch_29	NAN	NAN
	ch_30	NAN	NAN	ch_30	NAN	NAN	ch_30	NAN	NAN	ch_30	NAN	NAN
	ch_31	NAN	NAN	ch_31	NAN	NAN	ch_31	NAN	NAN	ch_31	NAN	NAN

Table B.1.: Mean μ and standard deviation σ of the noise distribution gained from the fit of S-curve for gain 60. ASIC 1 and ASIC 2 are the Citiroc1A ASICs of FPGA 1 and ASIC 3 and ASIC 4 are the Citiroc1A ASICs of FPGA 2

Appendix B. Fit parameters of the S-curve analysis

gain	FPGA 1	FPGA 2	Citiroc1A	Channel	μ	σ	FPGA 1	FPGA 2	Citiroc1A	Channel	μ	σ
61	ch_0	NAN	NAN	ch_0	NAN	NAN	ch_0	NAN	NAN	ch_0	NAN	NAN
	ch_1	NAN	NAN	ch_1	NAN	NAN	ch_1	NAN	NAN	ch_1	NAN	NAN
	ch_2	NAN	NAN	ch_2	NAN	NAN	ch_2	NAN	NAN	ch_2	NAN	NAN
	ch_3	NAN	NAN	ch_3	NAN	NAN	ch_3	NAN	NAN	ch_3	NAN	NAN
	ch_4	NAN	NAN	ch_4	NAN	NAN	ch_4	NAN	NAN	ch_4	NAN	NAN
	ch_5	NAN	NAN	ch_5	NAN	NAN	ch_5	NAN	NAN	ch_5	NAN	NAN
	ch_6	NAN	NAN	ch_6	NAN	NAN	ch_6	NAN	NAN	ch_6	NAN	NAN
	ch_7	NAN	NAN	ch_7	NAN	NAN	ch_7	NAN	NAN	ch_7	NAN	NAN
	ch_8	NAN	NAN	ch_8	NAN	NAN	ch_8	NAN	NAN	ch_8	NAN	NAN
	ch_9	NAN	NAN	ch_9	NAN	NAN	ch_9	NAN	NAN	ch_9	NAN	NAN
	ch_10	NAN	NAN	ch_10	NAN	NAN	ch_10	NAN	NAN	ch_10	NAN	NAN
	ch_11	NAN	NAN	ch_11	NAN	NAN	ch_11	NAN	NAN	ch_11	NAN	NAN
	ch_12	NAN	NAN	ch_12	NAN	NAN	ch_12	NAN	NAN	ch_12	NAN	NAN
	ch_13	NAN	NAN	ch_13	NAN	NAN	ch_13	NAN	NAN	ch_13	NAN	NAN
	ch_14	NAN	NAN	ch_14	NAN	NAN	ch_14	NAN	NAN	ch_14	NAN	NAN
	ch_15	NAN	NAN	ch_15	NAN	NAN	ch_15	NAN	NAN	ch_15	NAN	NAN
	ch_16	NAN	NAN	ch_16	NAN	NAN	ch_16	NAN	NAN	ch_16	NAN	NAN
	ch_17	NAN	NAN	ch_17	NAN	NAN	ch_17	NAN	NAN	ch_17	NAN	NAN
	ch_18	NAN	NAN	ch_18	NAN	NAN	ch_18	NAN	NAN	ch_18	NAN	NAN
	ch_19	NAN	NAN	ch_19	NAN	NAN	ch_19	NAN	NAN	ch_19	NAN	NAN
	ch_20	NAN	NAN	ch_20	NAN	NAN	ch_20	NAN	NAN	ch_20	NAN	NAN
	ch_21	NAN	NAN	ch_21	NAN	NAN	ch_21	NAN	NAN	ch_21	NAN	NAN
	ch_22	NAN	NAN	ch_22	NAN	NAN	ch_22	NAN	NAN	ch_22	NAN	NAN
	ch_23	NAN	NAN	ch_23	NAN	NAN	ch_23	NAN	NAN	ch_23	NAN	NAN
	ch_24	NAN	NAN	ch_24	NAN	NAN	ch_24	NAN	NAN	ch_24	NAN	NAN
	ch_25	NAN	NAN	ch_25	NAN	NAN	ch_25	NAN	NAN	ch_25	NAN	NAN
	ch_26	NAN	NAN	ch_26	NAN	NAN	ch_26	NAN	NAN	ch_26	NAN	NAN
	ch_27	NAN	NAN	ch_27	NAN	NAN	ch_27	NAN	NAN	ch_27	NAN	NAN
	ch_28	NAN	NAN	ch_28	NAN	NAN	ch_28	NAN	NAN	ch_28	NAN	NAN
	ch_29	NAN	NAN	ch_29	NAN	NAN	ch_29	NAN	NAN	ch_29	NAN	NAN
	ch_30	NAN	NAN	ch_30	NAN	NAN	ch_30	NAN	NAN	ch_30	NAN	NAN
	ch_31	NAN	NAN	ch_31	NAN	NAN	ch_31	NAN	NAN	ch_31	NAN	NAN

Table B.2.: Mean μ and standard deviation σ of the noise distribution gained from the fit of S-curve for gain 61. ASIC 1 and ASIC 2 are the Citiroc1A ASICs of FPGA 1 and ASIC 3 and ASIC 4 are the Citiroc1A ASICs of FPGA 2

gain	FPGA 1	FPGA 2	Citiroc1A	Channel	μ	σ	FPGA 1	FPGA 2	Citiroc1A	Channel	μ	σ
62	ch_0	NAN	NAN	ch_0	NAN	NAN	ch_0	NAN	NAN	ch_0	NAN	NAN
	ch_1	NAN	NAN	ch_1	NAN	NAN	ch_1	NAN	NAN	ch_1	NAN	NAN
	ch_2	NAN	NAN	ch_2	NAN	NAN	ch_2	NAN	NAN	ch_2	NAN	NAN
	ch_3	NAN	NAN	ch_3	NAN	NAN	ch_3	NAN	NAN	ch_3	NAN	NAN
	ch_4	NAN	NAN	ch_4	NAN	NAN	ch_4	NAN	NAN	ch_4	NAN	NAN
	ch_5	NAN	NAN	ch_5	NAN	NAN	ch_5	NAN	NAN	ch_5	NAN	NAN
	ch_6	NAN	NAN	ch_6	NAN	NAN	ch_6	NAN	NAN	ch_6	NAN	NAN
	ch_7	NAN	NAN	ch_7	NAN	NAN	ch_7	NAN	NAN	ch_7	NAN	NAN
	ch_8	NAN	NAN	ch_8	NAN	NAN	ch_8	NAN	NAN	ch_8	NAN	NAN
	ch_9	NAN	NAN	ch_9	NAN	NAN	ch_9	NAN	NAN	ch_9	NAN	NAN
	ch_10	NAN	NAN	ch_10	NAN	NAN	ch_10	NAN	NAN	ch_10	NAN	NAN
	ch_11	NAN	NAN	ch_11	NAN	NAN	ch_11	NAN	NAN	ch_11	NAN	NAN
	ch_12	NAN	NAN	ch_12	NAN	NAN	ch_12	NAN	NAN	ch_12	NAN	NAN
	ch_13	NAN	NAN	ch_13	NAN	NAN	ch_13	NAN	NAN	ch_13	NAN	NAN
	ch_14	NAN	NAN	ch_14	NAN	NAN	ch_14	NAN	NAN	ch_14	NAN	NAN
	ch_15	NAN	NAN	ch_15	NAN	NAN	ch_15	NAN	NAN	ch_15	NAN	NAN
	ch_16	NAN	NAN	ch_16	NAN	NAN	ch_16	NAN	NAN	ch_16	NAN	NAN
	ch_17	NAN	NAN	ch_17	NAN	NAN	ch_17	NAN	NAN	ch_17	NAN	NAN
	ch_18	NAN	NAN	ch_18	NAN	NAN	ch_18	NAN	NAN	ch_18	NAN	NAN
	ch_19	NAN	NAN	ch_19	NAN	NAN	ch_19	NAN	NAN	ch_19	NAN	NAN
	ch_20	NAN	NAN	ch_20	NAN	NAN	ch_20	NAN	NAN	ch_20	NAN	NAN
	ch_21	NAN	NAN	ch_21	NAN	NAN	ch_21	NAN	NAN	ch_21	NAN	NAN
	ch_22	NAN	NAN	ch_22	NAN	NAN	ch_22	NAN	NAN	ch_22	NAN	NAN
	ch_23	NAN	NAN	ch_23	NAN	NAN	ch_23	NAN	NAN	ch_23	NAN	NAN
	ch_24	NAN	NAN	ch_24	NAN	NAN	ch_24	NAN	NAN	ch_24	NAN	NAN
	ch_25	NAN	NAN	ch_25	NAN	NAN	ch_25	NAN	NAN	ch_25	NAN	NAN
	ch_26	NAN	NAN	ch_26	NAN	NAN	ch_26	NAN	NAN	ch_26	NAN	NAN
	ch_27	NAN	NAN	ch_27	NAN	NAN	ch_27	NAN	NAN	ch_27	NAN	NAN
	ch_28	NAN	NAN	ch_28	NAN	NAN	ch_28	NAN	NAN	ch_28	NAN	NAN
	ch_29	NAN	NAN	ch_29	NAN	NAN	ch_29	NAN	NAN	ch_29	NAN	NAN
	ch_30	NAN	NAN	ch_30	NAN	NAN	ch_30	NAN	NAN	ch_30	NAN	NAN
	ch_31	NAN	NAN	ch_31	NAN	NAN	ch_31	NAN	NAN	ch_31	NAN	NAN

Table B.3.: Mean μ and standard deviation σ of the noise distribution gained from the fit of S-curve for gain 62. ASIC 1 and ASIC 2 are the Citiroc1A ASICs of FPGA 1 and ASIC 3 and ASIC 4 are the Citiroc1A ASICs of FPGA 2

APPENDIX C

Code

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1 this is code
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