MAE de la partie Réception Rst **E9 E0** RxError = '0'Data out <= reg Rx = 0DataValid = '1' **E1** Clr = '1' Rx = '1'i = 0DataValid = '0' **E8** RxError = '1' **E7** Rx = '0'**E2** CIr = '0'Tick = '1' **E6** Tick = '1' **E3** reg(i) = RxTick = '1' i = 8j++ **E5 Entrées:** Tick = '1' Tick = '1' - Rx - Clk - Tick **E4** - Rst **Sorties:** - Data_out - Data_valid Signaux: - Signal reg : std_logic_vector(7 downto 0)

- Signal i : natural := '0'

- RxError

- Clr