Interfacing the ADS8361 to the TMS320VC5416 DSP

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ABSTRACT

This application note presents a method for interfacing the ADS8361 16-bit SAR analog-to-digital converter to the TMS320VC5416™ DSP using McBSP1. The software developed reads 1024 samples continuously from the ADS8361. In an effort to reduce development time, the source code for this application note can be found on the Texas Instruments web site at http://www.ti.com. Search for document number SLAA162 from the home page and follow the links to down load the source code.

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1 Introduction

The ADS8361 is a 2+2 channel, 16-bit upgrade for the ADS7861 (12-bit) 2+2 channel analog-to-digital converters. The converter is able to gluelessly interface to the TMS320VC5416 digital signal processor (C5416™ DSP). For development of this application note, the TMS320VC5416™ DSP starter kit (DSK) and ADS8361EVM were used in conjunction with the DAP data acquisition system interface board.

2 Hardware

The combination of the TMS320VC5416™ DSK and the DAP data acquisition system interface board is a convenient way to experiment with interfacing the TMS320VC5416™ DSP to the ADS8361. The ADS8361EVM plugs onto the DAP data acquisition system interface board, which then plugs directly into the C5416™ DSK through mating connectors compatible with the TMS320™ cross-platform daughtercard interface *(SPRA711)* connectors found on the DSK platform.

2.1 TMS320VC5416 DSK

The TMS320VC5416™ DSP starter kit (DSK) not only provides an introduction to C5000™ DSP platform technology, but also is powerful enough to use for fast development of networking, communications, imaging and other applications like data acquisition. See TI's website (www.ti.com) for more information on the C5416™ DSK.

3 ADS8361EVM

The ADS8361 is a member of the motor control products family of serial ADCs available from Texas Instruments. The EVM provides a platform to demonstrate the functionality of the ADS8361 ADC with various Texas Instruments DSP's and microcontrollers, while allowing easy access to all analog and digital signals for customized end-user applications. For more information on the EVM, search for document number SLAU094 from the main page of the Texas Instruments website at http://www.ti.com.

3.1 Hardware Interface

The hardware interface is seamless between the C5416™ DSK and the ADS8361 EVM. The DAP data acquisition system interface board provides direct access to the C5416™ DSP McBSP ports (note: this report uses McBSP1). The hardware connections shown in Figure 1 are via the DAP data acquisition system interface board. The CLOCK, RD(+ CONVST), and SDA pins from the ADS8361 are connected to CLKX1, FSX1, and DRR1 pins of McBSP1 respectively. The chip select (CS) pin is grounded because only one A/D converter is placed on the port. If more than one device is on the bus, then chip select should be controlled by any available GPIO on the C5416™ DSK.

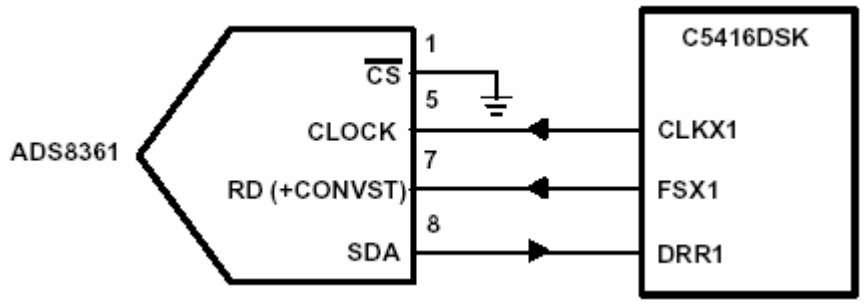

Figure 1. Hardware Interface Block Diagram

4 Software Interface

All of the software was written and compiled using Code Composer Studio™ version 2.10. The most involved portion of writing the code for this simple interface is programming the multichannel buffered serial port (McBSP).

4.1 McBSP Setting

The GUI interface of the configuration tool (i.e., CDB file); DSP/BIOS and CSL has made it easier than ever to write programs and set up the multichannel buffered serial port. To see how easy it is to set up the McBSP registers, double click on the *.cdb* file (in the code example provided, choose the ADS8361.CDB) from within the project window. Browse through the CDB tree, and find the McBSP configuration manger under CSL. Right click on *mcbspCfg1* and select *properties*. This is where the McBSP registers are found as tabs, with individual bit field settings found as pulldown options. After all options have been selected, click OK, and then choose *Rebuild All* from the *Project* pull down menu. Register options can be confirmed by opening the file ADS8361cfc_c.c under the *Generated Files* branch in the project manager window. The GUI-generated code for this application is shown below.

```
MCBSP_Config mcbspCfg1 = {
    0x0020,         /*  Serial Port Control Register 1   */
    0x02c0,         /*  Serial Port Control Register 2   */
    0x0060,         /*  Receive Control Register 1   */
    0x0044,         /*  Receive Control Register 2   */
    0x0000,         /*  Transmit Control Register 1   */
    0x0041,         /*  Transmit Control Register 2   */
    0x000f,         /*  Sample Rate Generator Register 1   */
    0x2013,         /*  Sample Rate Generator Register 2   */
    0x0000,         /*  Multichannel Control Register 1   */
    0x0000,         /*  Multichannel Control Register 2   */
    0x0600,         /*  Pin Control Register   */
    0x0000,         /*  Note: Multi Channel Elements removed for clarity   */
    };
```

The McBSP is programmed as a serial port, in non-stop clock mode (or DSP mode). Frame sync and serial clock signals are output pins. The receiver is set for 20-bit transfers with zero-bit delay on data receive. The frame sync (FSX1) is generated by the sample rate generator and is used for both the RD and CONVST signal on the ADS8361 by jumper W2 on the EVM.

In the sample code, the ADS8361 is running at 500 ksps, with a serial clock of 10 MHz. The C5416™ DSK clocks the C5416™ DSP at 160 MHz. The 10 MHz clock on CLKX was achieved by setting CLKDIV bit field in the sample rate generator register to 16. The formula for calculating the serial clock is given below as equation 1.

$$CLOCK = (CPUCLOCK)/(CLKDIV) \quad (1)$$

By Equation 1, each clock cycle is approximately 100 ns; triggering a frame-sync pulse every 20 serial clock cycles gives a sample rate of 500 kHz. The frame period (FPER) field, in the sample rate generator register, is where the 20-cycle period is set.

4.2 Software Flow

The software presented in this application report reads 1024 samples at 500 ksps continuously. As selected in the configuration tool, all the register and peripheral programming is done during initialization. DSP/BIOS pre-initializes all the McBSP registers and other DSP registers before arriving in the main function. As a result, the main function simply enables McBSP1, and then samples data in a continuous loop. When the buffer is full, it resets the index pointer, flushes the receive buffer, then starts the process over again.

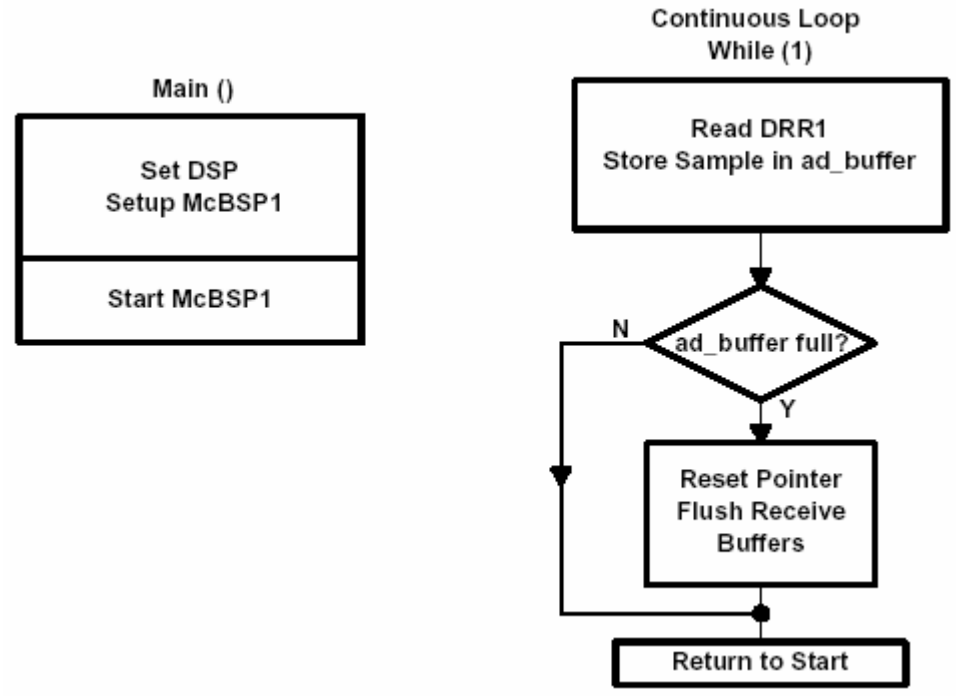

Figure 2. Software Flow Chart

5 References

1. ADS8361 data sheet (SBAS230)
2. TMS320VC5416 data sheet (SPRS0951)
3. TMS320C5000 DSP/BIOS user's guide (SPRU326)
4. TMS320 Cross-Platform Daughtercard Interface Specification (SPRA711)

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