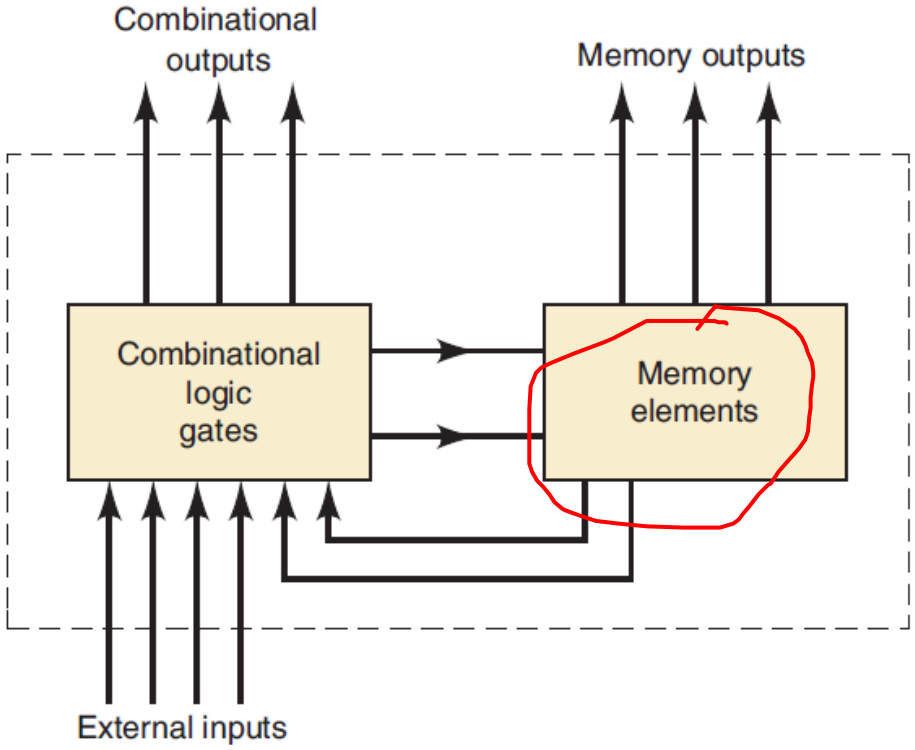
MEMORY DEVICES

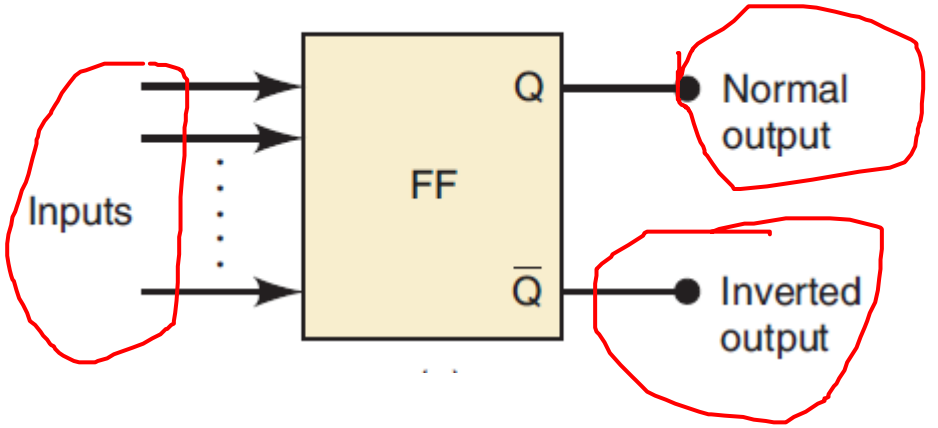
- The output of the combinational circuit depends on input of present time (not on the previous state).
- If memory elements is added with a combinational circuits, it becomes sequential circuits.
- Flip-flop is a memory device which is made of an assembly of logic gates.



Ref (1): pp 257-258

MEMORY DEVICES

- Flip-flop is a memory device which is made of an assembly of logic gates.
- It mainly has two outputs:
  - Normal output labelled as Q
  - Inverted output labelled as $\bar{Q}$

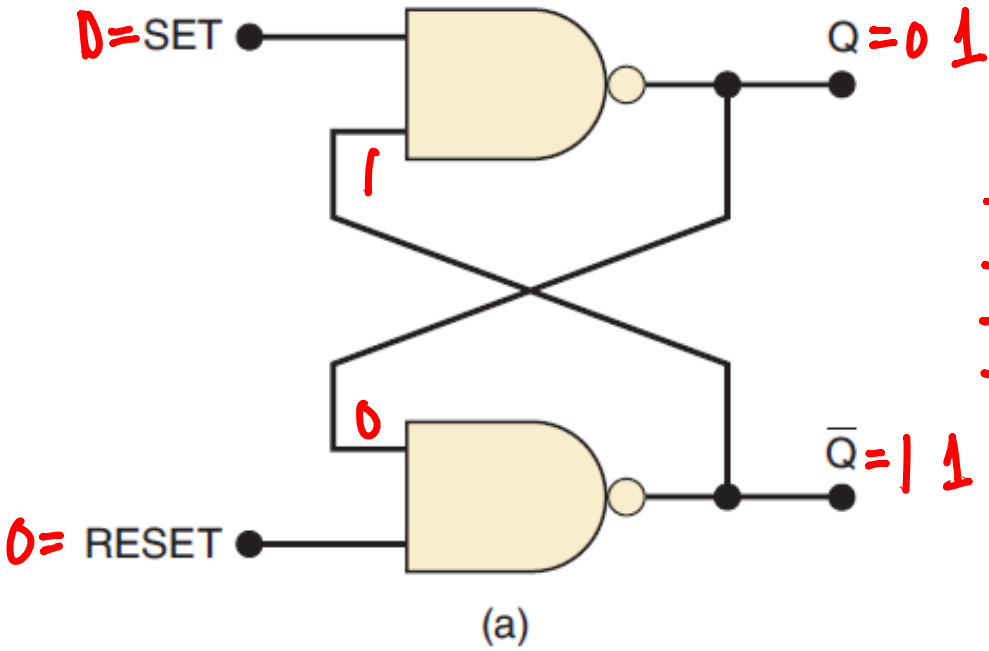


Ref (1): pp 257-258

LATCH

- Basic latch is a feedback connection of two NOR gates or two NAND gates, which can store one bit of information. It can be set to 1 using the S input and reset to 0 using the R input.

- SR Latch with NAND gates:



(a)

Set	Reset	Output
1	1	No change
0	1	Q = 1
1	0	Q = 0
0	0	Invalid *

*Produces Q = $\overline{Q}$ = 1

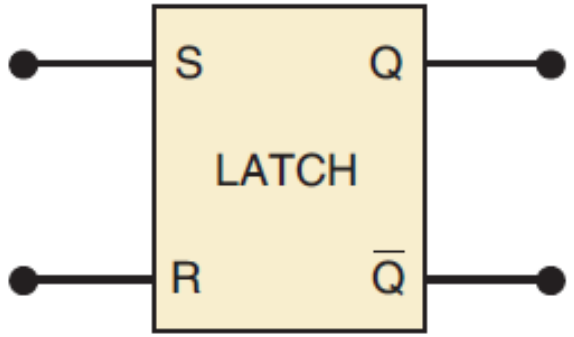
(b)

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

A = 0

$\overline{A}$ = 1

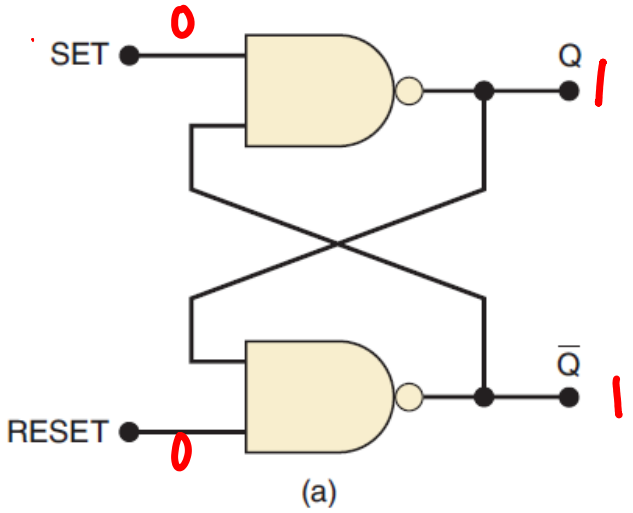
Q = $\overline{Q}$ = 1 Invalid condition.



Ref (1): pp 262

LATCH

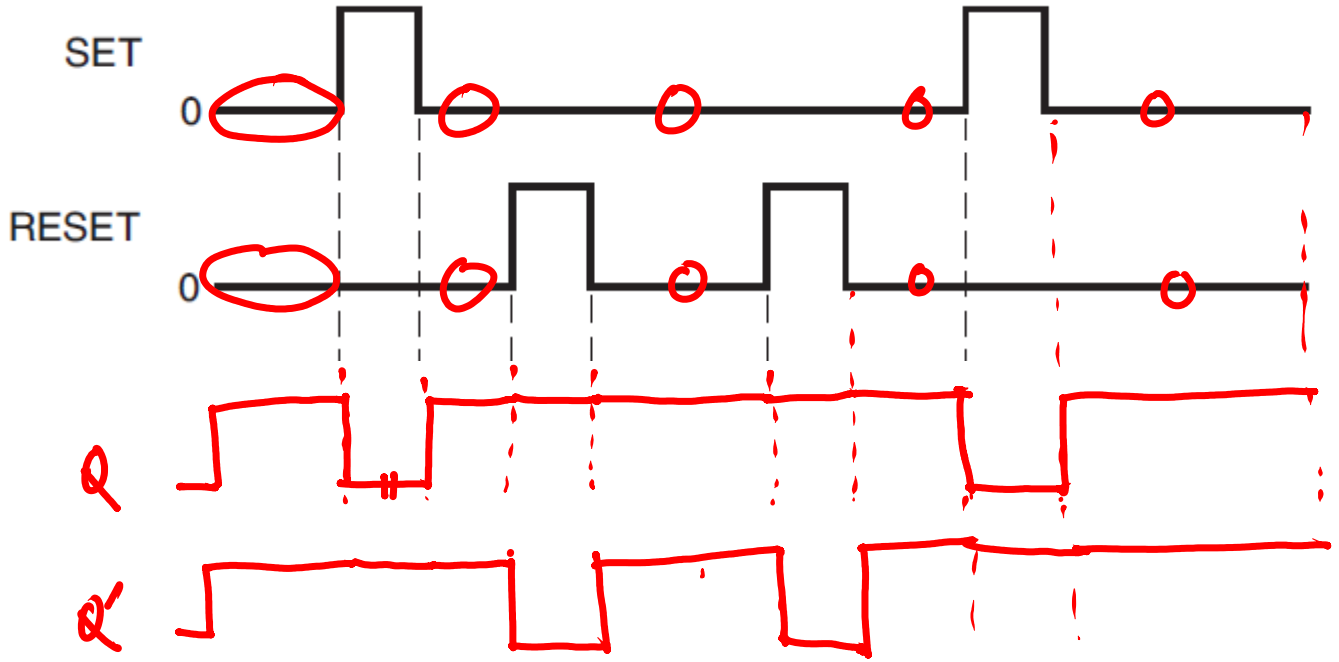
- SR Latch with NAND gates:



Set	Reset	Output
1	1	No change
0	1	Q = 1
1	0	Q = 0
0	0	Invalid *

*Produces $Q = \overline{Q} = 1$

(b)

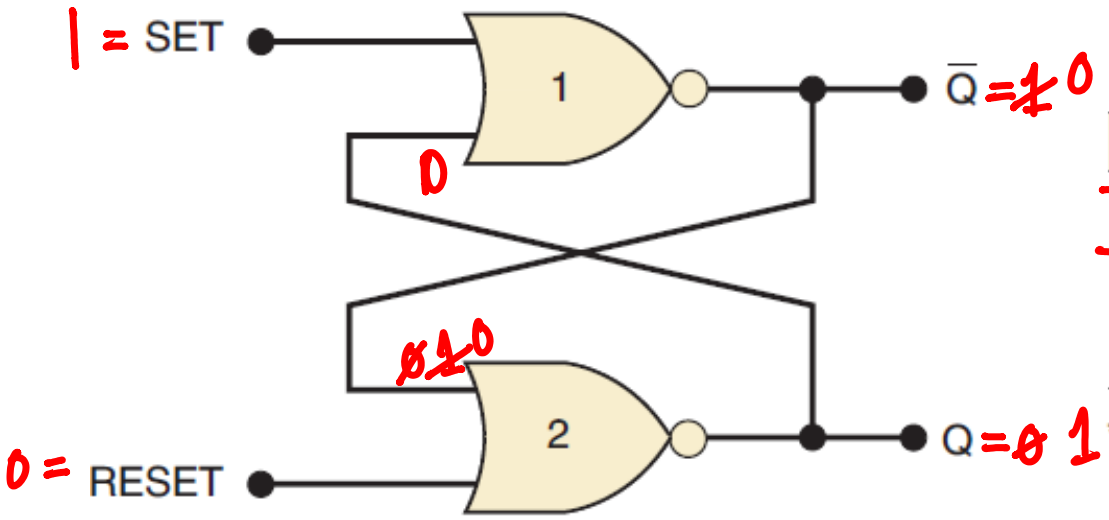


Ref (1): pp 262

LATCH

- SR Latch with NOR gates:

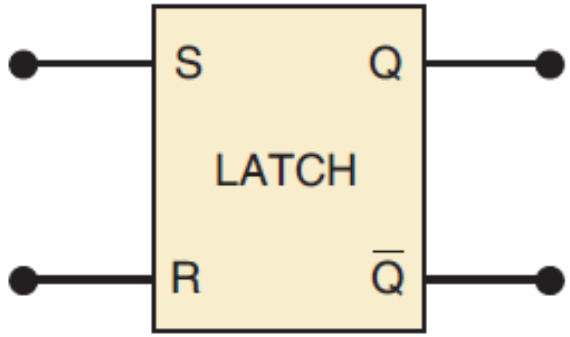
A	B	Z
→ 0	0	1
0	1	0
→ 1	0	0
1	1	0



Set	Reset	Output
→ 0	0	No change
→ 1	0	Q = 1 → $Q^* = 0/1$
0	1	Q = 0
1	1	Invalid *

*Produces Q = $\overline{Q}$ = 0.

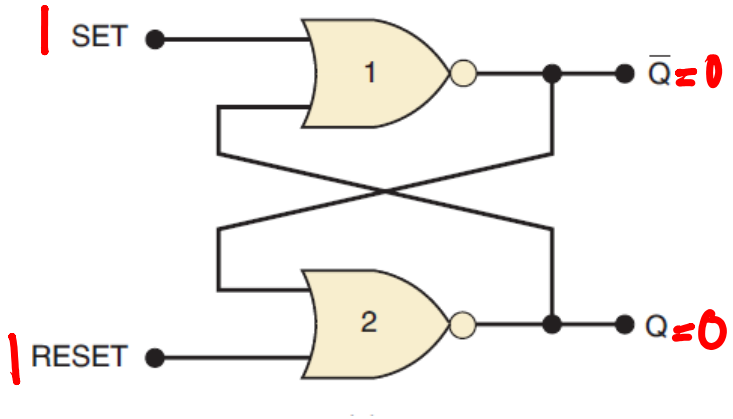
(b)



Ref (1): pp 262

LATCH

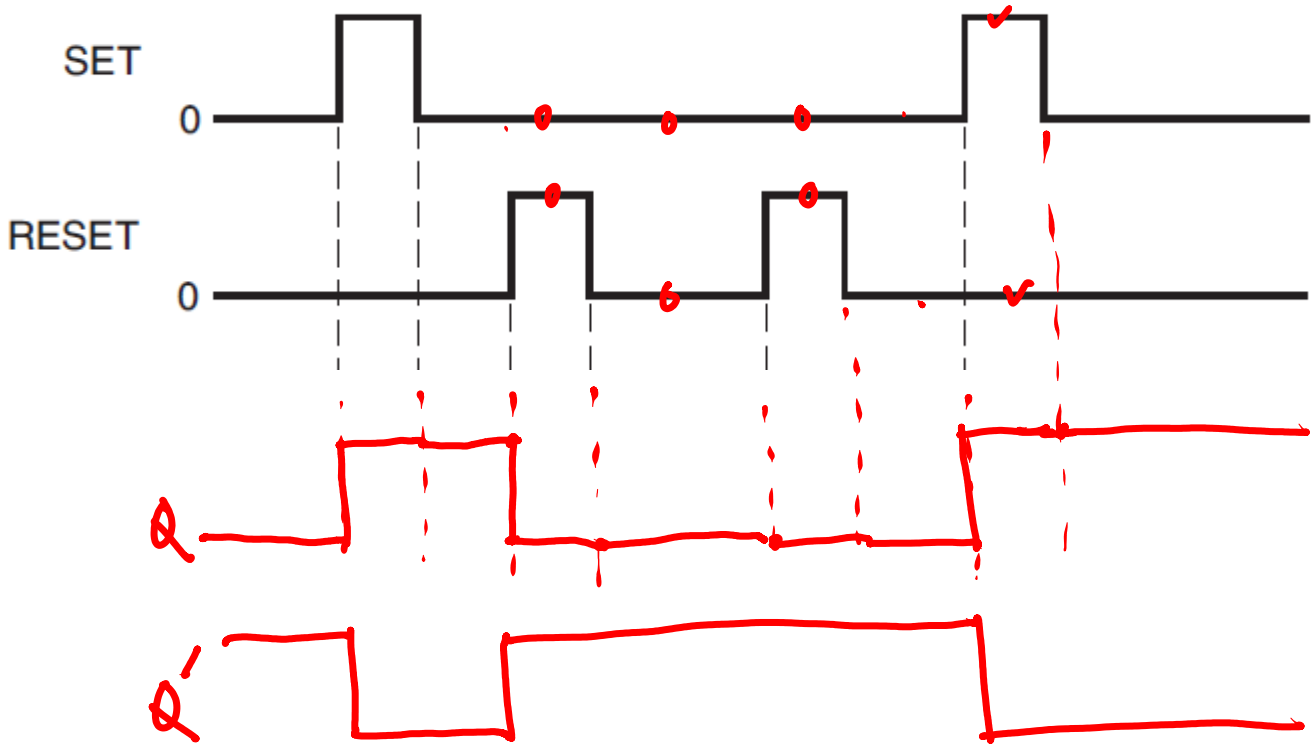
- SR Latch with NOR gates:



Set	Reset	Output
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid*

*Produces Q = $\bar{Q}$ = 0.

(b)

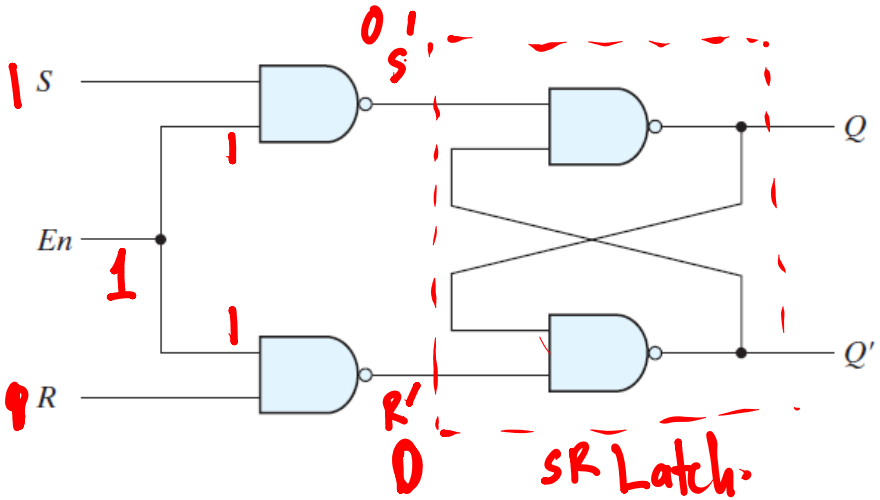


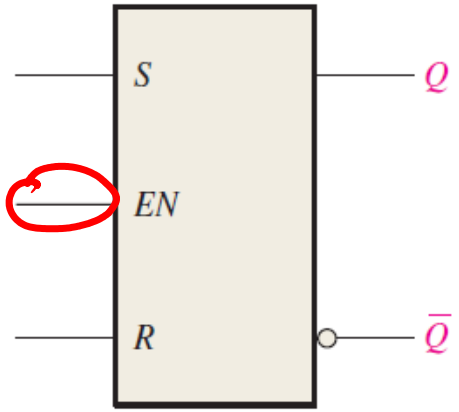
Ref (1): pp 262

LATCH

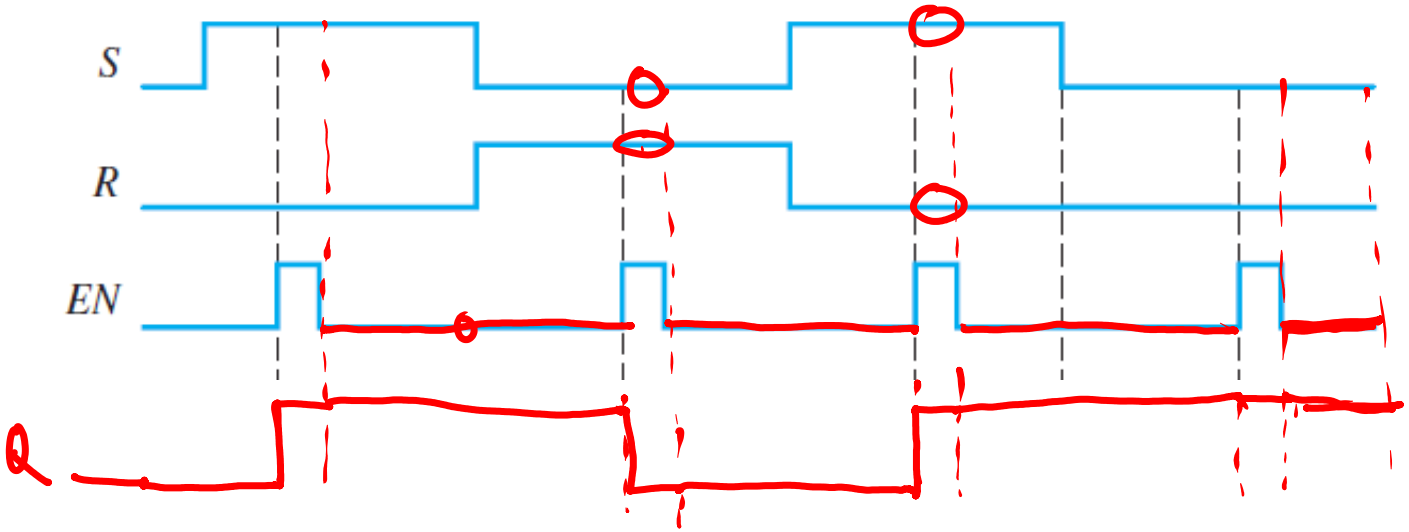
- SR Latch with control input:

Gated latch is a basic latch that includes input gating and a control input signal. The latch retains its existing state when the control input is equal to 0. Its state may be changed when the control signal is equal to 1.





S'	R'	Q
0	0	Invalid
0	1	1
1	0	0
1	1	NC



En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$, reset state
1	1	0	$Q = 1$, set state
1	1	1	Indeterminate (Invalid)

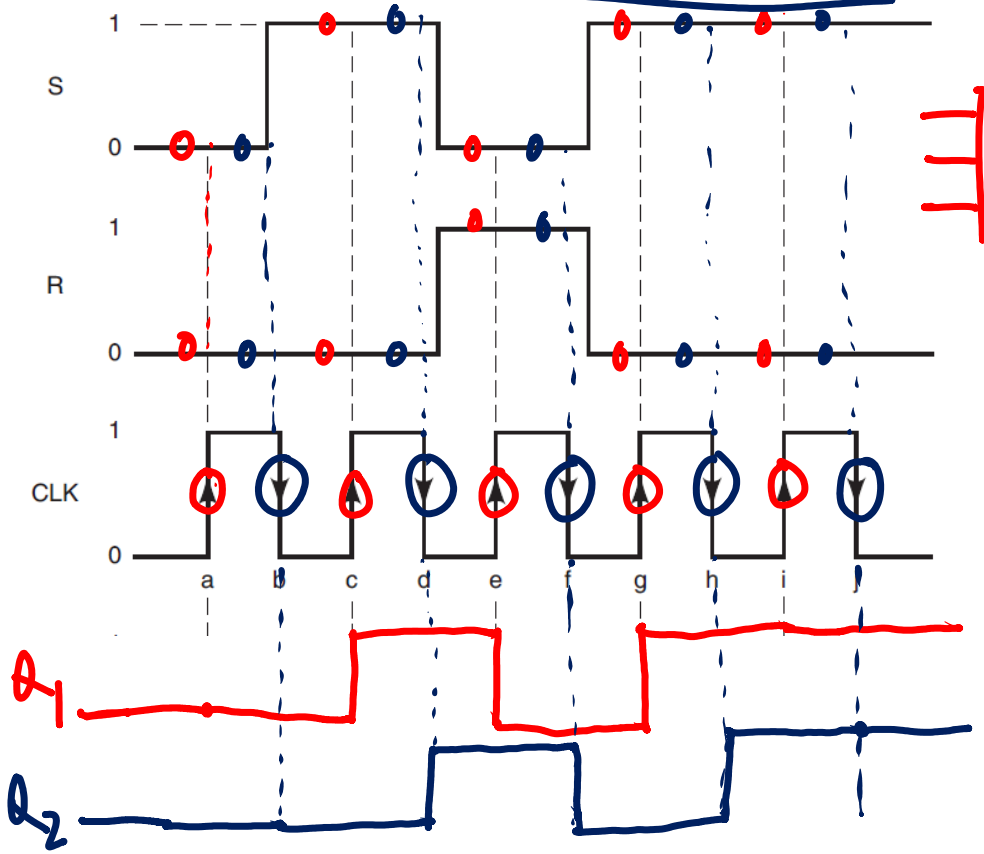
$Q = \overline{Q} = 1$

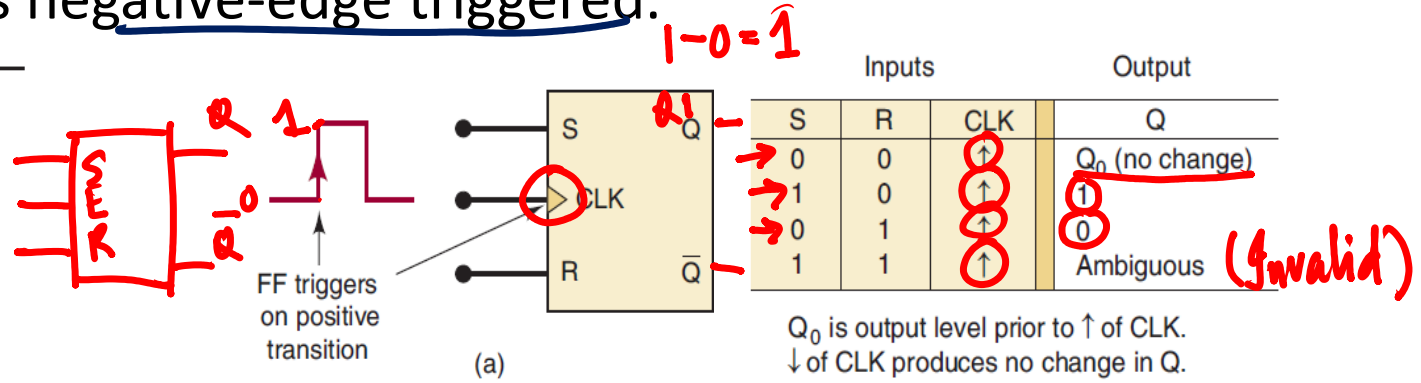
Ref (2): pp 262

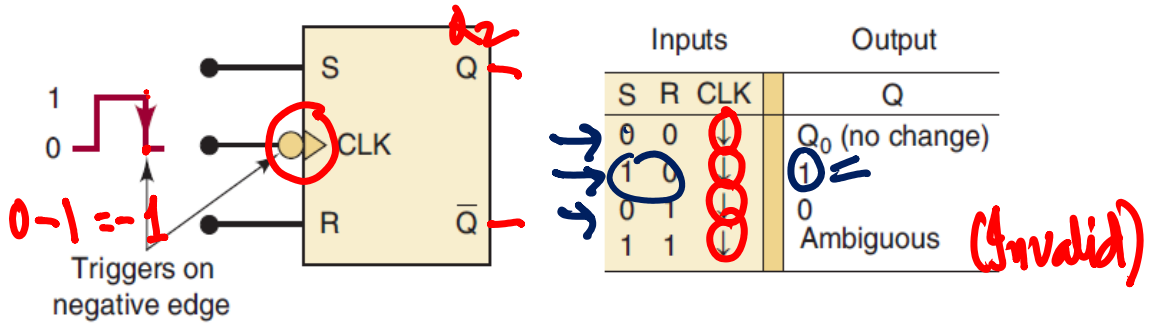
FLIP-FLOPS

- SR Flip-flop:

A flip-flop is a storage element that can have its output state changed only on the edge of the controlling clock signal. If the state changes when the clock signal goes from 0 to 1, then the flip-flop is positive-edge triggered. If the state changes when the clock signal goes from 1 to 0, then the flip-flop is negative-edge triggered.







Ref (1): pp 275