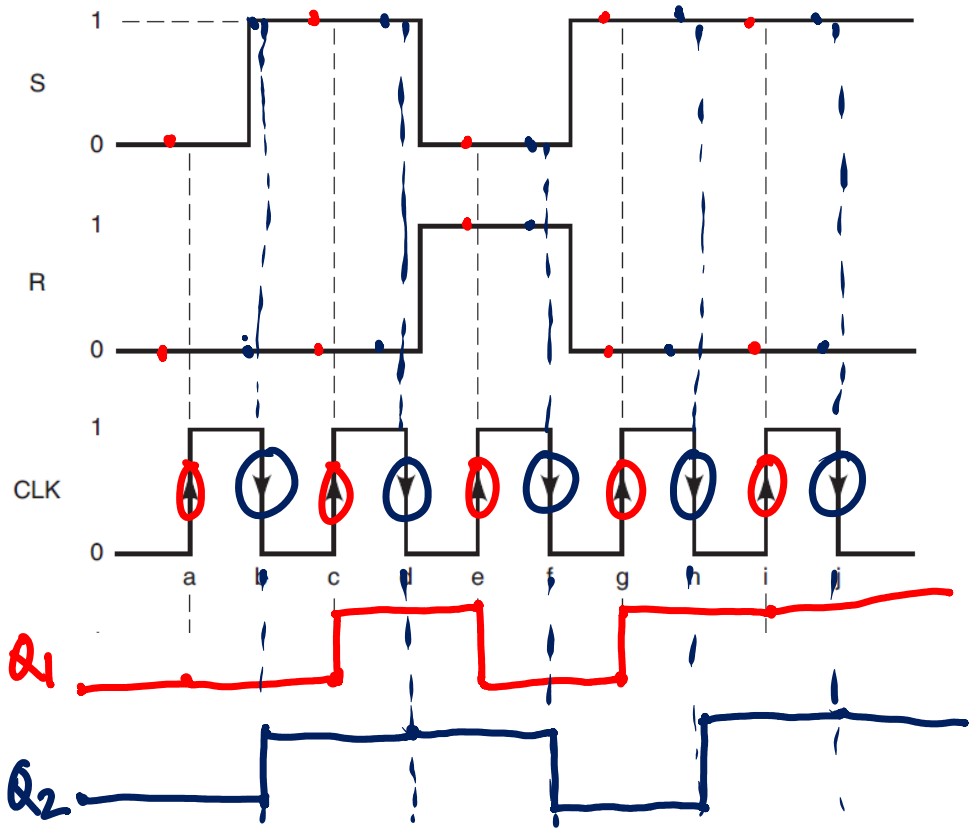
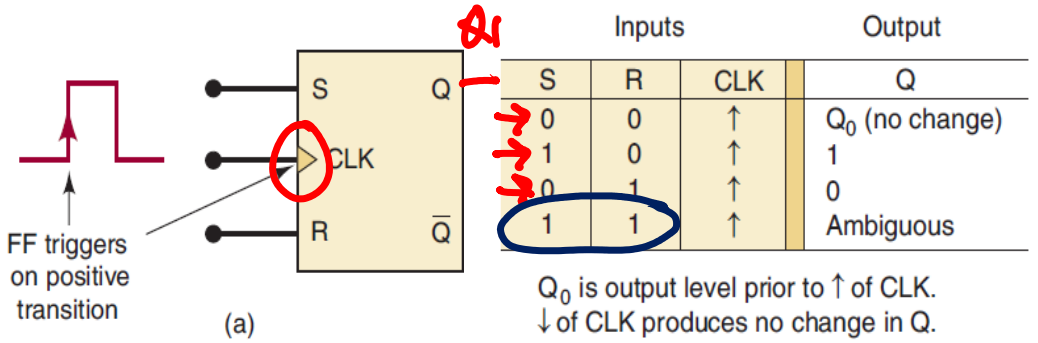
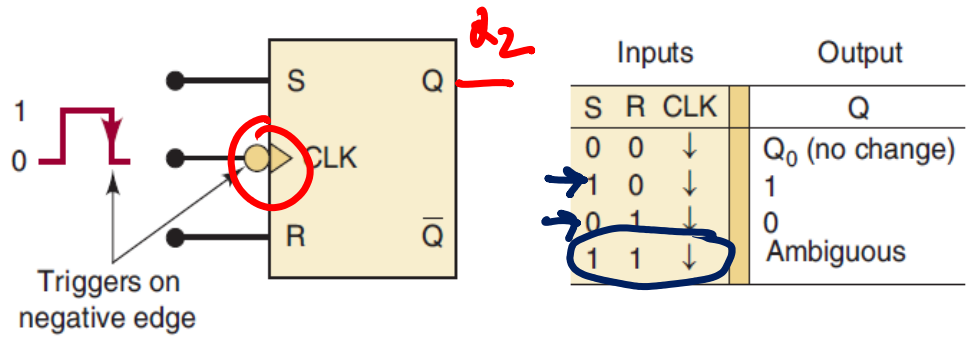
FLIP-FLOPS

- SR Flip-flop:

A flip-flop is a storage element that can have its output state changed only on the edge of the controlling clock signal. If the state changes when the clock signal goes from 0 to 1, then the flip-flop is positive-edge triggered. If the state changes when the clock signal goes from 1 to 0, then the flip-flop is negative-edge triggered.



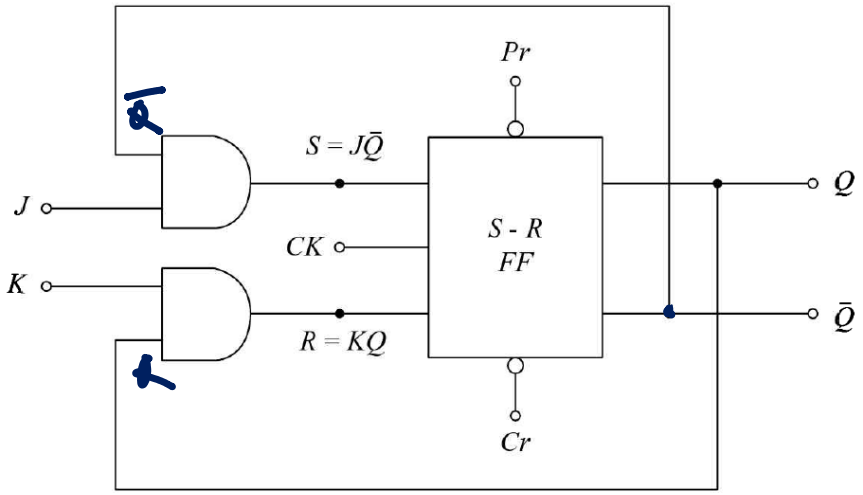


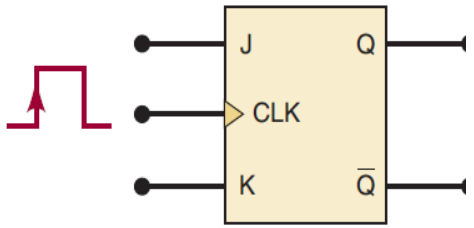


Ref (1): pp 275

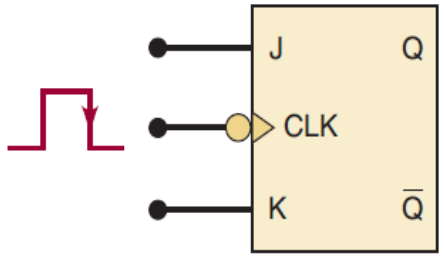
FLIP-FLOPS

- Clocked JK Flip-flop:

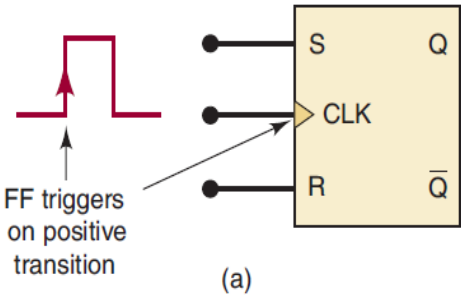




J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q_0}$ (toggles)



J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	Q_0 (toggles)



Inputs			Output
S	R	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

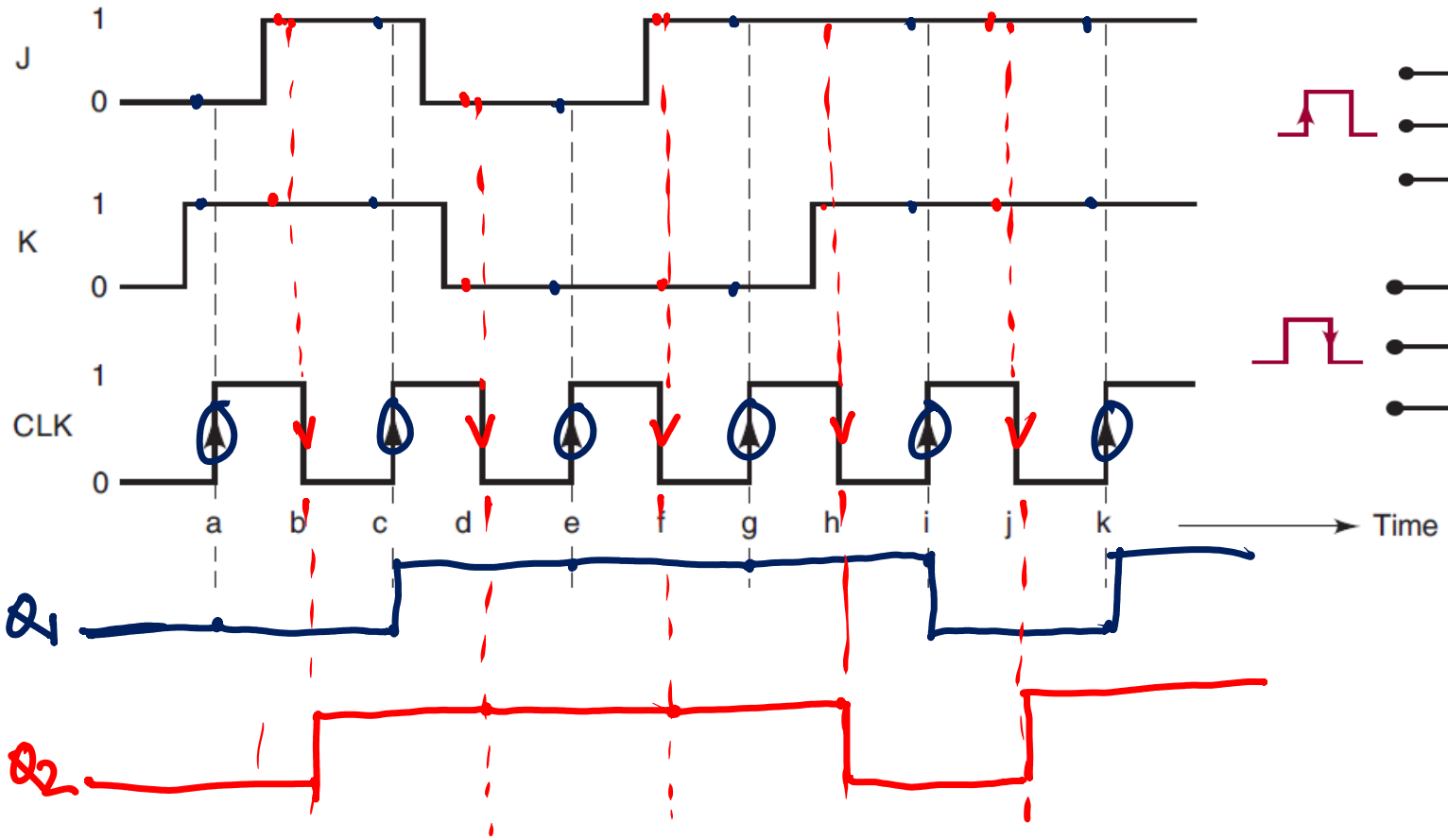
Q_0 is output level prior to ↑ of CLK.
↓ of CLK produces no change in Q.

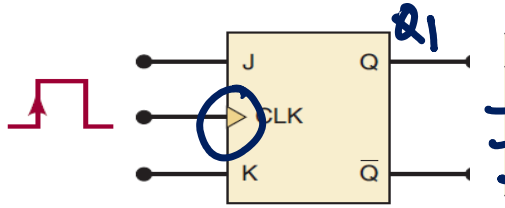
J_n	K_n	Q_{n-1}	$\overline{Q}_{n-1}$	S_n	R_n	Q_n	
0	0	0	1	0	0	0	$Q_n = Q_{n-1}$
		1	0	0	0	1	
1	0	0	1	1	0	1	$Q_n = 1$
		1	0	0	0	1	
0	1	0	1	0	0	0	$Q_n = 0$
		1	0	0	1	0	
1	1	0	1	1	0	1	$Q_n = \overline{Q_{n-1}}$
		1	0	0	1	0	

Ref (1): pp 278-279

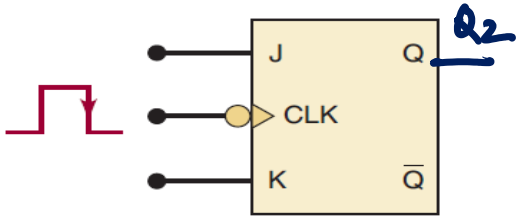
FLIP-FLOPS

- Clocked JK Flip-flop:





J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

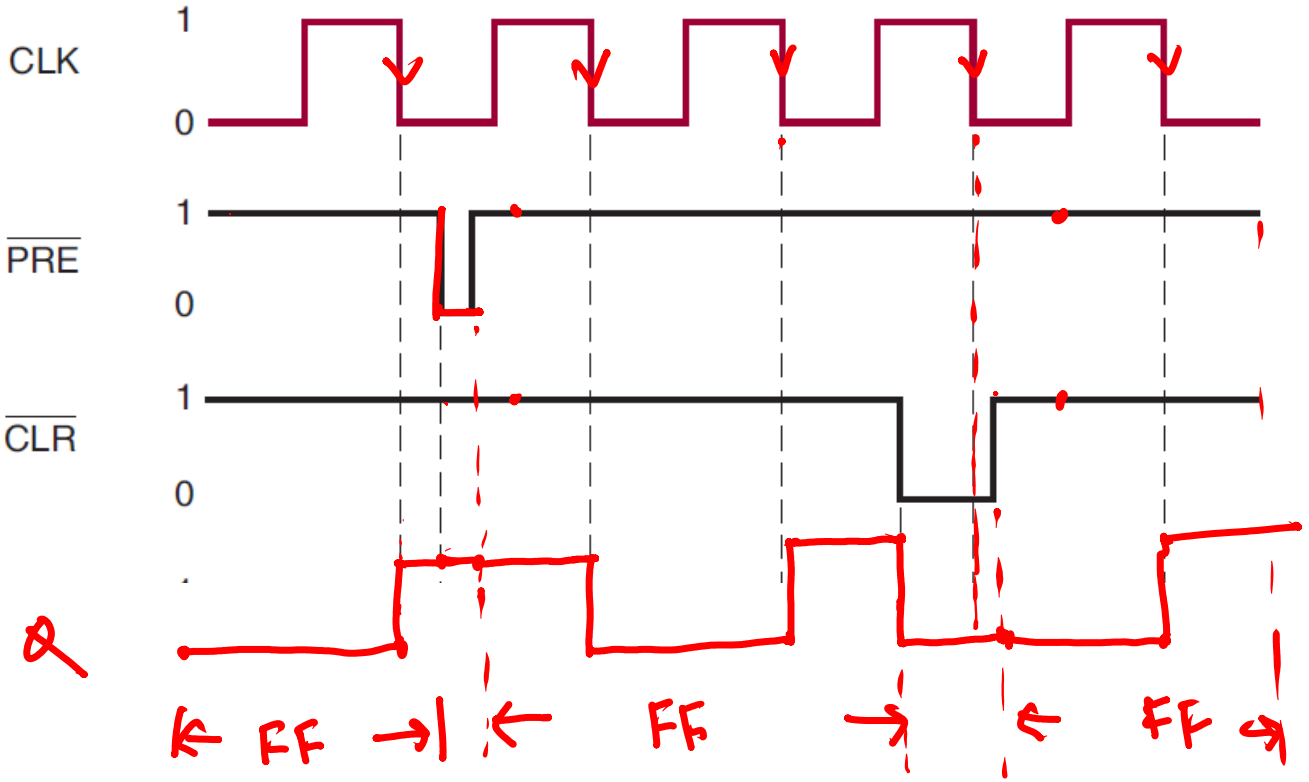


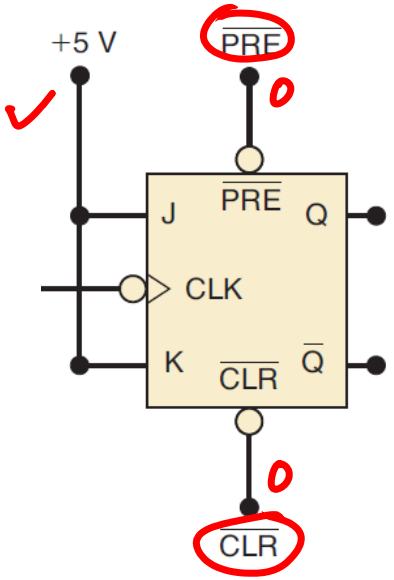
J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	$\overline{Q}_0$ (toggles)

Ref (1): pp 278-279

FLIP-FLOPS

- Clocked JK Flip-flop:



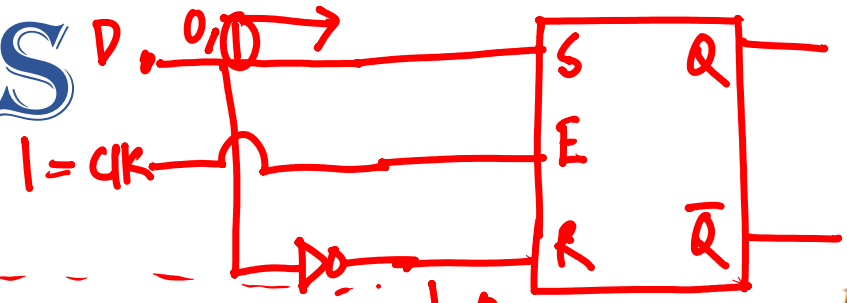


J	K	Clk	$\overline{PRE}$	$\overline{CLR}$	Q
0	0	↓	1	1	Q (no change)
0	1	↓	1	1	0 (Synch reset)
1	0	↓	1	1	1 (Synch set)
1	1	↓	1	1	$\overline{Q}$ (Synch toggle)
x	x	x	1	1	Q (no change)
x	x	x	1	0	0 (asynch clear)
x	x	x	0	1	1 (asynch preset)
x	x	x	0	0	(Invalid)

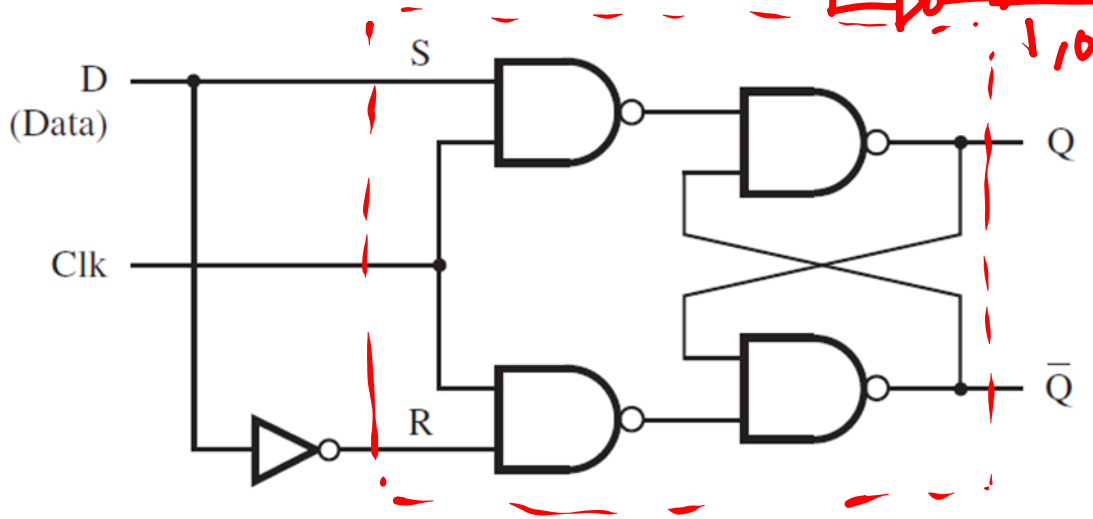
$\overline{PRE}=1$, $\overline{CLR}=1$, FF → No operation

$J=K=+5V=1$

FLIP-FLOPS



- D Latch:



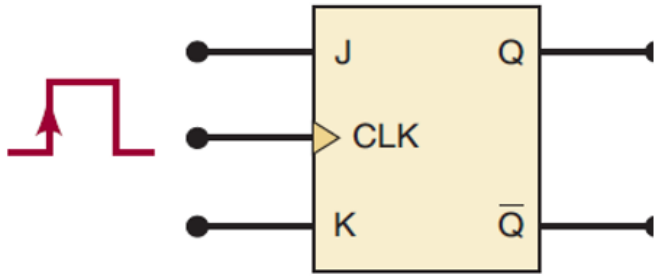
En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

Clk	D	$Q(t+1)$
0	x	$Q(t)$ (NC)
1	0	0
1	1	1

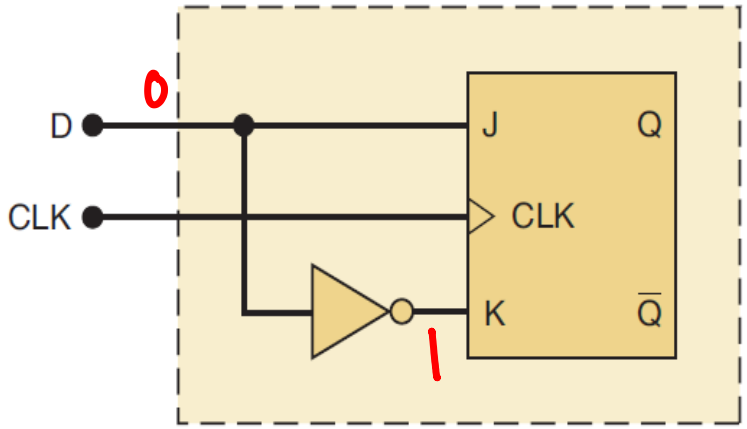
D	S=D	R=$\bar{D}$	Q
0	0	1	Q=0
1	1	0	Q=1

FLIP-FLOPS

- Clocked D Flip-flop:



J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)



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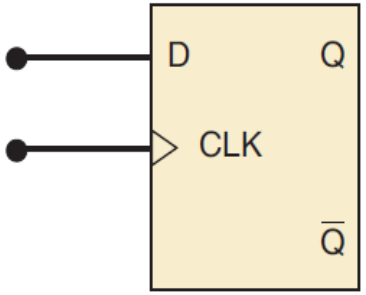
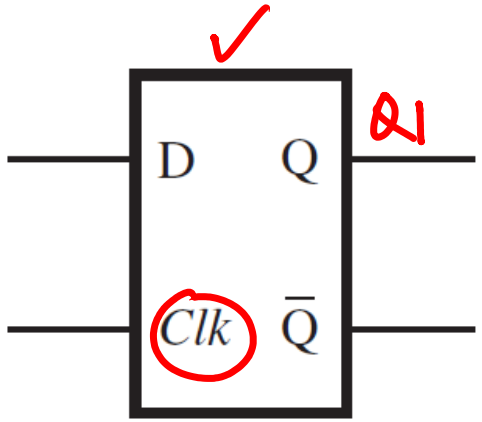


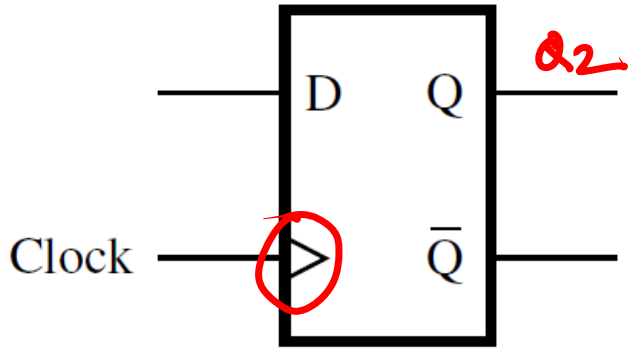
D	J=D	K=$\overline{D}$	Q
0	0	1	0
1	1	0	1

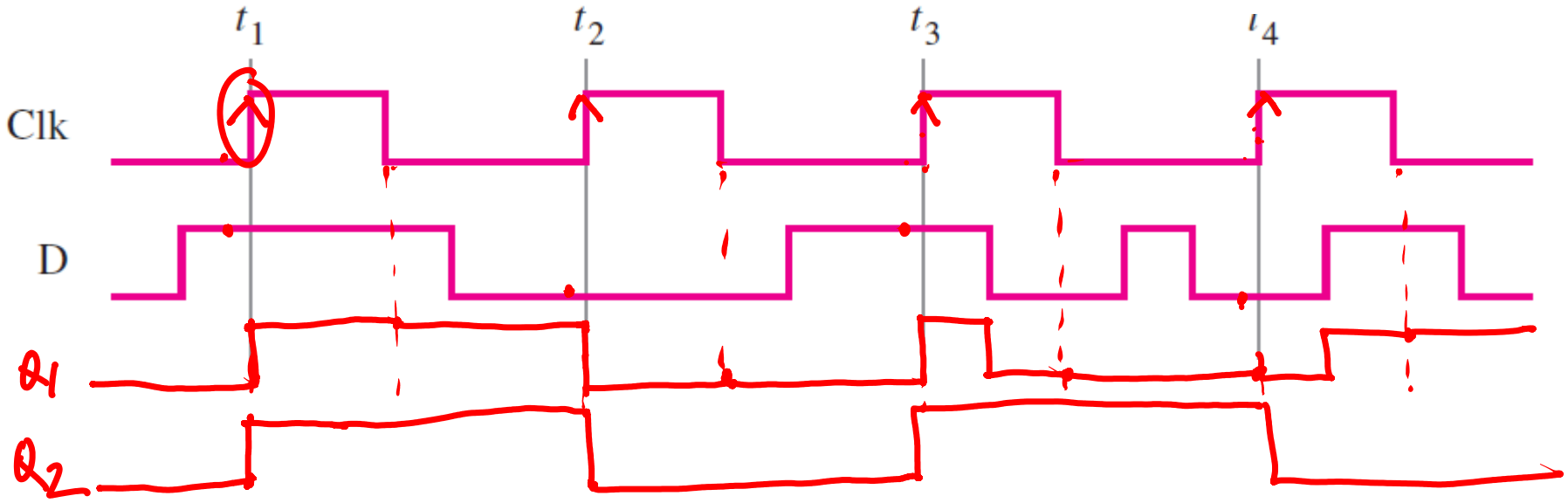
FLIP-FLOPS

- Clocked D Flip-flop:



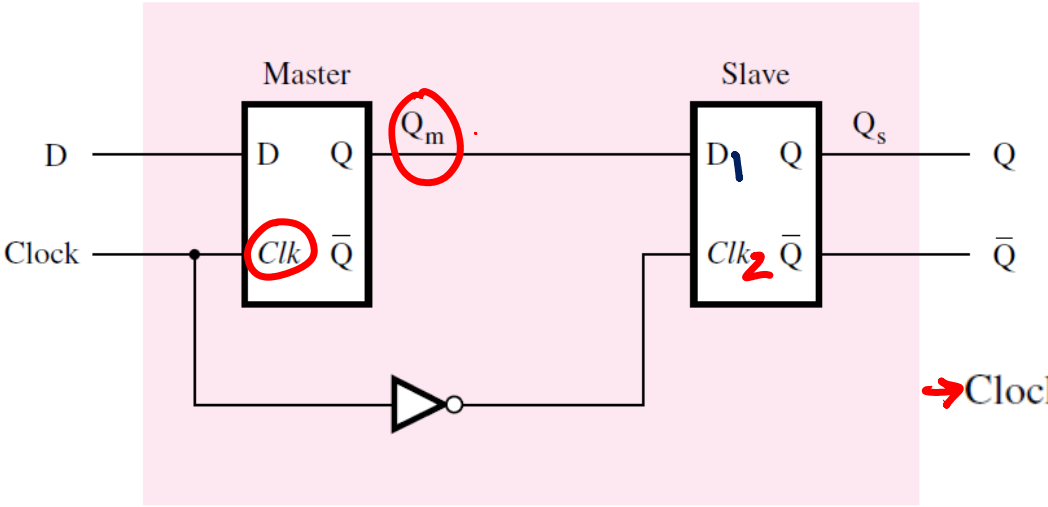
Clk	D	Q(t + 1)
0	x	Q(t)
1	0	0
1	1	1





FLIP-FLOPS

- Clocked D Latch:



Clk	D	Q(t + 1)
0	x	Q(t)
1	0	0
1	1	1