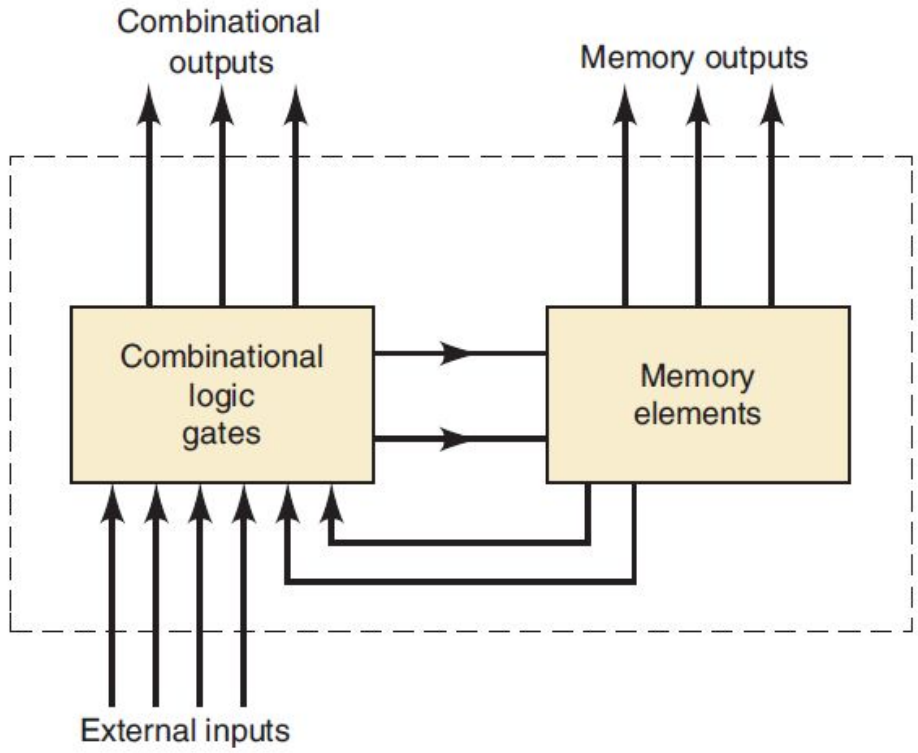
MEMORY DEVICES

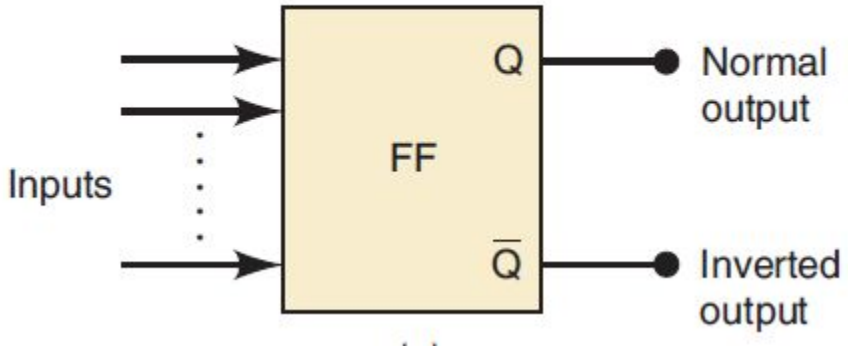
- The output of the combinational circuit depends on input of present time (not on the previous state).
- If memory elements is added with a combinational circuits, it becomes sequential circuits.
- Flip-flop is a memory device which is made of an assembly of logic gates.



Ref (1): pp 257-258

MEMORY DEVICES

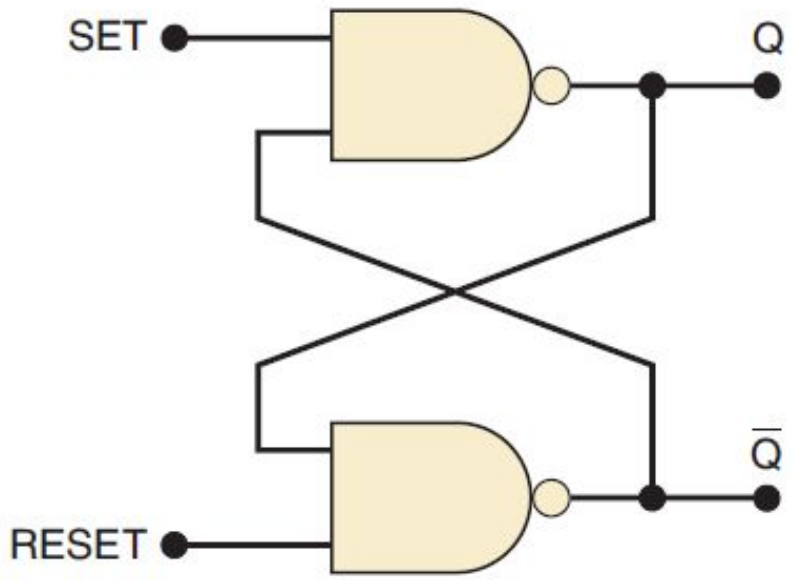
- Flip-flop is a memory device which is made of an assembly of logic gates.
- It mainly has two outputs:
  - Normal output labelled as Q
  - Inverted output labelled as $\bar{Q}$



Ref (1): pp 257-258

LATCH

- Basic latch is a feedback connection of two NOR gates or two NAND gates, which can store one bit of information. It can be set to 1 using the S input and reset to 0 using the R input.
- SR Latch with NAND gates:

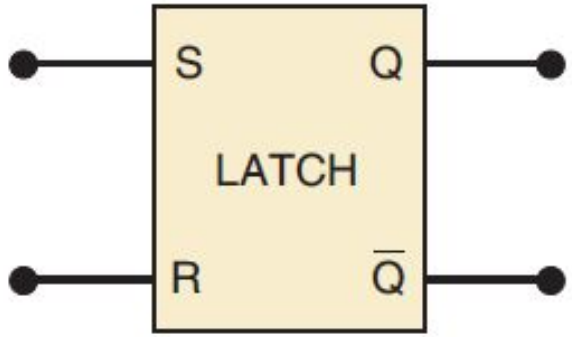


(a)

Set	Reset	Output
1	1	No change
0	1	Q = 1
1	0	Q = 0
0	0	Invalid *

*Produces $Q = \overline{Q} = 1$.

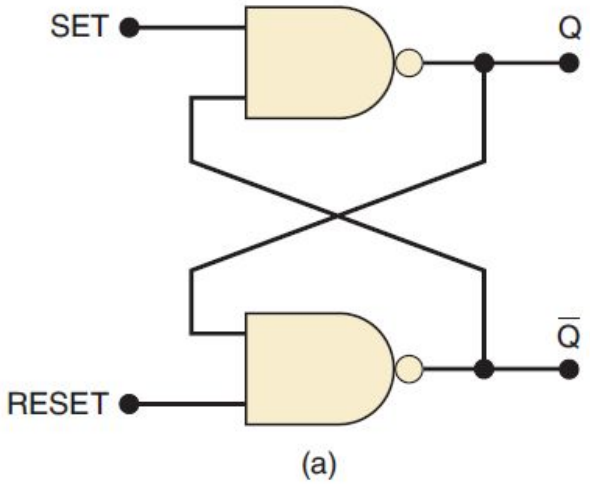
(b)



Ref (1): pp 262

LATCH

- SR Latch with NAND gates:

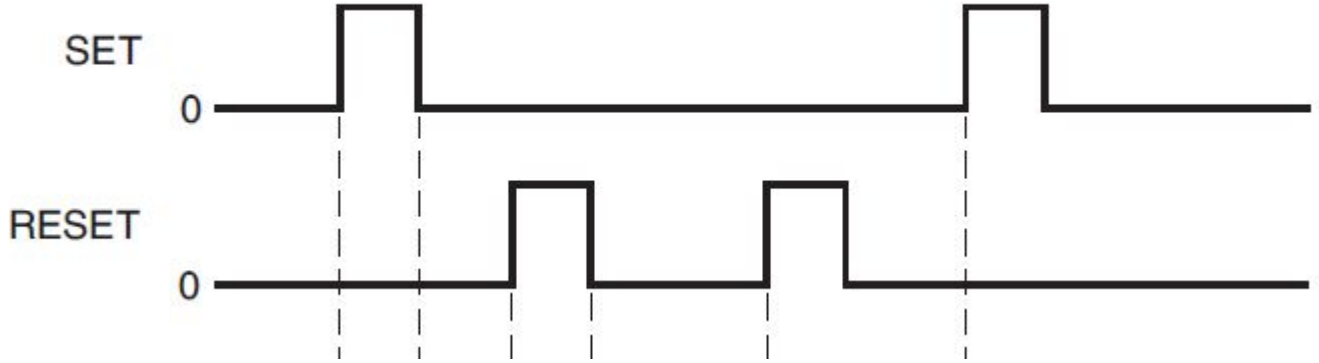


(a)

Set	Reset	Output
1	1	No change
0	1	Q = 1
1	0	Q = 0
0	0	Invalid *

*Produces Q = $\overline{Q}$ = 1.

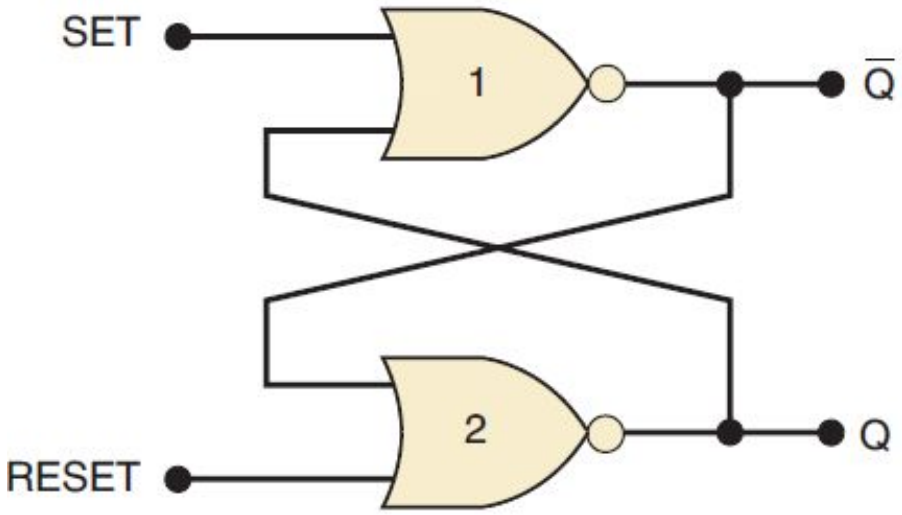
(b)



Ref (1): pp 262

LATCH

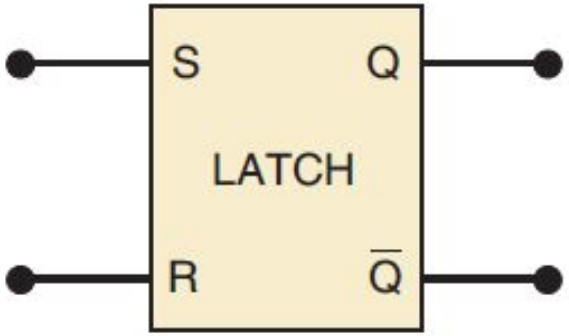
- SR Latch with NOR gates:



Set	Reset	Output
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid *

*Produces $Q = \overline{Q} = 0$.

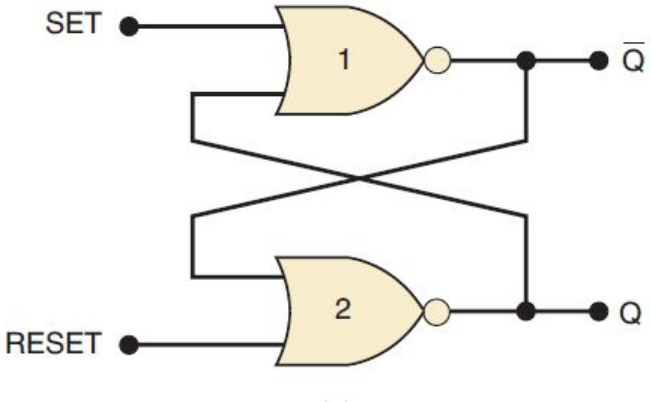
(b)



Ref (1): pp 262

LATCH

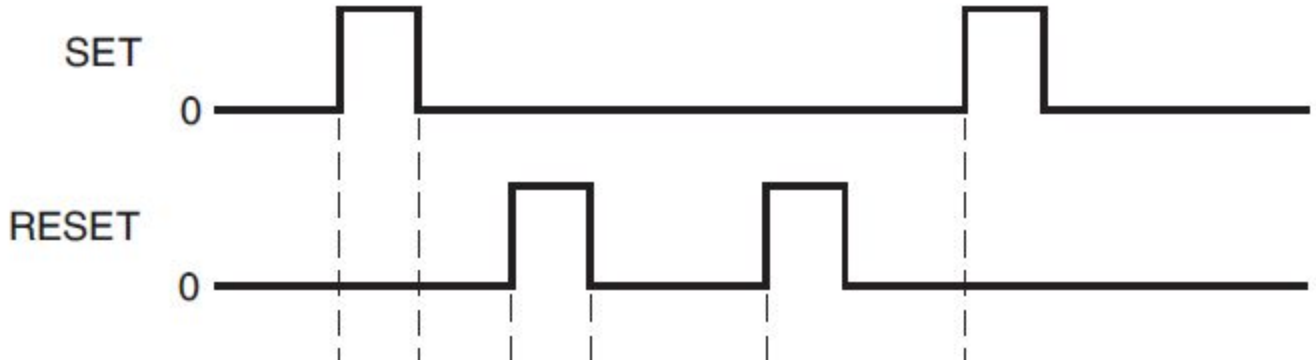
- SR Latch with NOR gates:



Set	Reset	Output
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid *

*Produces $Q = \overline{Q} = 0$.

(b)

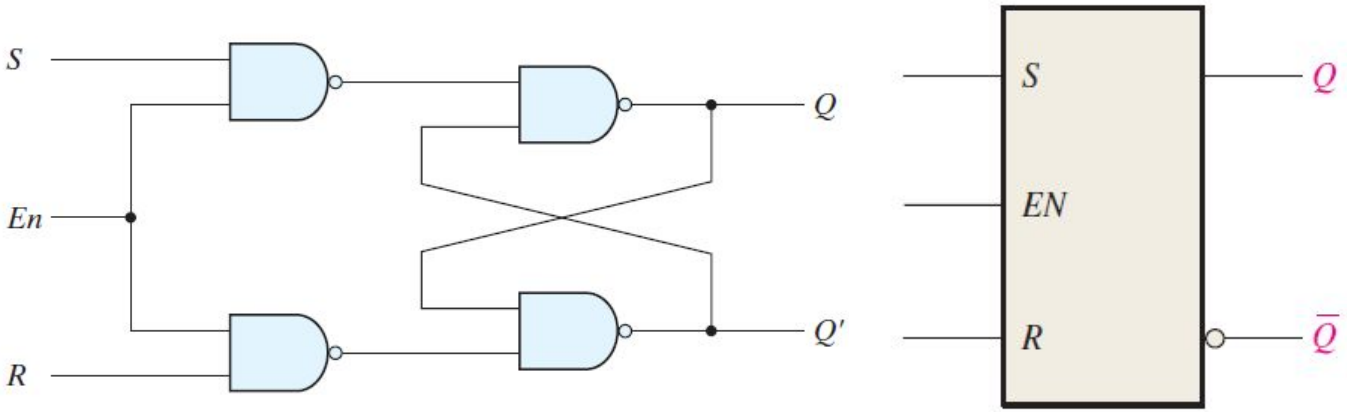


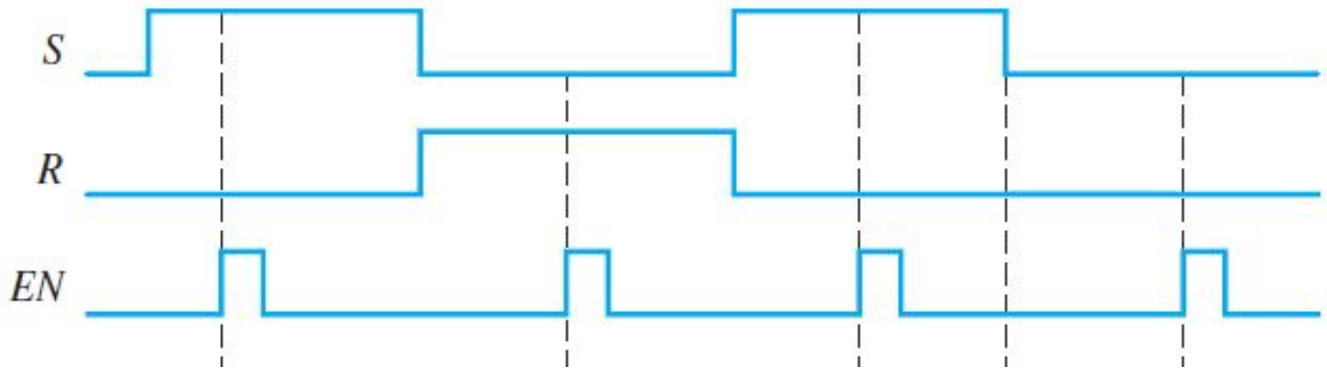
Ref (1): pp 262

LATCH

- SR Latch with control input:

Gated latch is a basic latch that includes input gating and a control input signal. The latch retains its existing state when the control input is equal to 0. Its state may be changed when the control signal is equal to 1.



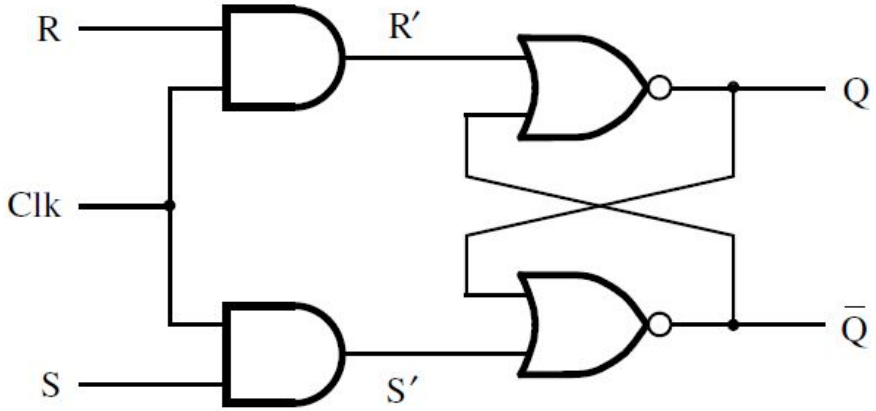


En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

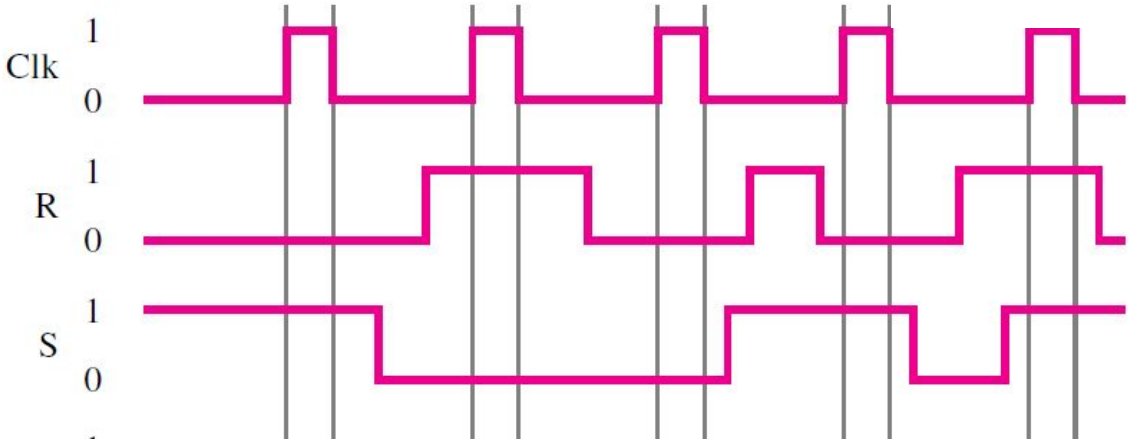
Ref (2): pp 262

LATCH

- SR Latch with control input:



Clk	S	R	Q(t + 1)
0	x	x	Q(t) (no change)
1	0	0	Q(t) (no change)
1	0	1	0
1	1	0	1
1	1	1	x

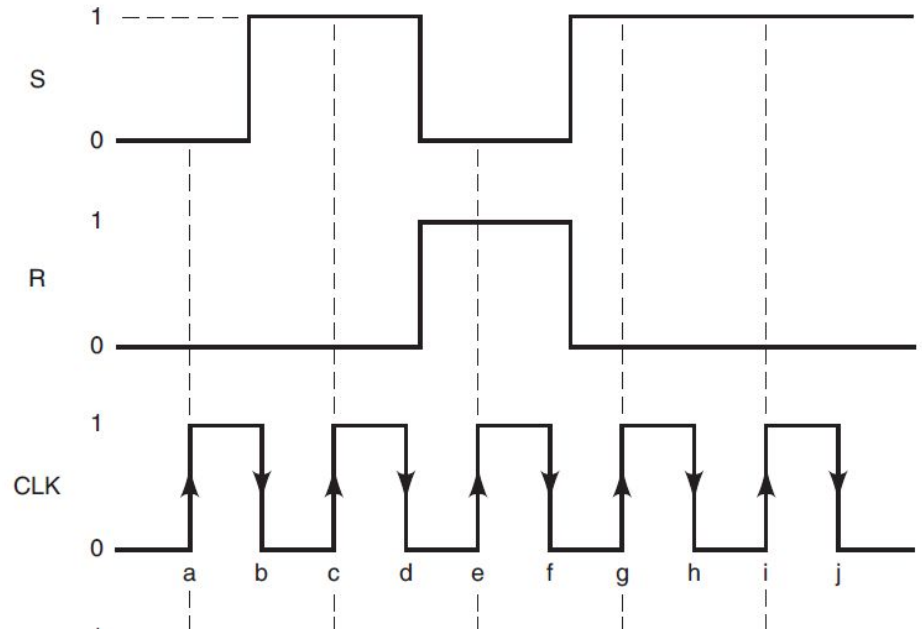


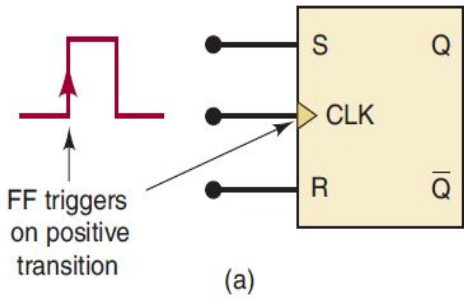
Ref ():

FLIP-FLOPS

- SR Flip-flop:

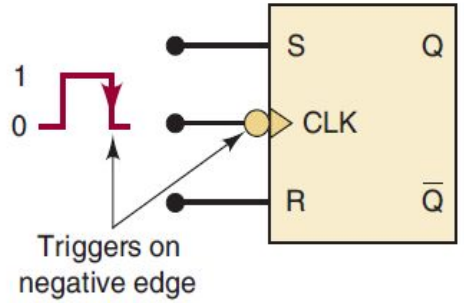
A flip-flop is a storage element that can have its output state changed only on the edge of the controlling clock signal. If the state changes when the clock signal goes from 0 to 1, then the flip-flop is positive-edge triggered. If the state changes when the clock signal goes from 1 to 0, then the flip-flop is negative-edge triggered.





Inputs			Output
S	R	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

Q_0 is output level prior to ↑ of CLK.
↓ of CLK produces no change in Q.

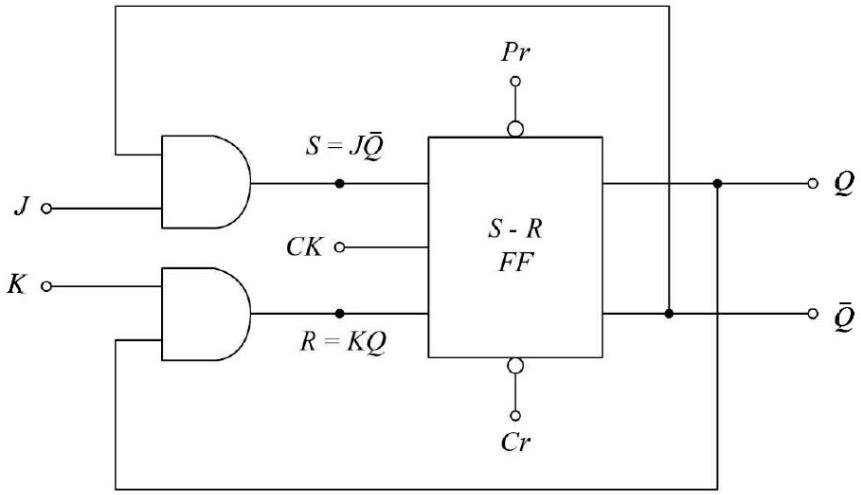


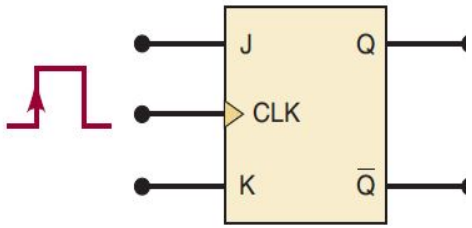
Inputs			Output
S	R	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	Ambiguous

Ref (1): pp 275

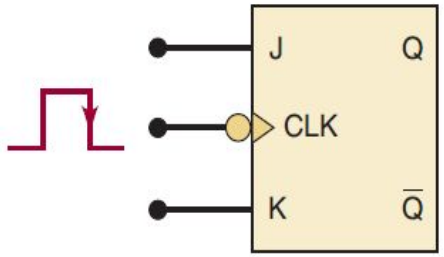
FLIP-FLOPS

- Clocked JK Flip-flop:

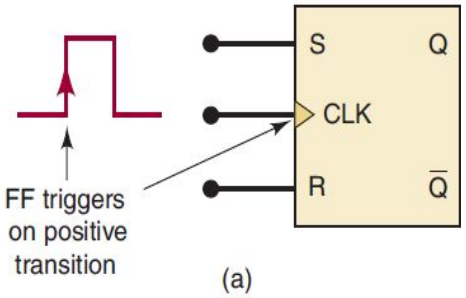




J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)



J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	Q_0 (toggles)



Inputs			Output
S	R	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

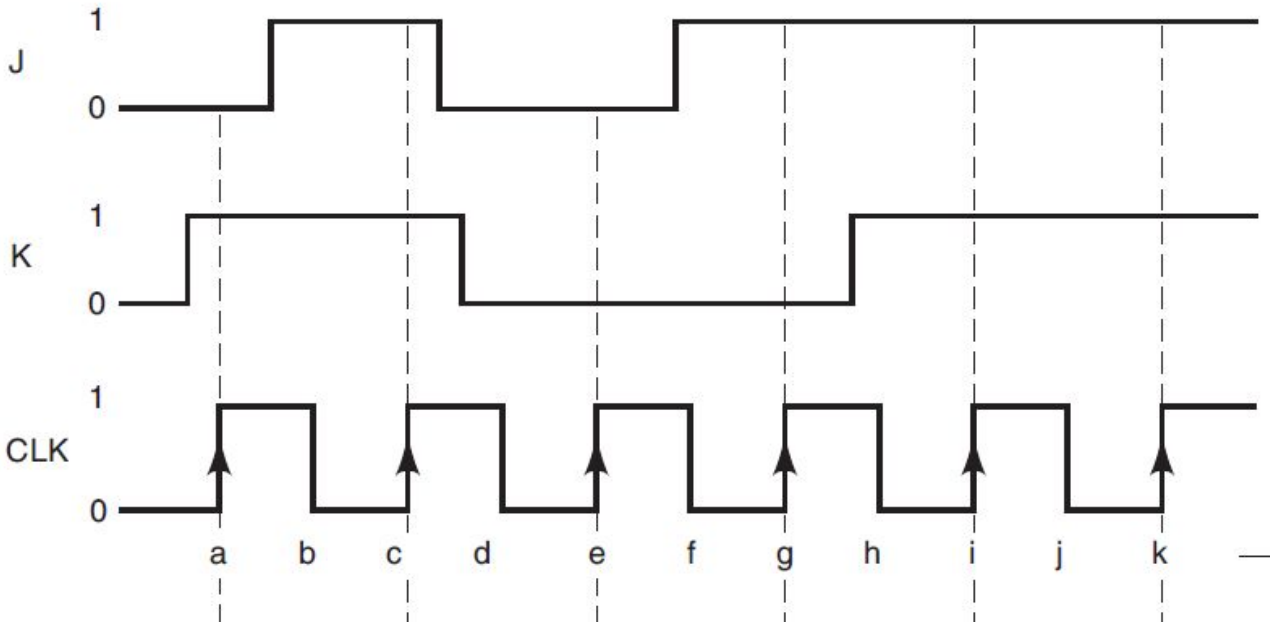
Q_0 is output level prior to ↑ of CLK.
↓ of CLK produces no change in Q.

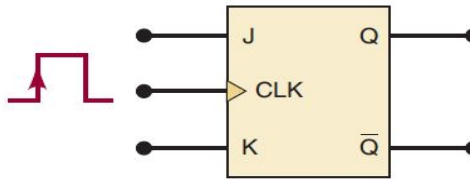
J_n	K_n	Q_{n-1}	$\overline{Q_{n-1}}$	S_n	R_n	Q_n
0	0					
1	0					
0	1					
1	1					

Ref (1): pp 278-279

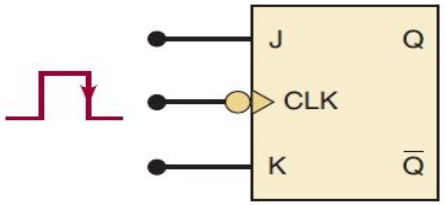
FLIP-FLOPS

- Clocked JK Flip-flop:





J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

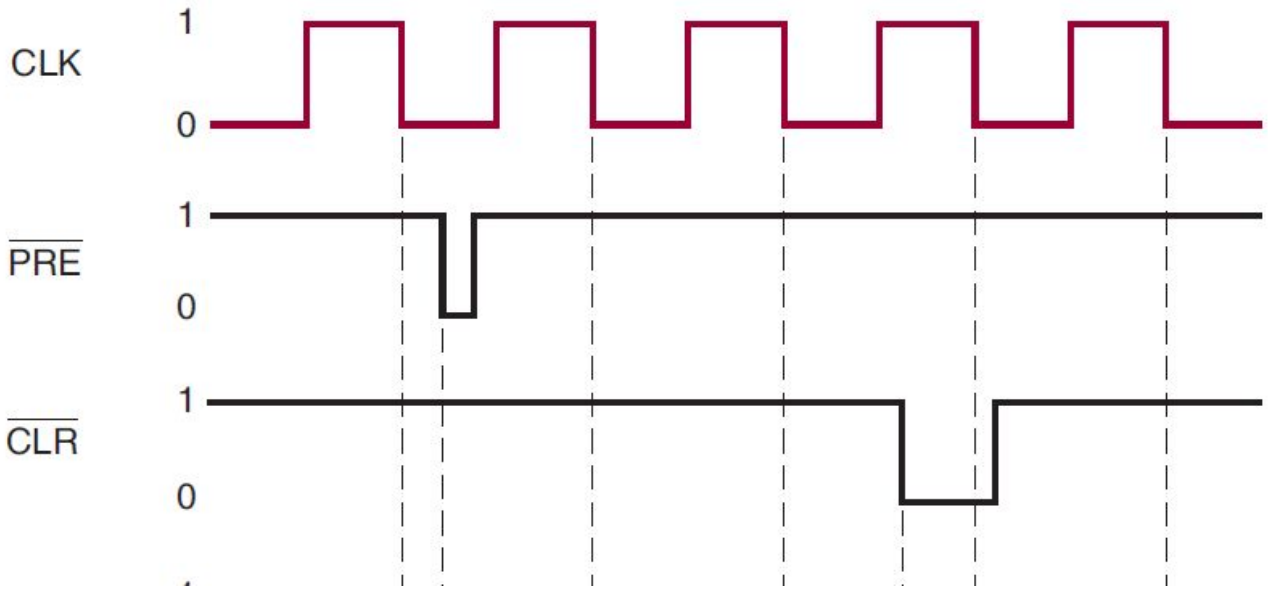


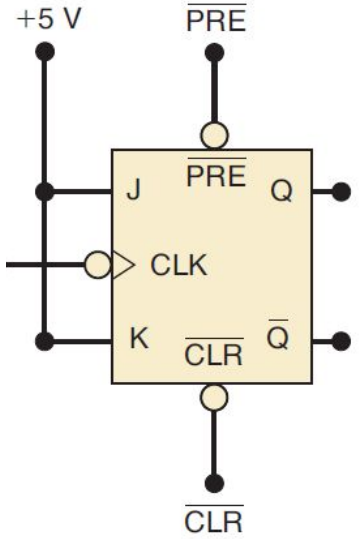
J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	$\overline{Q}_0$ (toggles)

Ref (1): pp 278-279

FLIP-FLOPS

- Clocked JK Flip-flop:



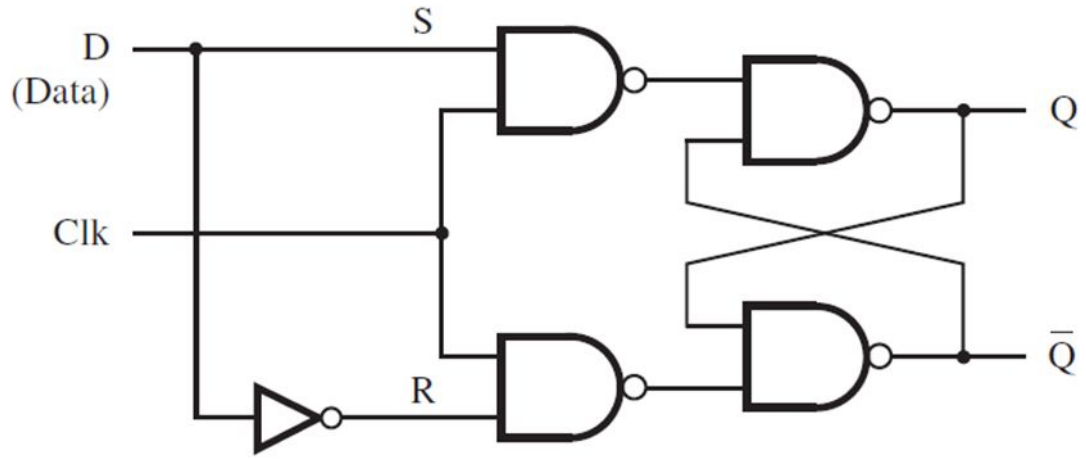


J	K	Clk	$\overline{PRE}$	$\overline{CLR}$	Q
0	0	↓	1	1	Q (no change)
0	1	↓	1	1	0 (Synch reset)
1	0	↓	1	1	1 (Synch set)
1	1	↓	1	1	$\overline{Q}$ (Synch toggle)
x	x	x	1	1	Q (no change)
x	x	x	1	0	0 (asynch clear)
x	x	x	0	1	1 (asynch preset)
x	x	x	0	0	(Invalid)

Ref (1): pp 286

FLIP-FLOPS

- D Latch:



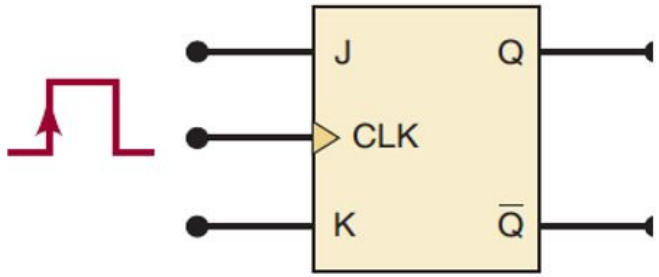
Set	Reset	Output
1	1	No change
0	1	Q = 1
1	0	Q = 0
0	0	Invalid *

*Produces $Q = \overline{Q} = 1$.

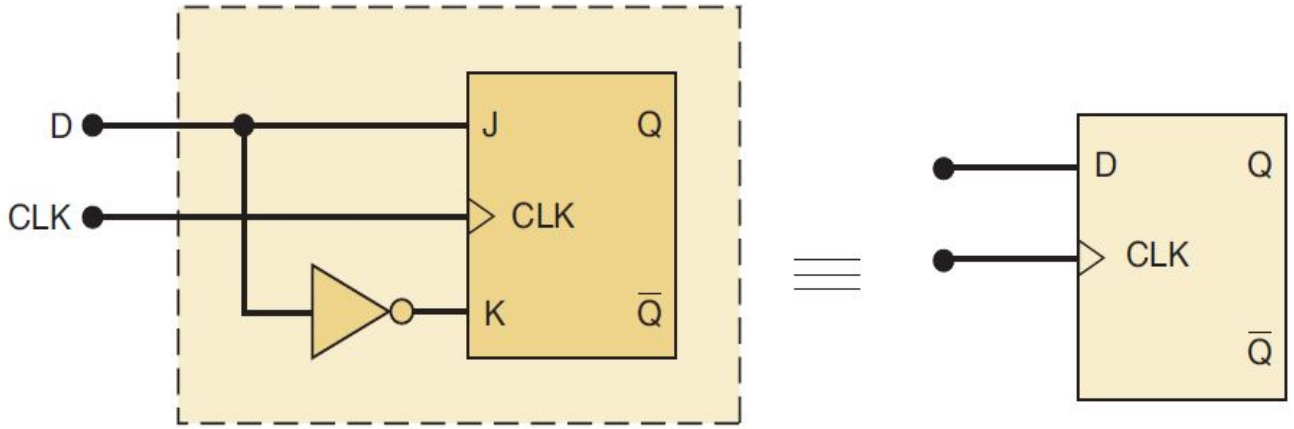
Clk	D	$Q(t+1)$
0	x	$Q(t)$
1	0	0
1	1	1

FLIP-FLOPS

- Clocked D Flip-flop:

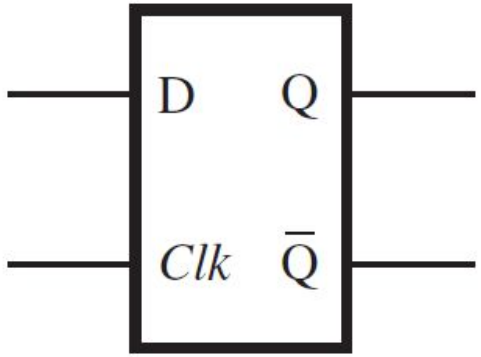


J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

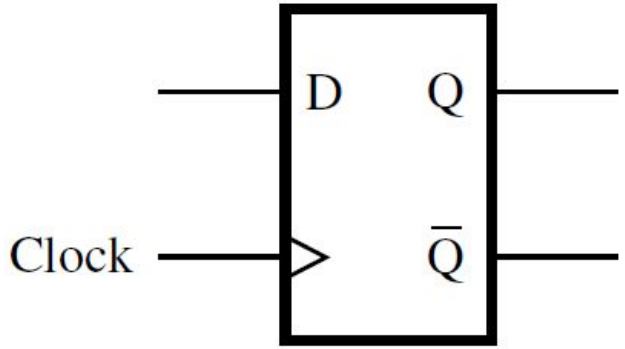


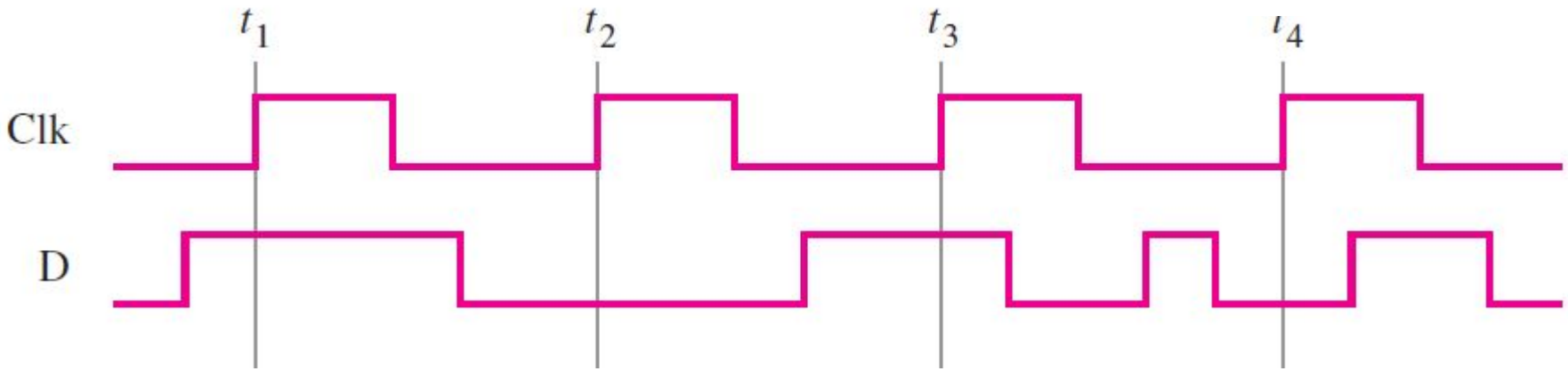
FLIP-FLOPS

- Clocked D Flip-flop:



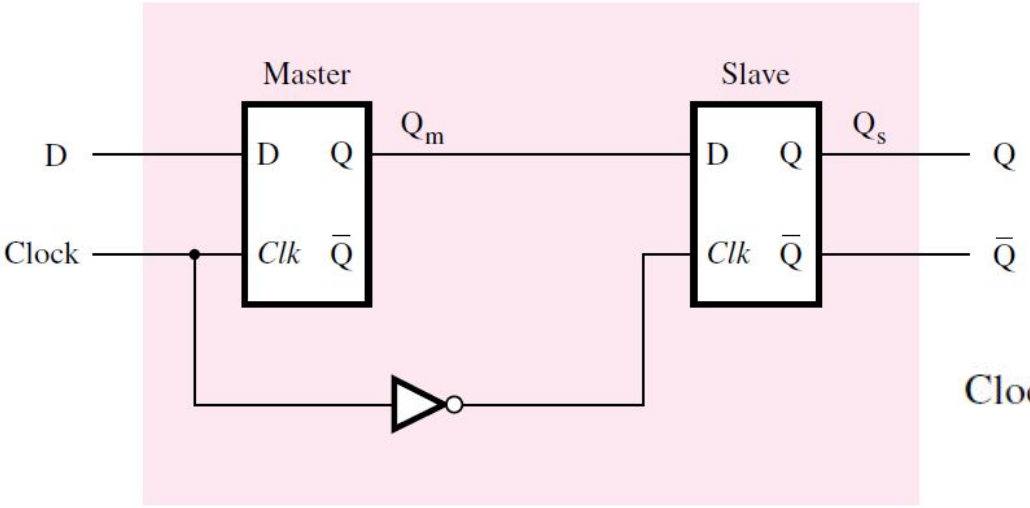
Clk	D	Q(t + 1)
0	x	Q(t)
1	0	0
1	1	1

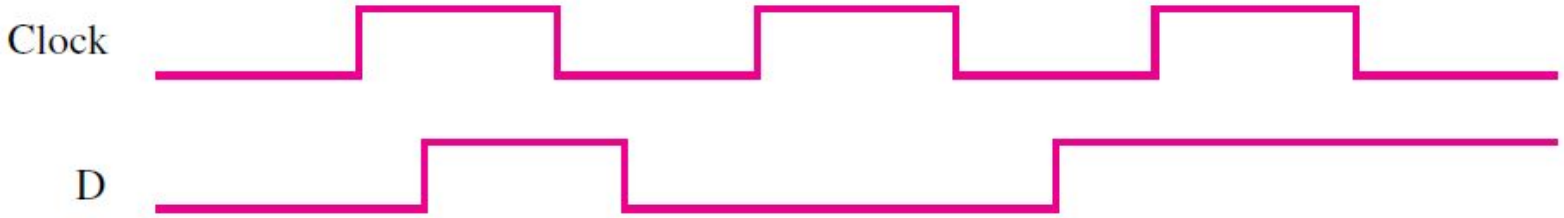




FLIP-FLOPS

- Clocked D Latch:

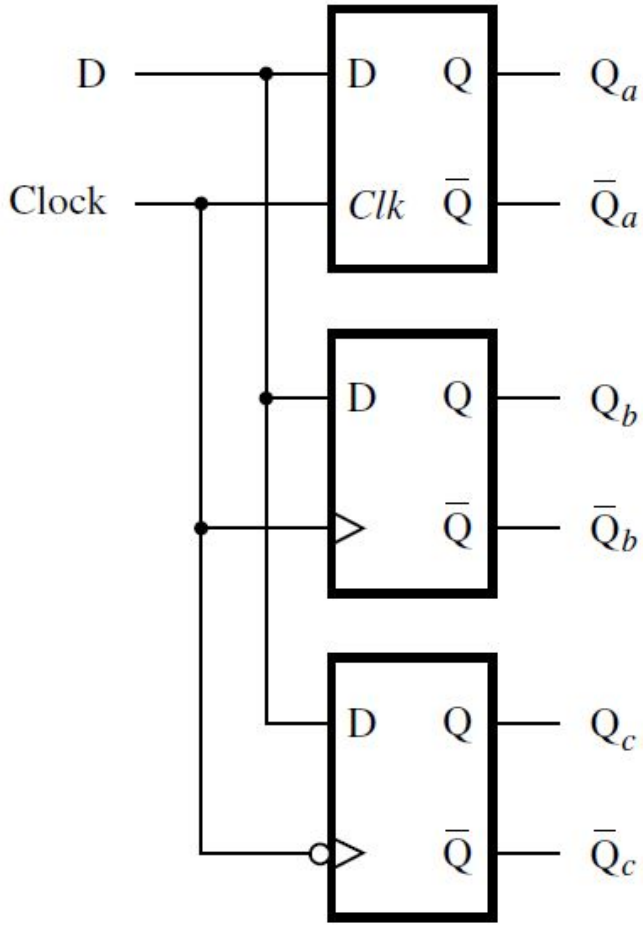


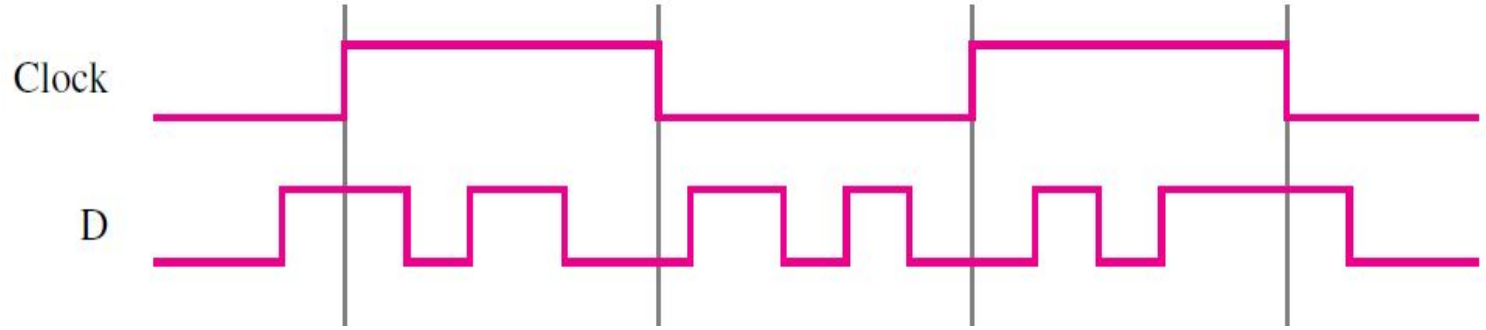


Clk	D	Q(t + 1)
0	x	Q(t)
1	0	0
1	1	1

FLIP-FLOPS

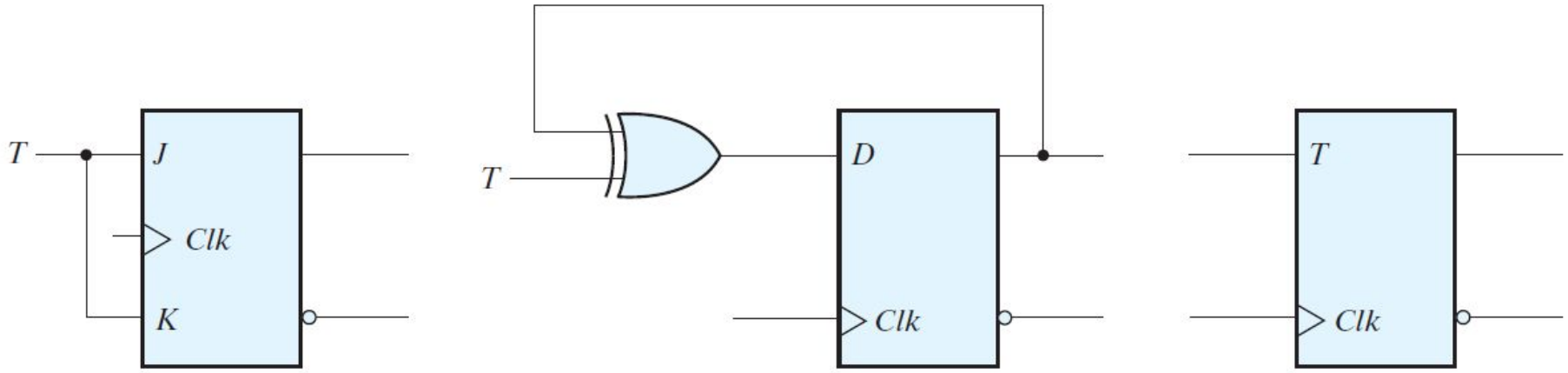
- Clocked D Flip-flop and latch:





FLIP-FLOPS

- Clocked T Flip-flop:



JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D Flip-Flop

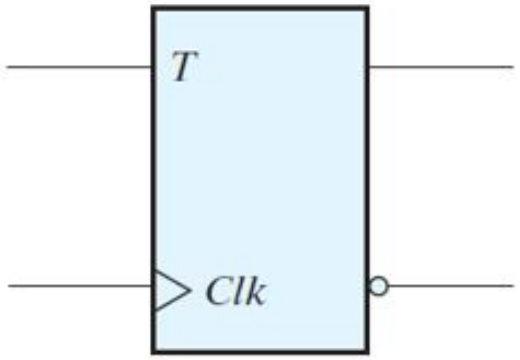
D	Q(t + 1)	
0	0	Reset
1	1	Set

T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

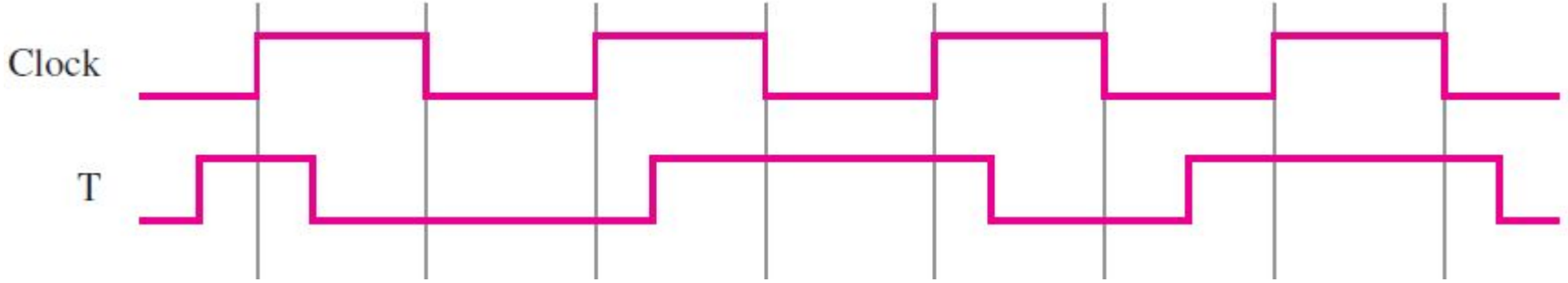
FLIP-FLOPS

- Clocked T Flip-flop:



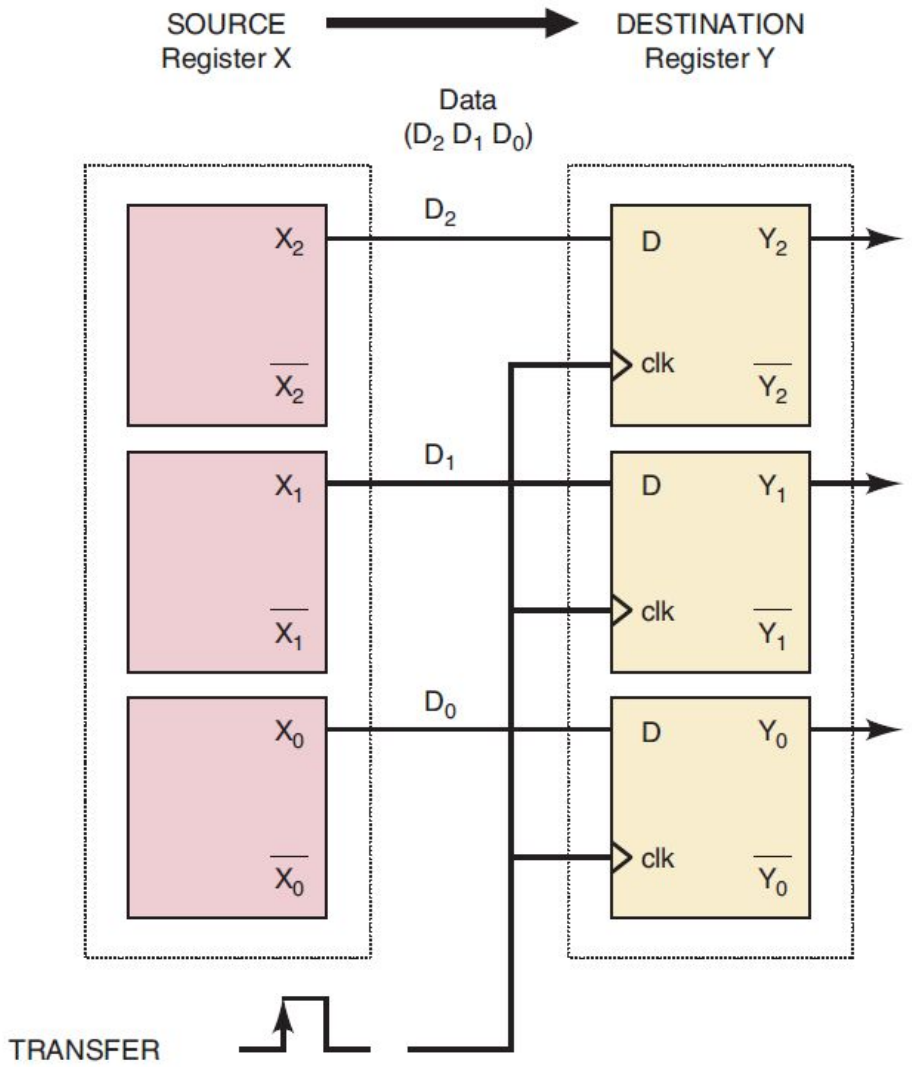
T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement



FLIP-FLOPS

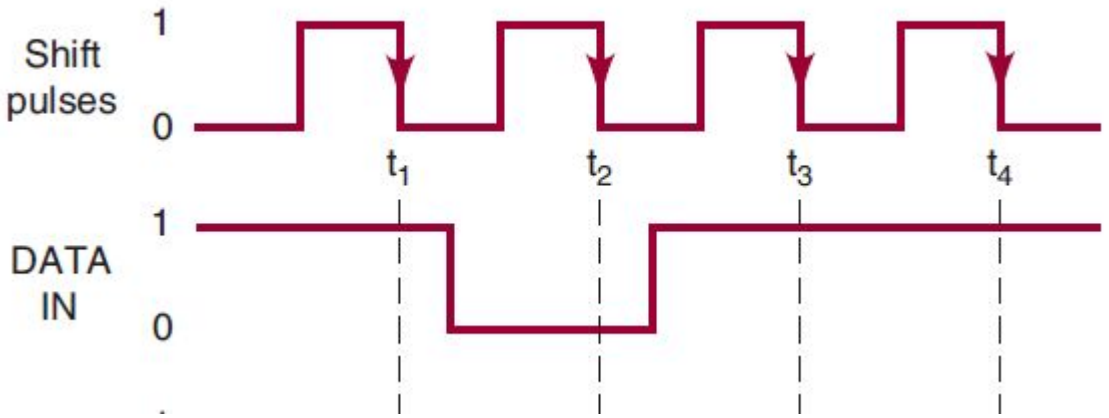
- Parallel data transfer:

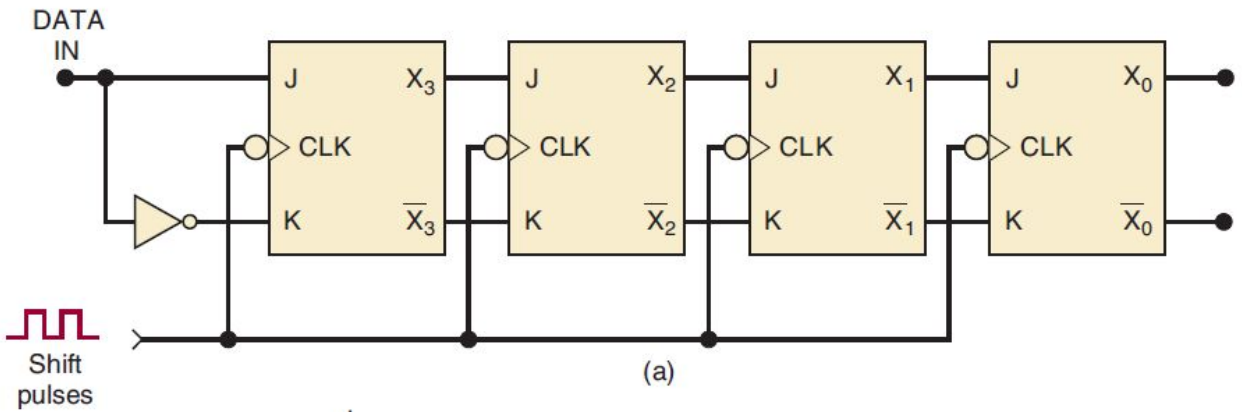


Ref (1): pp 297

FLIP-FLOPS

- Serial data transfer (Shift register):

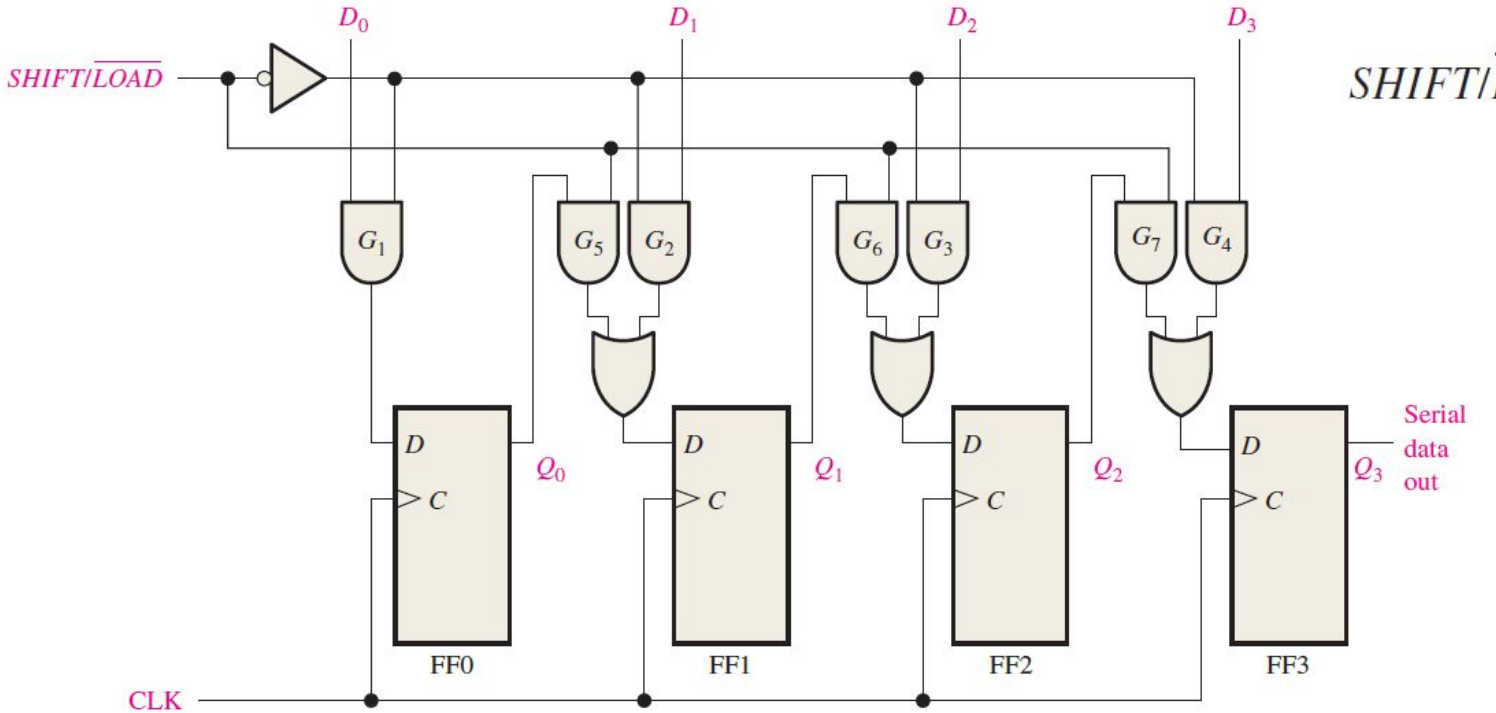


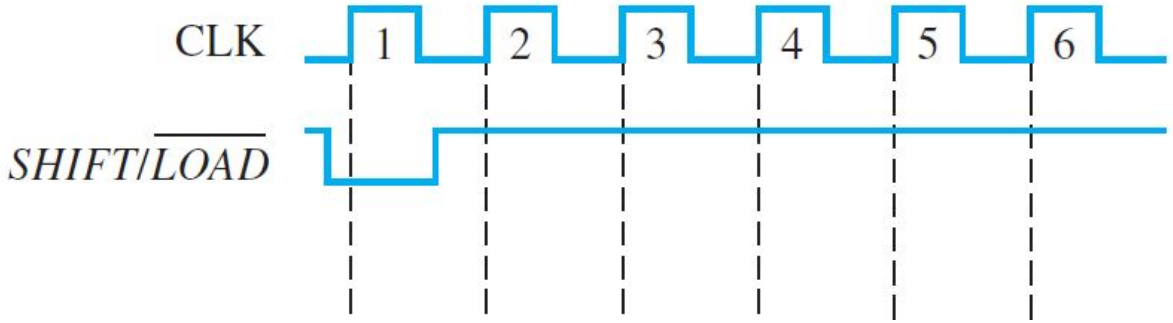


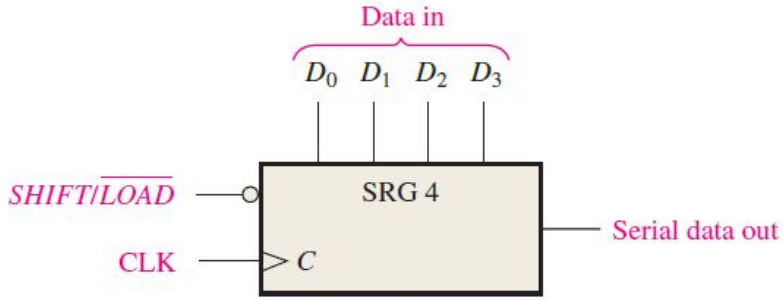
Ref (1): pp 299

FLIP-FLOPS

- Parallel data in/ serial data out Shift register:





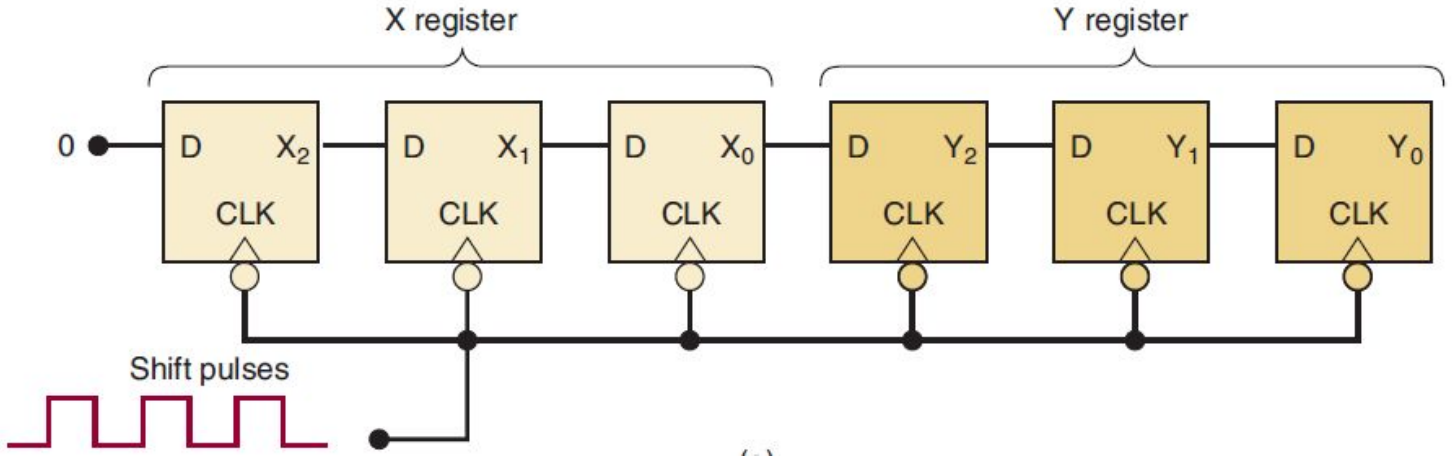


Ref (3): pp 457

FLIP-FLOPS

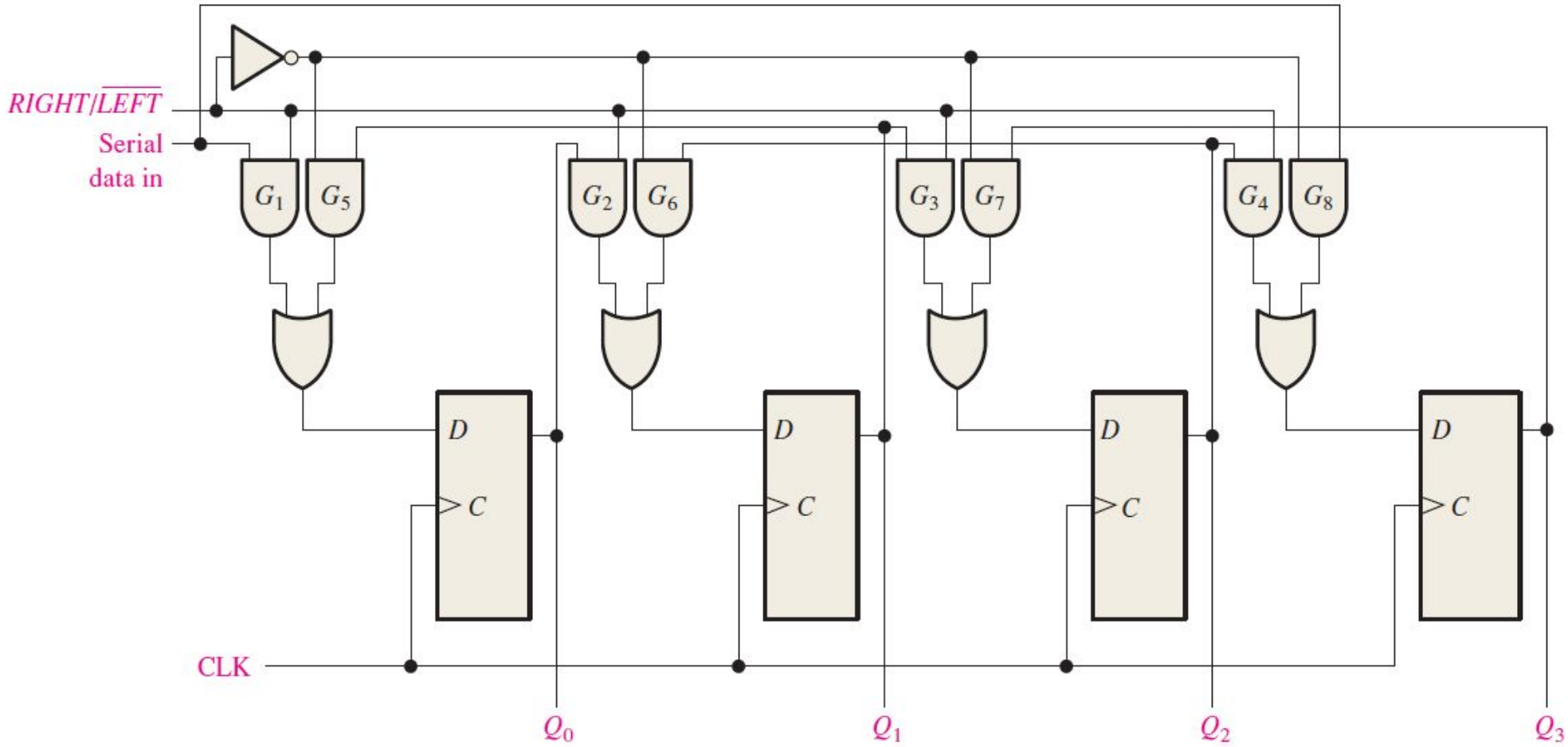
- Serial transfer between registers:

X_2	X_1	X_0	Y_2	Y_1	Y_0	
1	0	1	0	0	0	← Before puls



FLIP-FLOPS

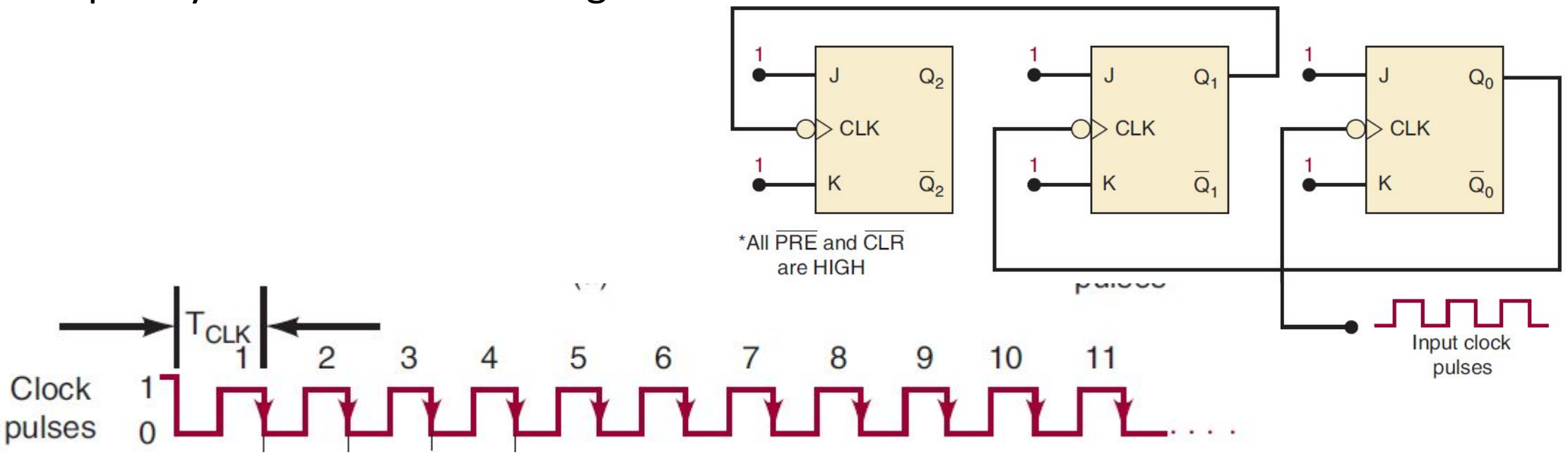
- Bi-directional shift registers:



Ref (3): pp 462

FLIP-FLOPS

- Frequency division and counting:



Ref (1): pp 299