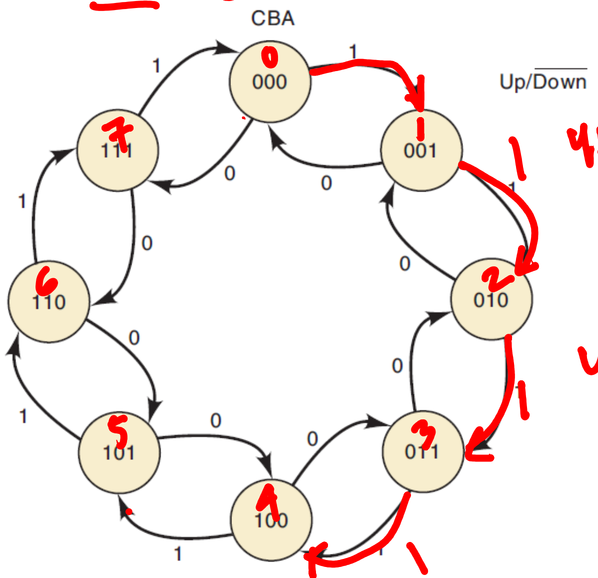
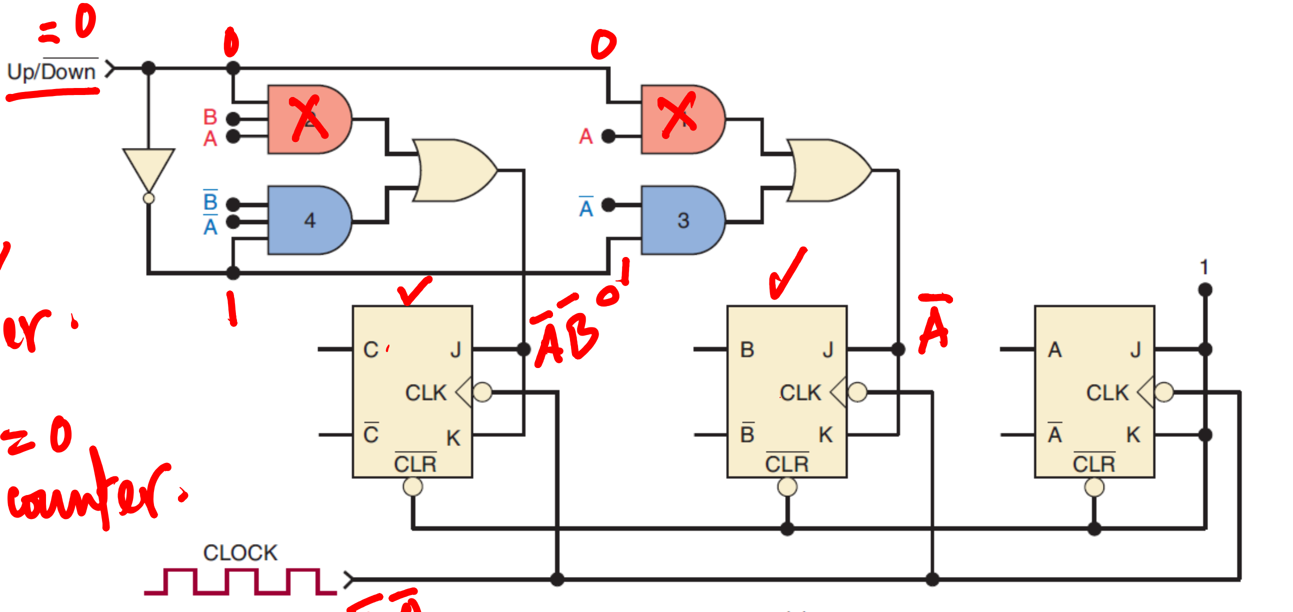
COUNTER CIRCUIT

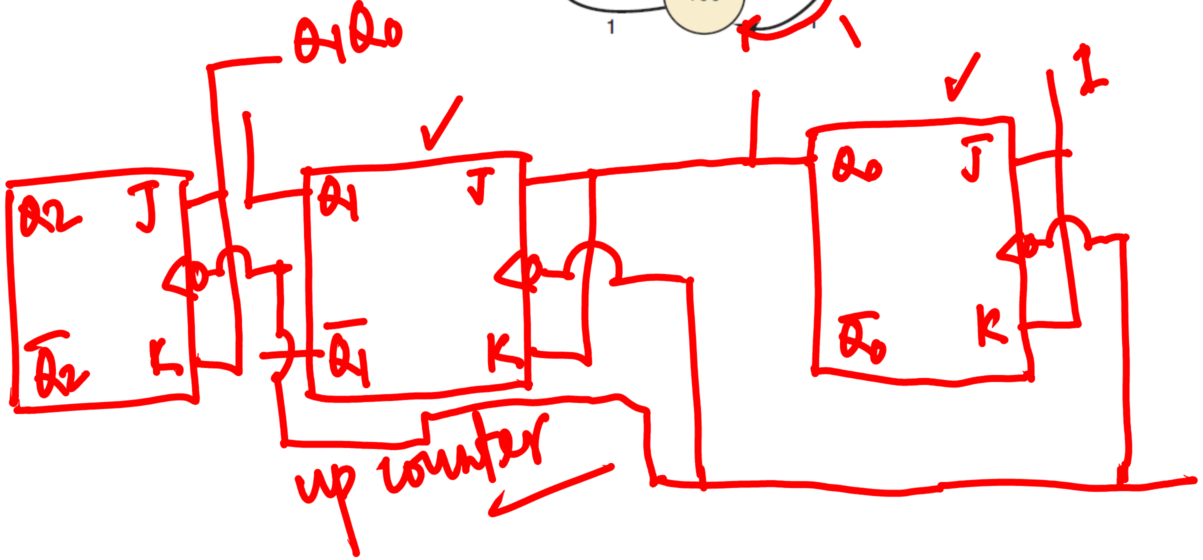
- Synchronous up/down counter:

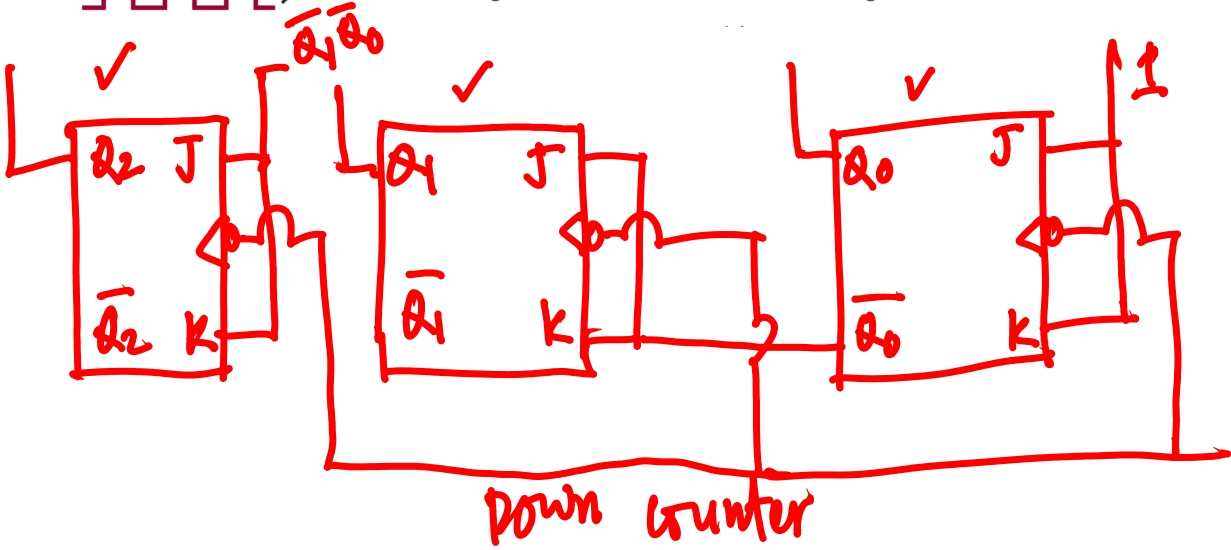


up/down = 1, up counter.

up/down = 0 down counter.







COUNTER CIRCUIT

0 → 0000

- BCD counter: (up counter) (T flip-flop) · (4 bit)

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	T_{Q8}	T_{Q4}	T_{Q2}	T_{Q1}
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

T_{Q4}, T_{Q8} } → practice.

$$T_{Q1} = 1$$
$$T_{Q2} = Q_8'Q_1$$
$$T_{Q4} = Q_2Q_1$$
$$T_{Q8} = Q_8Q_1 + Q_4Q_2Q_1$$
$$y = Q_8Q_1$$

T_{Q1}

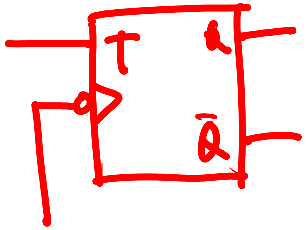
$Q_8Q_4 \backslash Q_2Q_1$	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

$T_{Q1} = 1$

T_{Q2}

$Q_8Q_4 \backslash Q_2Q_1$	00	01	11	10
00		1	1	
01		1	1	
11	X	X	X	X
10			X	X

$T_{Q2} = \bar{Q}_8 Q_1$



T	Q
0	NC
1	Toggle.

Ref (2): pp 363-364

COUNTER CIRCUIT

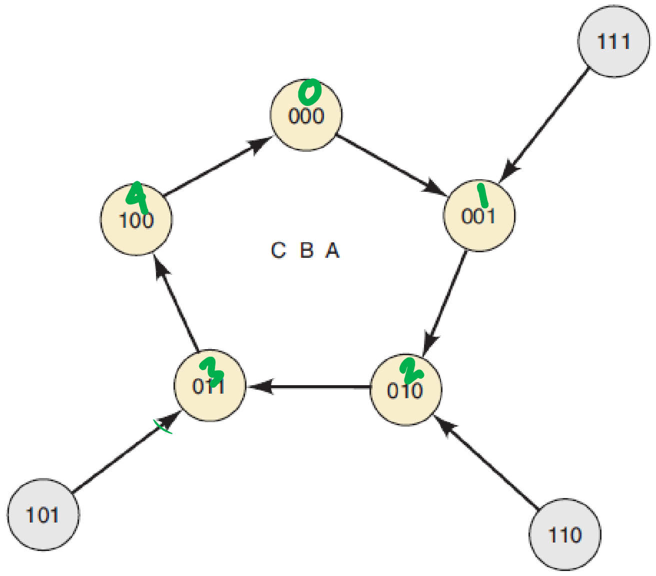
- Synchronous counter with different control input:

- A circuit with n flip-flops has 2^n binary states. There are occasions when a sequential circuit uses fewer than this maximum possible number of states.

- States that are not used in specifying the sequential circuit are not listed in the state table.

- In simplifying the input equations, the unused states may be treated as don't-care conditions or may be assigned specific next states

PRESENT State			Control Inputs						NEXT State		
C	B	A	J_C	K_C	J_B	K_B	J_A	K_A	C	B	A
0	0	0	0	0	0	0	1	1	0	0	1
0	0	1	0	0	1	1	1	1	0	1	0
0	1	0	0	0	0	0	1	1	0	1	1
0	1	1	1	0	1	1	1	1	1	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	1	0	1	1	1	0	0	0	1	1
1	1	0	0	1	0	0	0	0	0	1	0
1	1	1	1	1	1	1	0	0	0	0	1



Ref (1): pp 465

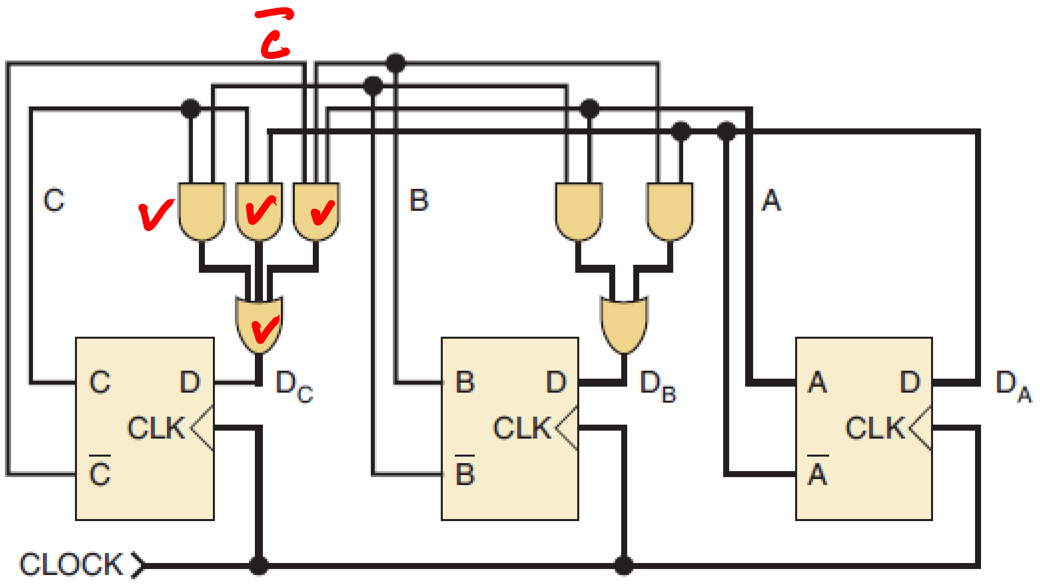
COUNTER CIRCUIT

- Synchronous counter with different control input:

	PRESENT State				NEXT State			Control Inputs		
	C	B	A		C	B	A	D_C	D_B	D_A
0→	0	0	0	1→	0	0	1	0	0	1 ✓
1→	0	0	1	2→	0	1	0	0	1	0
2→	0	1	0	3→	0	1	1	0	1	1
3→	0	1	1	4→	1	0	0	1	0	0
4→	1	0	0	5→	1	0	1	1	0	1
5→	1	0	1	6→	1	1	0	1	1	0
6→	1	1	0	7→	1	1	1	1	1	1
7→	1	1	1	0→	0	0	0	0	0	0

DC

Clk	D	$Q(t+1)$
0	x	$Q(t)$
↑	0	0
↑	1	1



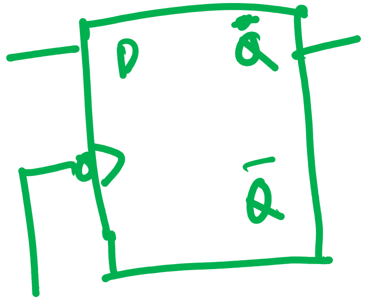
CB \ A	0	1
00		
01		1
11	1	
10	1	1

→ $\bar{C}BA$

→ $C\bar{A}$

→ $C\bar{B}$

$$D_C = \bar{C}BA + C\bar{A} + C\bar{B}$$



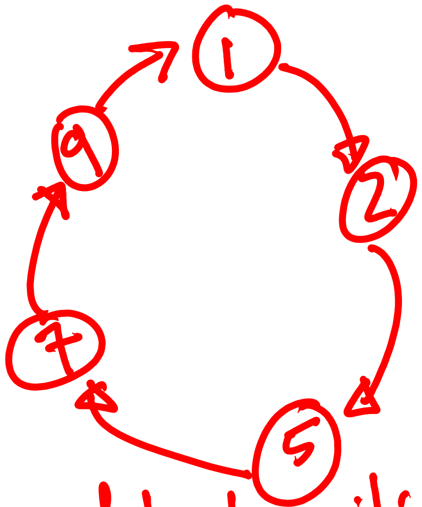
COUNTER CIRCUIT

- Synchronous counter with different control input:

- Homework:

PRESENT State			NEXT State		
C	B	A	C	B	A
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

T →



state transition diagram.

***T* Flip-Flop**

T	$Q(t+1)$	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

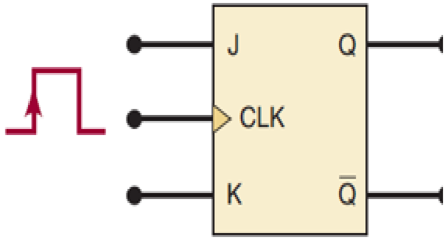
Ref (1): pp 466

COUNTER CIRCUIT

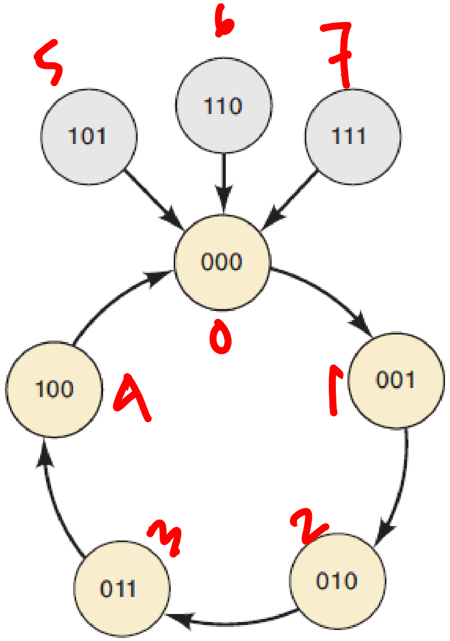
- Synchronous counter with different control input:

- J-K excitation Table:

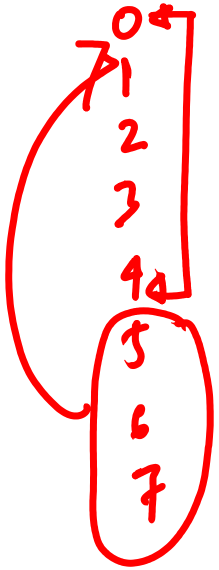
Transition at FF Output	PRESENT State Q_n	NEXT State Q_{n+1}	J	K
$0 \rightarrow 0$	0	0	0	x
$0 \rightarrow 1$	0	1	1	x
$1 \rightarrow 0$	1	0	x	1
$1 \rightarrow 1$	1	1	x	0



J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\bar{Q}_0$ (toggles)



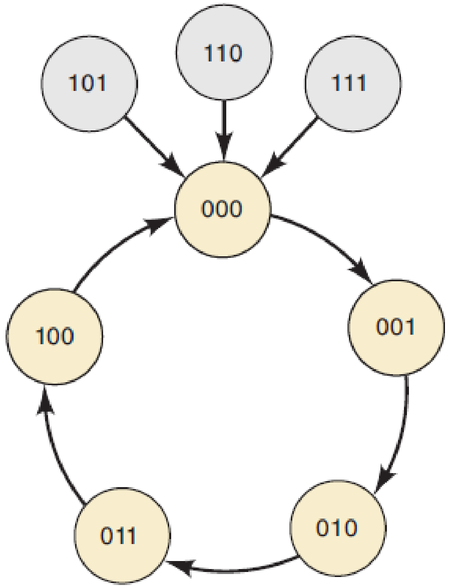
State		PRESENT State C	B	A	NEXT State C	B	A	J_C	K_C	J_B	K_B	J_A	K_A
0	Line 1	0	0	0	0	0	1	0	x	0	x	1	x
1	2	0	0	1	0	1	0	0	x	1	x	x	1
2	3	0	1	0	0	1	1	0	x	x	0	1	x
3	4	0	1	1	1	0	0	1	x	x	1	x	1
4	5	1	0	0	0	0	0	x	1	0	x	0	x
5	6	1	0	1	0	0	0	x	1	0	x	x	1
6	7	1	1	0	0	0	0	x	1	x	1	0	x
7	8	1	1	1	0	0	0	x	1	x	1	x	1



Ref (1): pp 469-470

COUNTER CIRCUIT

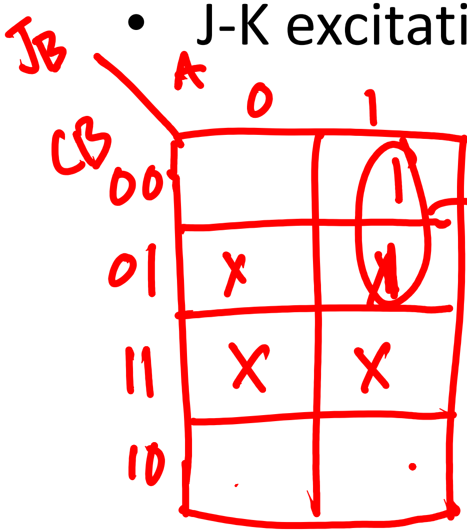
- Synchronous counter with different control input:
- J-K excitation Table:



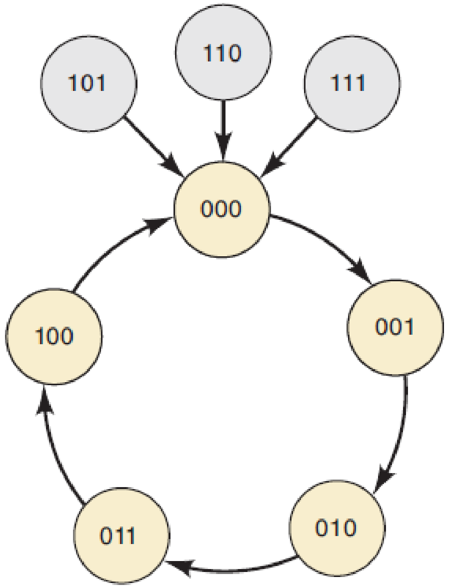
	PRESENT State			NEXT State								
	C	B	A	C	B	A	J_C	K_C	J_B	K_B	J_A	K_A
Line 1	0	0	0	0	0	1	0	x	0	x	1	x
2	0	0	1	0	1	0	0	x	1	x	x	1
3	0	1	0	0	1	1	0	x	x	0	1	x
4	0	1	1	1	0	0	1	x	x	1	x	1
5	1	0	0	0	0	0	x	1	0	x	0	x
6	1	0	1	0	0	0	x	1	0	x	x	1
7	1	1	0	0	0	0	x	1	x	1	0	x
8	1	1	1	0	0	0	x	1	x	1	x	1

COUNTER CIRCUIT

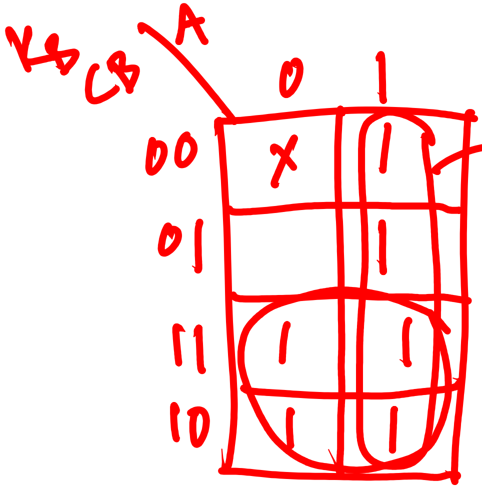
- Synchronous counter with different control input:
- J-K excitation Table:



$J_B = \bar{C}A$

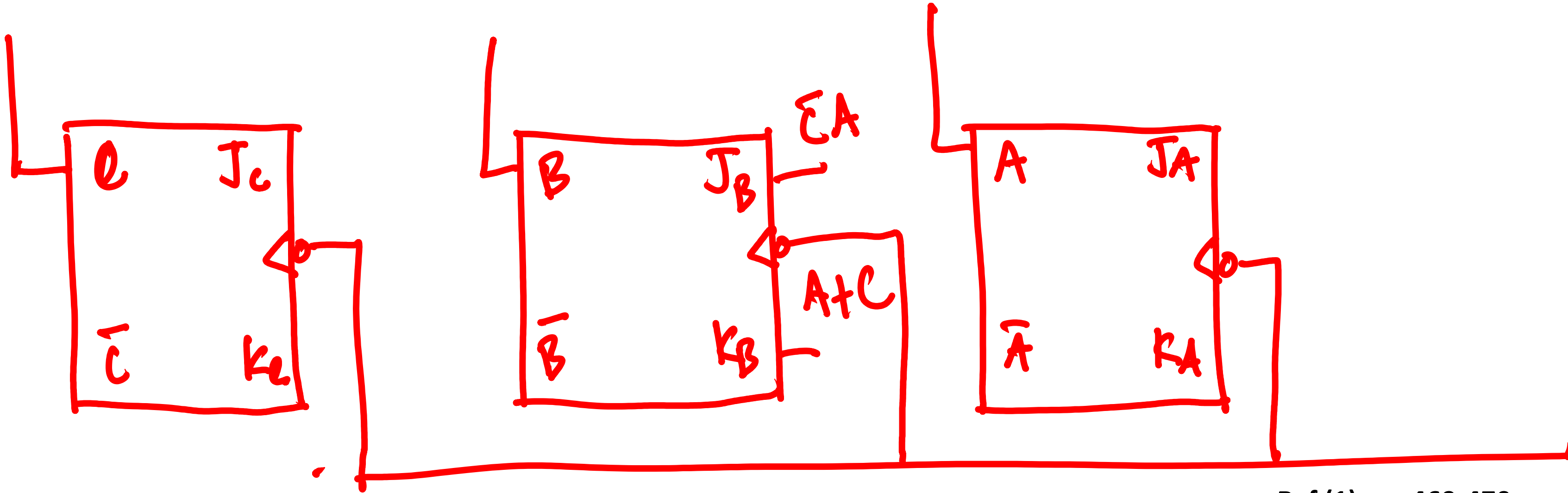


	PRESENT State			NEXT State								
	C	B	A	C	B	A	J_C	K_C	J_B	K_B	J_A	K_A
Line 1	0	0	0	0	0	1	0	x	0	x	1	x
2	0	0	1	0	1	0	0	x	1	x	x	1
3	0	1	0	0	1	1	0	x	x	0	1	x
4	0	1	1	1	0	0	1	x	x	1	x	1
5	1	0	0	0	0	0	x	1	0	x	0	x
6	1	0	1	0	0	0	x	1	0	x	x	1
7	1	1	0	0	0	0	x	1	x	1	0	x
8	1	1	1	0	0	0	x	1	x	1	x	1



$K_B = A + C$

LSB

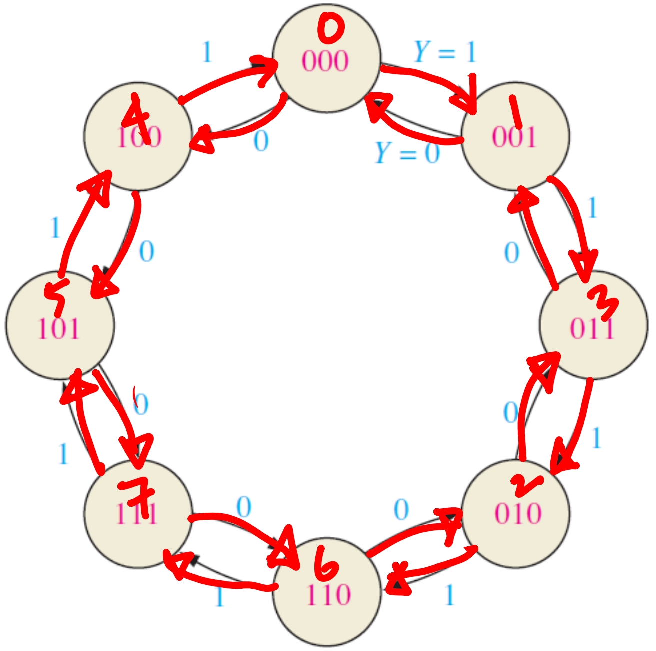


Ref (1): pp 469-470

COUNTER CIRCUIT

Y control command.

Develop a synchronous 3-bit up/down counter with a Gray code sequence using J-K flip-flops. The counter should count up when an UP/$\overline{\text{DOWN}}$ control input is 1 and count down when the control input is 0.



Next-state table for 3-bit up/down Gray code counter.

Present State			Next State Y = 0 (DOWN)			Next State Y = 1 (UP)		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0→ 0	0	0	4→ 1	0	0	1→ 0	0	1
1→ 0	0	1	0→ 0	0	0	3→ 0	1	1
3→ 0	1	1	1→ 0	0	1	2→ 0	1	0
2→ 0	1	0	3→ 0	1	1	6→ 1	1	0
6→ 1	1	0	2→ 0	1	0	7→ 1	1	1
7→ 1	1	1	6→ 1	1	0	5→ 1	0	1
5→ 1	0	1	7→ 1	1	1	4→ 1	0	0
4→ 1	0	0	5→ 1	0	1	0→ 0	0	0

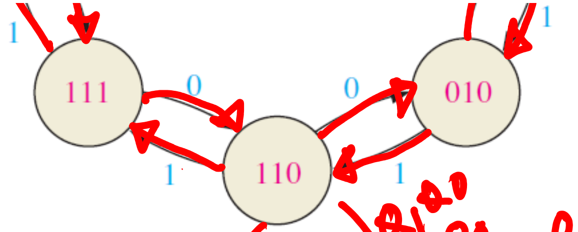
Y = UP/$\overline{\text{DOWN}}$ control input.

Ref (1): pp 469-470

COUNTER CIRCUIT

Develop a synchronous 3-bit up/down counter with a Gray code sequence using J-K flip-flops. The counter should count up when an UP/$\overline{\text{DOWN}}$ control input is 1 and count down when the control input is 0.

Transition at FF Output	PRESENT State Q_n	NEXT State Q_{n+1}	J	K
$0 \rightarrow 0$	0	0	0	x
$0 \rightarrow 1$	0	1	1	x
$1 \rightarrow 0$	1	0	x	1
$1 \rightarrow 1$	1	1	x	0



Y	Present stage Q_2	Q_1	Q_0	next stage Q_2^+	Q_1^+	Q_0^+	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	1	0	0	1	X				
0	0	0	1	0	0	0	0	X				
0	0	1	0	0	1	1	0	X				
0	0	1	1	0	0	1	0	X				
0	1	0	0	1	0	1	X	0				
0	1	0	1	1	1	1	X	0				
0	1	1	0	0	1	0	X	1				
0	1	1	1	1	1	0	X	0				
1	0	0	0	0	0	1	0	X				
1	0	0	1	0	1	1	0	X				
1	0	1	0	1	1	0	1	X				
1	0	1	1	0	1	0	0	X				
1	1	0	0	0	0	0	X	1				
1	1	0	1	1	0	0	X	0				
1	1	1	0	1	1	1	X	0				
1	1	1	1	1	0	1	X	0				

J_2

$YQ_2 \backslash Q_1Q_0$	00	01	11	10
00	1			
01	1	X	X	X
11	X	X	X	1
10				1

$\bar{Y}\bar{Q}_1\bar{Q}_0$

$Y Q_1 \bar{Q}_0$

$J_2 = \bar{Y}\bar{Q}_1\bar{Q}_0 + Y Q_1 \bar{Q}_0$

COUNTER CIRCUIT

Develop a synchronous 3-bit up/down counter with a Gray code sequence using J-K flip-flops. The counter should count up when an UP/$\overline{\text{DOWN}}$ control input is 1 and count down when the control input is 0.

Next-state table for 3-bit up/down Gray code counter.

Present State			Next State					
			$Y = 0$ (DOWN)			$Y = 1$ (UP)		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	1	1	0	0	1	0	1	0
0	1	0	0	1	1	1	1	0
1	1	0	0	1	0	1	1	1
1	1	1	1	1	0	1	0	1
1	0	1	1	1	1	1	0	0
1	0	0	1	0	1	0	0	0

$Y =$ UP/$\overline{\text{DOWN}}$ control input.

$$J_0 = Q_2Q_1Y + Q_2\overline{Q}_1\overline{Y} + \overline{Q}_2\overline{Q}_1Y + \overline{Q}_2Q_1\overline{Y}$$
$$J_1 = \overline{Q}_2Q_0Y + Q_2Q_0\overline{Y}$$
$$J_2 = Q_1\overline{Q}_0Y + \overline{Q}_1\overline{Q}_0\overline{Y}$$

$$K_0 = \overline{Q}_2\overline{Q}_1\overline{Y} + \overline{Q}_2Q_1Y + Q_2\overline{Q}_1Y + Q_2Q_1\overline{Y}$$
$$K_1 = \overline{Q}_2Q_0\overline{Y} + Q_2Q_0Y$$
$$K_2 = Q_1\overline{Q}_0\overline{Y} + \overline{Q}_1\overline{Q}_0Y$$

	00	01	11	10
00	m_0	m_1	m_3	m_2
01	m_4	m_5	m_7	m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}

	00	01	11	10
00	m_0	m_1	m_3	m_2
01	m_4	m_5	m_7	m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}

	00	01	11	10
00	m_0	m_1	m_3	m_2
01	m_4	m_5	m_7	m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}

	00	01	11	10
00	m_0	m_1	m_3	m_2
01	m_4	m_5	m_7	m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}

Ref (1): pp 469-470