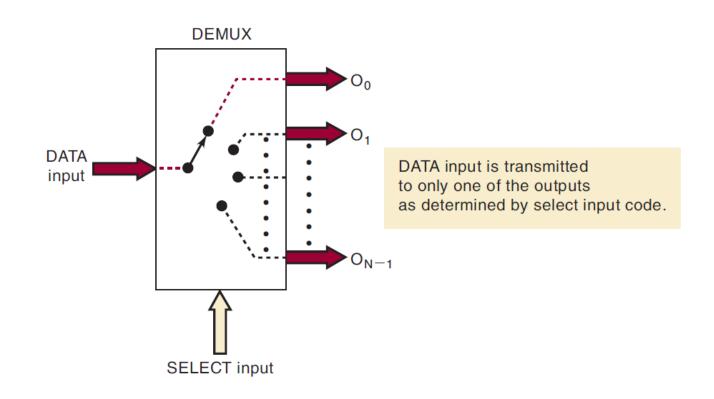
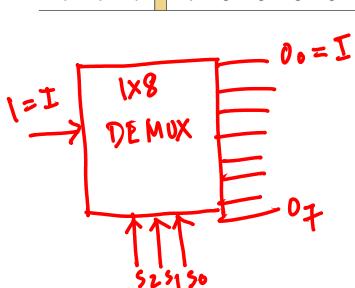
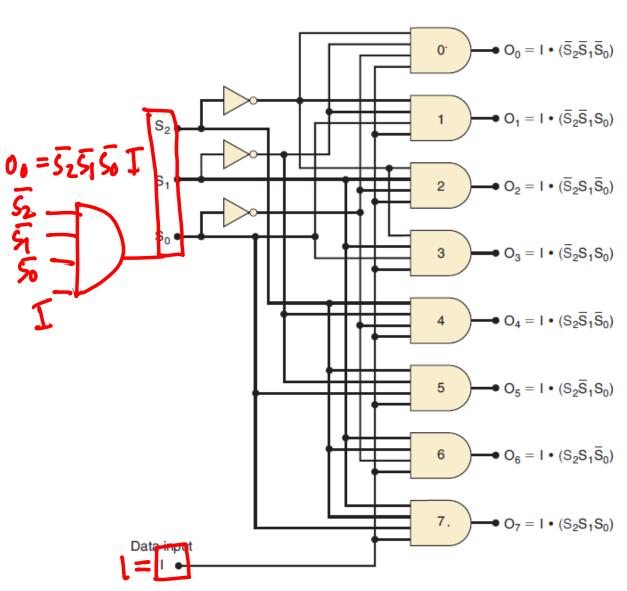
- A demultiplexer circuit performs the opposite operations of multiplexer circuit.
- It takes one input and distributes it over several outputs.



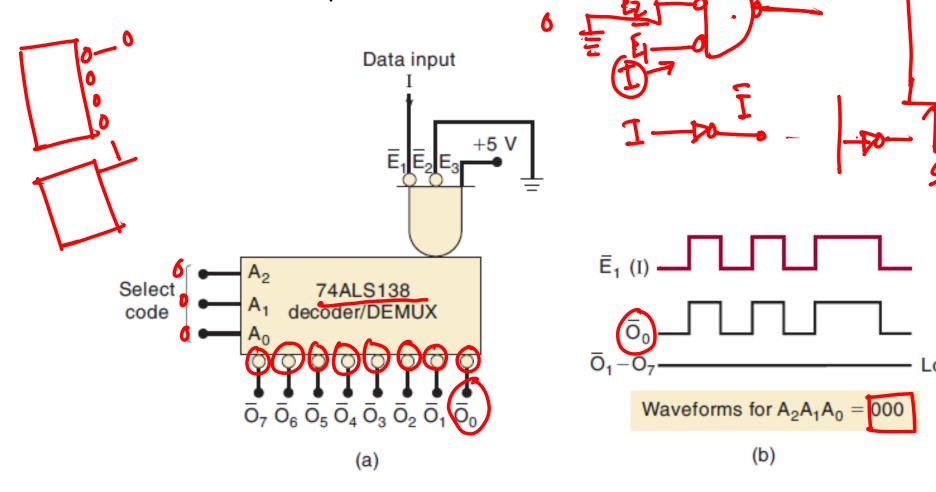
• 1-Line-to-8-Line Demultiplexer:

Select Code			Outputs							
S_2	S_1	S ₀	O ₇	O_6	O_5	O_4	O_3	O_2	01	O_0
0	0	0	0	0	0	0	0_	0	Q	
0	0	1	0	0	0	0	0	0	T	0
0	1	0	0	0	0	0	0	/	0	0
0	1	1	0	0	0	0	- 1	0	0	0
1	0	0	0	0	0	- 1	0	0	0	0
1	0	1	0	0	- 1	0	0	0	0	0
1	1	0	0	- 1	0	0	0	0	0	0
1	1	1	- 1	0	0	0	0	0	0	0

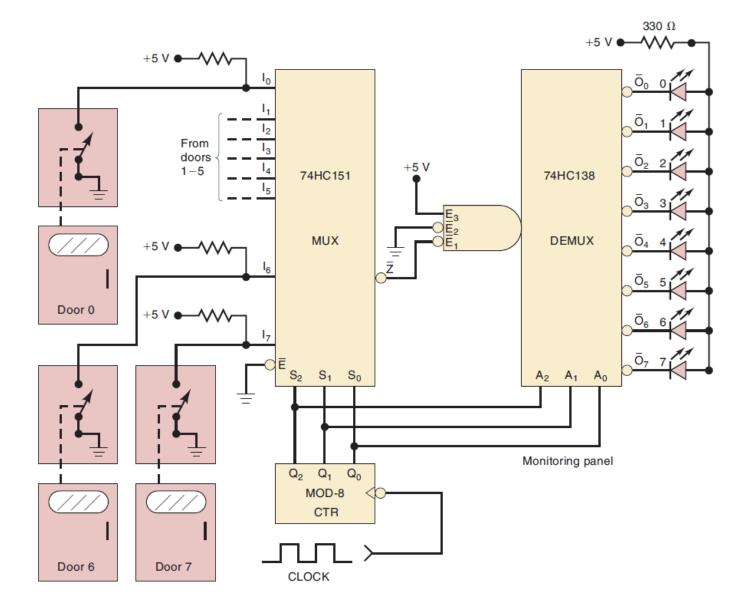




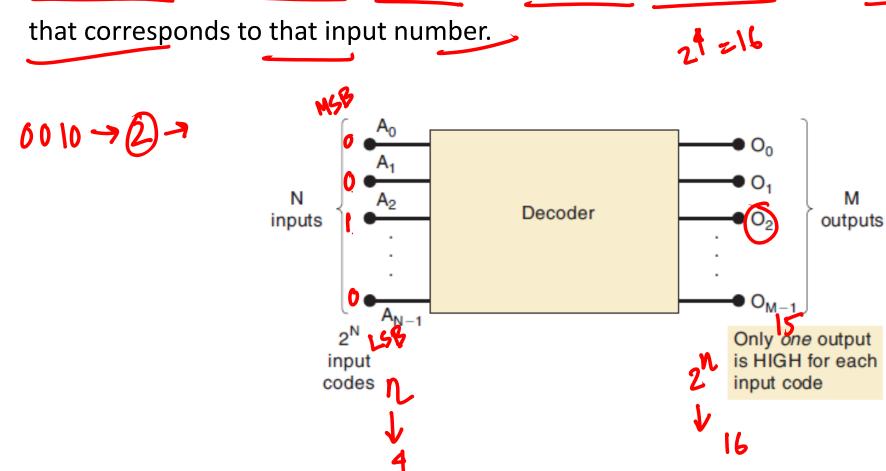
1-Line-to-8-Line Demultiplexer:

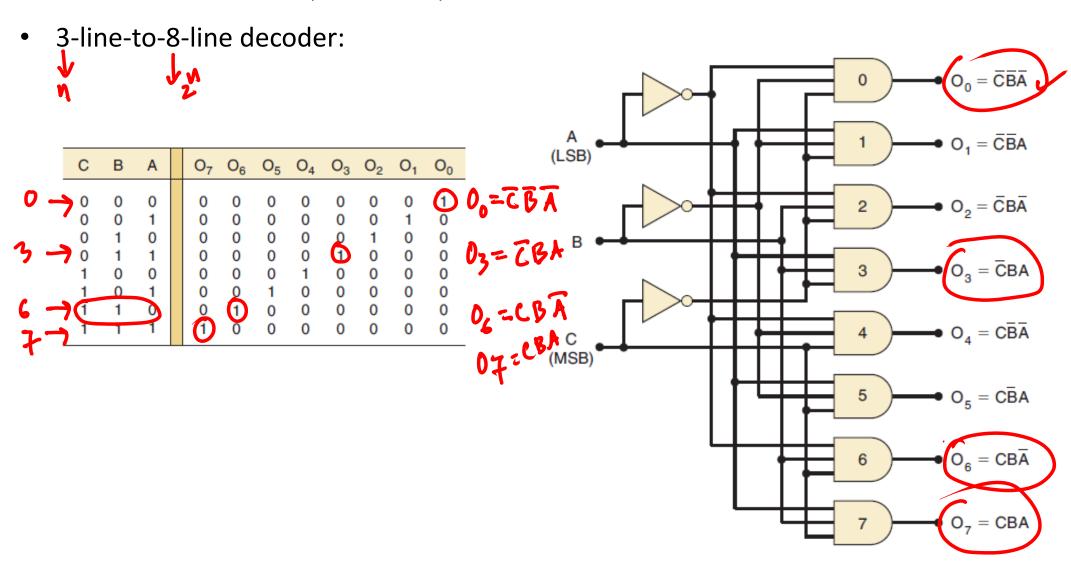


• Application:



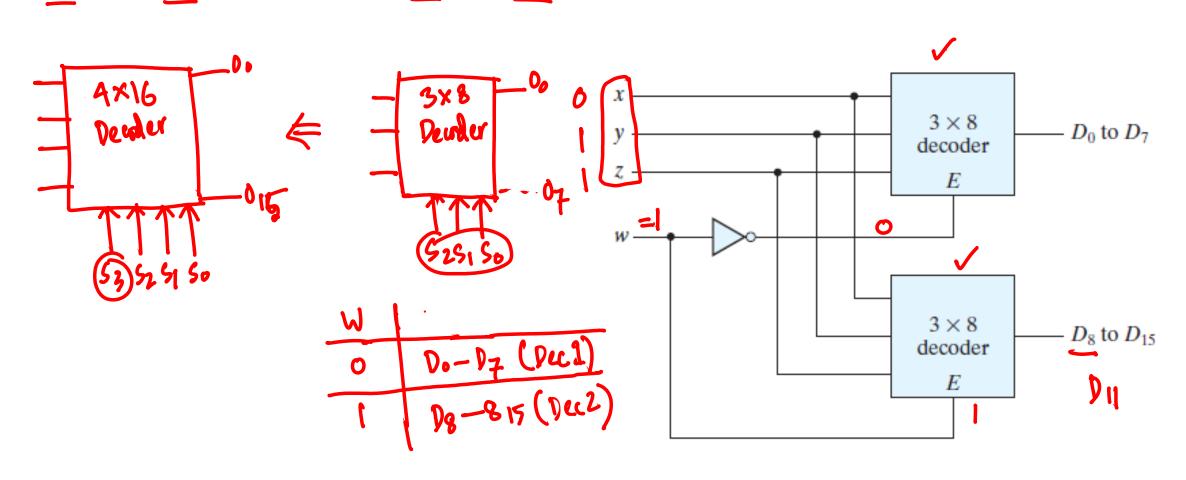
• A decoder receives a set of inputs representing a binary number and activates only the output



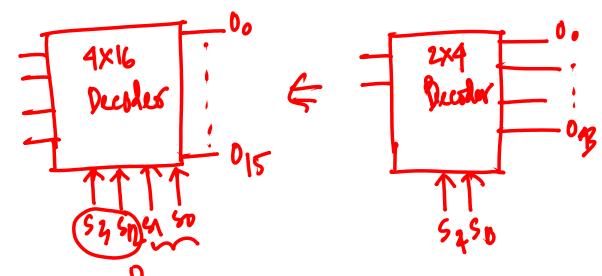


3-line-to-8-line decoder with enable input: $\overline{\mathsf{E}}_2$ Outputs (MSB) Respond to input code A₂A₁A₀ $\overline{E}_1\,\overline{E}_2\,E_3$ Disabled - all HIGH Disabled – all HIGH Disabled - all HIGH 1 of 8 eq0 eq1 E eq2 data[2..0] 74ALS138 eq3 1-of-8 decoder enable eq4 eq5 eq6 eq7 $\overline{\mathsf{O}}_7\,\overline{\mathsf{O}}_6\,\overline{\mathsf{O}}_5\,\overline{\mathsf{O}}_4\,\overline{\mathsf{O}}_3\,\overline{\mathsf{O}}_2\,\overline{\mathsf{O}}_1\,\overline{\mathsf{O}}_0$ inst1

• 4-line-to-16-line decoder with 3-line-to-8-line decoder:



4-line-to-16-line decoder with decoder tree:



M32/1 M2 NO

N3	W2	22
0	0	Jo -> Pec 1
D	1	y -> Dec2
I	0	12 7 Dec 3
ļ	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	ys -> Deca

