COUNTER CIRCUIT

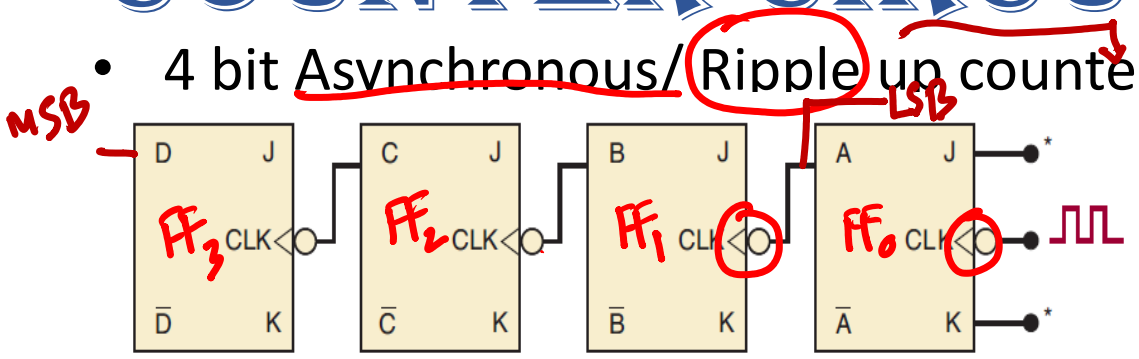
- Asynchronous counter:
  - A register that repeats prescribed sequence of states upon the application of input pulses is called a counter
  - An asynchronous counter is one in which the flip-flops (FF) within the counter do not change states at exactly the same time because they do not have a common clock pulse.

i) Asynchronous counter
ii) Synchronous "

Ref ():

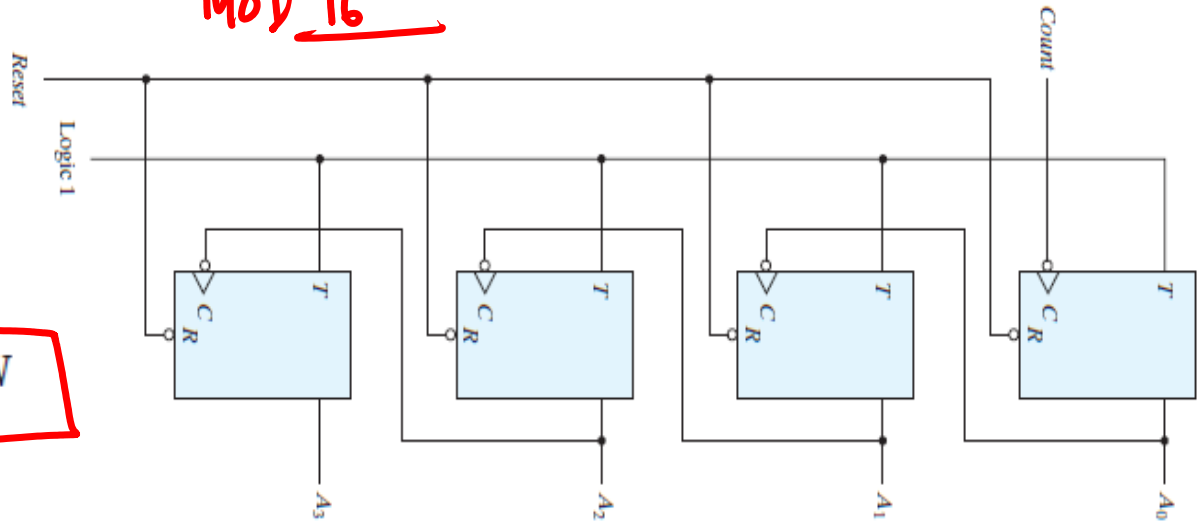
COUNTER CIRCUIT

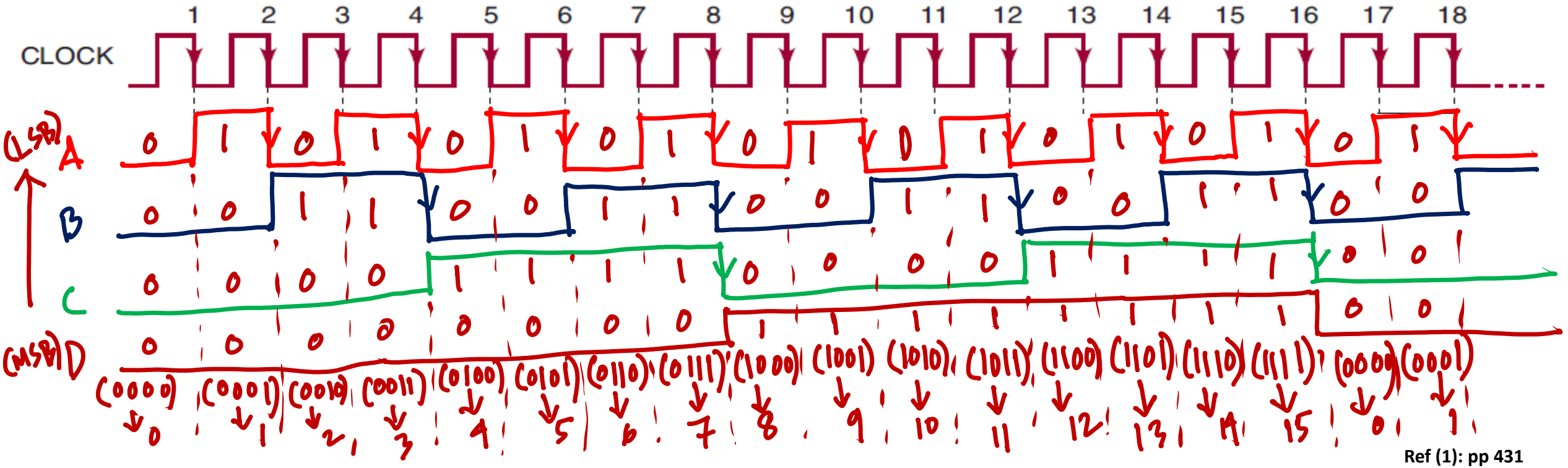
- 4 bit Asynchronous/ Ripple up counter:



$$\text{MOD number} = 2^N$$

MOD 16

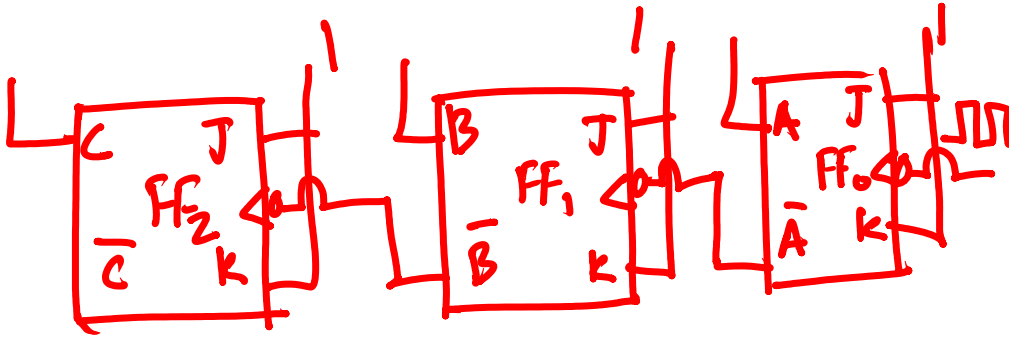




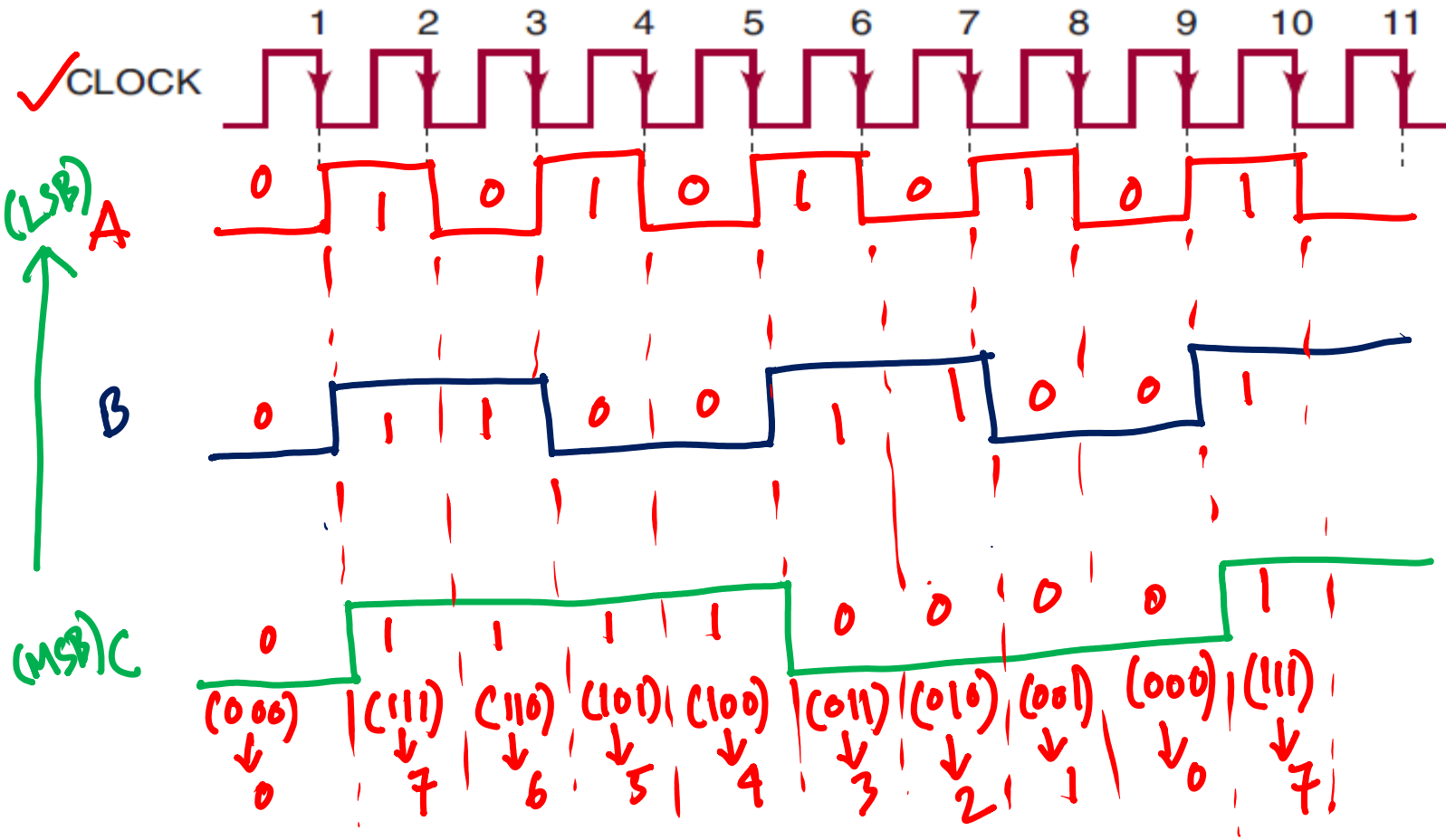
Ref (1): pp 431

COUNTER CIRCUIT

- ~~4~~ 3 bit Asynchronous/ Ripple counter (down counter):



$$\text{MOD number} = 2^N$$



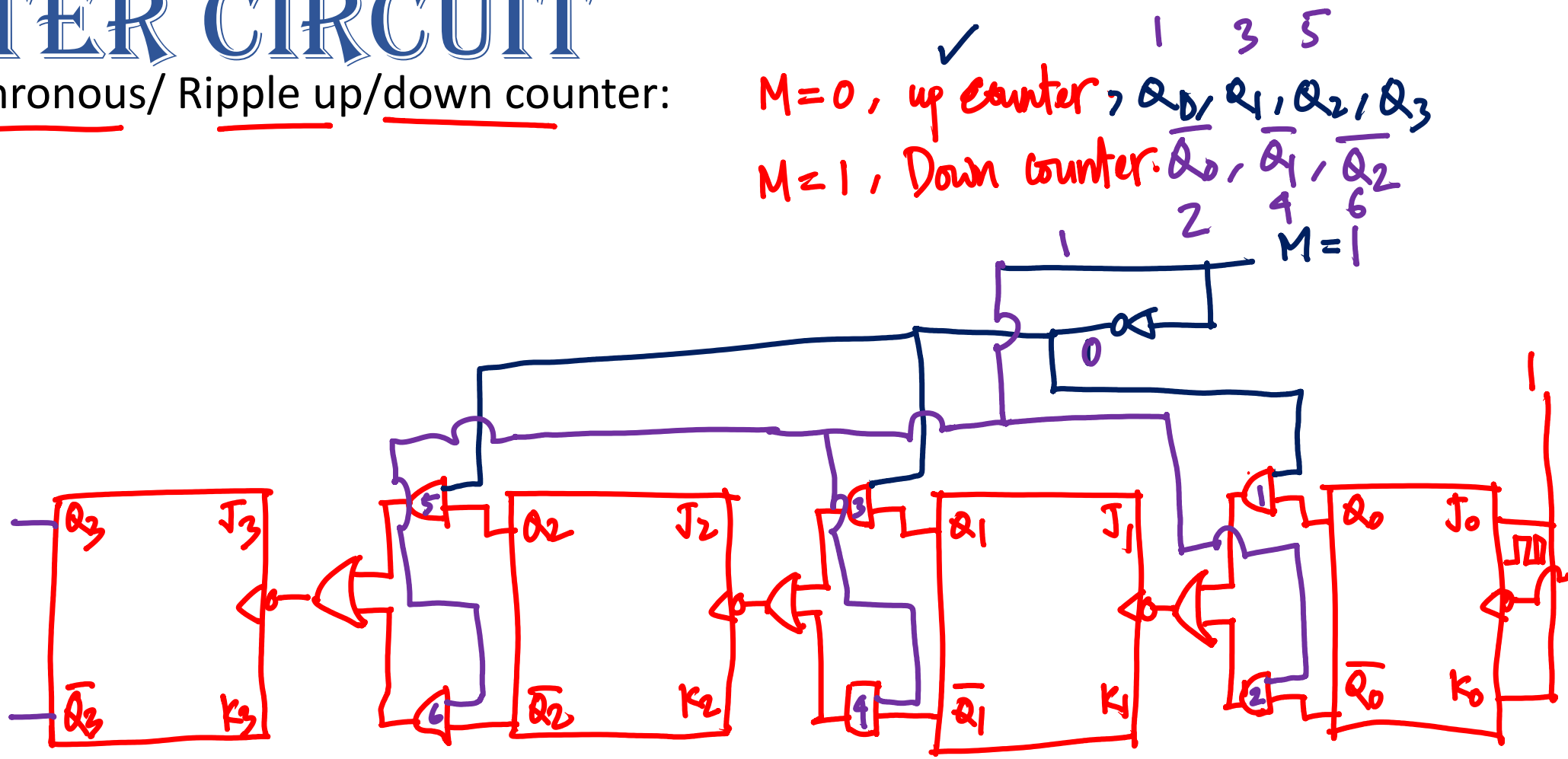
Ref (1): pp 431

COUNTER CIRCUIT

- 4 bit Asynchronous/ Ripple up/down counter:

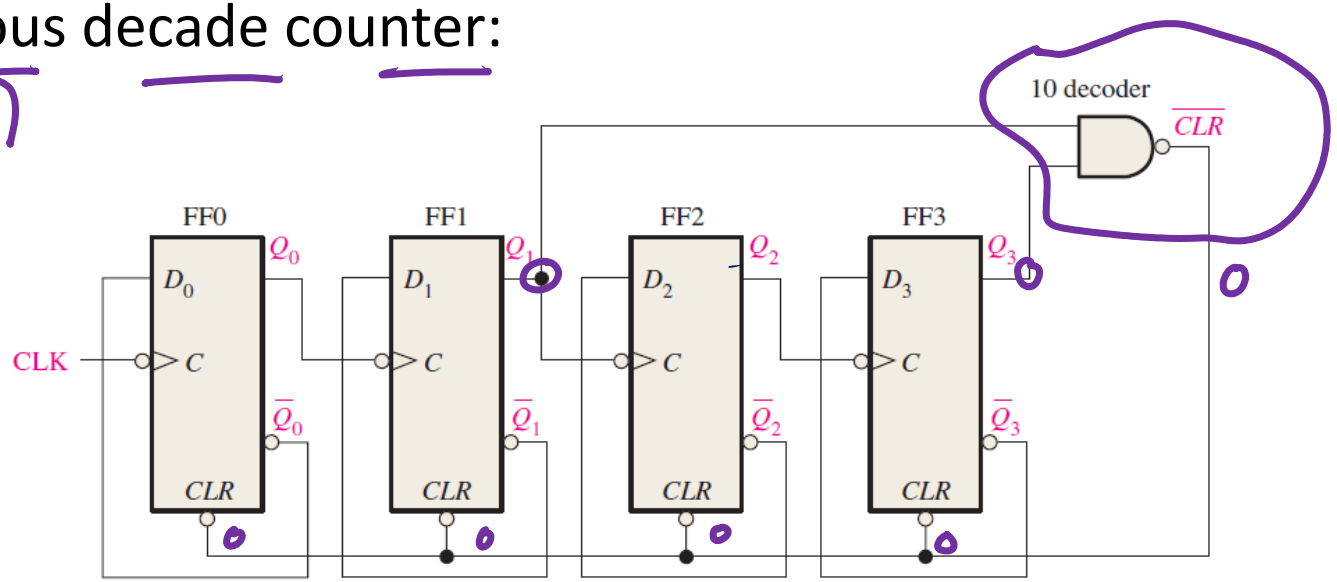
M=0, up counter; Q_0, Q_1, Q_2, Q_3

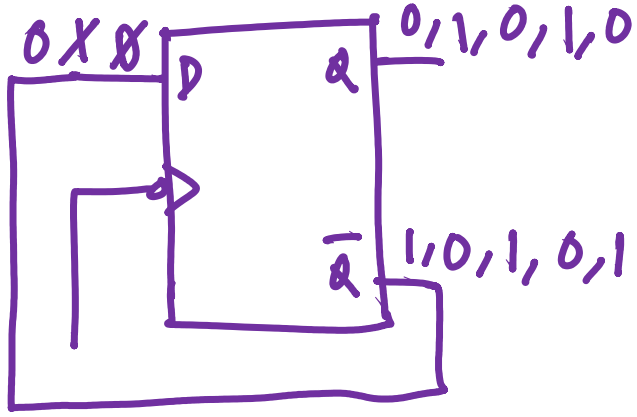
M=1, Down counter: $\overline{Q_0}, \overline{Q_1}, \overline{Q_2}$



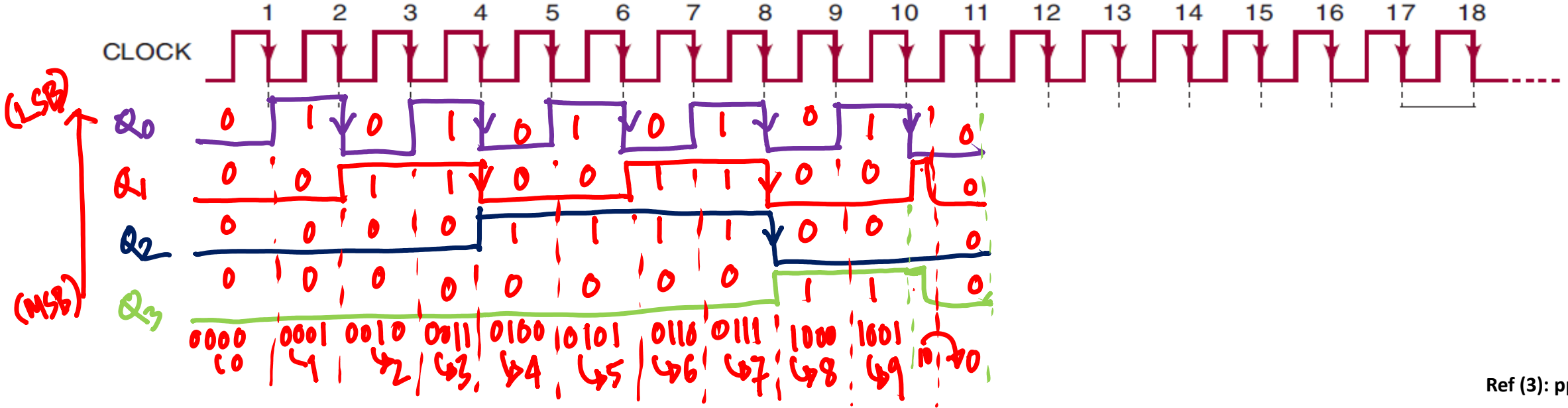
COUNTER CIRCUIT

- Asynchronous decade counter:





$$\text{MOD number} = 2^N$$

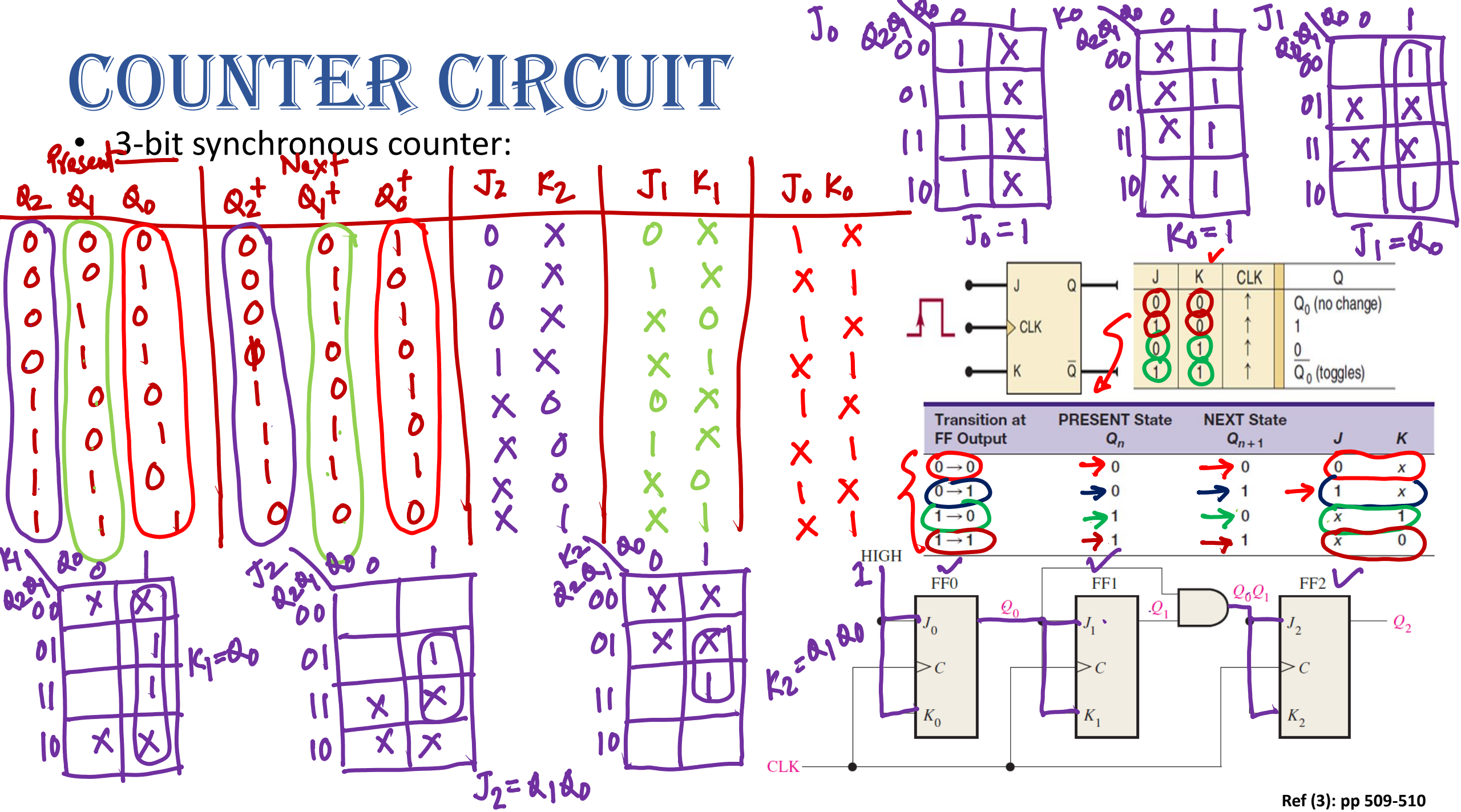


Ref (3): pp 505

COUNTER CIRCUIT

- 3-bit synchronous counter:

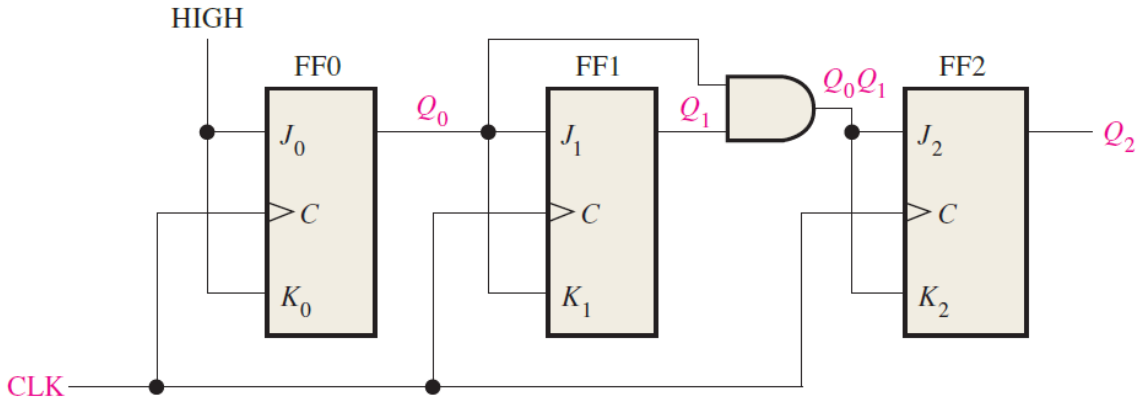
Present Q_2	Q_1	Q_0	Next Q_2^+	Q_1^+	Q_0^+	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	0	X

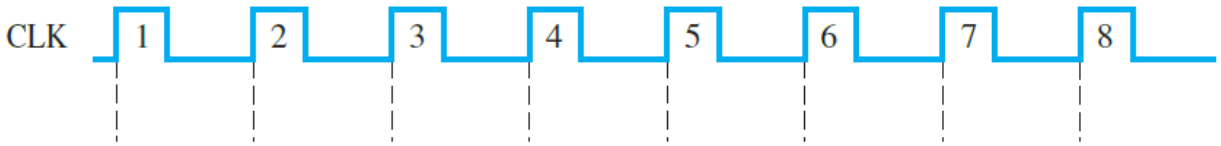


Ref (3): pp 509-510

COUNTER CIRCUIT

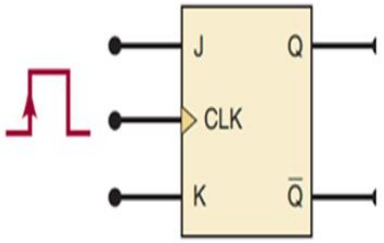
- 3-bit synchronous counter:





Clock Pulse	Outputs Q_2	Q_1	Q_0	J-K Inputs J_2	K_2	J_1	K_1	J_0	K_0	At the Next Clock Pulse FF2	FF1	FF0
Initially	0	0	0	0	0	0	0	1	1	NC*	NC	Toggle
1	0	0	1	0	0	1	1	1	1	NC	Toggle	Toggle
2	0	1	0	0	0	0	0	1	1	NC	NC	Toggle
3	0	1	1	1	1	1	1	1	1	Toggle	Toggle	Toggle
4	1	0	0	0	0	0	0	1	1	NC	NC	Toggle
5	1	0	1	0	0	1	1	1	1	NC	Toggle	Toggle
6	1	1	0	0	0	0	0	1	1	NC	NC	Toggle
7	1	1	1	1	1	1	1	1	1	Toggle	Toggle	Toggle
										Counter recycles back to 000.		

Transition at FF Output	PRESENT State Q_n	NEXT State Q_{n+1}	J	K
0 → 0	0	0	0	x
0 → 1	0	1	1	x
1 → 0	1	0	x	1
1 → 1	1	1	x	0

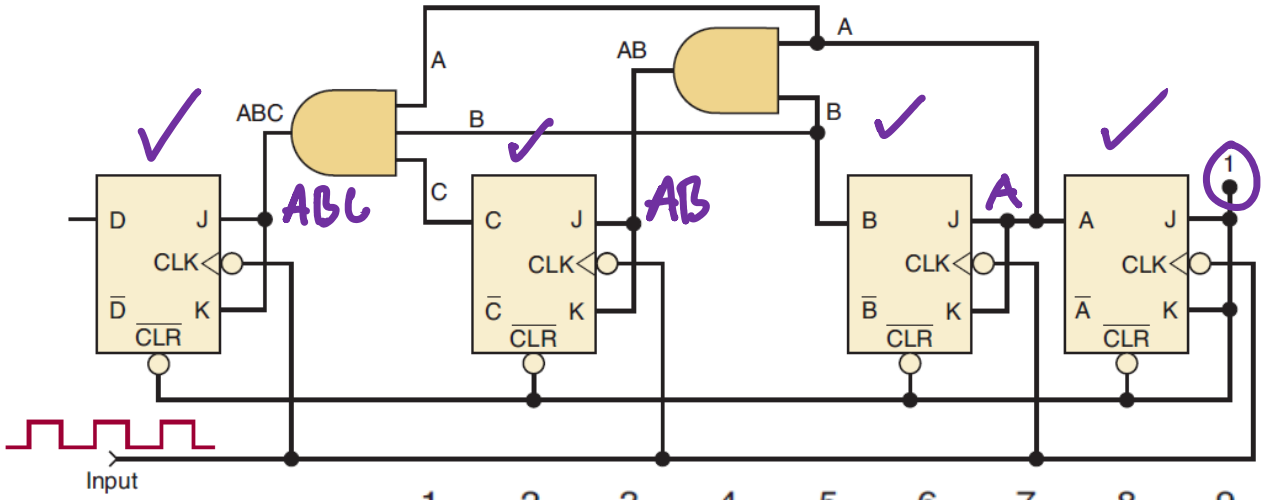


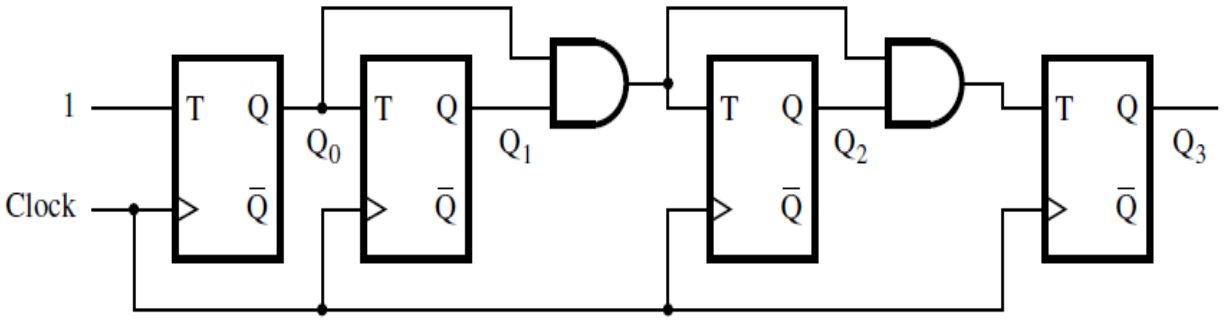
J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\bar{Q}_0$ (toggles)

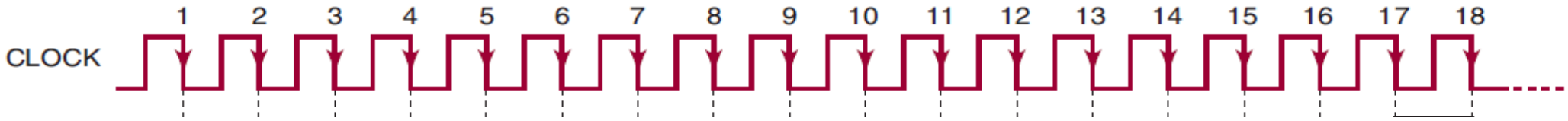
Ref (3): pp 309-310

COUNTER CIRCUIT

- 4-bit synchronous counter:



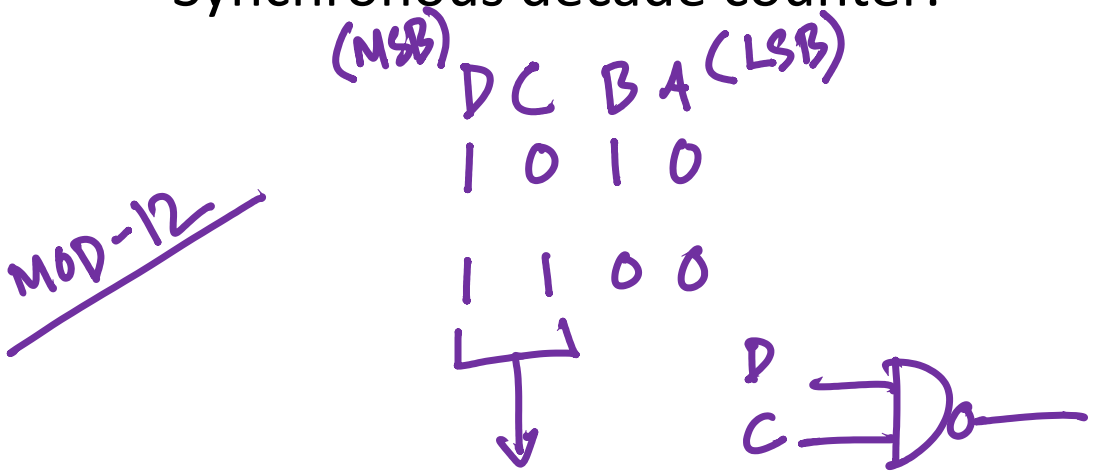


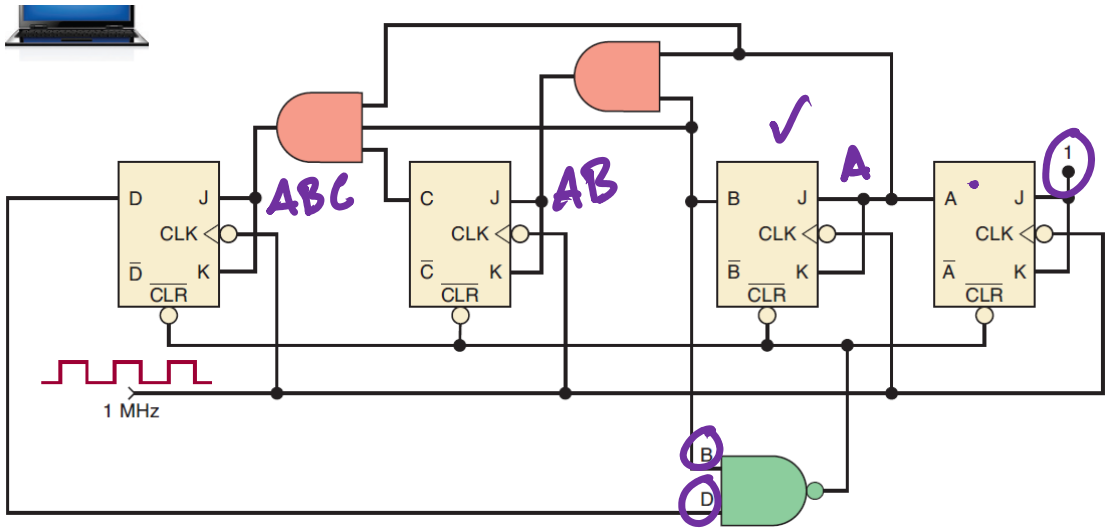


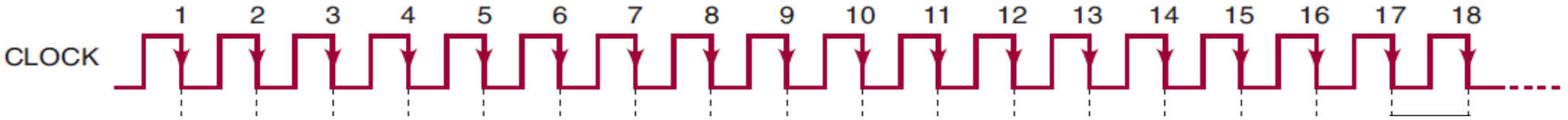
Ref (1): pp 431

COUNTER CIRCUIT

- Synchronous decade counter:





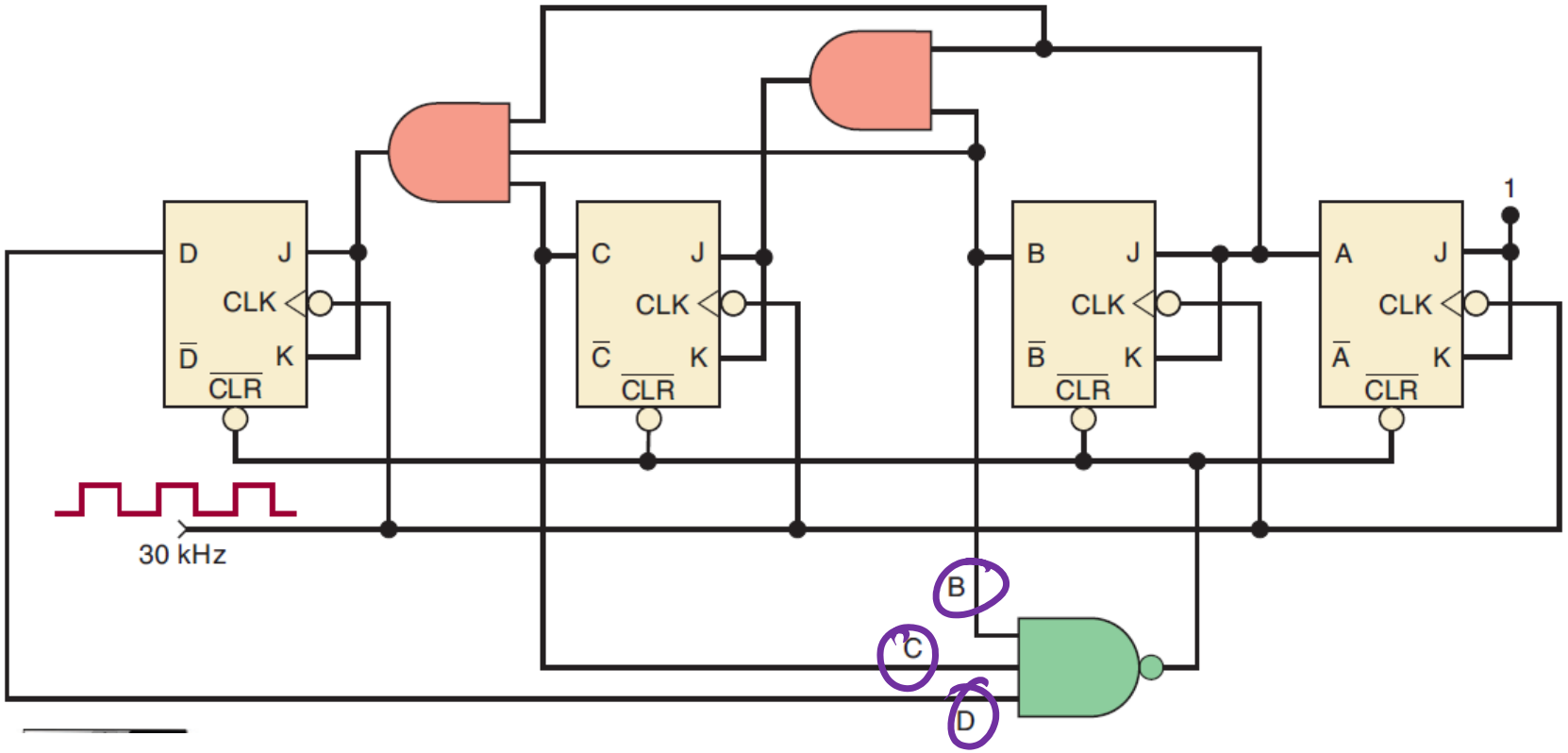


Ref (1): pp 444

COUNTER CIRCUIT

D C B A
1 1 1 0

- Synchronous MOD-14 counter:



Ref (1): pp 444