# 1. Decoders and multiplexers

(9) Implement a 1:4 demultiplexer with one data input active-high, two control inputs active-high and 4 data outputs active-high, using AND, OR and NOT gates

| I | Selection inputs | | Outputs | | | |
|---|---|---|---|---|---|---|
| | $S_1$ | $S_0$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 |

← Truth table

NOT, AND gates

$Y_3 = S_1 \cdot S_0 \cdot I$

$Y_2 = S_1 \cdot S_0' \cdot I$

$Y_1 = S_1' \cdot S_0 \cdot I$

$Y_0 = S_1' \cdot S_0' \cdot I$

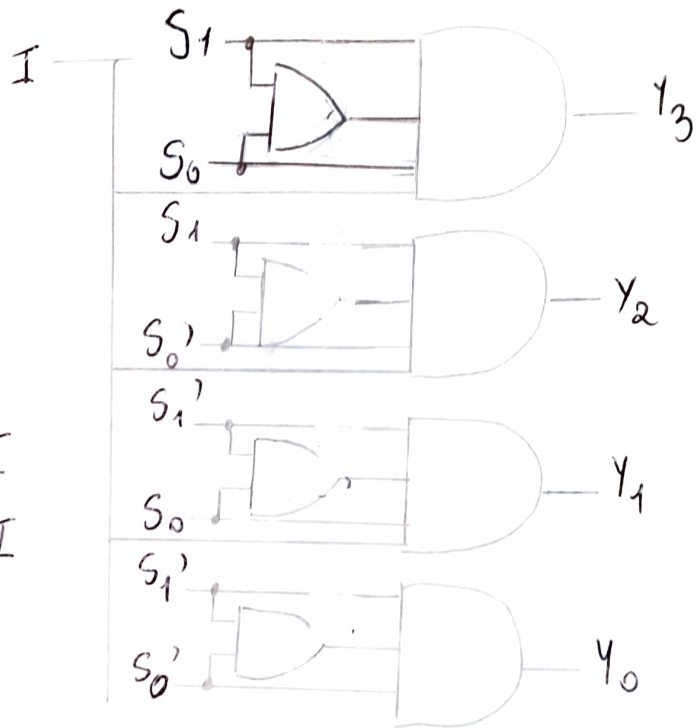
NOT, AND, OR gates

$Y_3 = S_1 (S_1 + S_0) \cdot S_0 \cdot I$

$Y_2 = S_1 (S_1 + S_0') \cdot S_0' \cdot I$

$Y_3 = S_1' (S_1' + S_0) \cdot S_0 \cdot I$

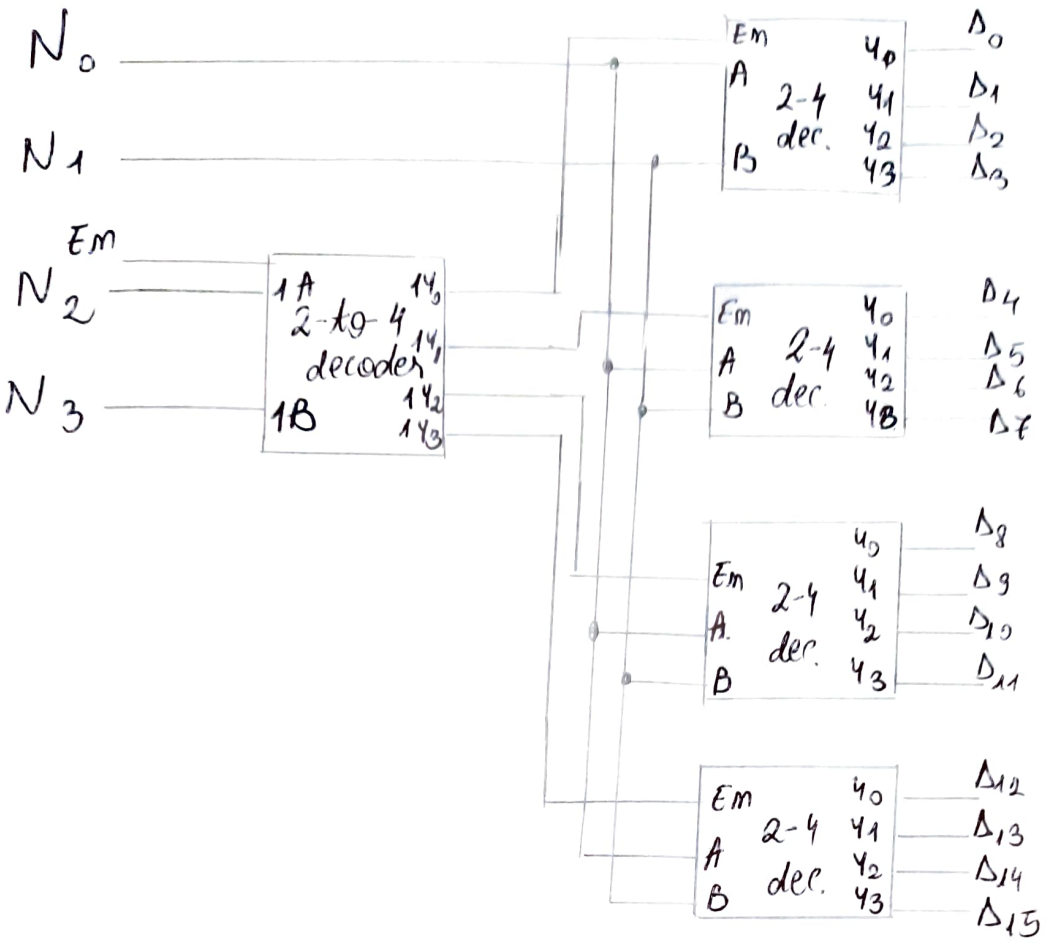
$Y_4 = S_1' (S_1' + S_0') \cdot S_0' \cdot I$




← circuit diagram

# 2. Expanding decoders and multiplexers

(1) Expand the 2-to-4 decoder to obtain a 4-to-16 decoder


N0
N1
Em
N2
N3
1A
2-to-4
decoder
1B
1Y0
1Y1
1Y2
1Y3
Em
A
B
2-4
dec.
Y0
Y1
Y2
Y3
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15