Zhang **Xiao**

(+86) 152-0192-0081 | zx15201920081@gmail.com | timez-zx.github.io | Timez-zx

About me

I am a master student in Shanghai Jiao Tong University advised by Prof. **Shizhen Zhao** and also work together with Prof. **Vincent Liu** now. My research interests focus on systems, networking and programmable hardware like FPGA. The simple but efficient thoughts in system, the combination between theory and network and the flexibility of programmable devices all leave me with deep impressions. So I am attempting to find a balance and preference among these three aspects.

Education

Shanghai Jiao Tong University *Shanghai, China*
M.E. in Communication Engineering, GPA: 3.76/4.0 *Sept. 2021 - Present*

Shanghai Jiao Tong University *Shanghai, China*
B.E. in Information Engineering, GPA: 3.81/4.3 *Sept. 2017 - June. 2021*

- Thesis title: Design of Robust and Efficient Edge Server Placement and Server Scheduling Policies

Research Experience

University of Pennsylvania, advised by Prof. Vincent Liu *Philadelphia, USA*
Visiting Student *July. 2023 - Present*

- *Beaver*: asynchronous snapshot for services in distributed system.

Shanghai Jiao Tong University, advised by Prof. Shizhen Zhao *Shanghai, China*
Master Student *Sep. 2021 - July. 2023*

- *Flattened Clos Plus (FC+)*: Design a deadlock-free routing algorithm without performance loss for RDMA-based expander networks.
- *Flattened Clos (FC)*: Design a deadlock-free routing algorithm for RDMA-based expander networks.
- *Time synchronization with eBPF*: Try to use eBPF and flooding method to achieve time synchronization with high precision for small smart devices.

Shanghai Jiao Tong University, advised by Prof. Shizhen Zhao *Shanghai, China*
Undergraduate Student *March. 2020 - Feb. 2021*

- Design of Robust and Efficient Edge Server Placement and Server Scheduling Policies.

Publication & Insubmission

Publication

- **Xiao Zhang**, Peirui Cao, Yongxi Lyu, Qizhou Zhang, Shizhen Zhao, Xinbing Wang, Chenghu Zhou "FC+: Near-optimal Deadlock-free Expander Data Center Networks", Wuhan, China, December, 2023. ISPA
- Shizhen Zhao*, Qizhou Zhang*, Peirui Cao, **Xiao Zhang**, Xinbing Wang, Chenghu Zhou, "Flattened Clos: Designing High-performance Deadlock-free Expander Data Center Networks Using Graph Contraction" in Boston, MA, USA (2023). NSDI
- Shizhen Zhao*, **Xiao Zhang***, Peirui Cao, Xinbing Wang, "Design of Robust and Efficient Edge Server Placement and Server Scheduling Policies" Virtual Event (2021). IWQOS

Projects

FPGA

- **Earliest Deadline Fist Switch (EDF switch)**: The EDF switch is to transmit packets based on the timestamp of each packet. The packets which have the earliest deadline go first.
- **64-FFT acceleration**: Use FPGA to accelerate the compute of 64-FFT algorithm.

System

- **Beaver's basic testbed**: Implement a small distributed platform with L4 load balancers and managers to deploy beaver snapshot protocol. L4 load balancer is realized by DPDK and SNAT in backends is realized by eBPF.

- **Concurrent Map Reduce System**: Use multiple threads on single hosts to realize a small map reduce system.
- **Concurrent web server**: Simple web server by multiple threads to handle user requests.

Honors & Awards

2021	**awardee,** Outstanding Graduate of Shanghai	*Shanghai, China*
2020	**awardee,** Liu Yongling Scholarship	*Shanghai, China*
2018-20	**awardee,** Category B Academic Scholarship	*Shanghai, China*