DDR Memory Module - Lattice Radiant Software

User Guide

FPGA-IPUG-02060-1.3

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DDR	Double Data Rate
FPGA	Field Programmable Gate Array
LPDDR	Low-Power Double Data Rate
LSE	Lattice Synthesis Engine

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1. Introduction

The Lattice Semiconductor Double Data Rate (DDR) Memory Module generates a module that can be used to interface to a DDR Memory and includes a bidirectional port and the associated clocking scheme. The design is implemented in Verilog HDL. It can be targeted to Lattice FPGA devices built on the Lattice Nexus™ platform and implemented using the Lattice Radiant® software integrated with the synthesis tool.

1.1. Features

Key features of Double Data Rate Memory Module include:

- Supports DDR3, DDR3L, and LPDDR2/3 memory interface
- Frequency Supported: 400, 533 MHz
- Supported gearing ratio – 4:1, 8:1
- Write Leveling support for DDR3/LPDDR3
- Dynamic valid window optimization (Read and Write Path)
- Configurable address and data bus width
- Configurable number of chip selects
- Configurable number of clocks
- Optional PLL generation

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1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals
- *_io* are bi-directional input/output signals

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2. Functional Description

2.1. Overview

DDR Memory Interface is bi-directional:

- On write (transmitting from controller to memory as a receiver), it is centered;
- On read (transmitting from memory to receiver on controller), it is aligned.

Table 2.1. Available DDR Memory Interfaces

Feature	Description	Comments
DDR3/DDR3L		
MDDRX2/4.DQ	Input/Output Data Bus	—
MDDRX2/4.DQS	Input/Output Data Strobe	Read Training support
MDDRX2/4.DM	Input Data Mask	—
ODDRX2/4.CK	DDR Memory Clock	—
MOSHX2/4.CSN	Chip Select	—
ODDRX2/4.ADDR_CMD_CKE_ODT	Address, Command, Clock Enable, On-Die Termination	—
LPDDR2/LPDDR3		
MDDRX2/4.DQ	Input/Output Data Bus	—
MDDRX2/4.DQS	Input/Output Data Strobe	Read Training/Write Levelling for LPDDR3 only
MDDRX2/4.DM	Input Data Mask	—
MDDRX2/4.CK_CKE_ODT	DDR Clock, Clock Enable, On-Die Termination	ODT for LPDDR3 only. A separate DQSBUF is used.
MDDRX2/4.CA	Command/Address Inputs	CA Training supported. A separate DQSBUF is used. Margin test is not required in LPDDR2.

Notes:

- MDDRX2/4.DQ, MDDRX2/4.DQS, and MDDRX2/4.DM implementation is same for DDR3, DDR3L, LPDDR2, and LPDDR3.
- ODDRX2/4.CK, MOSHX2/4.CSN and ODDRX1/4.ADDR_CMD_CKE_ODT are applicable only to DDR3 and DDR3L.
- MDDRX2/4.CK_CKE_ODT and MDDRX2/4.CA are applicable only to LPDDR2 and LPDDR3.

Table 2.2. Summary of DDR Memory Interface Support Logic

Module	Description
MEM_SYNC	Needed to avoid issues on DDR Memory bus and update code in operation without interrupting interface operation.

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Figure 2.1 illustrates the top-level design of DDR Memory Module.

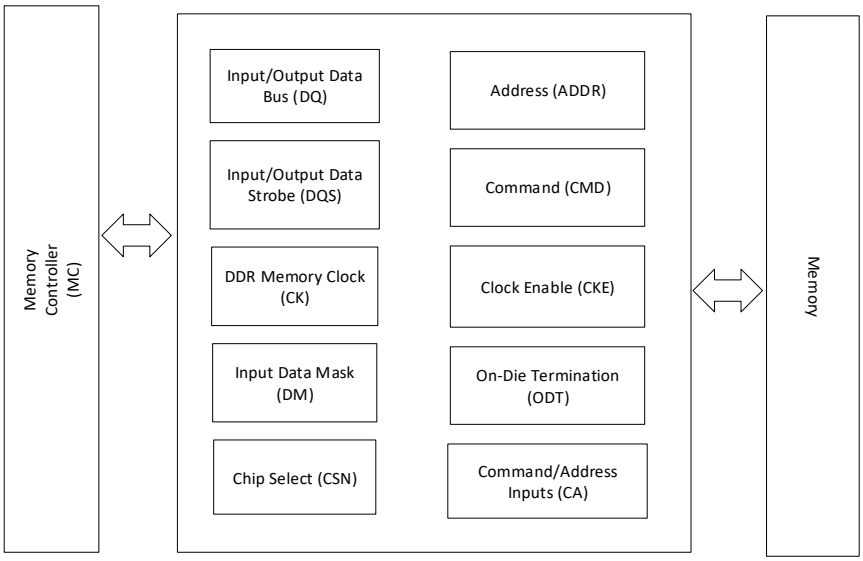

Figure 2.1. DDR Memory Soft IP Top-level Diagram

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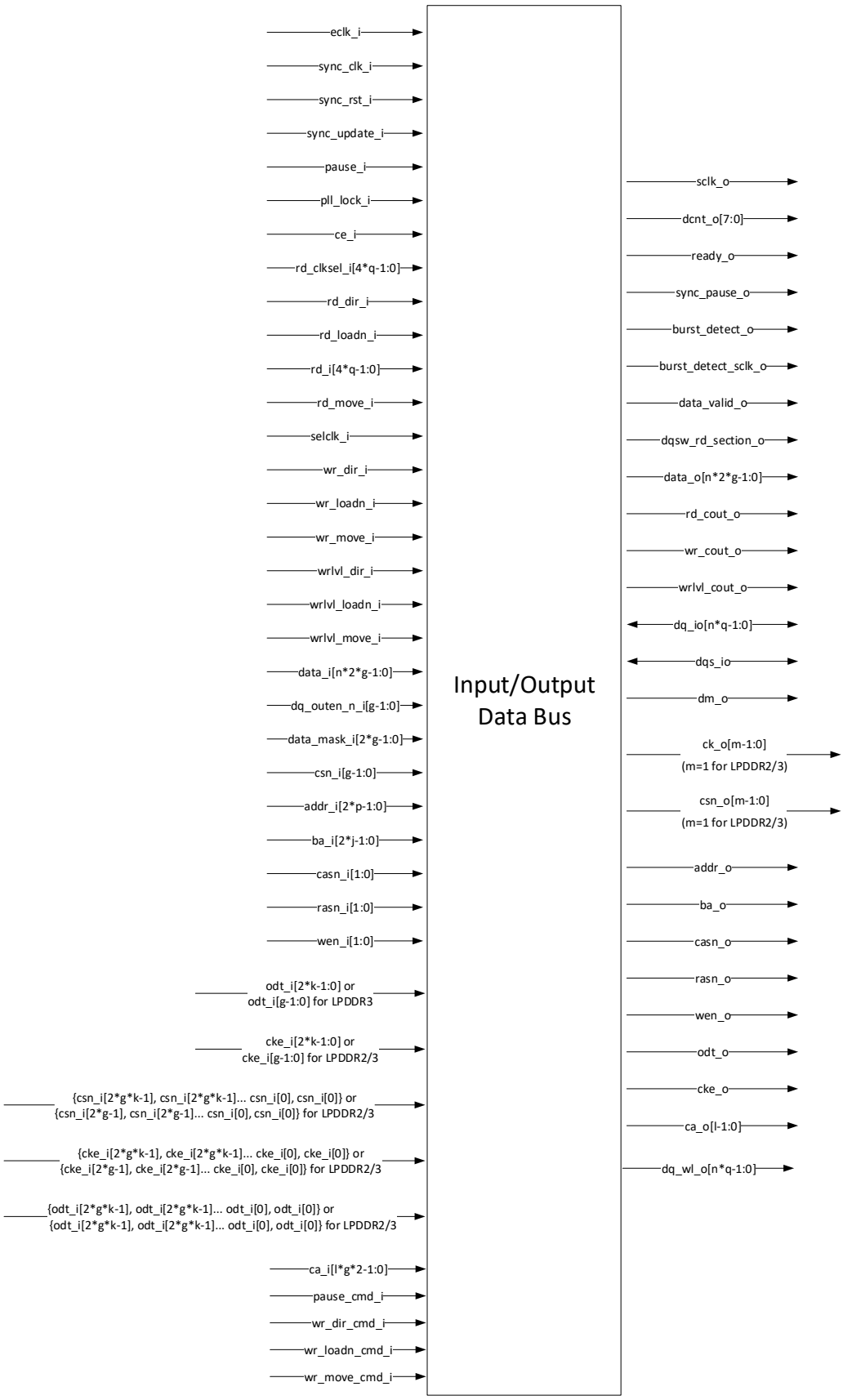

Figure 2.2. DDR Memory Block Diagram

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2.2. Signal Description

Table 2.3. DDR Memory Ports

Pin Name	Direction	Width (Bits)	Description
Clocks and Reset			
eclk_i	IN	1	Input clock
sync_clk_i	IN	1	Low speed continuously running clock input
sync_rst_i	IN	1	Active HIGH reset signal
sclk_o	OUT	1	Output divided clock
User Interface			
sync_update_i	IN	1	Used to update the code, perform training, or write leveling after ready_o goes high
pll_lock_i	IN	1	Used to indicate that clock source is already stable
pause_i	IN	1	Used to stop input clock for write leveling and code update
rd_clksel_dqs0_i, rd_clksel_dqs1_i, … rd_clksel_dqs(q)_i	IN	4	Used to select read clock source and polarity control per DQS group.
rd_dir_dqs0_i, rd_dir_dqs1_i, … rd_dir_dqs(q)_i	IN	1	Used to control the direction for DDR Read operation per DQS group. *0* to increase and *1* to decrease the code. Available only when *Enable Dynamic Margin Control on Clock Delay* is set.
rd_loadn_dqs0_i, rd_loadn_dqs1_i, … rd_loadn_dqs(q)_i	IN	1	Asynchronous reset the final delay code to factory default value for DDR Read operation per DQS group. Available only when *Enable Dynamic Margin Control on Clock Delay* is set.
rd_dqs0_i, rd_dqs1_i … rd_dqs(q)_i	IN	4	Read signal for DDR Read mode per DQS group. This is used to determine the location of the DQS signal.
rd_move_dqs0_i, rd_move_dqs1_i, … rd_move_dqs(q)_i	IN	4	At rising edge, it changes the code according to the direction set for DDR Read operation per DQS group. Available only when *Enable Dynamic Margin Control on Clock Delay* is set.
selclk_i	IN	1	Selects between output of the read section's delay cell or sclk for the clock to be used
wr_dir_dqs0_i, wr_dir_dqs1_i, … wr_dir_dqs(q)_i	IN	1	Used to control the direction for DDR Write operation per DQS group. *0* to increase and *1* to decrease the code. Available only when *Enable Dynamic Margin Control on Clock Delay* is set.
wr_loadn_dqs0_i, wr_loadn_dqs1_i, … wr_loadn_dqs(q)_i	IN	1	Asynchronous reset the final delay code to factory default value for DDR Write operation per DQS group. Available only when *Enable Dynamic Margin Control on Clock Delay* is set.
wr_move_dqs0_i, wr_move_dqs1_i, … wr_move_dqs(q)_i	IN	1	At rising edge, it changes the code according to the direction set for DDR Write operation per DQS group. Available only when *Enable Dynamic Margin Control on Clock Delay* is set.
wrlvl_loadn_dqs0_i, wrlvl_loadn_dqs1_i, … wrlvl_loadn_dqs(q)_i	IN	1	Asynchronous reset the final delay code to factory default value for DDR Write Leveling operation per DQS group. Available only when *Enable Dynamic Margin Control on Clock Delay* is set and 'Interface Type' is DDR3/LPDDR3.
wrlvl_dir_dqs0_i, wrlvl_dir_dqs1_i, … wrlvl_dir_dqs(q)_i	IN	1	Used to control the direction for DDR Write Leveling operation per DQS group. *0* to increase and *1* to decrease the code. Available only when *Enable Dynamic Margin Control on Clock Delay* is set and *Interface Type* is DDR3/LPDDR3..

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Pin Name	Direction	Width (Bits)	Description
wrlvl_move_dqs0_i, wrlvl_move_dqs1_i, … wrlvl_move_dqs(q)_i	IN	1	At rising edge, it changes the code according to the direction set for DDR Write Leveling operation per DQS group. Available only when *Enable Dynamic Margin Control on Clock Delay* is set and *Interface Type* is DDR3/LPDDR3.
dq_outen_n_i	IN	g	Tristate control port for DQ
data_dqs0_i, data_dqs1_i, … data_dqs(q)_i	IN	n*2*g	Parallel data bus input
dcnt_o	OUT	8	DDRDLL delay code
ready_o	OUT	1	Indicate that startup is finished and RX circuit is ready to operate.
sync_pause_o	OUT	1	PAUSE signal from MEM_SYNC module
data_dqs0_o, data_dqs1_o, … data_dqs(q)_o	OUT	n*2*g	Parallel data bus output
dqs_rd_section_o	OUT	1*q	Read training clock adjusted in the write section per DQS group. 1-bit output bus width per DQS group.
burst_detect_dqs0_o, burst_detect_dqs1_o, … burst_detect_dqs(q)_o	OUT	1	Read burst detect output
burst_detect_sclk_dqs0_o, burst_detect_sclk_dqs1_o, … burst_detect_sclk_dqs(q)_o	OUT	1	Clock generated using burst_detect_o
data_valid_dqs0_o, data_valid_dqs1_o, … data_valid_dqs(q)_o	OUT	1	Data valid flag for READ mode per DQS group
rd_cout_dqs0_o, rd_cout_dqs1_o, … rd_cout_dqs(q)_o	OUT	1	Margin test output flag for READ to indicate the under-flow or over-flow per DQS group. Available only when *Enable Dynamic Margin Control on Clock Delay* is set.
wr_cout_dqs0_o, wr_cout_dqs1_o, … wr_cout_dqs(q)_o	OUT	1	Margin test output flag for WRITE to indicate the under-flow or over-flow per DQS group. Available only when *Enable Dynamic Margin Control on Clock Delay* is set.
wrlvl_cout dqs0_o, wrlvl_cout dqs1_o, … wrlvl_cout dqs(q)_o	OUT	1	Margin test output flag for WRITE LEVELING to indicate the under-flow or over-flow per DQS group. Available only when *Enable Dynamic Margin Control on Clock Delay* is set and *Interface Type* is DDR3/LPDDR3.
dqwl_dqs0_o, dqwl_dqs1_o, … dqwl_dqs(q)_o	OUT	8	Data output of write leveling. Available only when *Interface Type* is DDR3/DDR3L.
dqs_outen_n_dqs0_i, dqs_outen_n_dqs1_i, … dqs_outen_n_dqs(q)_i	IN	g	Tristate control port for DQS per DQS group
dqs0_i, dqs1_i, … dqs(q)_i	IN	g	Parallel DQS input per DQS group
data_mask_dqs0_i, data_mask_dqs1_i, … data_mask_dqs(q)_i	IN	2*g	Parallel Data Mask input per DQS group. Available only when *Data Mask Enable* attribute is set.

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Pin Name	Direction	Width (Bits)	Description
csn_din0_i, csn_din1_i, csn_din2_i and csn_din3_i	IN	k	Chip Select input Available only when *Clock/Address/Command Enable* is set.
addr_din0_i and addr_din1_i	IN	p	Address input Available only when *Clock/Address/Command Enable* is set and *Interface Type* is DDR3/DDR3L.
ba_din0_i and ba_din1_i	IN	j	Bank Address input Available only when *Clock/Address/Command Enable* is set and *Interface Type* is DDR3/DDR3L.
casn_din0_i and casn_din1_i	IN	1	Column Address input Available for DDR3 and DDR3L only, when *Clock/Address/Command Enable* is set.
rasn_din0_i and rasn_din1_i	IN	1	Row Address input Available only when *Clock/Address/Command Enable* is set and *Interface Type* is DDR3/DDR3L.
wen_din0_i and wen_din1_i	IN	1	Write Enable input Available only when *Clock/Address/Command Enable* is set and *Interface Type* is DDR3/DDR3L.
odt_din0_i and odt_din1_i	IN	1	On-die Termination input Available only when *Clock/Address/Command Enable* is set and *Interface Type* is DDR3/DDR3L/LPDDR3.
cke_din0_i and cke_din1_i	IN	2*k (for non-LPDDR2/3), or g (otherwise)	Clock Enable input Available only when *Clock/Address/Command Enable* is set.
pause_cmd_i	IN	1	Separate pause input for DQSBUF used for Command/Address output path. Available only when *Clock/Address/Command Enable*, *Enable Dynamic Margin Control on Clock Delay* are set and *Interface Type* is LPDDR3.
ca_i	IN	I*2*g	Command/Address input Available only when *Clock/Address/Command Enable* is set and *Interface Type* is LPDDR2/LPDDR3.
I/O Pad Interface			
dq_dqs0_io, dq_dqs1_io, .. dq_dqs(q)_io	INOUT	8	Data bus to/from I/O
dqs0_io, dqs1_io, … dqs2_io	INOUT	1	Data strobe to/from I/O
dm_dqs0_o, dm_dqs1_o, … dm_dqs(q)_o	OUT	1	Data Mask output to I/O per DQS group Available only when *Data Mask Enable* attribute is set.
ck_o	OUT	m (for non-LPDDR2/3), or 1 (otherwise)	DDR Clock output to I/O Available only when *Clock/Address/Command Enable* is set.
csn_o	OUT	k (for non-LPDDR2/3), or 1 (otherwise)	Chip Select output to I/O Available only when *Clock/Address/Command Enable* is set.
addr_o	OUT	p	Address output to I/O Available only when *Clock/Address/Command Enable* is set and *Interface Type* is DDR3/DDR3L.
ba_o	OUT	j	Bank Address output to I/O Available only when *Clock/Address/Command Enable* is set and *Interface Type* is DDR3/DDR3L.

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Pin Name	Direction	Width (Bits)	Description
casn _o	OUT	1	Column Address output to I/O Available only when *Clock/Address/Command Enable* is set and *Interface Type* is DDR3/DDR3L.
rasn_o	OUT	1	Row Address output I/O Available only when *Clock/Address/Command Enable* is set and *Interface Type* is DDR3/DDR3L.
wen_o	OUT	1	Write Enable output to I/O Available only when *Clock/Address/Command Enable* is set and *Interface Type* is DDR3/DDR3L.
odt_o	OUT	k (for non-LPDDR3), or 1 (otherwise)	On-die termination output to I/O Available only when *Clock/Address/Command Enable* is set and *Interface Type* is DDR3/DDR3L/LPDDR3.
cke_o	OUT	k (for non-LPDDR2/3), or 1 (otherwise)	Clock Enable output to I/O Available only when *Clock/Address/Command Enable* is set.
ca_o	OUT	l	Command/Address output to I/O Available only when *Clock/Address/Command Enable* is set and *Interface Type* is LPDDR2/LPDDR3.

Notes:

- n = number of DQ per DQS group; currently set to 8;
- q = number of DQS groups;
- m = number of DDR clocks selected (NUM_DDRCLK);
- p = Address width selected (ADDR_WIDTH);
- k = number of Chip Select (NUM_CS);
- j = Bank Address bus width selected (BA_WIDTH);
- g = DDR gearing used (2 = X2 gearing; 4 = X4 gearing);
- l = command/address bus width; currently set to 10.

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2.3. Attribute Summary

Table 2.4. Attribute Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General Tab			
General Group			
Interface Type	DDR3, DDR3L, LPDDR2, LPDDR3	LPDDR3	—
I/O Buffer Type	SSTL15_I, SSTL15_II	SSTL15_I	*Interface Type* = DDR3
	SSTL135_I, SSTL135_II	SSTL135_I	*Interface Type* = DDR3L
	HSUL12	HSUL12	*Interface Type* = LPDDR2 or LPDDR3
Gearing Ratio	4:1, 8:1	4:1	—
Number of DQ per DQS	8	8	Display Information only
Data Bus Width	8, 16, 24, 32	16	*Interface Type* = DDR3 or DDR3L
	16		*Interface Type* = LPDDR2 or LPDDR3
Number of DQS Group	Calculated = (Data Bus Width)/ (Number of DQs per DQS group, which is set to 8)	N/A	*Data Bus Width*
Data Mask Enable	Checked, Unchecked	Unchecked	—
Clock/ Address/ Command Enable	Checked, Unchecked	Unchecked	—
Enable Dynamic Margin Control on Clock Delay	Checked, Unchecked	Unchecked	—
DDR Memory Frequency (MHz)	400, 533	400	533 is only available If *Gearing Ratio* = 8:1
System Clock Frequency (MHz)	Calculated = (DDR Memory Frequency) /Gearing Ratio	N/A	Display Information only
Enable PLL	Checked, Unchecked	Unchecked	—
PLL CLKI: Frequency (MHz)	10 – 800	100	*Enable PLL* is Checked
PLL Reference Clock from Pin	Checked, Unchecked	Unchecked	*Enable PLL* is Checked
I/O Standard for Reference Clock	LVDS, SUBLVDS, SLVS, HSTL15_I, HSTL15D_I, LVTTL33, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS18H, HSTL15D_I, LVCMOS15, LVCMOS15H, LVCMOS12, LVCMOS12H, LVCMOS10H, LVCMOS10, LVCMOS10R	SLVS	*Enable PLL* and *PLL Reference Clock from Pin* are both Checked
CLKOP Tolerance (%)	0.0, 0.1, 0.2, 0.5, 1.0, 2.0, 5.0, 10.0	0.1	*Enable PLL* is Checked
DDR Memory Actual Frequency (MHz)	Calculated	N/A	Display Information only
Clock/Address/Command			
Number of Clocks	1, 2, 4	1	*Interface Type* = DDR3 or DDR3L and *Clock/Address/Command Enable* is Checked
Address Width	13, 14, 15, 16	13	
Number of Chip Selects	1, 2	1	
Number of Chip ODT	Calculated = *Number of Chip Selects*	1	
Number of Clock Enables	Calculated = *Number of Chip Selects*	1	
Bank Address Width	3	3	

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Attribute	Selectable Values	Default	Dependency on Other Attributes
Advanced Settings			
DQS Read Delay Adjustment Enable	Checked, Unchecked	Unchecked	*Enable Dynamic Margin Control on Clock Delay* is Checked
DQS Read Delay Adjustment Sign	POSITIVE, COMPLEMENT	POSITIVE	
DQS Read Delay Adjustment Value	0-511	0	
DQS Read Delay Adjustment Actual Value	Calculated: Performs 2's complement of 'DQS Read Delay Adjustment Value' when selected sign is COMPLEMENT	N/A	Display Information only
DQS Write Delay Adjustment Enable	Checked, Unchecked	Unchecked	*Enable Dynamic Margin Control on Clock Delay* is Checked
DQS Write Delay Adjustment Sign	POSITIVE, COMPLEMENT	POSITIVE	
DQS Write Delay Adjustment Value	0 – 511	0	
DQS Write Delay Adjustment Actual Value	Calculated: Performs 2's complement of 'DQS Write Delay Adjustment Value' when selected sign is COMPLEMENT	N/A	Display Information only

Table 2.5 shows a brief summary of possible Clock/Address/Command attribute options depending on the *Interface Type* you have chosen from the user interface:

Table 2.5. Clock/Address/Command Attribute Values

	Interface Type			
Attribute	**DDR3**	**DDR3L**	**LPDDR2**	**LPDDR3**
CLK	1, 2, 4	1, 2, 4	1	1
CA	13,14,15,16	13,14,15,16	Set to 10	Set to 10
BA	3	3	0 (N/A)	0 (N/A)
CSN	1, 2	1, 2	1	1
ODT	Same as CSN	Same as CSN	0 (N/A)	1
CKE	Same as CSN	Same as CSN	1	1

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3. Generation, Synthesis, and Validation

This chapter provides information on how to generate and synthesize DDR Memory Module using Lattice Radiant software. For more on Lattice Radiant software, refer to the Lattice Radiant Software 2.1 User Guide.

3.1. Generating and Synthesizing the IP

Lattice Radiant software allows you to generate and customize modules and IPs and integrate them into the device architecture.

To generate the DDR Memory Module in Lattice Radiant software:

1. In the Module/IP Block Wizard create a new Lattice Radiant Software project for DDR Memory module.
2. In the dialog box of the Module/IP Block Wizard window, configure DDR Memory module according to custom specifications using drop-down menus and check boxes. As a sample configuration, see Figure 3.1. For configuration options, see Table 2.4.

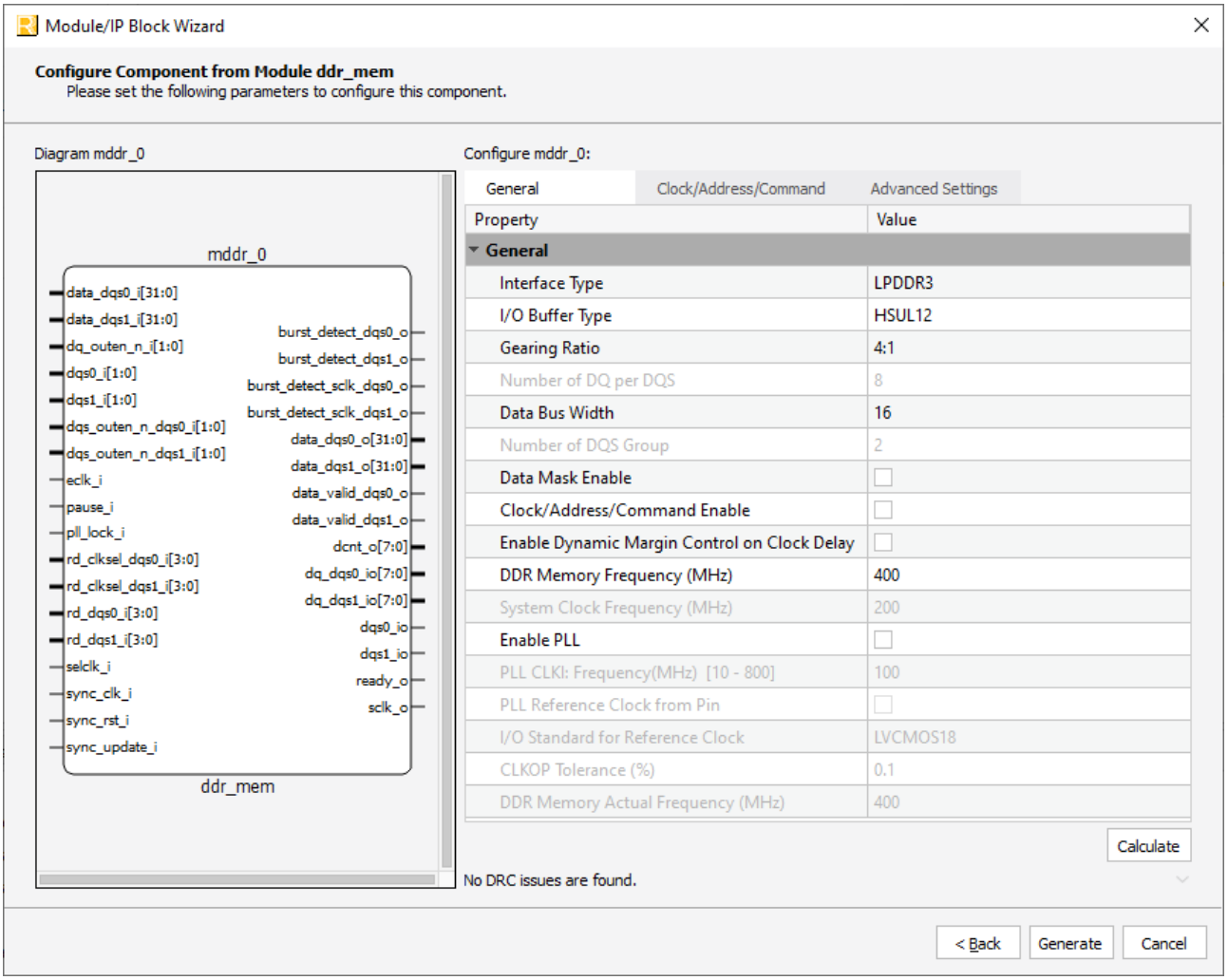

Figure 3.1. Configure Block of DDR Memory Module

3. Click **Generate**. The Check Generating Result dialog box opens, showing design block messages and results as shown in Figure 3.2.

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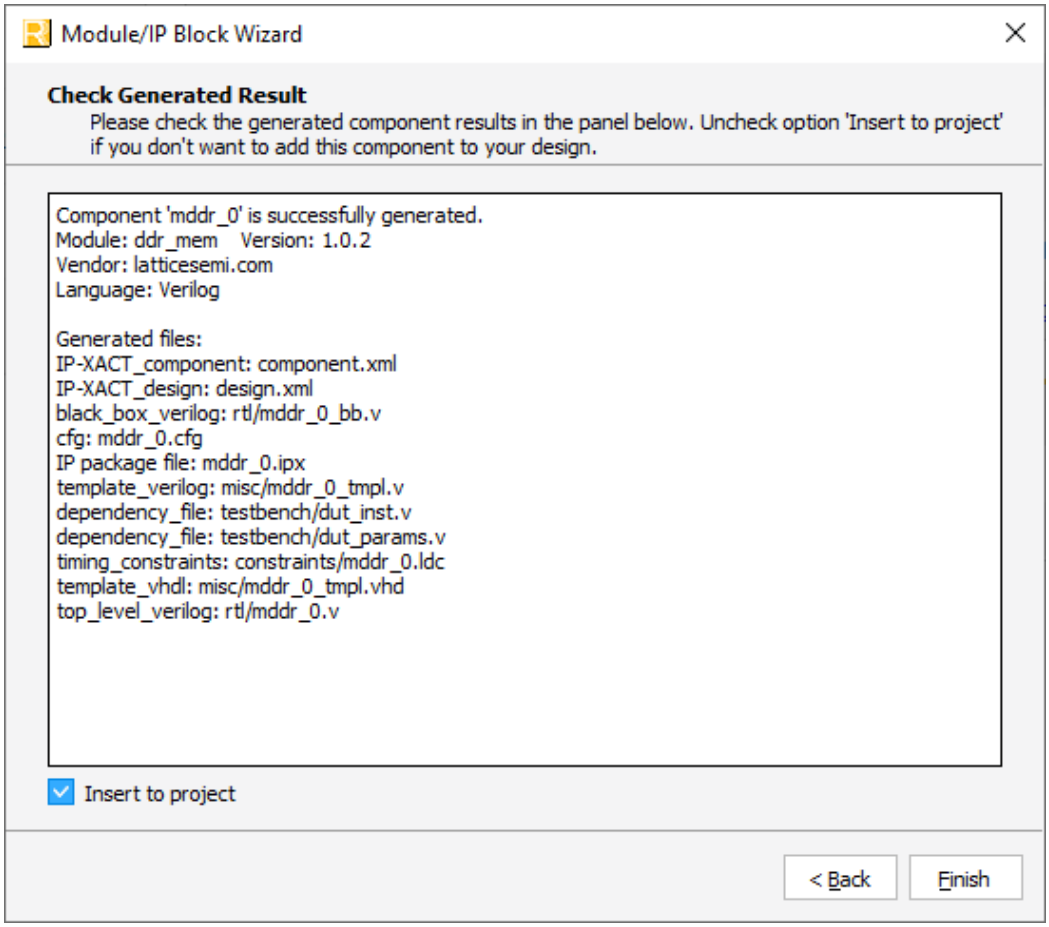

Figure 3.2. Check Generating Result

4. Click **Finish** to generate the Verilog file.
5. Upon generating your desired design, you can synthesize it by pressing **Synthesize Design** located on the top left corner of the screen, as shown in Figure 3.3.

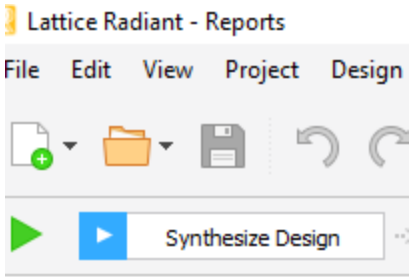

Figure 3.3. Synthesizing Design

For general information and details on Lattice Radiant Software, refer to the Lattice Radiant Software User Guide and tutorials.

3.2. Core Validation

The functionality of the DDR Memory Module has been verified via simulation using Lattice's in-house testbench environment and hardware validation.

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4. Running the Simulation

To run simulation, perform the following steps:

1. Press the button located on the Toolbar on the top of your screen to initiate Simulation Wizard, as shown in Figure 4.1.

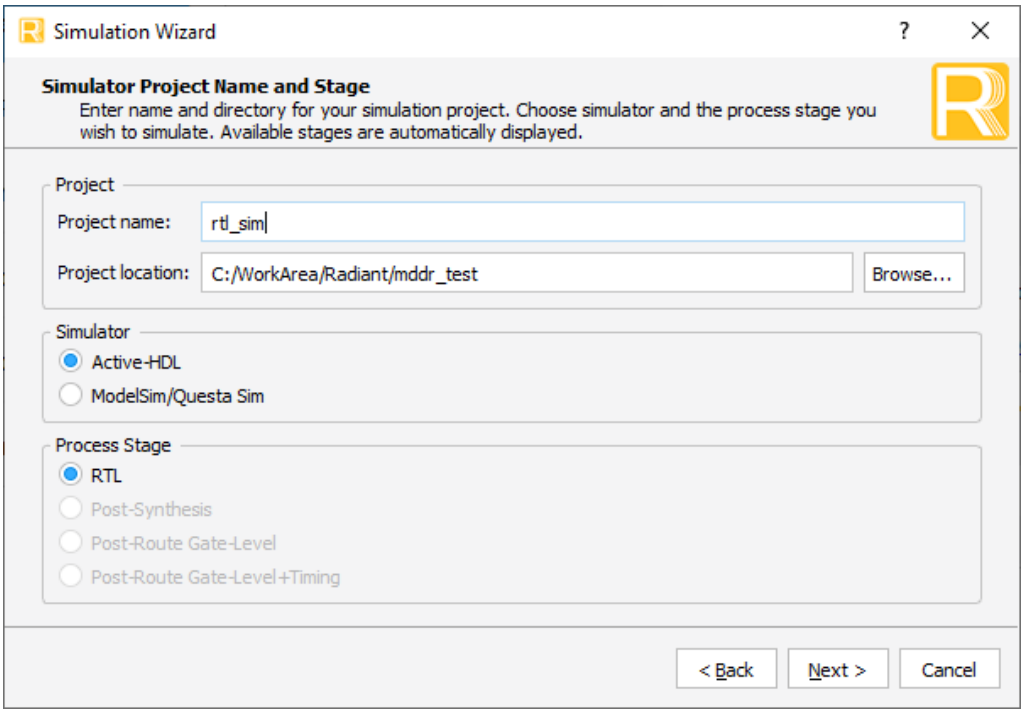

Figure 4.1. Simulation Wizard

2. Press **Next** to get to the Add and Reorder Source Screen, shown in Figure 4.2.

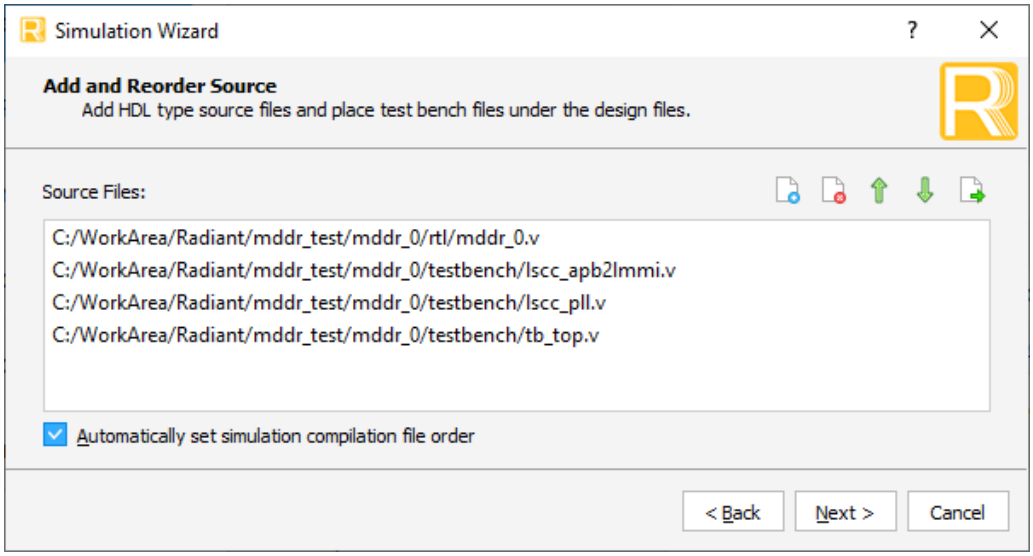

Figure 4.2. Adding and Reordering Source

3. Press **Next** to run simulation.

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5. Licensing and Evaluation

5.1. Hardware Evaluation

There is no restriction on the hardware evaluation of this module.

5.2. Licensing the IP

No license is required for this module.

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Appendix A. Resource Utilization

Table A.1 show configuration and resource utilization for LIFCL-40-9BG400I using Synplify Pro of Lattice Radiant Software 2.1. The configuration used in generating the resource utilization is shown in Figure A.1.

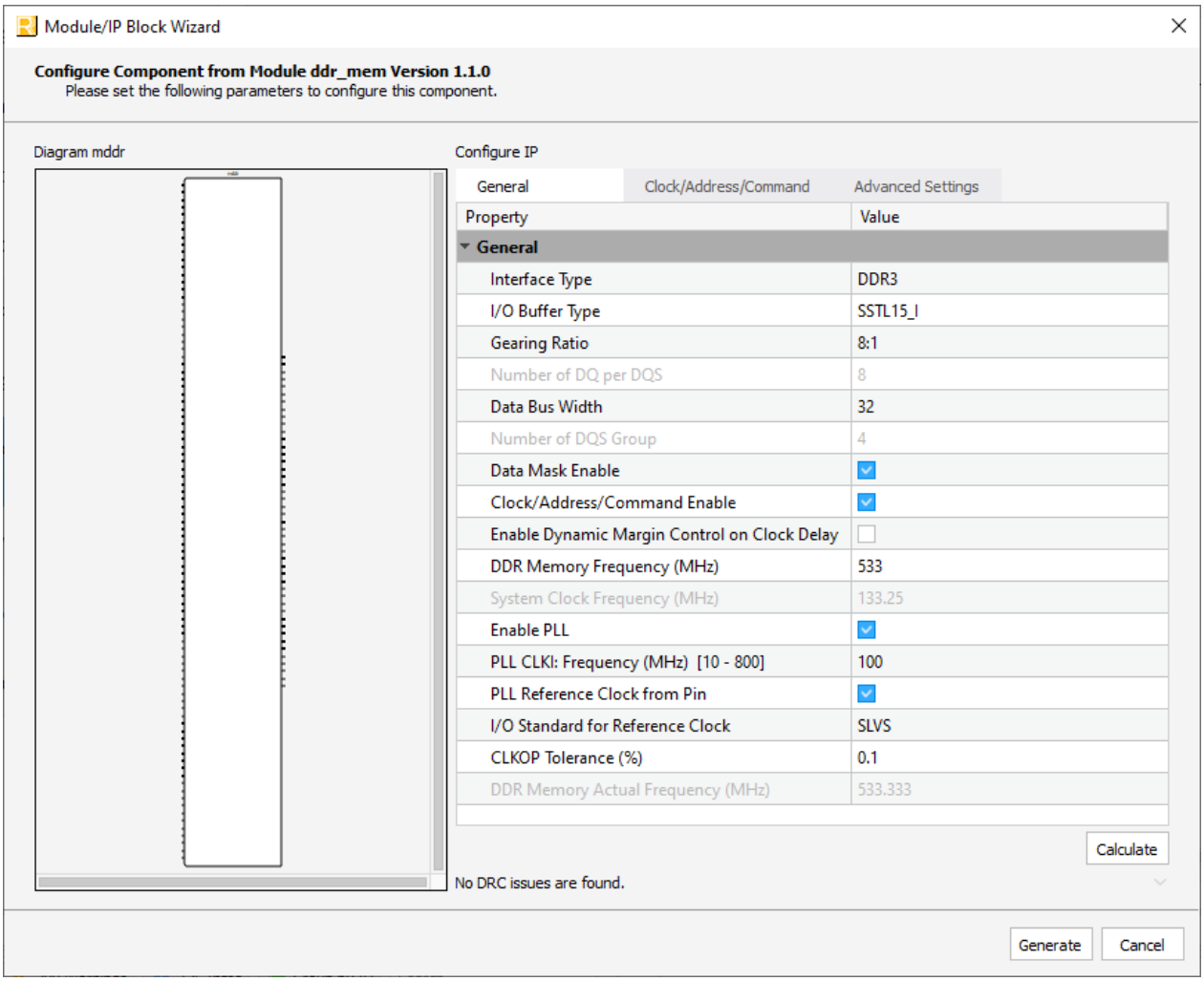

Figure A.1. Configuration for Resource Utilization

Table A.1. Resource Utilization

Configuration	sclk_o Fmax (MHz)*	Registers	LUTs	IDDR/ODDR/TDDR
Data Bus Width = 32, Others = Figure A.1	200	25	68	131
Data Bus Width = 24, Others = Figure A.1	200	25	68	104
Data Bus Width = 16, Others = Figure A.1	200	25	68	77
Data Bus Width = 8, Others = Figure A.1	200	25	68	50
Data Bus Width = 32, DDR Memory Frequency = 400MHz, Others = Figure A.1	200	25	68	131

*__Note:__ The sclk_o Fmax is generated using a design that only contains the DDR Memory Module and a few linear-feedback shift registers. These values may be reduced when the IP Core is used with the user logic.

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References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software User Guide.

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Revision History

Document Revision 1.3, Lattice Radiant SW version 2.1, June 2021

Section	Change Summary
Introduction	• Replaced specific product names with *Lattice FPGA devices built on the Lattice Nexus platform or Lattice Nexus devices*. • Removed Quick Facts section.
References	Updated this section.

Document Revision 1.2, Lattice Radiant SW version 2.1, June 2020

Section	Change Summary
Introduction	Added Certus-NX and LFD2NX-40 as supported FPGA family and device.
Attribute Summary	• Updated Table 2.4 format and updated information to match DDR Memory Module v1.1.0. • Updated CK and CSN entry in Table 2.5.
Generating and Synthesizing the IP	Updated Figure 3.1 and Figure 3.2.
Appendix A. Resource Utilization	Added this section.

Document Revision 1.1, Lattice Radiant SW version 2.0 Service Pack 1, February 2020

Section	Change Summary
Introduction	Updated Table 1.1 with the following changes: • Removed Minimal Device Needed. • Added LIFCL-17 as targeted device. • Removed Data Path Width item.
Attribute Summary	Updated Table 2.4 format and updated information to match DDR Memory Module v1.0.1.
Generating and Synthesizing the IP	Updated Figure 3.1 and Figure 3.2.
Running the Simulation	Updated Figure 4.1 and Figure 4.2.

Document Revision 1.0, Lattice Radiant SW version 2.0, December 2019

Section	Change Summary
All	Changed document status from Preliminary to final.
Acronyms in This Document	Added this section.

Document Revision 0.80, Lattice Radiant SW version 0.80, October 2019

Section	Change Summary
All	Preliminary release

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