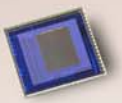
OmniVision



datasheet

PRELIMINARY SPECIFICATION

1/4" CMOS QSXGA (5 megapixel) image sensor
with OmniBSI™ and embedded TrueFocus™ technology

OV5642

color 5 megapixel image sensor with OmniBSI™ and embedded TrueFocus™ technology

datasheet (CSP3)
PRELIMINARY SPECIFICATION

version 1.11
january 2009

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular phones
- toys
- PC multimedia
- digital still cameras

ordering information

- **OV05642-A63A** (color, lead-free)
  63-pin CSP3

features

- ultra high performance
- automatic image control functions: automatic exposure control (AEC), automatic white balance (AWB), automatic band filter (ABF), automatic 50/60 Hz luminance detection, and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC 16-zone size/position/weight control, mirror and flip, scaling, cropping, windowing, and panning
- image quality controls: color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defective pixel canceling, and noise canceling
- support for output formats: RAW RGB, RGB565/555/444, CCIR656, YUV422/420, YCbCr422, and compression
- support for images sizes: 5 megapixel, and any arbitrary size scaling down from 5 megapixel
- embedded TrueFocus™ light, enabling extended depth of field (EDoF)
- support for auto focus control (AFC)
- support for video or snapshot operations
- support for horizontal and vertical sub-sampling
- support for binning
- support for data compression output
- support for anti-shake
- support for external frame synchronization in frame exposure mode
- support for LED and flash strobe mode
- standard serial SCCB interface
- digital video port (DVP) parallel output interface
- MIPI serial input and output interface
- support for second camera chip-sharing ISP and MIPI interface
- embedded microcontroller
- embedded one-time programmable (OTP) memory for part identification, etc.
- on-chip phase lock loop (PLL)
- programmable I/O drive capability
- support for mechanical shutter, ND filter and IRIS control
- built-in 1.5V regulator for core

key specifications

- **active array size:** 2592 x 1944
- **power supply:**
  core: 1.5VDC ± 5% (internal regulator)
  analog: 2.6 ~ 3.0V
  I/O: 1.7 ~ 3.0V
- **power requirements:**
  active: TBD
  standby: TBD
- **temperature range:**
  operating: -30°C to 70°C (see **table 8-1**)
  stable image: 0°C to 50°C (see **table 8-1**)
- **output formats (8-bit):** YUV(422/420) / YCbCr422, RGB565/555/444, CCIR656, 8-bit compression data, 8/10-bit raw RGB data
- **lens size:** 1/4"
- **lens chief ray angle:** 24° non-linear (see **table 10-1**)
- **input clock frequency:** 6 ~ 27 MHz
- **shutter:** rolling shutter
- **maximum image transfer rate:**
  5 megapixel (2592x1944): 15 fps
  (and any size scaling down from 5 megapixel)
  1080p (1920x1080): 30 fps
  720p (1280x720): 60 fps
  VGA (640x480): 60 fps
  QVGA (320x240): 120 fps
- **sensitivity:** TBD
- **S/N ratio:** TBD
- **dynamic range:** TBD
- **scan mode:** progressive
- **maximum exposure interval:** 1968 x t_{ROW}
- **gamma correction:** programmable
- **pixel size:** 1.4 µm x 1.4 µm
- **well capacity:** TBD
- **dark current:** TBD
- **fixed pattern noise (FPN):** TBD
- **image area:** 3673.6 µm x 2738.4 µm
- **package dimensions:** 6945 µm x 6695 µm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV5642 image sensor. The package information is shown in **section 9**.

table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description
A1	EGND	ground	ground for MIPI TX circuit
A2	DGND	ground	ground for digital circuit
A3	XVCLK	input	system input clock
A4	NC	–	no connect
A6	VHT	reference	internal analog reference
A7	SVDD	power	power for sensor circuit
A8	SGND	ground	ground for sensor circuit
A9	AGND	ground	ground for analog circuit
A10	AVDD	power	power for analog circuit
B2	MDN1	I/O	MIPI TX first data lane negative output
B3	DVDD	DVDD	reference
B4	NC	–	no connect
B5	VN	reference	internal analog reference
B6	VH	reference	internal analog reference
B7	NC	–	no connect
B8	NC	–	no connect
B9	NC	–	no connect
B10	NC	–	no connect
C1	EVDD	reference	power for MIPI TX circuit
C2	MDP1	I/O	MIPI TX first data lane positive output
C9	NC	–	no connect
C10	AVDD	power	power for analog circuit
D2	MCN	I/O	MIPI TX clock lane negative output
D3	EGND	ground	ground for MIPI TX circuit
D9	TM	input	test mode, active high with internal pull-down resistor
D10	AGND	ground	ground for analog circuit

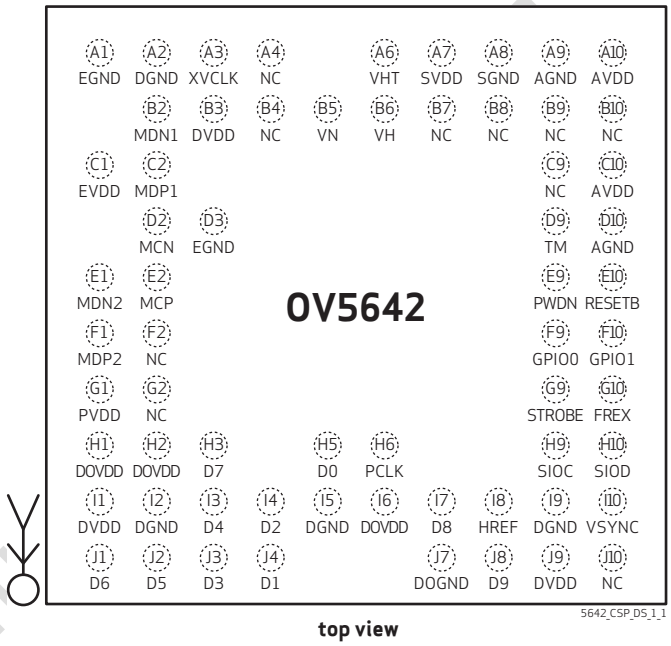
table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description
E1	MDN2	I/O	MIPI TX second data lane negative output
E2	MCP	I/O	MIPI TX clock lane positive output
E9	PWDN	input	power down, active high with internal pull-down resistor
E10	RESET_B	input	reset, active low with internal pull-up resistor
F1	MDP2	I/O	MIPI TX second data lane positive output
F2	NC	–	no connect
F9	GPIO0	I/O	GPIO port 0 / AFC port 0
F10	GPIO1	I/O	GPIO port 1 / AFC port 1
G1	PVDD	power	power for PLL circuit
G2	NC	–	no connect
G9	STROBE	I/O	strobe output
G10	FREX	I/O	frame exposure / mechanical shutter / GPIO port 12
H1	DOVDD	power	power for I/O circuit
H2	DOVDD	power	power for I/O circuit
H3	D7	I/O	DVP data output port 7 / GPIO port 9 / MIPI RX MCP input
H5	D0	I/O	DVP data output port 0 / GPIO port 2 / AFC port 2
H6	PCLK	I/O	DVP PCLK output / GPIO port 15
H9	SIOC	input	SCCB input clock
H10	SIOD	I/O	SCCB data
I1	DVDD	reference	power for digital circuit
I2	DGND	ground	ground for digital circuit
I3	D4	I/O	DVP data output port 4 / GPIO port 6 / MIPI RX MDN input
I4	D2	I/O	DVP data output port 2 / GPIO port 4 / IRIS filter
I5	DGND	ground	ground for digital circuit
I6	DOVDD	power	power for I/O circuit
I7	D8	I/O	DVP data output port 8 / GPIO port 10
I8	HREF	I/O	DVP HREF output / GPIO port 14
I9	DGND	ground	ground for digital circuit
I10	VSYNC	I/O	DVP VSYNC output / GPIO port 13
J1	D6	I/O	DVP data output port 6 / GPIO port 8 / MIPI RX MCN input

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description
J2	D5	I/O	DVP data output port 5 / GPIO port 7 / MIPI RX MDP input
J3	D3	I/O	DVP data output port 3 / GPIO port 5 / ND filter
J4	D1	I/O	DVP data output port 1 / GPIO port 3 / AFC port 3
J7	DOGND	ground	ground for I/O circuit
J8	D9	I/O	DVP data output port 9 / GPIO port 11
J9	DVDD	reference	power for digital circuit
J10	NC	–	no connect

figure 1-1 pin diagram



top view

2 system level description

2.1 overview

The OV5642 (color) image sensor is a low voltage, high-performance, 1/4-inch 5 megapixel CMOS image sensor that provides the full functionality of a single chip 5 megapixel (2592x1944) camera using OmniBSI™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed or arbitrarily scaled 8-bit/10-bit images in various formats via the control of the Serial Camera Control Bus (SCCB) interface or MIPI interface.

The OV5642 has an image array capable of operating at up to 15 frames per second (fps) in 5 megapixel resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface, MIPI interface or embedded microcontroller. The OV5642 also includes a compression engine for increased processing power. In addition, Omnivision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

The OV5642 has an embedded microcontroller, which can be combined with an internal autofocus engine and programmable general purpose I/O modules (GPIO) for external autofocus control. It also provides an anti-shake function with an internal anti-shake engine. For identification and storage purposes, the OV5642 also includes a one-time programmable (OTP) memory.

Compared to its predecessor, the OV5642 has embedded TrueFocus™ Lite that enables extended depth of field (EDoF).

The OV5642 supports both a digital video parallel port and a serial MIPI port. The MIPI and ISP interface can be used for a second camera sensor without requiring a dual serial port camera system.

2.2 architecture

The OV5642 sensor core generates streaming pixel data at a constant frame rate, indicated by HREF and VSYNC. **figure 2-1** shows the functional block diagram of the OV5642 image sensor. **figure 2-2** shows an example application using an OV5642 sensor.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of the array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV5642 block diagram

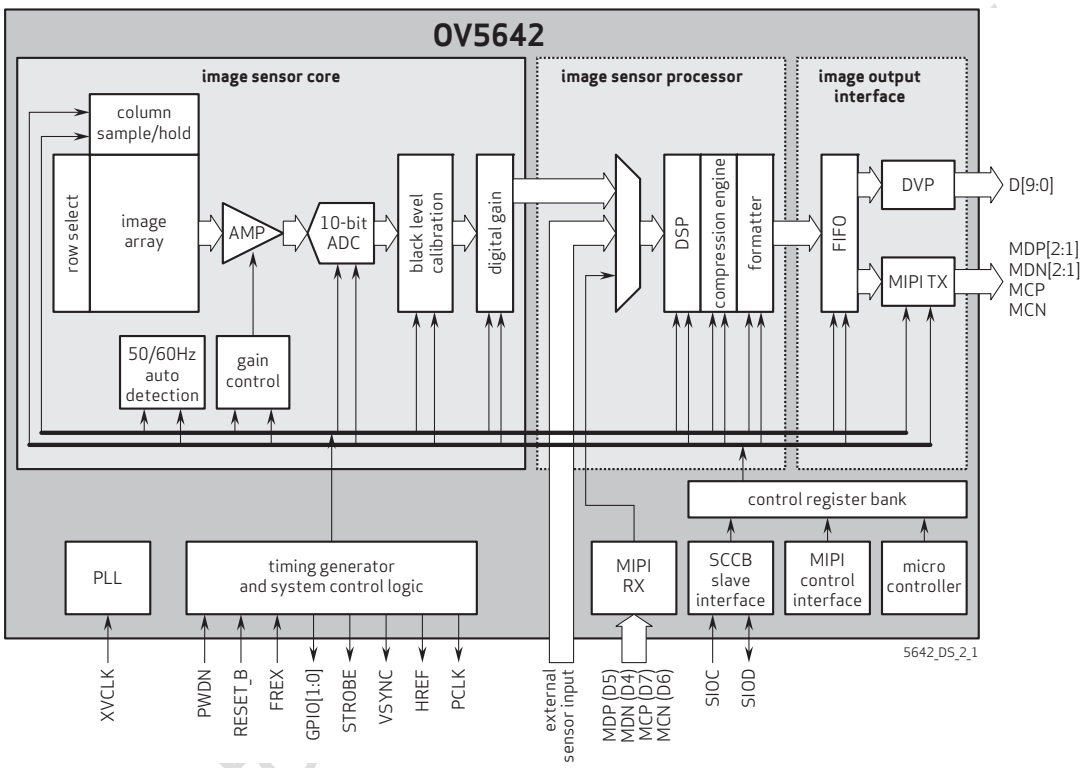
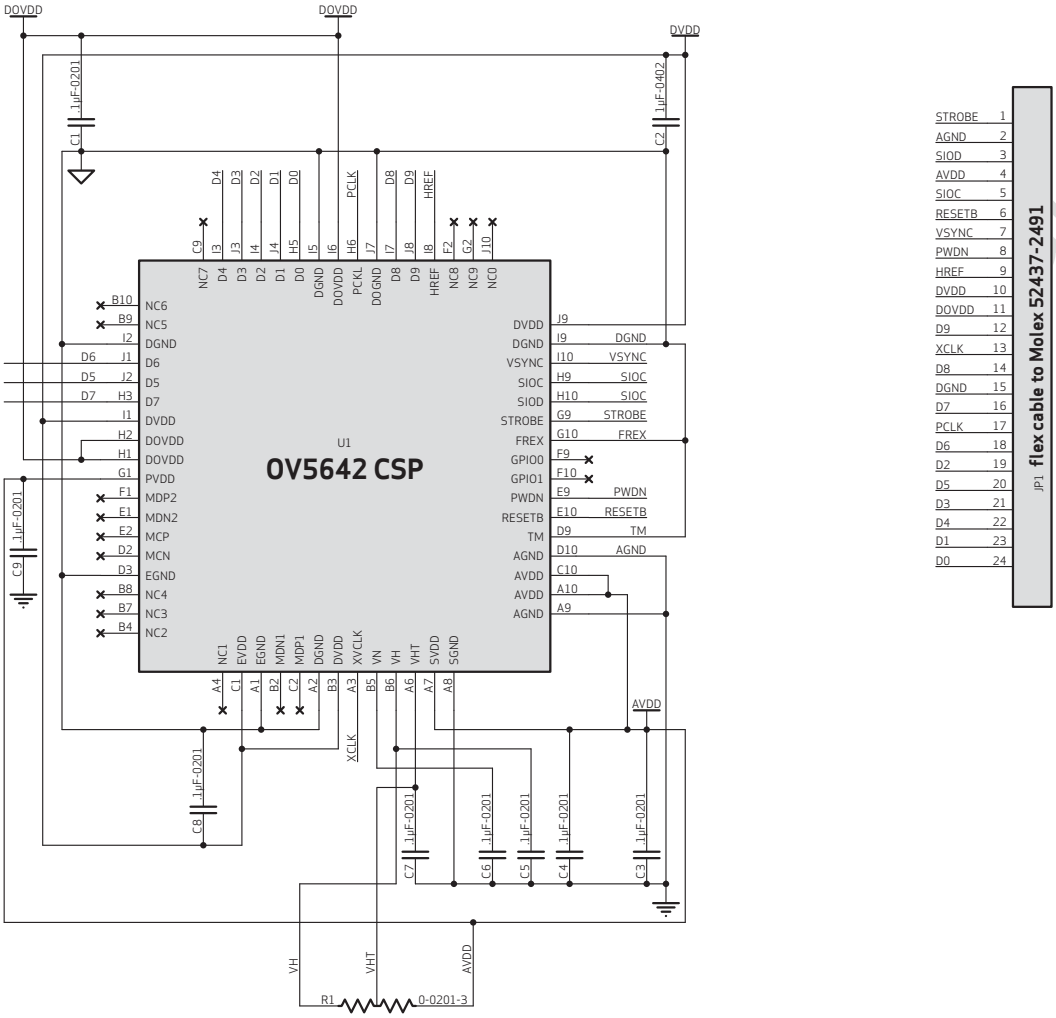


figure 2-2 reference design schematic



note 1 PWDN, active HIGH as DOVDD to power down OV5642, should be connected to ground outside of module if unused.

note 2 RESETB, active LOW to reset OV5642, should be connected to DOVDD outside of module if unused.

note 3 AVDD is 2.6 - 3.0V of sensor analog power (clean). 2.8V is recommended.

note 4 DVDD is 1.5V ±5% of sensor digital power (clean). Using the internal DVDD regulator is strongly recommended.

note 5 DOVDD, 1.8V recommended, is 1.7 - 3.0V of sensor digital IO power (clean).

note 6 sensor AGND and DGND should be separated and connected to a single point outside PCB (DO NOT connect inside module).

note 7 capacitors should be close to the related sensor pins.

note 8 D[9:0] is sensor 10-bit RGB output (D9: MSB, D0: LSB). D[9:2] is sensor 8-bit RGB output

note 9 R1 is a three-pad resistor (similar to two resistors near each other with one pad of the each resistor overlapped), the pad can only hold one 0 ohm resistor between VH and VHT or between VHT and AVDD.

5642_CSP_DS_2_2

2.3 I/O control

The OV5642 I/O pad direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pads.

table 2-1 driving capability and direction control for I/O pads (sheet 1 of 2)

function	register	R/W	description
output drive capability control	0x302C	RW	Bit[7:6]: output drive capability 00: 1x 01: 2x 10: 3x 11: 4x
D[9:0] I/O control	0x3017[3:0], 0x3018[7:2]	RW	input/output control for the D[9:0] pins: 0: input 1: output If input is selected: D7 can also be MIPI RX MCP input D6 can also be MIPI RX MCN input D5 can also be MIPI RX MDP input D4 can also be MIPI RX MDN input
D[9:0] output select	0x301D[3:0], 0x301E[7:2]	RW	output selection for the D[9:0] pins: 0: normal data path 1: register-controlled value
D[9:0] output value	0x301A[3:0], 0x301B[7:2]	RW	D[9:0] output value
D[9:0] input value	0x3041[3:0], 0x3042[7:2]	R	D[9:0] input value
VSYNC I/O control	0x3017	RW	Bit[6]: input/output control for the VSYNC pin: 0: input 1: output
VSYNC output select	0x301D	RW	Bit[6]: output selection for the VSYNC pin: 0: normal data path 1: register-controlled value
VSYNC output value	0x301A	RW	Bit[6]: VSYNC output value
VSYNC input value	0x3041	R	Bit[6]: VSYNC input value
HREF I/O control	0x3017	RW	Bit[5]: input/output control for the HREF pin: 0: input 1: output
HREF output select	0x301D	RW	Bit[5]: output selection for the HREF pin: 0: normal data path 1: register-controlled value
HREF output value	0x301A	RW	Bit[5]: HREF output value

table 2-1 driving capability and direction control for I/O pads (sheet 2 of 2)

function	register	R/W	description
HREF input value	0x3041	R	Bit[5]: HREF input value
PCLK I/O control	0x3017	RW	Bit[4]: input/output control for the PCLK pin: 0: input 1: output
PCLK output select	0x301D	RW	Bit[4]: output selection for the PCLK pin: 0: normal data path 1: register-controlled value
PCLK output value	0x301A	RW	Bit[4]: PCLK output value
PCLK input value	0x3041	R	Bit[4]: PCLK input value
STROBE I/O control	0x3016	RW	Bit[1]: input/output control for the STROBE pin: 0: input 1: output
STROBE output select	0x301C	RW	Bit[1]: output selection for the STROBE pin: 0: normal data path 1: register-controlled value
STROBE output value	0x3019	RW	Bit[1]: STROBE output value
STROBE input value	0x3040	R	Bit[5]: STROBE input value
FREX I/O control	0x3017	RW	Bit[7]: input/output control for the FREX pin: 0: input 1: output This port can be used for frame exposure/mechanical shutter
FREX output select	0x301D	RW	Bit[7]: output selection for the FREX pin: 0: normal data path 1: register-controlled value
FREX output value	0x301A	RW	Bit[7]: FREX output value
FREX input value	0x3040	R	Bit[4]: FREX input value
GPIO I/O control	0x3018	RW	Bit[1:0]: input/output control for the GPIO[1:0] pin: 0: input 1: output GPIO1 can used as AFC port1 and ND filter GPIO0 can used as AFC port1 and IRIS
GPIO output select	0x301E	RW	Bit[1:0]: output selection for the GPIO[1:0] pin: 0: normal data path 1: register-controlled value
GPIO output value	0x301B	RW	Bit[1:0]: GPIO[1:0] output value
GPIO input value	0x3042	R	Bit[1:0]: GPIO[1:0] input value

2.4 system clock control

The OV5642 PLL allows for an input clock frequency ranging from 6~27 MHz and has a maximum VCO frequency of 800 MHz. MipiClk is for the MIPI and SysClk is for the internal clock of the Image Signal Processing (ISP) block. The PLL can be bypassed by setting register 0x3011[7] to 1.

2.5 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

Group write is supported in order to update a group of registers in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary.

The OV5642 supports up to four groups. These groups share 1 KB RAM and the size of each group is programmable by adjusting the start address.

table 2-2 group sharing registers

address	register name	default value	R/W	description
0x3200	GROUP ADDR0	0x40	RW	Start Address for Group0 {group_addr0[7:0], 4'h0}
0x3201	GROUP ADDR1	0x4A	RW	Start Address for Group1 {group_addr1[7:0], 4'h0}
0x3202	GROUP ADDR2	0x54	RW	Start Address for Group2 {group_addr2[7:0], 4'h0}
0x3203	GROUP ADDR3	0x5E	RW	Start Address for Group3 {group_addr3[7:0], 4'h0}

The group write function is controlled by register **0x3212**.

table 2-3 group write register

address	register name	default value	R/W	description
0x3212	GROUP ACCESS	0x00	RW	Bit[7]: group_launch_en Bit[6]: Debug mode (must be 0) Bit[5]: group_launch Bit[4]: group_hold_end Bit[3:0]: group_id 00~11: ID of the group to hold register

The SCCB will enter group write mode after writing to register **0x3212** with a valid group ID. The subsequent registers will be held to the buffer specified by the group_id instead of writing to the registers. Make sure the number of registers does not exceed the capacity of the group. Setting group_hold_end to 1 will exit the group write mode. After that, setting both group_launch and group_launch_en to 1 will write the buffered values to the real registers. Multiple groups of registers can be prepared before writing to the real registers but be sure the correct group_id is specified when the group write is launched.

The following is an example demonstrating the group write operation:

```
78  3212  00    Enable group0
78  3600  00    Write registers to be held in group0
78  3601  01
78  3212  10    End group0
78  3212  01    Enable group1
78  3602  02    Write registers to be held in group1
78  3603  03
78  3212  11    End group1

.....           Other direct register access

78  3212  02    Enable group2
78  3604  04    Write registers to be held in group2
78  3605  05
78  3212  12    End group2

78  3212  A0    Launch group0

.....           Other direct register access

78  3212  03    Enable group3
78  3606  06    Write registers to be held in group3
78  3607  07
78  3212  13    End group3

78  3212  A1    Launch group1
78  3212  A2    Launch group2
78  3212  A3    Launch group3
```

2.6 power up sequence

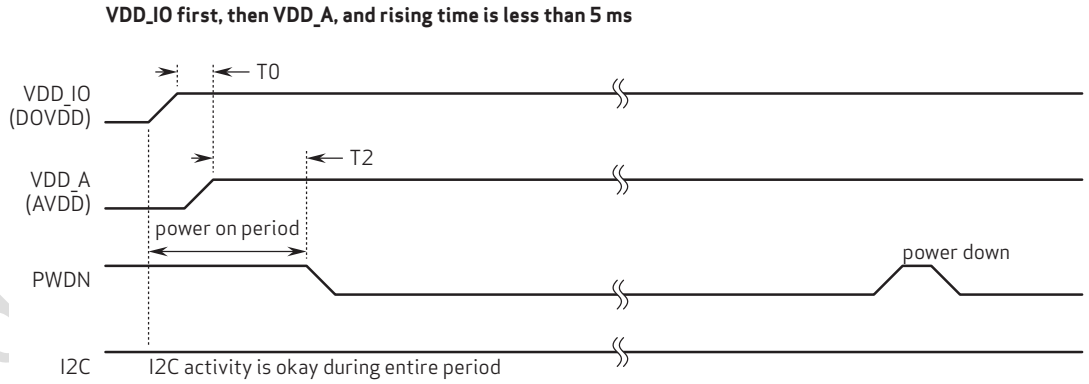
Based on the system power configuration (1.8V or 2.8V for I/O power, using external DVDD or internal DVDD, requiring access to the I2C during power up period or not), the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred. If 2.8V is used for I/O power, due to a high voltage drop at the internal DVDD regulator, there is a potential heat issue. Hence, for a 2.8V power system, OmniVision recommends using an external DVDD source. Due to the higher power down current when using an external DVDD source, OmniVision strongly recommends cutting off all powers, including the external DVDD, when the sensor is not in use in the case of 2.8V I/O and external DVDD.

2.6.1 power up with internal DVDD and I2C access during power up period

For powering up with the internal DVDD and I2C access during the power ON period, the following conditions must occur:

1. if V_{DD-IO} and V_{DD-A} are turned ON at the same time, make sure V_{DD-IO} becomes stable before V_{DD-A} becomes stable
2. PWDN is active high with an asynchronized design (does not need clock)
3. PWDN must go high if I2C is accessed during the power up period
4. for PWDN to go low, power up must first become stable (AVDD to PWDN ≥ 1 ms)
5. RESETB is active low with an asynchronized design
6. state of RESETB does not matter during power up period once DOVDD is up

figure 2-3 power up timing with internal DVDD and I2C access during power up period



note T0 ≥ 0 ms: delay from VDD_IO stable to VDD_A stable
T2 ≥ 1 ms: delay from VDD_A stable to sensor power up stable

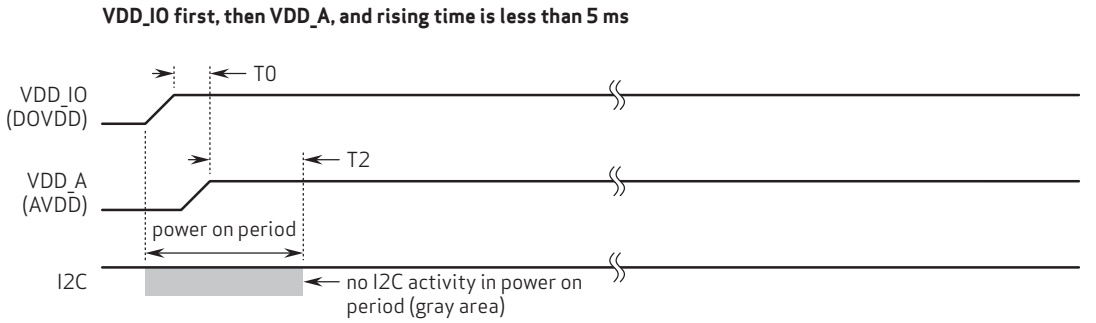
5642_DS_2_3

2.6.2 power up with internal DVDD and no I2C access during power up period

For powering up with the internal DVDD and no I2C access during the power ON period, the following conditions must occur:

1. if V_{DD-IO} and V_{DD-A} are turned ON at the same time, make sure V_{DD-IO} becomes stable before V_{DD-A} becomes stable
2. PWDN is not required if there is no I2C access during the power up period
3. no I2C activity is allowed during the power up period (see gray area in **figure 2-4**)
4. RESETB is active low with an asynchronized design
5. state of RESETB does not matter during power up period once DOVDD is up

figure 2-4 power up timing with internal DVDD and no I2C access during power up period



note T0 ≥ 0 ms: delay from VDD_IO stable to VDD_A stable
T2 ≥ 1 ms: delay from VDD_A stable to sensor power up stable

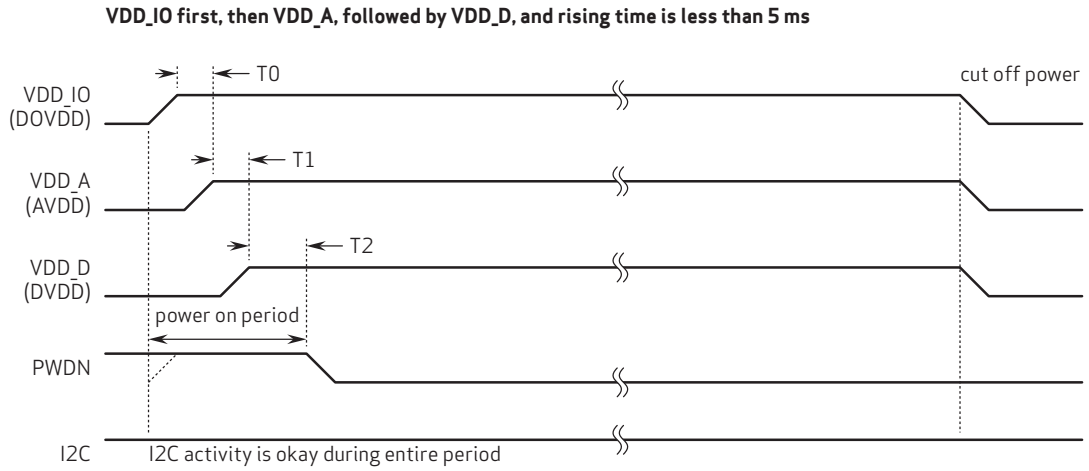
5642_DS_2_4

2.6.3 power up with external DVDD source and I2C access during power up period

For powering up with an external DVDD source and I2C access during the power ON period, the following conditions must occur:

1. if V_{DD-IO} and V_{DD-A} are turned ON at the same time, make sure V_{DD-IO} becomes stable before V_{DD-A} becomes stable
2. if V_{DD-A} and V_{DD-D} are turned ON at the same time, make sure VDD-A becomes stable before V_{DD-D} becomes stable
3. PWDN is active high with an asynchronized design (does not need clock)
4. for PWDN to go low, power up must first become stable (DVDD to PWDN ≥ 1 ms)
5. all powers are cut off when the camera is not in use (power down mode is not recommended
6. RESETB is active low with an asynchronized design
7. state of RESETB does not matter during power up period once DOVDD is up

figure 2-5 power up timing with external DVDD source and I2C access during power up period



note T0 ≥ 0 ms: delay from VDD_IO stable to VDD_A stable
T1 ≥ 0 ms: delay from VDD_A stable to VDD_C stable
T2 ≥ 1 ms: delay from VDD_C stable to sensor power up stable

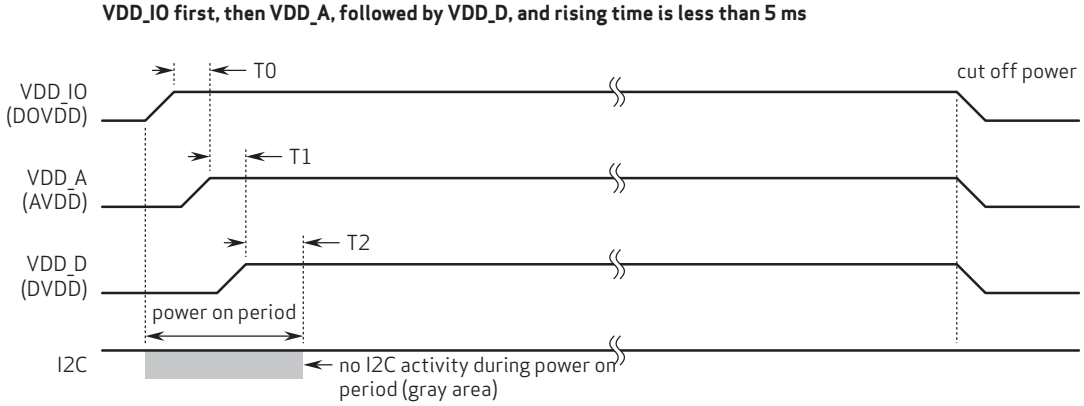
5642_DS_2_5

2.6.4 power up with external DVDD and no I2C access during power up period

For powering up with an external DVDD source and no I2C access during the power ON period, the following conditions must occur:

1. if V_{DD-IO} and V_{DD-A} are turned ON at the same time, make sure V_{DD-IO} becomes stable before V_{DD-A} becomes stable
2. if V_{DD-A} and V_{DD-D} are turned ON at the same time, make sure VDD-A becomes stable before V_{DD-D} becomes stable
3. all powers are cut off when the camera is not in use (power down mode is not recommended
4. RESETB is active low with an asynchronized design
5. state of RESETB does not matter during power up period once DOVDD is up

figure 2-6 power up timing with external DVDD source and I2C access during power up period



note T0 ≥ 0 ms: delay from VDD_IO stable to VDD_A stable
T1 ≥ 0 ms: delay from VDD_A stable to VDD_D stable
T2 ≥ 1 ms: delay from VDD_D stable to sensor power up stable

5642_DS_2_6

2.7 reset

The OV5642 sensor includes a **RESET_B** pin that forces a complete hardware reset when it is pulled low (GND). The OV5642 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register **0x3008**[7] to high.

2.8 standby and sleep

Two suspend modes are available for the OV5642:

- hardware standby
- SCCB software sleep

To initiate hardware standby mode, the **PWDN** pin must be tied to high. When this occurs, the OV5642 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software power down through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

The OV5642 also supports MIPI ultra low power state (ULPS). After receiving ULPS command from host, the OV5642 will enter into ULPS mode. Except for the low-speed part of the MIPI PHY and SCCB, all other blocks are enter into power down mode in ULPS mode.

3 block level description

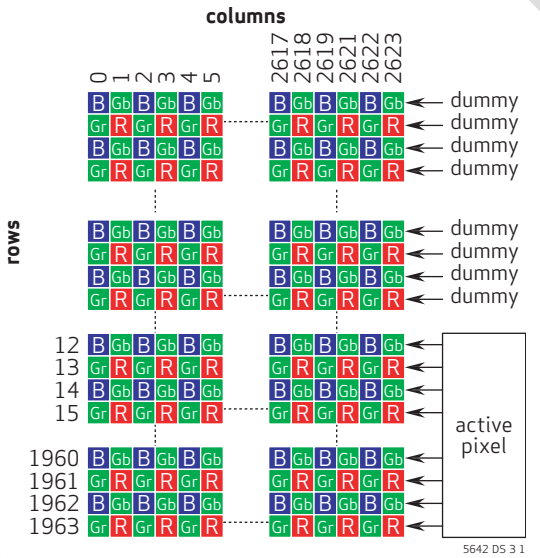
3.1 pixel array structure

The OV5642 sensor has an image array of 2624 columns by 1964 rows (5,153,536 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 5,153,536 pixels, 5,038,848 (2592x1944) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

figure 3-1 sensor array region color filter layout



3.2 binning

Binning mode is usually used for subsampling. During subsampling, information is periodically dropped when data is output. When the binning function is ON, voltage levels of adjacent pixels are averaged before being sent to the ADC. If the binning function is OFF, the pixels, which are not output, are merely skipped. The OV5642 supports 2x2, 1x2, and 2x1 binning. **figure 3-2** illustrates 2x2 binning, where the voltage levels of four (2x2) adjacent same-color pixels are averaged before entering the ADC.

figure 3-2 example of 2x2 binning

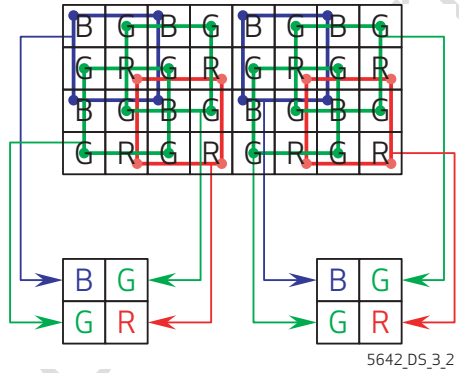


table 3-1 binning-related registers

address	register name	default value	R/W	description
0x370D	ANALOG CONTROL D	0x05	RW	Analog Control Bit[6]: Vertical binning enable
0x3621	ARRAY CONTROL 01	0x10	RW	Array Control 01 Bit[7]: Horizontal binning enable

4 image sensor core digital functions

4.1 mirror and flip

The OV5642 provides Mirror and Flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**). In flip, the OV5642 does not need additional settings because the ISP block will auto-detect whether the pixel is in the red line or blue line and make the necessary adjustments.

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

5642_DS_4_1

table 4-1 mirror and flip registers

address	register name	default value	R/W	description
0x3818	TIMING TC REG18	0x80	RW	Timing Control Bit[6]: Mirror[a] Bit[5]: Vertical flip

a. for the mirror function, it is also necessary to set registers 0x3621[5:4] and 0x3801

4.2 image windowing

An image windowing area is defined by four parameters, HS (horizontal start), HW (horizontal width), VS (vertical start), and VH (vertical height). By properly setting the parameters, any portion or size within the sensor array can be defined as a visible area. This windowing is achieved by simply masking the pixels outside the defined window; thus, it will not affect the original timing.

figure 4-2 image windowing

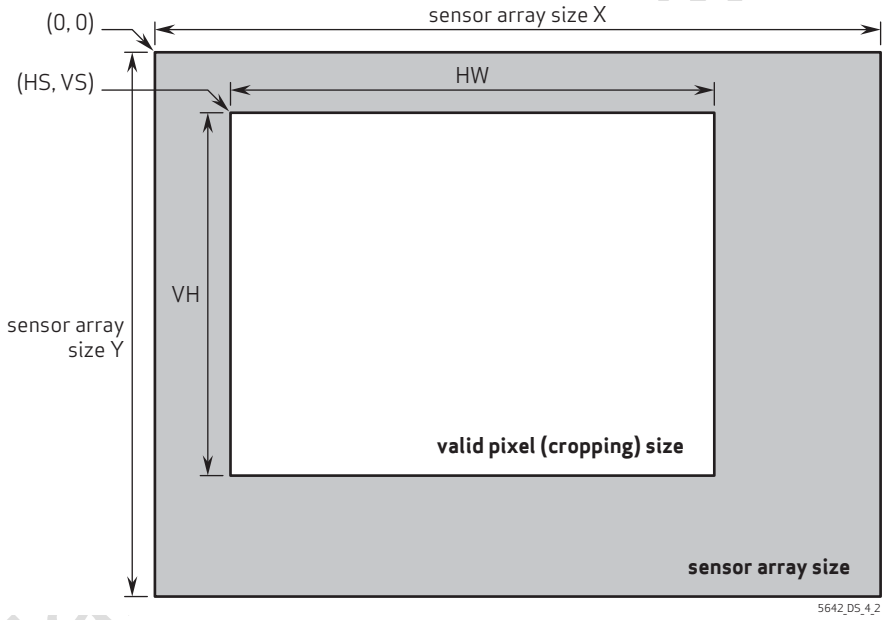


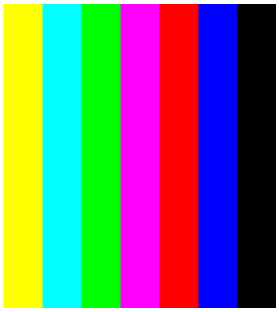
table 4-2 image windowing registers

address	register name	default value	R/W	description
0x3800	TIMING CONTROL HS	0x01	RW	HREF Horizontal Start Point high byte[11:8]
0x3801	TIMING CONTROL HS	0xB4	RW	HREF Horizontal Start Point low byte[7:0]
0x3802	TIMING CONTROL VS	0x00	RW	HREF Vertical Start Point high byte[11:8]
0x3803	TIMING CONTROL VS	0x0A	RW	HREF Vertical Start Point high byte[7:0]
0x3804	TIMING HW	0x08	RW	Bit[3:0]: HREF horizontal width high byte[11:8]
0x3805	TIMING HW	0x00	RW	Bit[7:0]: HREF horizontal width high byte[7:0]
0x3806	TIMING VH	0x06	RW	Bit[3:0]: HREF vertical height high byte[11:8]
0x3807	TIMING VH	0x00	RW	Bit[7:0]: HREF vertical height high byte[7:0]

4.3 test pattern

For testing purposes, the OV5642 offers one type of test pattern, color bar.

figure 4-3 test pattern



color bar

table 4-3 test pattern selection control

function	register	description
color bar	0x503D	Bit[7]: color bar enable 0: color bar OFF 1: color bar enable
	0x503D	Bit[5:4]: color bar pattern select 00: color bar pattern

4.4 50/60hz detection

4.4.1 overview

When the integration time is not an integer multiple of the period of light intensity, the image will flicker. The function of the detector is to detect whether the sensor is under a 50 Hz or 60 Hz light source so that the basic step of integration time can be determined. Contact your local OmniVision FAE for auto detection settings.

4.5 AEC/AGC algorithms

4.5.1 overview

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in **table 4-4**.

table 4-4 AEC/AGC control functions

address	register name	default value	R/W	description
0x3500	AEC PK LONG EXPO	0x00	RW	Long Channel Exposure Output Bit[3:0]: Exposure[19:16]
0x3501	AEC PK LONG EXPO	0x00	RW	Long Channel Exposure Output Bit[7:0]: Exposure[15:8]
0x3502	AEC PK LONG EXPO	0x00	RW	Long Channel Exposure Output Bit[7:0]: Exposure[7:0]
0x3503	AEC PK MANUAL	0x00	RW	AEC Manual Mode Control Bit[2]: VTS manual 0: Auto enable 1: Manual enable Bit[1]: AGC manual 0: Auto enable 1: Manual enable Bit[0]: AEC manual 0: Auto enable 1: Manual enable
0x3508	AEC PK LONG GAIN	0x00	RW	Long Channel Gain Output Bit[0]: Gain high bit
0x3509	AEC PK LONG GAIN	0x00	RW	Long Channel Gain Output Bit[7:0]: Gain low bits
0x350A	AEC PK AGC ADJ	0x00	RW	Gain Output to Sensor Bit[0]: Gain high bit
0x350B	AEC PK AGC ADJ	0x00	RW	Gain Output to Sensor Bit[7:0]: Gain low bits
0x350C	AEC PK VTS	0x06	RW	AEC VTS Output Bit[7:0]: VTS high bits[15:8]
0x350D	AEC PK VTS	0x18	RW	AEC VTS Output Bit[7:0]: VTS low bits[7:0]

4.5.2 average-based algorithm

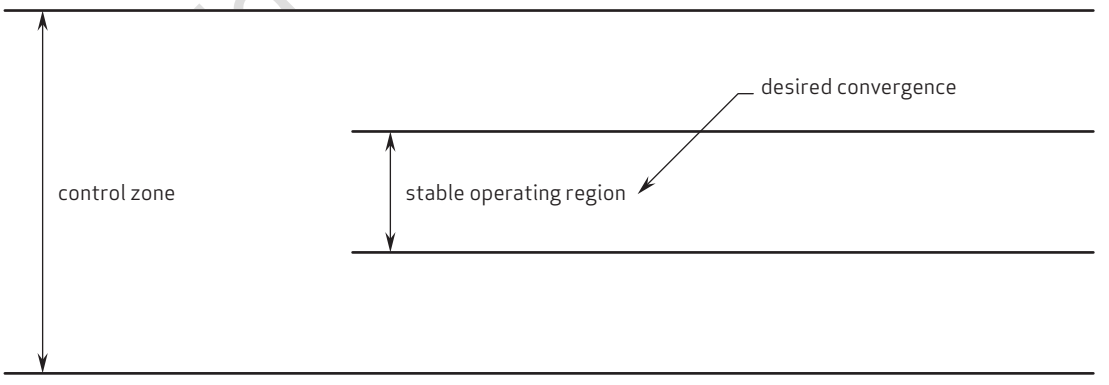
The average-based AEC controls image luminance using registers **AEC CTRL0F** (0x3A0F), **AEC CTRL10** (0x3A10), **AEC CTRL1B** (0x3A1B), and **AEC CTRL1E** (0x3A1E). In average-based mode, the value of register **AEC CTRL0F** (0x3A0F) indicates the high threshold value, and the value of register **AEC CTRL10** (0x3A10) indicates the low threshold value. The value of register **AEC CTRL1B** (0x3A1B) indicates the high threshold value for image change from stable state to unstable state and the value of register **AEC CTRL1E** (0x3A1E) indicates the low threshold value for image change from stable state to unstable state. When the target image luminance average value **AVG R10** (0x5690) is within the range specified by registers **AEC CTRL1B** (0x3A1B) and **AEC CTRL1E** (0x3A1E), the AEC keeps the image exposure and gain. When register **AVG R10** (0x5690) is greater than the value in register **AEC CTRL1B** (0x3A1B), the AEC will decrease the image exposure and gain until it falls into the range of {0x3A10, 0x3A0F}. When register **AVG R10** (0x5690) is less than the value in register **AEC CTRL1B** (0x3A1E), the AEC will increase the image exposure and gain until it falls into the range of {0x3A10, 0x3A0F}. Accordingly, the value in register **AEC CTRL0F** (0x3A0F) should be greater than the value in register **AEC CTRL10** (0x3A10). The gap between the values of registers **AEC CTRL1B** (0x3A1B) and **AEC CTRL1E** (0x3A1E) controls the image stability.

The AEC function supports both manual and auto speed selections in order to bring the image exposure into the range set by the values in registers **AEC CTRL0F** (0x3A0F) and **AEC CTRL10** (0x3A10). For manual mode, the speed supports both normal and fast speed selection. AEC set to normal mode will allow for the slowest step increment or decrement in the image exposure to maintain the specified range. AEC set to fast mode will provide for an approximate ten-step increment or decrement in the image exposure to maintain the specified range. For auto mode, the speed step will automatically be adjusted according to the difference between the target and present values. The auto ratio of steps can be set by register bits **AVG R10**[6:2] (0x5690); thus, the AEC speed can be adjusted automatically by the image average value or controlled manually.

Register **AEC CTRL11** (0x3A11) and register **AEC CTRL1F** (0x3A1F) controls the fast AEC range in manual speed selection made. If the target image **AVG R10** (0x5690) is greater than **AEC CTRL11** (0x3A11), AEC will decrease by half. If register **AVG R10** (0x5690) is less than **AEC CTRL1F** (0x3A1F), AEC will double.

As shown in **figure 4-4**, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone, which defines the convergence step size of fast and slow conditions.

figure 4-4 desired convergence



As for auto mode, the AEC will automatically calculate the steps needed based on the difference between target and current values. So, the outer control zone is meaningless for this mode.

table 4-5 AEC/AGC control functions

address	register name	default value	R/W	description
0x3A0F	AEC CTRL0F	0x78	RW	Stable Range High Limit (enter) Bit[7:0]: WPT
0x3A10	AEC CTRL10	0x68	RW	Stable Range Low Limit (enter) Bit[7:0]: BPT
0x3A11	AEC CTRL11	0xD0	RW	Step Manual Mode, Fast Zone High Limit Bit[7:0]: vpt_high
0x3A1B	AEC CTRL1B	0x78	RW	Stable Range High Limit (go out) Bit[7:0]: WPT2
0x3A1E	AEC CTRL1E	0x68	RW	Stable Range Low Limit (go out) Bit[7:0]: BPT2
0x3A1F	AEC CTRL1F	0x40	RW	Step Manual Mode, Fast Zone Low Limit Bit[7:0]: vpt_low

For the average-based AEC/AGC algorithm, the measured window is horizontally and vertically adjustable and divided by sixteen (4x4) zones (see **figure 4-5**). Each zone (or block) is 1/16th of the image and has a 4-bit weight in calculating the average luminance (YAVG). The 4-bit weight could be n/16 where n is from 0 to 15. The final YAVG is the weighted average of the sixteen zones.

4.5.2.1 average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. By properly setting x_start, x_end, y_start, and y_end as shown in **figure 4-5**, a 4x4 grid average window is defined. It will automatically divide each zone into 4x4 zones. The average value is the weighted average of the 16 sections. **table 4-6** lists the corresponding registers.

figure 4-5 average-based window definition

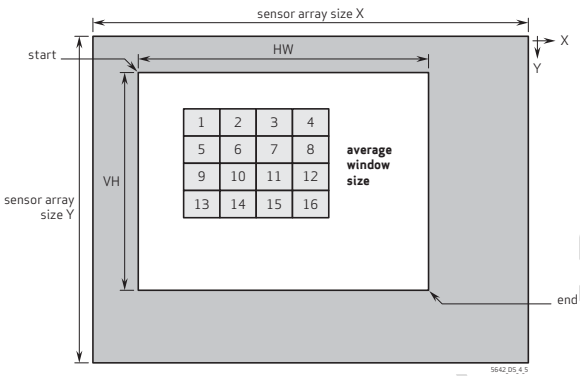


table 4-6 average-based algorithm functions

function	register	description
horizontal start pixel	{0x5680[3:0], 0x5681}	x_start[11:8] = 0x5680[3:0] x_start[7:0] = 0x5681[7:0]
vertical start pixel	{0x5684[2:0], 0x5685}	y_start[10:8] = 0x5684[2:0] y_start[7:0] = 0x5685[7:0]
horizontal end pixel	{0x5682[3:0], 0x5683}	x_end[11:8] = 0x5682[3:0] x_end[7:0] = 0x5683[7:0]
vertical end pixel	{0x5686[2:0], 0x5687}	y_end[11:8] = 0x5686[2:0] y_end[7:0] = 0x5687[7:0]
average section weighting	0x5688~0x568F	section 1 weight = 0x5688[3:0] section 2 weight = 0x5688[7:4] section 3 weight = 0x5689[3:0] section 4 weight = 0x5689[7:4] section 5 weight = 0x568A[3:0] section 6 weight = 0x568A[7:4] section 7 weight = 0x568B[3:0] section 8 weight = 0x568B[7:4] section 9 weight = 0x568C[3:0] section 10 weight = 0x568C[7:4] section 11 weight = 0x568D[3:0] section 12 weight = 0x568D[7:4] section 13 weight = 0x568E[3:0] section 14 weight = 0x568E[7:4] section 15 weight = 0x568F[3:0] section 16 weight = 0x568F[7:4]

4.6 AEC/AGC steps

The AEC and AGC work together to obtain adequate exposure/gain based on the current environmental illumination. In order to achieve the best SNR, extending the exposure time is always preferred rather than raising the gain when the current illumination is getting brighter. Vice versa, under dark conditions, the action to decrease the gain is always taken prior to shortening the exposure time.

4.6.1 auto exposure control (AEC)

The function of the AEC is to calculate the integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remain the same.

In extremely bright situations, the LAEC activates, allowing integration time to be less than one row. In extremely dark situations, the night mode activates, allowing integration time to be larger than one frame.

To avoid image flickering under a periodic light source, the integration time can be adjusted in steps of integer multiples of the period of the light source. This new AEC step system is called the banding filter, suggesting that the exposure time is not continuous but falls in some steps.

4.6.1.1 LAEC

If the integration time is only one row period but the image is too bright, AEC will enter LAEC mode. Within LAEC, the integration time can be further decreased to the minimum of 1/16 row. LAEC ON/OFF can be set in register bit 0x3A00[6].

4.6.1.2 banding mode ON with AEC

In Banding ON mode, the exposure time will fall in steps of integer multiples of the period of light intensity. This design is to reject image flickering when the light source is not steady but periodical.

For a given light flickering frequency, the band step can be expressed in units of row period.

Band Step = 'period of light intensity' × 'frame rate' × 'rows per frame'.

The band steps for 50Hz and 60Hz light sources can be set in registers {0x3A08[5:0], 0x3A09[7:0]} and {0x3A0A[5:0], 0x3A0B[7:0]}, respectively.

When auto-banding is ON, if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If auto-banding is disabled, the minimum integration time is one band step. Auto banding can be set in register bit 0x3A00[4].

4.6.1.3 banding mode OFF with AEC

When banding mode is OFF, integration time increases/decreases as normal. It is not necessarily multiples of band steps.

4.6.1.4 night mode

The OV5642 supports long integration time such as 1 frame, 2 frames, 3 frames, 4 frames, 5 frames, 6 frames, 7 frames, and 8 frames in dark conditions. This is achieved by slowing down the original frame rate and waiting for exposure. Night mode ceiling can be set in register bits 0x3A02[19:16], 0x3A03[15:8], and 0x3A04[7:0]. Night mode can be disabled by setting register bit 0x3A00[2] to 0. Also, when in night mode, the increase and decrease step can be based on band or frames, depending on register 0x3A05[6]. The minimum increase/decrease step can be one band. The step can be based both on bands and frames.

4.6.2 manual exposure control

To manually change exposure value, you must first set both 0x3503[0] and 0x3503[2], where 0x3503[0] enables manual exposure control and 0x3503[2] enables manual frame length - the number of lines in each frame or maximum exposure time, which is defined by registers 0x350C and 0x350D. In auto exposure mode, the maximum exposure values in registers 0x350C/0x350D automatically change. In manual exposure mode, these registers will not automatically change. The manually set exposure in registers 0x3500~0x03502 must be less than the maximum exposure value in 0x350C/0x350D. The exposure value in registers 0x3500~0x3502 is in units of line*16 - the low 4 bits (0x3502[3:0]) is the fraction of line, the maximum value in 0x350C/0x350D is in unit of line. If the manually set exposure value is less than one pre-defined frame period (e.g., 1/15 second in 15fps), there is no need to change 0x350C/0x350D. If the exposure value needs to be set beyond the pre-defined frame period; in another words, if the frame period needs to be extended to extend exposure time, then the maximum frame value in 0x350C/0x350D needs to be set first, then the exposure can be set in registers 0x3500~0x3502 accordingly.

4.6.3 auto gain control (AGC)

Unlike prolonging integration time, increasing gain will amplify both signal and noise. Thus, AGC usually starts after AEC is full. However, in cases where adjacent AEC step changes are too large (>1/16), AGC steps should be inserted in between; otherwise, the integration time will keep switching between two adjacent steps and the image flickers.

4.6.3.1 integration time between 1~16 rows

When integration time is less than 16 rows, the changes between adjacent AEC steps are larger than 1/16, which may possibly make the image oscillate between two AEC levels; thus, some AGC steps are added in between.

4.6.3.2 gain insertion between AEC banding steps

When banding mode is ON, the integration time changes in step of the period of light intensity. For the first 16 band steps, since the exposure time change between adjacent steps is larger than 1/16, AGC steps are inserted to ensure image stability.

4.6.3.3 gain insertion between night mode steps

Between night mode steps (e.g., integration time = 1 frame and 2 frames), AGC steps are inserted to ensure no adjacent step change is larger than 1/16.

4.6.3.4 when AEC reaches maximum

When AEC reaches its maximum step while the image is still too dark, the gain starts to increase until the new frame average falls into the stable range or AGC reaches its maximum step. The AGC ceiling can be set in {0x3A18[9:8], 0x3A19[7:0]}.

4.6.4 manual gain control

To manually change gain, first set register bit 0x3503[1] to enable manual control, then change the values in 0x350A/0x350B for the manual gain. The OV5642 has a maximum of 64x gain.

4.7 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration. There are three main functions of the BLC:

- Combining two ADC data paths into one data path
- Adjusting all normal pixel values based on the values of the black levels
- Applying multiplication to all pixel values based on digital gain

Black level adjustments can be made with registers 0x4000 through 0x401E.

table 4-7 BLC control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x4000	BLC CTRL 00	0x09	RW	BLC Control 00 Bit[1]: Freeze enable 0: BLC will be updated when necessary 1: BLC will keep original value Bit[0]: BLC enable
0x4006	LONG EXPOSURE BLACK LEVEL TARGET	0x00	RW	Black Level Target for Long Exposure Bit[1:0]: l_blacklevel_target[9:8] Black level target for long exposure
0x4007	LONG EXPOSURE BLACK LEVEL TARGET	0x20	RW	Black Level Target for Long Exposure Bit[7:0]: l_blacklevel_target[7:0] Black level target for long exposure
0x400C	BLC CTRL 03	0x00	RW	BLC Control 03 Bit[7]: frame_up_flag n frames of BLC form its rising edge when BLC is enabled where n is the number set in the **BLC FRAME** register Bit[6]: format_change_en 1: Do n frames of BLC when image format changes

table 4-7 BLC control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x401D	BLC FRAME CTRL	0x00	RW	Black Line Frame Control Bit[5:4]: blc_en_mode 00: BLC always updates 01: BLC updates when the lowest 4 bits of the sensor gain changes 10: BLC updates when the highest 5 bits of the sensor gain changes 11: BLC updates only when the frame number is less than max frame Bit[1]: format_change_en If this function is enabled and the format_change_flag_i is active, the frame count is cleared to update BLC Bit[0]: frames_up_flag Clear the frame count to update BLC
0x401E	BLC FRAME	0xFF	RW	BLC will be updated when the current frame number is less than its value

4.8 light frequency selection

The OV5642 can detect the light flickering frequency. When this function is enabled, the sensor can detect the light frequency and select the corresponding banding filter value. To remove banding, the banding filter should be turned on and the banding filter value should be set to the appropriate value.

table 4-8 light frequency registers

address	register name	default value	R/W	description
0x3C01	ALFD_CTRL1	0x00	RW	Bit[7]: Auto detection enable 0: Enable auto detection 1: Disable auto detection
0x3C00	ALFD_CTRL2	0x00	RW	Bit[2]: Manual light frequency selection 0: 60 Hz 1: 50 Hz
0x3C0C	ALFD_CTRLC	0x00	R	Bit[0]: Auto light frequency indicator 0: 60 Hz 1: 50 Hz

4.9 digital gain

The OV5642 supports 1/2/3/4 digital gain. Normally, the gain is controlled automatically by the automatic gain control (AGC) block. Manual mode is also provided.

table 4-9 digital gain control functions

address	register name	default value	R/W	description
0x4000	BLC CTRL 00	0x09	RW	BLC Control 00 Bit[4]: dig_gain_man_en Manual digital gain enable
0x4003	BLC CTRL 03	0x80	RW	BLC Control 03 Bit[1:0]: dig_gain_man Manual digital gain 00: 1x 01: 2x 10: 3x 11: 4x

4.10 strobe flash and frame exposure

4.10.1 strobe flash control

The strobe signal is programmable. It supports both LED and Xenon modes. The polarity of the pulse can be changed. The strobe signal is enabled (turned high/low depending on the pulse's polarity) by requesting the signal via the SCCB interface. Flash modules are triggered by the rising edge by default or by the falling edge if the signal polarity is changed. It supports the following flashlight modes (see **table 4-10**).

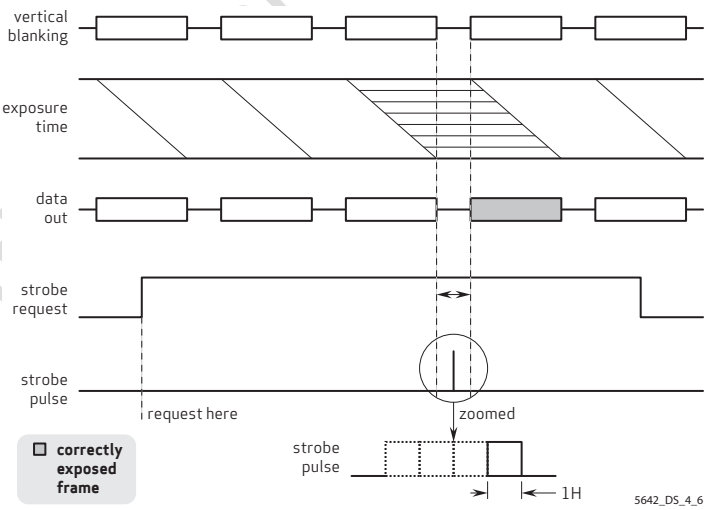
table 4-10 flashlight modes

mode	output	AEC / AGC	AWB
xenon	one-pulse	no	no
LED 1	pulse	no	no
LED 2	pulse	no	yes
LED 3	continuous	yes	yes

4.10.1.1 xenon flash control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see **figure 4-6**). The third frame will be correctly exposed. The pulse width can be changed in Xenon mode between 1H and 4H, depending on register 0x3B00[3:2], where H is one row period.

figure 4-6 xenon flash mode



4.10.1.2 LED 1 & 2 mode

Two frames after the strobe request is submitted, the third frame is correctly exposed. The strobe pulse will be activated only one time if the strobe end request is set correctly (see **figure 4-7**). If end request is not sent, the strobe signal is activated intermittently until the strobe end request is set (see **figure 4-8**). The number of skipped frames is programmable using registers {0x3A1C, 0x3A1D}.

figure 4-7 LED 1 & 2 mode - one pulse output

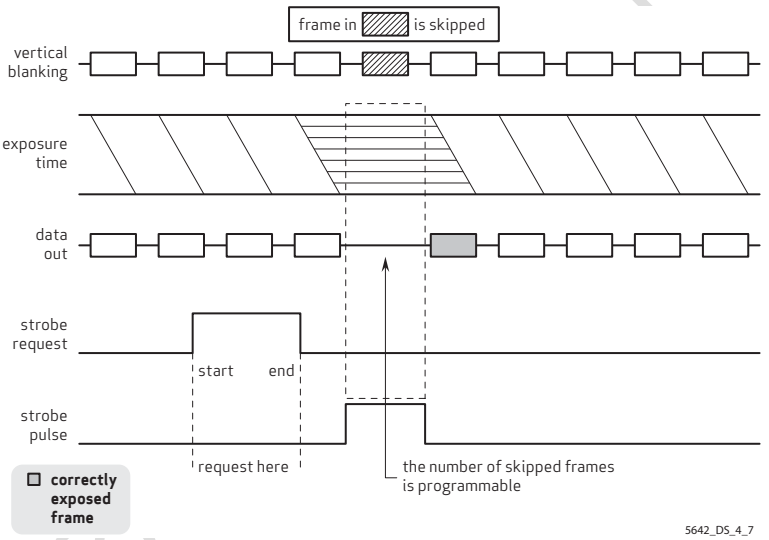
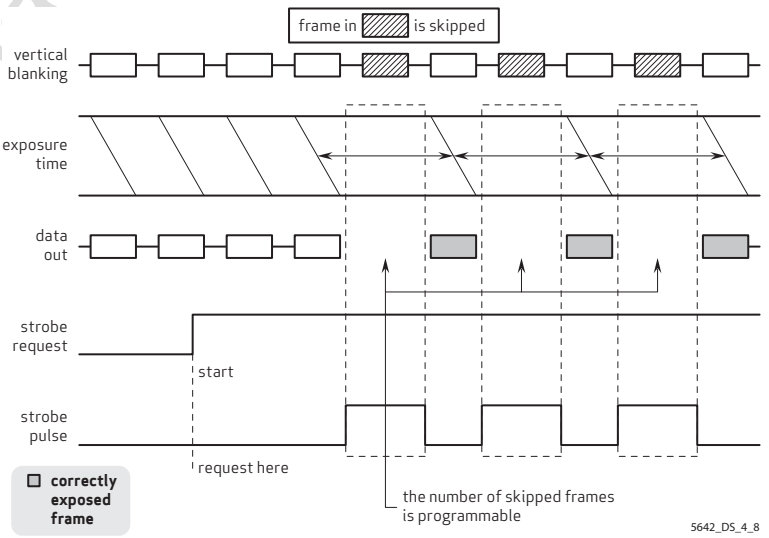


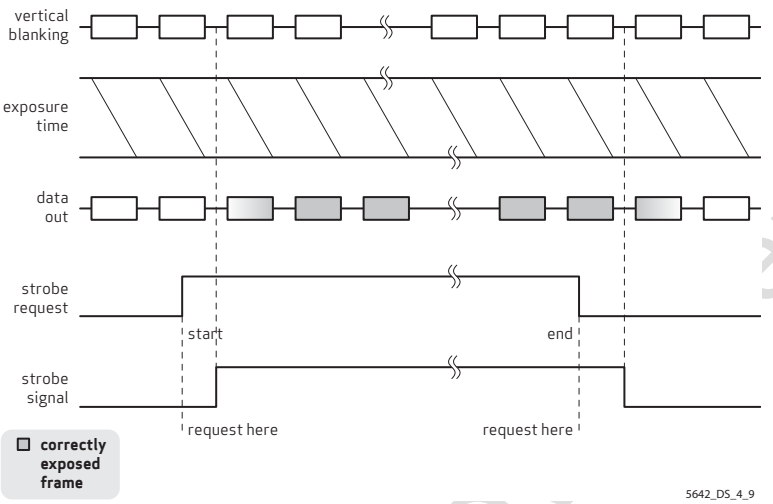
figure 4-8 LED 1 & 2 mode - multiple pulse output



4.10.1.3 LED 3 mode

In LED 3 mode, the strobe signal stays active until the strobe end request is sent (see **figure 4-9**).

figure 4-9 LED 3 mode



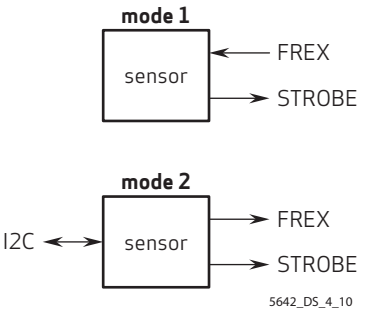
4.10.2 frame exposure (FREX) mode

In FREX mode, whole frame pixels start integration at the same time, rather than integrating row by row. After the user-defined exposure time (registers {0x3B04, 0x3B05}), the shutter closes, preventing further integration and the image begins to read out. After the readout finishes, the shutter opens again and the sensor resumes normal mode, waiting for the next FREX request.

The OV5642 supports two modes of FREX (see **figure 4-10**):

- mode 1 - frame exposure and shutter control requests come from the external system via the FREX pin. The sensor will send a strobe output signal to control the flash light.
- mode 2 - frame exposure request comes from the external system via the I2C register 0x3B08[0]. The sensor will output two signals, shutter control signal through the FREX pin and strobe signal through the STROBE pin.

figure 4-10 FREX modes



In mode 1, the FREX pin is configured as an input while it is configured as an output in mode 2. In both mode 1 and mode 2, the strobe output is irrelevant with the rolling strobe function. When in rolling shutter mode, the strobe function and this FREX/shutter control function do not work at the same time.

4.10.3 FREX strobe flash control

See **table 4-11** for FREX strobe control functions.

table 4-11 FREX strobe control functions

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Strobe Control Bit[7]: Strobe request ON/OFF 0: OFF/BLC 1: ON Bit[6]: Strobe pulse reverse Bit[3:2]: width_in_xenon 00: 1H 01: 2H 10: 3H 11: 4H Bit[1:0]: Strobe mode 00: xenon 01: LED 1 10: LED 2 11: LED 3
0x3B04	STROBE FREX EXP	0x04	RW	Strobe FREX Explore High
0x3B05	STROBE FREX EXP	0x00	RW	Strobe FREX Explore Low
0x3B06	FREX CTRL	0x04	RW	FREX Control Bit[7:4]: FREX frame delay number
0x3B07	FREX MODE SEL	0x08	RW	FREX Mode Select Bit[1:0]: FREX mode select 0x: Rolling strobe 10: FREX strobe mode 1 11: FREX strobe mode 2
0x3B08	FREX EXPLORE REQ	0x00	RW	Strobe FREX Explore Request

4.11 one time programmable (OTP) memory

The OV5642 supports a maximum of 128 bits of one-time programmable (OTP) memory to store chip identification and manufacturing information. It can be controlled through the SCCB (see **table 4-12**).

table 4-12 OTP control functions

function	register	description
OTP dump / program[a]	0x3D10[7:0]	Bit[1:0]: OTP_opt_mode 00: OTP off 01: load / dump OTP 10: write / program OTP 11: OTP off
dump / program data 0[b]	0x3D00[7:0]	data dumped or data to be programmed for bits 0 ~ 7
dump / program data 1[b]	0x3D01[7:0]	data dumped or data to be programmed for bits 8 ~ 15
dump / program data 2[b]	0x3D02[7:0]	data dumped or data to be programmed for bits 16 ~ 23
dump / program data 3[b]	0x3D03[7:0]	data dumped or data to be programmed for bits 24 ~ 31
dump / program data 4	0x3D04[7:0]	data dumped or data to be programmed for bits 32 ~ 39
dump / program data 5	0x3D05[7:0]	data dumped or data to be programmed for bits 40 ~ 47
dump / program data 6	0x3D06[7:0]	data dumped or data to be programmed for bits 48 ~ 55
dump / program data 7	0x3D07[7:0]	data dumped or data to be programmed for bits 56 ~ 63
dump / program data 8	0x3D08[7:0]	data dumped or data to be programmed for bits 64 ~ 71
dump / program data 9	0x3D09[7:0]	data dumped or data to be programmed for bits 72 ~ 79
dump / program data A	0x3D0A[7:0]	data dumped or data to be programmed for bits 80 ~ 87
dump / program data B	0x3D0B[7:0]	data dumped or data to be programmed for bits 88 ~ 95
dump / program data C	0x3D0C[7:0]	data dumped or data to be programmed for bits 96 ~ 103
dump / program data D	0x3D0D[7:0]	data dumped or data to be programmed for bits 104 ~ 111
dump / program data E	0x3D0E[7:0]	data dumped or data to be programmed for bits 112 ~ 119
dump / program data F	0x3D0F[7:0]	data dumped or data to be programmed for bits 120 ~ 127

a. AVDD must be 2.5V ± 5% when writing/programming OTP; otherwise, there will be reliability issues. There is no such limitation when reading OTP under normal operating conditions.

b. 0x3D00 ~ 0x3D04 is reserved for OmniVision internal use.

5 image sensor processor digital functions

5.1 ISP general controls

The ISP module provides lens correction, gamma, de-noise, sharpen, auto focus, etc. These functions are enabled by registers 0x5000 ~ 0x5007.

table 5-1 ISP general control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0xDF	RW	ISP Control 00 Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6]: Gamma (in YUV domain) enable 0: Disable 1: Enable Bit[5]: RAW gamma enable 0: Disable 1: Enable Bit[4]: Even odd removing enable 0: Disable 1: Enable Bit[3]: De-noise enable 0: Disable 1: Enable Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Color interpolation (CIP) enable 0: Disable 1: Enable

table 5-1 ISP general control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x4F	RW	ISP Control 01 Bit[7]: Special Digital Effects (SDE) enable 0: Disable 1: Enable Bit[6]: UV adjust enable 0: Disable 1: Enable Bit[5]: Vertical scaling enable 0: Disable 1: Enable Bit[4]: Horizontal scaling enable 0: Disable 1: Enable Bit[3]: Line stretch enable 0: Disable 1: Enable Bit[2]: UV average enable 0: Disable 1: Enable Bit[1]: Color matrix enable 0: Disable 1: Enable Bit[0]: Auto white balance (AWB) enable 0: Disable 1: Enable
0x5002	ISP CONTROL 02	0xE0	RW	ISP Control02 Bit[7]: Thumbnail scaling enable 0: Disable 1: Enable Bit[4]: Dithering enable 0: Disable 1: Enable Bit[3]: YUV to RGB enable 0: Disable 1: Enable Bit[2]: Horizontal sub-sampling enable 0: Disable 1: Enable

table 5-1 ISP general control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5003	ISP CONTROL 03	0xA8	RW	ISP Control 03 Bit[3]: YUV to YCbCr enable 0: Disable 1: Enable Bit[2]: YUV422 input enable 0: Disable 1: Enable Bit[1]: Draw window for AFC enable 0: Disable 1: Enable
0x5005	ISP CONTROL 05	0xDC	RW	ISP Control 05 Bit[7]: Raw gamma option 1 0: Does not add back BLC bias after raw gamma correction 1: Adds back BLC bias after raw gamma correction Bit[6]: Raw gamma option 2 0: Raw gamma applied on input data directly regardless of the black level 1: Subtract black level before applying raw gamma Bit[4]: Advanced AWB option 1 0: Do not subtract black level 1: Subtract black level before statistics and apply gain Bit[3]: Lens correction option 1 0: Does not add back BLC bias after lens correction 1: Adds back BLC bias after lens correction Bit[2]: Lens correction option 2 0: Lens correction applied on input data directly regardless of the black level 1: Subtract black level before applying lens correction

table 5-1 ISP general control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x501C	HORIZON SUBSAMPLE MODE	0x00	RW	Mode Selection for Horizontal Sub-sampling when **0x5002**[2] = 1 Bit[7:6]: B channel mode 00: Average mode x1: Not allowed 10: Skip mode Bit[5:4]: Gb channel mode 00: Average mode x1: Not allowed 10: Skip mode Bit[3:2]: Gr channel mode 00: Average mode x1: Not allowed 10: Skip mode Bit[1:0]: R channel mode 00: Average mode x1: Not allowed 10: Skip mode
0x501E	RGB DITHER CONTROL	0x40	RW	RGB Dither Control Bit[6]: Dither register control selection enable 0: From register control 1: From system control Bit[5:4]: R channel register control when 0x501E[6] = 0 00: Not allowed 01: RGB444 10: RGB565/555 11: Not allowed Bit[3:2]: G channel register control when 0x501E[6] = 0 00: Not allowed 01: RGB444 10: RGB565/555 11: Not allowed Bit[1:0]: B channel register control when 0x501E[6] = 0 00: Not allowed 01: RGB444 10: RGB565/555 11: Not allowed

5.2 even odd

The main function of even odd is to eliminate the different average values between even and odd columns, which may be caused by some electrical characteristics of the AD quantizer or other devices in the sensor.

table 5-2 even odd control registers

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0xDF	RW	Bit[4]: Even odd removing enable 0: Disable 1: Enable
0x5080	EVEN CTRL 00	0x40	RW	Bit[7:0]: Threshold Threshold for even odd cancelling.

5.3 lens correction (LENC)

The main purpose of the LENC is to compensate for lens imperfection. According to the area where each pixel is located, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature. The LENC correcting curve automatic calculation according sensor gain is also added so that the LENC can adapt with the sensor gain. Also, the LENC supports the subsample function in both horizontal and vertical directions. Contact your local OmniVision FAE for lens correction settings (registers 0x5800~0x5887).

note Registers **0x5888~0x588F** need to change only when DSP input is not generated internally. In other words, the DSP input is from an external sensor.

table 5-3 LENC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0xDF	RW	Bit[7]: LENC correction enable 0: Disable LENC 1: Enable LENC
0x5888	LENC BRV SCALE	0x01	RW	Bit[0]: LENC_BRV_SCALE[8] Reciprocal of vertical step for B/R channel. B/R channel in whole image is divided into 4x4 blocks. The step is used to point to the border of the adjacent block. BRVScale = ((4<<17) + (nHeight>>1)) / nHeight (nHeight = 1956)
0x5889	LENC BRV SCALE	0x0C	RW	Bit[7:0]: LENC_BRV_SCALE[7:0] Reciprocal of vertical step at B/R channel. B/R channel in whole image is divided into 4x4 blocks. The step is used to point to the border of the adjacent block. BRVScale = ((4<<17) + (nHeight>>1)) / nHeight
0x588A	LENC BRH SCALE	0x00	RW	Bit[0]: LENC_BRH_SCALE[8] Reciprocal of horizontal step for B/R channel. B/R channel in whole image is divided into 4x4 blocks. The step is used to point to the border of the adjacent block. BRHScale = ((4<<17) + (nWidth>>1)) / nWidth (nWidth = 2616)

table 5-3 LENC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x588B	LENC BRH SCALE	0xC8	RW	Bit[7:0]: LENC_BRH_SCALE[7:0] Reciprocal of horizontal step for B/R channel. B/R channel in whole image is divided into 4x4 blocks. The step is used to point to the border of the adjacent block. BRHScale = ((4<<17) + (nWidth>>1)) / nWidth
0x588C	LENC GV SCALE	0x00	RW	Bit[0]: LENC_GV_SCALE[8] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block. GVScale = ((4<<17) + (nHeight>>1)) / nHeight
0x588D	LENC GV SCALE	0xC9	RW	Bit[7:0]: LENC_GV_SCALE[7:0] Reciprocal of vertical step at G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block. GVScale = ((4<<17) + (nHeight>>1)) / nHeight
0x588E	LENC GH_SCALE	0x01	RW	Bit[0]: LENC_GH_SCALE[8] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block. GHScale = ((4<<17) + (nWidth>>1)) / nWidth
0x588F	LENC GH_SCALE	0x2D	RW	Bit[7:0]: LENC_GH_SCALE[7:0] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block. GHScale = ((4<<17) + (nWidth>>1)) / nWidth

5.4 VarioPixel (VAP)

The VarioPixel™ module can decrease the width of the original image by one-half. It supports three modes which selects the either the first, second, or average value of a pair of pixels to compose the new image.

table 5-4 VAP control registers

address	register name	default value	R/W	description
0x5002	ISP CONTROL 02	1'b0	RW	Bit[2]: VAP enable 0: Disable VAP 1: Enable VAP
0x501C	HORIZON SUBSAMPLE MODE	0x00	RW	Mode Selection for Horizontal Sub-sampling when **0x5002**[2] = 1 Bit[7:6]: B channel mode 00: Average mode x1: Not allowed 10: Skip mode Bit[5:4]: Gb channel mode 00: Average mode x1: Not allowed 10: Skip mode Bit[3:2]: Gr channel mode 00: Average mode x1: Not allowed 10: Skip mode Bit[1:0]: R channel mode 00: Average mode x1: Not allowed 10: Skip mode

5.5 auto white balance (AWB)

The main function of Auto White Balance (AWB) is the process of removing unrealistic color casts so that objects which appear white in person are rendered white in the image or video. Thus, the AWB makes sure that the white color is always a white color in different color temperatures. It supports manual white balance and auto white balance. For auto white balance, simple AWB and advanced AWB methods are supplied. Advance AWB takes into account the *color temperature* of a light source. For advanced AWB settings, contact your local OmniVision FAE.

table 5-5 AWB control registers

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	1'b1	RW	Bit[0]: AWB enable 0: Disable AWB algorithm and gain 1: Enable AWB
0x5183	AWB CONTROL 03	0x90	RW	Bit[7]: AWB mode 0: Advanced 1: Simple
0x5193	AWB CONTROL 19	0xF0	RW	Bit[7:0]: red_limit
0x5194	AWB CONTROL 20	0xF0	RW	Bit[7:0]: green_limit
0x5195	AWB CONTROL 21	0xF0	RW	Bit[7:0]: blue_limit
0x5196~ 0x5197	AWB CONTROL 22~23	–	RW	Advanced AWB Parameters Contact OmniVision FAE for settings.
0x3400	AWB R GAIN	0x04	RW	Bit[3:0]: AWB red gain[11:8] Red gain = AWB red gain[11:0] / 0x400
0x3401	AWB R GAIN	0x00	RW	Bit[7:0]: AWB red gain[7:0] Red gain = AWB red gain[11:0] / 0x400
0x3402	AWB G GAIN	0x04	RW	Bit[3:0]: AWB green gain[11:8] Green gain = AWB green gain[11:0] / 0x400
0x3403	AWB G GAIN	0x00	RW	Bit[7:0]: AWB green gain[7:0] Green gain = AWB green gain[11:0] / 0x400
0x3404	AWB B GAIN	0x04	RW	Bit[3:0]: AWB blue gain[11:8] Blue gain = AWB blue gain[11:0] / 0x400
0x3405	AWB B GAIN	0x00	RW	Bit[7:0]: AWB blue gain[7:0] Blue gain = AWB blue gain[11:0] / 0x400
0x3406	AWB MANUAL	0x00	RW	Bit[0]: AWB manual enable 0: Auto 1: Manual

5.6 raw gamma

The main purpose of the Gamma (GMA) function is to compensate for the non-linear characteristics of the sensor. GMA converts the pixel values according to the Gamma curve to compensate the sensor output under different light strengths. The non-linear gamma curve is approximately constructed with different linear functions. Raw gamma compensates the image in the RAW domain and shares the curve parameters with Y gamma. Raw gamma should be turned OFF when YUV gamma is ON. For YUV gamma, refer to **section 5.12**.

table 5-6 raw gamma control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	1'b0	RW	Bit[5]: Raw gamma enable 0: Disable GMA 1: Enable GMA
0x5480	GAMMA CONTROL 00	0x1A	RW	Gamma Control 00 Bit[7:0]: y_list_00 Position 0 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x5481	GAMMA CONTROL 01	0x28	RW	Gamma Control 01 Bit[7:0]: y_list_01 Position 1 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x5482	GAMMA CONTROL 02	0x3E	RW	Gamma Control 02 Bit[7:0]: y_list_02 Position 2 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x5483	GAMMA CONTROL 03	0x5E	RW	Gamma Control 03 Bit[7:0]: y_list_03 Position 3 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x5484	GAMMA CONTROL 04	0x6B	RW	Gamma Control 04 Bit[7:0]: y_list_04 Position 4 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1

table 5-6 raw gamma control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5485	GAMMA CONTROL 05	0x77	RW	Gamma Control 05 Bit[7:0]: y_list_05 Position 5 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x5486	GAMMA CONTROL 06	0x81	RW	Gamma Control 06 Bit[7:0]: y_list_06 Position 6 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x5487	GAMMA CONTROL 07	0x8B	RW	Gamma Control 07 Bit[7:0]: y_list_07 Position 7 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x5488	GAMMA CONTROL 08	0x94	RW	Gamma Control 08 Bit[7:0]: y_list_08 Position 8 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x5489	GAMMA CONTROL 09	0x9C	RW	Gamma Control 09 Bit[7:0]: y_list_09 Position 9 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x548A	GAMMA CONTROL 0A	0xAB	RW	Gamma Control 0A Bit[7:0]: y_list_10 Position 10 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x548B	GAMMA CONTROL 0B	0xB8	RW	Gamma Control 0B Bit[7:0]: y_list_11 Position 11 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1

table 5-6 raw gamma control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x548C	GAMMA CONTROL 0C	0xCE	RW	Gamma Control 0C Bit[7:0]: y_list_12 Position 12 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x548D	GAMMA CONTROL 0D	0xDF	RW	Gamma Control 0D Bit[7:0]: y_list_13 Position 13 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x548E	GAMMA CONTROL 0E	0xEC	RW	Gamma Control 0E Bit[7:0]: y_list_14 Position 14 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1
0x548F	GAMMA CONTROL 0F	0x0D	RW	Gamma Control 0F Bit[7:0]: y_list_15 Position 15 at raw gamma curve. Valid for raw gamma when register **ISP CONTROL 00**[5] (**0x5000**) = 1

5.7 defect pixel cancellation (DPC)

Due to processes and other reasons, pixel defects in the sensor array will occur. Thus, these bad or wounded pixels will generate wrong color values. The main purpose of Defect Pixel Cancellation (DPC) function is to remove the effect caused by these bad or wounded pixels. Also, some special functions are available for those pixels located at the image boundary. To remove the defect pixel effect correctly, the proper threshold should first be determined.

table 5-7 DPC control registers

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0xDF	RW	Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable
0x5780	DPC CTRL 00	0x77	RW	DPC Control 00 Bit[6]: Detail enable Bit[5:4]: Boundary selection Bit[2]: Smooth enable Bit[1]: Different channel enable Bit[0]: Single channel enable
0x5781	DPC THRESHOLD	0x30	RW	DPC Threshold Bit[7:0]: Threshold for DPC
0x5782	DPC CTRL 02	0x20	RW	DPC Control 02 Bit[6:0]: White threshold for DPC
0x5783	DPC B THRESHOLD	0x40	RW	DPC Black Threshold Bit[7:0]: Black threshold for DPC

5.8 de-noise (DNS)

Each pixel in a sensor converts the incoming light into an electrical signal which is processed into the color value of the pixel in the final image. If the same pixel is exposed several times by the same amount of light, the resulting color values would not be identical and thus, be called "noise". Even without incoming light, the electrical activity of the sensor itself will generate some signal. This additional signal is "noise". Noise in digital images is most visible in uniform surfaces. The main purpose of the DNS function is to decrease the noise.

Two thresholds, Y de-noise threshold and UV de-noise threshold, are used to suppress the Y noise and UV noise, respectively. These two thresholds are retrieved from Y list and UV list table based on the gain, respectively, and then further adjusted based on the Y of each pixel.

table 5-8 DNS control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0xDF	RW	Bit[3]: De-noise enable 0: Disable 1: Enable
0x5280	DNS CONTROL 10	0x04	RW	DNS Control 10 Bit[3:0]: noise y_a De-noise weight for Y
0x5281	DNS CONTROL 11	0x08	RW	DNS Control 11 Bit[4:0]: noise uv_a De-noise weight for UV
0x5282	DNS CONTROL 12	0x00	RW	DNS Control 12 Bit[0]: De-noise manual setting enable
0x5283	NOISE Y	0x02	RW	Noise Y De-noise level for Y when **0x5282**[0]=1
0x5284	NOISE U	0x00	RW	Noise U High Byte De-noise level for U when **0x5282**[0]=1
0x5285	NOISE U	0x02	RW	Noise U High Byte De-noise level for U when **0x5282**[0]=1
0x5286	NOISE V	0x00	RW	Noise V High Byte De-noise level for V when **0x5282**[0]=1
0x5287	NOISE V	0x02	RW	Noise V High Byte De-noise level for V when **0x5282**[0]=1
0x5288	DNS EDGETHRE	0x06	RW	DNS Edge Threshold Edge threshold for DNS when **0x5282**[0]=1
0x5289	DNS GBGR EXTRA	0x04	RW	DNS GbGr Extra GbGr extra level for DNS

table 5-8 DNS control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x528A	NOISE Y LIST 0	0x02	RW	Noise Y List 0 Noise Y curve position 0 for automatic noise Y computation according sensor gain
0x528B	NOISE Y LIST 1	0x04	RW	Noise Y List 1 Noise Y curve position 1 for automatic noise Y computation according sensor gain
0x528C	NOISE Y LIST 2	0x08	RW	Noise Y List 2 Noise Y curve position 2 for automatic noise Y computation according sensor gain
0x528D	NOISE Y LIST 3	0x14	RW	Noise Y List 3 Noise Y curve position 3 for automatic noise Y computation according sensor gain
0x528E	NOISE Y LIST 4	0x1E	RW	Noise Y List 4 Noise Y curve position 4 for automatic noise Y computation according sensor gain
0x528F	NOISE Y LIST 5	0x28	RW	Noise Y List 5 Noise Y curve position 5 for automatic noise Y computation according sensor gain
0x5290	NOISE Y LIST 6	0x32	RW	Noise Y List 6 Noise Y curve position 6 for automatic noise Y computation according sensor gain
0x5291	DNS DUMMY	0x00	RW	DNS Dummy
0x5292	NOISE UV LIST 0	0x00	RW	Noise UV List 0 Noise UV curve position 0 for automatic noise U / noise V computation according to sensor gain
0x5293	NOISE UV LIST 0	0x02	RW	Noise UV List 0 Noise UV curve position 0 for automatic noise U / noise V computation according to sensor gain
0x5294	NOISE UV LIST 1	0x00	RW	Noise UV List 1 Noise UV curve position 1 for automatic noise U / noise V computation according to sensor gain
0x5295	NOISE UV LIST 1	0x04	RW	Noise UV List 1 Noise UV curve position 1 for automatic noise U / noise V computation according to sensor gain
0x5296	NOISE UV LIST 2	0x00	RW	Noise UV List 2 Noise UV curve position 2 for automatic noise U / noise V computation according to sensor gain
0x5297	NOISE UV LIST 2	0x0C	RW	Noise UV List 2 Noise UV curve position 2 for automatic noise U / noise V computation according to sensor gain

table 5-8 DNS control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5298	NOISE UV LIST 3	0x00	RW	Noise UV List 3 Noise UV curve position 3 for automatic noise U / noise V computation according to sensor gain
0x5299	NOISE UV LIST 3	0x28	RW	Noise UV List 3 Noise UV curve position 3 for automatic noise U / noise V computation according to sensor gain
0x529A	NOISE UV LIST 4	0x00	RW	Noise UV List 4 Noise UV curve position 4 for automatic noise U / noise V computation according to sensor gain
0x529B	NOISE UV LIST 4	0x32	RW	Noise UV List 4 Noise UV curve position 4 for automatic noise U / noise V computation according to sensor gain
0x529C	NOISE UV LIST 5	0x00	RW	Noise UV List 5 Noise UV curve position 5 for automatic noise U / noise V computation according to sensor gain
0x529D	NOISE UV LIST 5	0x3C	RW	Noise UV List 5 Noise UV curve position 5 for automatic noise U / noise V computation according to sensor gain
0x529E	NOISE UV LIST 6	0x00	RW	Noise UV List 6 Noise UV curve position 6 for automatic noise U / noise V computation according to sensor gain
0x529F	NOISE UV LIST 6	0x4C	RW	Noise UV List 6 Noise UV curve position 6 for automatic noise U / noise V computation according to sensor gain
0x52A0	DNS NOISEY READ OUT	0x00	R	DNS NoiseY Read Out
0x52A1	DNS EDGETHRE READ OUT	0x00	R	DNS Edgethre Read Out
0x52A2	DNS NOISEU READ OUT	0x00	R	DNS NoiseU Read Out
0x52A3	DNS NOISEU READ OUT	0x00	R	DNS NoiseU Read Out
0x52A4	DNS NOISEV READ OUT	0x00	R	DNS NoiseV Read Out
0x52A5	DNS NOISEV READ OUT	0x00	R	DNS NoiseV Read Out
0x52A6	REAL GAIN	0x00	R	Real Gain Read Out
0x52A7	REAL GAIN	0x00	R	Real Gain Read Out

5.9 color interpolation (CIP)

The CIP functions include de-noising of raw images, RAW to RGB interpolation, and edge enhancement. In sensor RAW format, each pixel will be either R, G or B. CIP will calculate the other two color values using the neighboring pixel of the same color. Thus, we can get the full RGB information for each pixel. For edge enhancement, the OV5642 provides both manual and auto modes.

table 5-9 CIP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0xDF	RW	Bit[0]: CIP enable 0: Disable 1: Enable
0x5300	CIP MIN GAIN	0x00	RW	Bit[1:0]: cip_mingain[9:8] Minimum real gain for calculation of CIP parameters normalized by 0x10.
0x5301	CIP MIN GAIN	0x10	RW	Bit[7:0]: cip_mingain[7:0] Minimum real gain for calculation of CIP parameters normalized by 0x10.
0x5302	CIP MAX GAIN	0x00	RW	Bit[1:0]: cip_maxgain[9:8] Maximum real gain for calculation of CIP parameters normalized by 0x10.
0x5303	CIP MAX GAIN	0x80	RW	Bit[7:0]: cip_maxgain[7:0] Maximum real gain for calculation of CIP parameters normalized by 0x10.
0x5304	CIP MIN INTNOISE	0x00	RW	Bit[1:0]: cip_min_intnoise[8] CIP de-noise at CIP MIN GAIN. The larger the value, the blurrier the image.
0x5305	CIP MIN INTNOISE	0x30	RW	Bit[7:0]: cip_min_intnoise[7:0] CIP de-noise at CIP MIN GAIN. The larger the value, the blurrier the image.
0x5306	CIP MAX INTNOISE	0x01	RW	Bit[1:0]: cip_max_intnoise[8] CIP de-noise at CIP MAX GAIN. The larger the value, the blurrier the image.
0x5307	CIP MAX INTNOISE	0x20	RW	Bit[7:0]: cip_max_intnoise[7:0] CIP de-noise at CIP MAX GAIN. The larger the value, the blurrier the image.

table 5-9 CIP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5308	CIP SHARPEN MASK 0	0x10	RW	Bit[7:0]: cip punsharpen mask0[7:0] (sign + abs) Weight for position 0 and 4 in the 5-point filter when evaluating edge effect.
0x5309	CIP SHARPEN MASK 1	0x30	RW	Bit[7:0]: cip punsharpen mask1[7:0] (sign + abs) Weight for position 1 and 3 in the 5-point filter when evaluating edge effect.
0x530A	CIP CONTROL10	0x01	RW	CIP Control 10 Bit[3]: Sharpen manual enable Bit[0]: Anti-aliasing enable 0: Anti-aliasing mode disable 1: Anti-aliasing mode enable
0x531E	CIP MANUAL SHARPENP	0x0C	RW	Bit[5:0]: CIP sharpenp[5:0] manual setting when **0x530A**[3]=1
0x531F	CIP MANUAL SHARPENM	0x0C	RW	Bit[6:0]: CIP sharpenm[6:0] manual setting when **0x530A**[3]=1
0x5320	CIP MANUAL SHARPENTP	0x20	RW	Bit[7:0]: CIP sharpentp[7:0] manual setting when **0x530A**[3]=1
0x5321	CIP MANUAL SHARPENTM	0x20	RW	Bit[7:0]: CIP sharpentm[7:0] manual setting when **0x530A**[3]=1

5.10 color matrix (CMX)

The main purpose of the Color Matrix (CMX) function is to cancel out crosstalk and convert color space. Given the color correction matrix, CCM, and RGB to YUV conversion matrix, RGB2YUV, the combined matrix is:

$$CMX = \begin{bmatrix} cmx00 & cmx01 & cmx02 \\ cmx10 & cmx11 & cmx12 \\ cmx20 & cmx21 & cmx22 \end{bmatrix} = RGB2YUV \times CCM \times \begin{bmatrix} 1 & -0.25 & 0.75 \\ 1 & -0.25 & -0.25 \\ 1 & 0.75 & -0.25 \end{bmatrix}$$

where $\begin{bmatrix} R \\ G \\ B \end{bmatrix} = CCM \begin{bmatrix} R_0 \\ G_0 \\ B_0 \end{bmatrix}$

The CMX is then normalized by $2^{0x5394[3:0]}$.

table 5-10 CMX control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x4F	RW	Bit[1]: Color matrix enable 0: Disable 1: Enable
0x5380	CMX 00	0x01	RW	Bit[1:0]: cmx 00[9:8]
0x5381	CMX 00	0x00	RW	Bit[7:0]: cmx 00[7:0]
0x5382	CMX 01	0x00	RW	Bit[1:0]: cmx 01[9:8]
0x5383	CMX 01	0x17	RW	Bit[7:0]: cmx 01[7:0]
0x5384	CMX 02	0x00	RW	Bit[1:0]: cmx 02[9:8]
0x5385	CMX 02	0x01	RW	Bit[7:0]: cmx 02[7:0]
0x5386	CMX 10	0x00	RW	Bit[1:0]: cmx 10[9:8]
0x5387	CMX 10	0x00	RW	Bit[7:0]: cmx 10[7:0]
0x5388	CMX 11	0x01	RW	Bit[1:0]: cmx 11[9:8]
0x5389	CMX 11	0x35	RW	Bit[7:0]: cmx 11[7:0]
0x538A	CMX 12	0x00	RW	Bit[1:0]: cmx 12[9:8]
0x538B	CMX 12	0x3E	RW	Bit[7:0]: cmx 12[7:0]
0x538C	CMX 20	0x00	RW	Bit[1:0]: cmx 20[9:8]
0x538D	CMX 20	0x00	RW	Bit[7:0]: cmx 20[7:0]
0x538E	CMX 21	0x0A	RW	Bit[1:0]: cmx 21[9:8]
0x538F	CMX 21	0x00	RW	Bit[7:0]: cmx 21[7:0]
0x5390	CMX 22	0xCD	RW	Bit[1:0]: cmx 22[9:8]
0x5391	CMX 22	0x00	RW	Bit[7:0]: cmx 22[7:0]

table 5-10 CMX control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5392	CMX CMXSIGN	0x00	RW	CMX High Byte Bit[0]: cmx 22 sign
0x5393	CMX CMXSIGN	0x20	RW	CMX Low Byte Bit[7]: cmx 21 sign Bit[6]: cmx 20 sign Bit[5]: cmx 12 sign Bit[4]: cmx 11 sign Bit[3]: cmx 10 sign Bit[2]: cmx 02 sign Bit[1]: cmx 01 sign Bit[0]: cmx 00 sign
0x5394	CMX CONTROL 20	0x08	RW	CMX Control 20 Bit[3:0]: cmx shift

5.11 line stretch (contrast)

The auto contrast module is designed to linearly stretch the image to adjust the contrast according to the statistics results. According to the parameters we set, the function can automatically calculate the maximum and minimum levels. Then this range will be stretched to the entire data range.

table 5-11 line stretch (contrast) control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x4F	RW	Bit[3]: Line stretch enable 0: Disable 1: Enable
0x5402	STRETCH MIN HIGH LEVEL	0x3C	RW	Bit[6:0]: Minimum high level high byte[14:8] Minimum high level threshold.
0x5403	STRETCH MIN HIGH LEVEL	0x00	RW	Bit[7:0]: Minimum high level low byte[7:0] Minimum high level threshold
0x5404	STRETCH MAX LOW LEVEL	0x02	RW	Bit[6:0]: Maximum low level high byte[14:8] Maximum low level threshold.
0x5405	STRETCH MAX LOW LEVEL	0x00	RW	Bit[7:0]: Maximum low level low byte[7:0] Maximum low level threshold.
0x540E	STRETCH THRES1	0x00	RW	Bit[6:0]: Thres1[22:16] high 2 byte Threshold1 for stretch algorithm

table 5-11 line stretch (contrast) control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x540F	STRETCH THRES1	0x3A	RW	Bit[7:0]: Thres1[15:8] low 1 byte Threshold1 for stretch algorithm
0x5410	STRETCH THRES1	0x98	RW	Bit[7:0]: Thres1[7:0] low 2 byte Threshold1 for stretch algorithm
0x5412	STRETCH THRES2	0x00	RW	Bit[6:0]: Thres2[22:16] high 2 byte Threshold2 for stretch algorithm
0x5413	STRETCH THRES2	0x3A	RW	Bit[7:0]: Thres2[15:8] low 1 byte Threshold2 for stretch algorithm
0x5414	STRETCH THRES2	0x98	RW	Bit[7:0]: Thres2[7:0] low 2 byte Threshold2 for stretch algorithm
0x541D	STRETCH STEP	0x20	RW	Bit[7:0]: Step[7:0] Step for stretch control

5.12 YUV gamma

YUV gamma compensates image in YUV domain for the non-linear characteristics of human visual perception. For this special gamma function, UV gamma is separated from Y gamma. The UV gamma curve has a special relationship with Y gamma. Also, some special functions related to UV and high frequency luminance component (H) processing in dark conditions are available.

table 5-12 YUV gamma control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0xDF	RW	Bit[6]: YUV gamma enable 0: Disable 1: Enable
0x5480	GAMMA CONTROL00	0x1A	RW	Bit[7:0]: Y list 00
0x5481	GAMMA CONTROL01	0x28	RW	Bit[7:0]: Y list 01
0x5482	GAMMA CONTROL02	0x3E	RW	Bit[7:0]: Y list 02
0x5483	GAMMA CONTROL03	0x5E	RW	Bit[7:0]: Y list 03
0x5484	GAMMA CONTROL04	0x6B	RW	Bit[7:0]: Y list 04
0x5485	GAMMA CONTROL05	0x77	RW	Bit[7:0]: Y list 05
0x5486	GAMMA CONTROL06	0x81	RW	Bit[7:0]: Y list 06
0x5487	GAMMA CONTROL07	0x8B	RW	Bit[7:0]: Y list 07
0x5488	GAMMA CONTROL08	0x94	RW	Bit[7:0]: Y list 08

table 5-12 YUV gamma control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5489	GAMMA CONTROL09	0x9C	RW	Bit[7:0]: Y list 09
0x548A	GAMMA CONTROL0A	0xAB	RW	Bit[7:0]: Y list 0a
0x548B	GAMMA CONTROL0B	0xB8	RW	Bit[7:0]: Y list 0b
0x548C	GAMMA CONTROL0C	0xCE	RW	Bit[7:0]: Y list 0c
0x548D	GAMMA CONTROL0D	0xDF	RW	Bit[7:0]: Y list 0d
0x548E	GAMMA CONTROL0E	0xEC	RW	Bit[7:0]: Y list 0e
0x548F	GAMMA CONTROL0F	00xD	RW	Bit[7:0]: Y list 0f
0x5490	GAMMA GAIN LIST 00	0x07	RW	Bit[3:0]: Gain list 00 high byte
0x5491	GAMMA GAIN LIST 00	0x81	RW	Bit[7:0]: Gain list 00 low byte
0x5492	GAMMA GAIN LIST 01	0x05	RW	Bit[3:0]: Gain list 01 high byte
0x5493	GAMMA GAIN LIST 01	0xF5	RW	Bit[7:0]: Gain list 01 low byte
0x5494	GAMMA GAIN LIST 02	0x04	RW	Bit[3:0]: Gain list 02 high byte
0x5495	GAMMA GAIN LIST 02	0xC8	RW	Bit[7:0]: Gain list 02 low byte
0x5496	GAMMA GAIN LIST 03	0x03	RW	Bit[3:0]: Gain list 03 high byte
0x5497	GAMMA GAIN LIST 03	0x96	RW	Bit[7:0]: Gain list 03 low byte
0x5498	GAMMA GAIN LIST 04	0x03	RW	Bit[3:0]: Gain list 04 high byte
0x5499	GAMMA GAIN LIST 04	0x3B	RW	Bit[7:0]: Gain list 04 low byte
0x549A	GAMMA GAIN LIST 05	0x02	RW	Bit[3:0]: Gain list 05 high byte
0x549B	GAMMA GAIN LIST 05	0xF5	RW	Bit[7:0]: Gain list 05 low byte
0x549C	GAMMA GAIN LIST 06	0x02	RW	Bit[3:0]: Gain list 06 high byte
0x549D	GAMMA GAIN LIST 06	0xB9	RW	Bit[7:0]: Gain list 06 low byte
0x549E	GAMMA GAIN LIST 07	0x02	RW	Bit[3:0]: Gain list 07 high byte
0x549F	GAMMA GAIN LIST 07	0x84	RW	Bit[7:0]: Gain list 07 low byte
0x54A0	GAMMA GAIN LIST 08	0x02	RW	Bit[3:0]: Gain list 08 high byte
0x54A1	GAMMA GAIN LIST 08	0x59	RW	Bit[7:0]: Gain list 08 low byte
0x54A2	GAMMA GAIN LIST 09	0x02	RW	Bit[3:0]: Gain list 09 high byte
0x54A3	GAMMA GAIN LIST 09	0x31	RW	Bit[7:0]: Gain list 09 low byte
0x54A4	GAMMA GAIN LIST 10	0x01	RW	Bit[3:0]: Gain list 10 high byte
0x54A5	GAMMA GAIN LIST 10	0xED	RW	Bit[7:0]: Gain list 10 low byte
0x54A6	GAMMA GAIN LIST 11	0x01	RW	Bit[3:0]: Gain list 11 high byte

table 5-12 YUV gamma control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x54A7	GAMMA GAIN LIST 11	0xB3	RW	Bit[7:0]: Gain list 11 low byte
0x54A8	GAMMA GAIN LIST 12	0x01	RW	Bit[3:0]: Gain list 12 high byte
0x54A9	GAMMA GAIN LIST 12	0x59	RW	Bit[7:0]: Gain list 12 low byte
0x54AA	GAMMA GAIN LIST 13	0x01	RW	Bit[3:0]: Gain list 13 high byte
0x54AB	GAMMA GAIN LIST 13	0x11	RW	Bit[7:0]: Gain list 13 low byte
0x54AC	GAMMA GAIN LIST 14	0x00	RW	Bit[3:0]: Gain list 14 high byte
0x54AD	GAMMA GAIN LIST 14	0xD4	RW	Bit[7:0]: Gain list 14 low byte
0x54AE	GAMMA GAIN LIST 15	0x00	RW	Bit[3:0]: Gain list 15 high byte
0x54AF	GAMMA GAIN LIST 15	0x1D	RW	Bit[7:0]: Gain list 15 low byte
0x54B0	GAMMA CONTROL 30	0x01	RW	Gamma Control 30 Bit[0]: UV dark enable 0: Do not apply 1: Apply UV process in dark area controlled by UV dark threshold
0x54B1	GAMMA CONTROL 31	0x20	RW	Gamma Control 31 Bit[7:0]: UV dark threshold Threshold for UV process in dark area
0x54B2	GAMMA CONTROL 32	0x01	RW	Gamma Control 32 Bit[0]: H dark enable 0: Do not apply 1: Apply H process in dark area controlled by UV dark threshold
0x54B3	GAMMA CONTROL 33	0x40	RW	Gamma Control 33 Bit[7:0]: H dark threshold Threshold for H process in dark area

5.13 UV average

The main function of the UV average is to average the U/V channel value using special filters.

table 5-13 UV average register

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x4F	RW	Bit[2]: UV average enable 0: Disable 1: Enable

5.14 UV adjust

The main function of the UV adjust is to adjust the U/V channel value according to sensor gain. It supports both manual and auto modes.

table 5-14 UV adjust control registers

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x4F	RW	Bit[6]: UV adjust enable 0: Disable 1: Enable
0x5500	UV UVADJUST CONTROL 0	0x00	RW	UV Adjust Control 0 Bit[4:0]: Adjust offset UV adjust in value minimum threshold
0x5501	UV UVADJUST CONTROL 3	0x1F	RW	UV Adjust Control 3 Bit[5]: UV adjust manual enable 0: Auto mode 1: Manual mode Bit[4:0]: UV adjust in manual UV adjust manual setting when 0x5501[5]=1
0x5502	UV ADJ TH1	0x00	RW	Bit[0]: UV adj th1[8] Real gain threshold for UV adjust in which will be limited to 31 if real gain is smaller than UV adj th1.
0x5503	UV ADJ TH1	0x00	RW	Bit[7:0]: UV adj th1 Real gain threshold for UV adjust in which will be limited to 31 if real gain is smaller than UV adj th1.
0x5504	UV ADJ TH2	0x01	RW	Bit[0]: UV adj th2[8] Real gain threshold for UV adjust in which will be limited to UV offset (UV **UV UVADJUST CONTROL 0**[4:0] (**0x5500**)) if real gain is larger than UV adj th1.
0x5505	UV ADJ TH2	0xFF	RW	Bit[7:0]: UV adj th2 Real gain threshold for UV adjust in which will be limited to UV offset (UV **UV UVADJUST CONTROL 0**[4:0] (**0x5500**)) if real gain is larger than UV adj th1.
0x5506	UV ADJUST IN AUTO	–	R	Bit[4:0]: UV adjust in readout

5.14.1 manual mode

By setting **UV UVADJUST CONTROL 3**[5] (**0x5501**) to 1, UV adust is controlled only by register **UV UVADJUST CONTROL 3**[4:0] (**0x5501**) for all gains.

5.14.2 auto mode

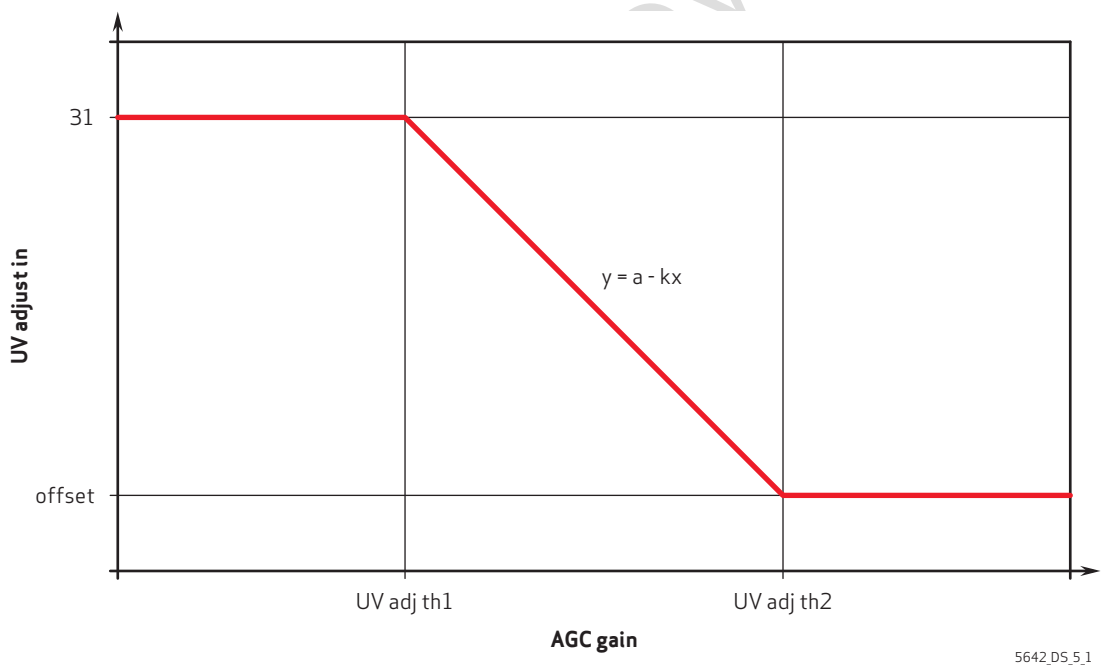
When the UV adjust is set for auto mode, the UV adjust curve parameters (see **figure 5-1**) should be entered into the corresponding registers. The UV adjust parameters, UV adj th1, UV adj th2, and offset should be entered into the registers to set the curve. To get these values, first set the values of UV adj th1, UV adj th2, and offset. Then, calculate the values of a and k as follows:

k = (31 – offset) / (UV adj th2 – UV adj th1)
a = 31 + k × UV adj th1

Registers to be changed:

- UV adj th1[8:0] = registers {**0x5502**[0], **0x5503**[7:0]}
- UV adj th2[8:0] = registers {**0x5504**[0], **0x5505**[7:0]}
- offset = register **0x5500**[4:0]

figure 5-1 UV adjust graph



5.15 special digital effects (SDE)

The Special Digital Effects (SDE) functions include hue/saturation control, brightness, contrast, etc. SDE also supports negative, black/white, sepia, greenish, blueish, redish, solarize and other image effects.

table 5-15 SDE control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x4F	RW	Bit[7]: SDE enable 0: Disable 1: Enable
0x5580	SDE CONTROL 0	0x00	RW	Bit[7]: Fixed Y enable - works with register **0x5587**[7:0] 0: Fixed Y disable 1: Fixed Y enable Bit[6]: Negative Y enable 0: Negative Y disable 1: Negative Y enable Bit[5]: Gray image enable 0: Gray image disable 1: Gray image enable Bit[4]: Fixed V enable - works with register **0x5586**[7:0] 0: Fixed V disable 1: Fixed V enable Bit[3]: Fixed U enable - works with register **0x5585**[7:0] 0: Fixed U disable 1: Fixed U enable Bit[2]: Contrast enable - works with registers **0x5587**[7:0], **0x5588**[7:0], and **0x5589**[7:0] 0: Contrast disable 1: Contrast enable Bit[1]: Saturation enable - works with registers **0x5583**[7:0] and **0x5584**[7:0] 0: Saturation disable 1: Saturation enable Bit[0]: Hue enable 0: Hue disable 1: Hue enable
0x5581	SDE CONTROL1	0x80	RW	Bit[7:0]: Hue cos Controlled by: hue_angle_en (**0x558A**[6]) hue_angle_en=1'b0: hue cos[7:0] hue_angle_en=1'b1: angle[7:0]

table 5-15 SDE control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5582	SDE CONTROL2	0x00	RW	Bit[7:0]: Hue sin Controlled by: hue_angle_en (**0x558A**[6]) hue_angle_en=1'b0: hue sin[7:0] hue_angle_en=1'b1: angle[8]
0x5583	SDE CONTROL3	0x40	RW	Bit[7:0]: Saturation U
0x5584	SDE CONTROL4	0x40	RW	Bit[7:0]: Saturation V
0x5585	SDE CONTROL5	0x80	RW	Bit[7:0]: Ureg for fixed U
0x5586	SDE CONTROL6	0x80	RW	Bit[7:0]: Vreg for fixed V
0x5587	SDE CONTROL7	0x00	RW	Bit[7:0]: Yoffset for contrast or Y value for fixed Y
0x5588	SDE CONTROL8	0x20	RW	Bit[7:0]: Ygain for contrast
0x5589	SDE CONTROL9	0x00	RW	Bit[7:0]: Ybright for contrast
0x558A	SDE CONTROL 10	0x01	RW	Bit[7]: Solarize enable Bit[6]: Hue angle enable Bit[5]: COS sign for Cr Bit[4]: COS sign for Cb Bit[3]: Offset sign for contrast Bit[2]: Bright sign for contrast Bit[1]: SIN sign for Cb Bit[0]: SIN sign for Cr

5.16 scaling

The main purpose of the scaling function is to zoom out the image. According to the new width and new height of the new image, the module uses the values of several pixels to generate the values of one pixel. The values of some pixels are divided and used in two or more adjacent pixels. The scaling function supports up to 16x scale.

table 5-16 scaling control registers

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x4F	RW	Bit[5]: Vertical scaling enable 0: Disable 1: Enable Bit[4]: Horizontal scaling enable 0: Disable 1: Enable
0x3804	TIMING HW	0x08	RW	Bit[3:0]: HREF horizontal width high byte[11:8] (scale input)
0x3805	TIMING HW	0x00	RW	Bit[7:0]: HREF horizontal width high byte[7:0] (scale input)
0x3806	TIMING VH	0x06	RW	Bit[3:0]: HREF vertical height high byte[11:8] (scale input)
0x3807	TIMING VH	0x00	RW	Bit[7:0]: HREF vertical height high byte[7:0] (scale input)
0x3808	TIMING DVPHO	0x08	RW	Bit[3:0]: DVP output horizontal width high byte[11:8]
0x3809	TIMING DVPHO	0x00	RW	Bit[7:0]: DVP output horizontal width high byte[7:0]
0x380A	TIMING DVPVO	0x06	RW	Bit[3:0]: DVP output vertical height high byte[11:8]
0x380B	TIMING DVPVO	0x00	RW	Bit[7:0]: DVP output vertical height high byte[7:0]

5.17 thumbnail control

The thumbnail image data can be added to the compression data stream.

table 5-17 DCW control registers

address	register name	default value	R/W	description
0x5002	ISP CONTROL 02	0xE0	RW	Bit[7]: Thumbnail enable 0: Disable 1: Enable
0x5700	THUMBNAIL CONTROL 00	0x10	RW	Bit[4]: Auto mode Scale auto mode versus manual mode select 0: Auto mode 1: Manual mode Bit[3]: hrounding / dcw_hrounding 0: No horizontal rounding 1: Horizontal rounding Bit[2]: hdrop / dcw_drop_mode 0: Horizontal average mode 1: Horizontal drop mode Bit[1]: vrounding / dcw_vrounding 0: No vertical rounding 1: Vertical rounding Bit[0]: vdrop / dcw_drop_mode 0: Vertical average mode 1: Vertical drop mode
0x3811	THUMBNAIL VH	0xF0	RW	Thumbnail Vertical Size
0x3812	THUMBNAIL HW HIGH	0x01	RW	Bit[0]: Thumbnail horizontal size[8]
0x3813	THUMBNAIL HW LOW	0x40	RW	Bit[7:0]: Thumbnail horizontal size[7:0]
0x3818	THUMBNAIL ENABLE	0x0	RW	Bit[4]: Thumbnail enable 0: Disable 1: Enable

5.18 ISP format

table 5-18 ISP format control registers

address	register name	default value	R/W	description
0x501F	FORMAT MUX CONTROL	0x04	RW	Format Mux Control Bit[5]: Swap Y and UV of external camera Bit[2:0]: ISP output format selection 000: ISP YUV 001: ISP RGB 010: ISP YUV 011: ISP RAW 100: Internal CIF RAW 101: External CIF RAW 110: External CIF YUV422 bypass enable

5.19 draw window

The draw window module is used to display a window on top of live video. It is usually used by autofocus to display a focus window.

table 5-19 draw window registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x501F	FORMAT MUX CONTROL	0x04	RW	Format Mux Control Bit[5]: Swap Y and UV of external camera Bit[2:0]: ISP output format selection 000: ISP YUV 001: ISP RGB 010: ISP YUV 011: ISP RAW 100: Internal CIF RAW 101: External CIF RAW 110: External CIF YUV422 bypass enable
0x5027	DRAW WINDOW CONTROL00	0x02	RW	Bit[0]: Draw window control 0: No fixed value 1: Fixed Y
0x5028	DRAW WINDOW LEFT POSITION CONTROL	0x03	RW	Bit[3:0]: Draw window left[11:8] high byte
0x5029	DRAW WINDOW LEFT POSITION CONTROL	0x6C	RW	Bit[7:0]: Draw window left[7:0] low byte

table 5-19 draw window registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x502A	DRAW WINDOW RIGHT POSITION CONTROL	0x04	RW	Bit[3:0]: Draw window right[11:8] high byte
0x502B	DRAW WINDOW RIGHT POSITION CONTROL	0xAC	RW	Bit[7:0]: Draw window right[7:0] low byte
0x502C	DRAW WINDOW TOP POSITION CONTROL	0x02	RW	Bit[2:0]: Draw window top[10:8] high byte
0x502D	DRAW WINDOW TOP POSITION CONTROL	0x91	RW	Bit[7:0]: Draw window top[7:0] low byte
0x502E	DRAW WINDOW BOTTOM POSITION CONTROL	0x03	RW	Bit[2:0]: Draw window bottom[10:8] high byte
0x502F	DRAW WINDOW BOTTOM POSITION CONTROL	0x81	RW	Bit[7:0]: Draw window bottom[7:0] low byte
0x5030	DRAW WINDOW HORIZONTAL BOUNDARY WIDTH CONTROL	0x00	RW	Bit[3:0]: Draw window horizontal boundary width[11:8] high byte
0x5031	DRAW WINDOW HORIZONTAL BOUNDARY WIDTH CONTROL	0x14	RW	Bit[7:0]: Draw window horizontal boundary width[7:0] low byte
0x5032	DRAW WINDOW VERTICAL BOUNDARY WIDTH CONTROL	0x00	RW	Bit[2:0]: Draw window vertical boundary width[10:8] high byte
0x5033	DRAW WINDOW VERTICAL BOUNDARY WIDTH CONTROL	0x14	RW	Bit[7:0]: Draw window vertical boundary width[7:0] low byte
0x5034	DRAW WINDOW Y CONTROL	0x80	RW	Bit[7:0]: Fixed Y for draw window
0x5035	DRAW WINDOW U CONTROL	0x2A	RW	Bit[7:0]: Fixed U for draw window
0x5036	DRAW WINDOW V CONTROL	0x14	RW	Bit[7:0]: Fixed V for draw window

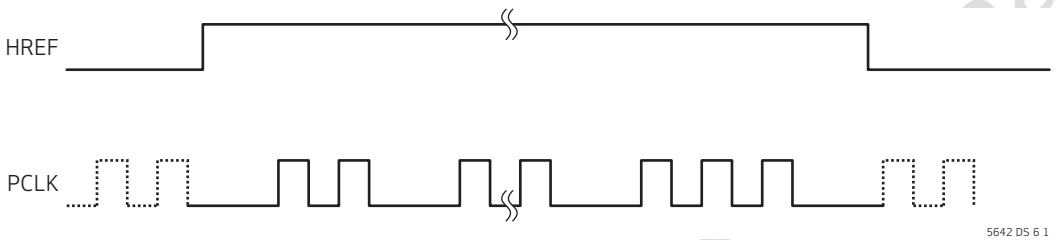
6 image sensor output interface digital functions

6.1 compression engine

6.1.1 compression mode 1 timing

The whole frame has only one line. PCLK will be gated when there is no valid image data transmitted.

figure 6-1 compression mode 1 timing



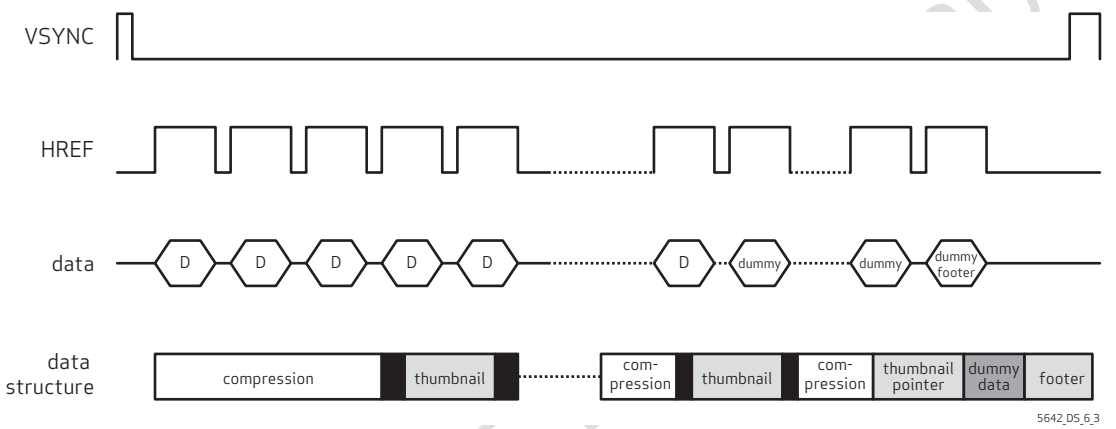
6.1.2 compression mode 2 timing

Compression data is transmitted with programmable line width. PCLK is free running. The last line may contain dummy data to match the width. By default, the line number varies from frame to frame. The user can set register **VFIFO CTRL 00**[5] (0x4600) to ensure every frame has a fixed line number (programmable).

figure 6-2 compression mode 2 timing

In this mode, compression data can be output with thumbnail data. Refer to **figure 6-3** for timing.

figure 6-3 compression mode 2 (with thumbnail data) timing



Frame data starts from video data with a compression header (SOI flag) at the beginning. Video data includes regular compression data (header, compressed bit stream data) and thumbnail data (in packet format - see below). Video data ends with a compression EOI flag (FF D9), followed by thumbnail packet position pointer, and dummy data if the pre-defined image size
(M x N) is bigger than the actual video data plus thumbnail pointer data. The last 6 bytes are the image footer which contains information including the presence of thumbnail (or not), compression status, and the total video data size (size from SOI to EOI).

Video data has two types of data:

- compressed data
- thumbnail data

The thumbnail data is embedded in the compressed data in packet format. The packet format is as below:

The Smaker (start marker) is composed of the first two bytes and third and fourth bytes are the packet Length, which is the size of length (2 bytes) plus the thumbnail one line data size. For instance, if the thumbnail size is I x J, then the one line data size will be I x 2 for the YUV format and the total thumbnail packet number is J. The Emaker (end marker) make up the last two bytes. Both Smaker and Emaker can be controlled by registers.

The thumbnail packet pointer is three bytes in size with MSB first. The packet pointer points to the first byte of the respective thumbnail packet (the first byte of Smaker). For instance, the ThmPt1 points to the first byte of the first thumbnail packet and ThmPt2 points to the first byte of the second thumbnail packet.

The last six bytes of the frame data are the image footer. The definition of the footer is as follows (see **figure 6-4**):

figure 6-4 image footer

thumbnail	compression status		length of video data		
byte 5	byte 4	byte 3	byte 2	byte 1	byte 0

5642_DS_6_4

byte5[7:4]: reserved

byte5[3:2]: thumbnail format 00: YUV 10: RGB565

byte5[1]: thumbnail overflows (thumbnail size too big)

byte5[0]: thumbnail present or not.

byte4[7:4]: reserved

byte4[2]: anti-shake status

byte4[1]: compression oversize

byte4[0]: compression overflow

byte3: reserved

byte2: video data size MSB

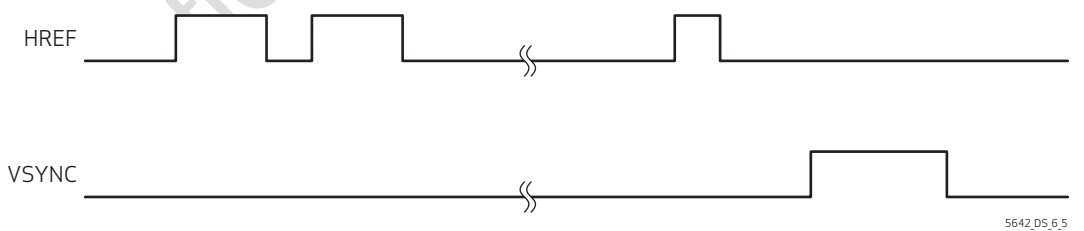
byte1: video data size

byte0: video data size LSB

6.1.3 compression mode 3 timing

Compression data is transmitted with programmable width. The last line width maybe different from the other line (there is no dummy data). In each frame, the line number may be different.

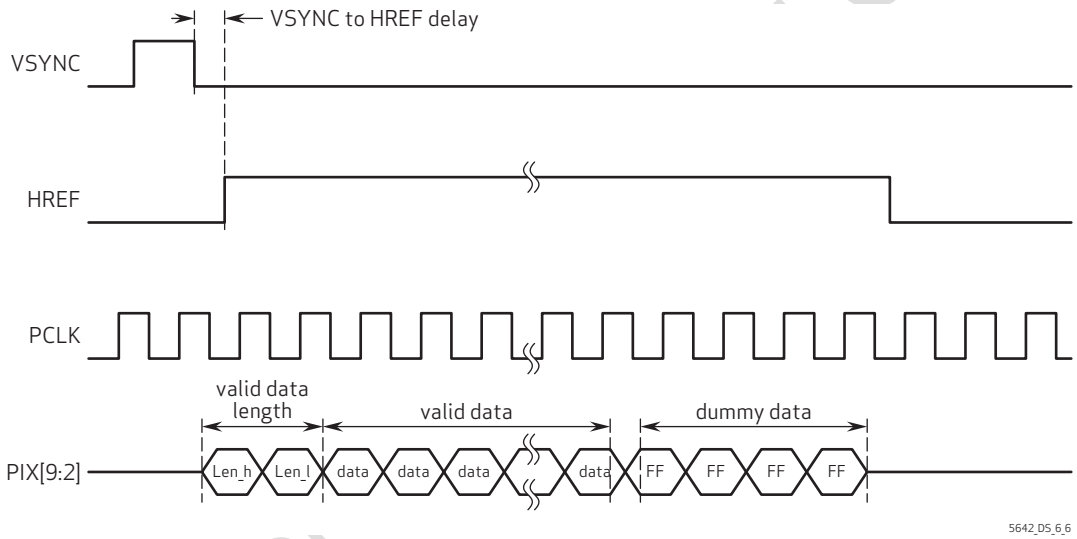
figure 6-5 compression mode 3 timing



6.1.4 compression mode 4 timing

The width and height are fixed in each frame. The first two bytes are valid data length in every line, followed by valid image data. Dummy data (0xFF) may be used as padding at each line end if the current valid image data is less than the line width.

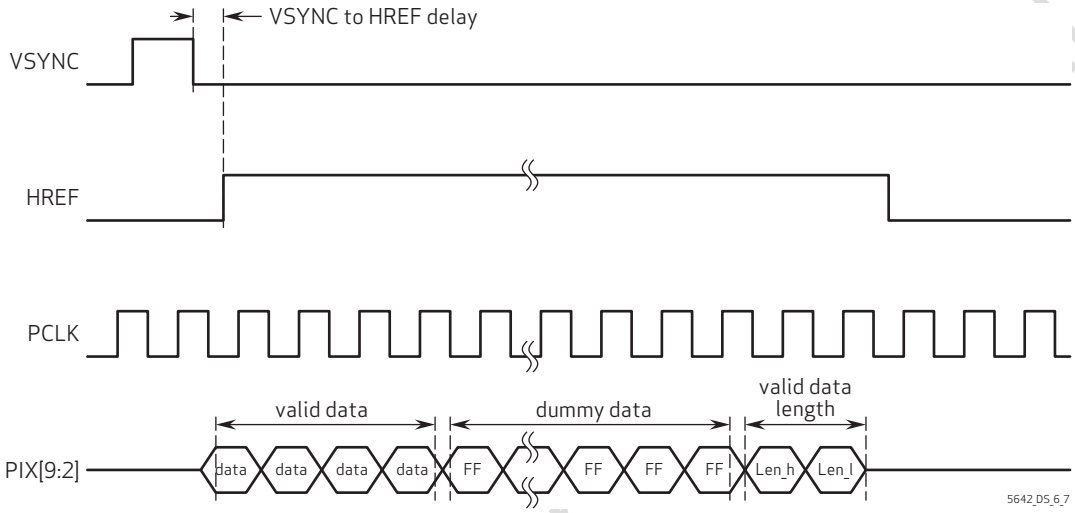
figure 6-6 compression mode 4 timing



6.1.5 compression mode 5 timing

The width and height are fixed in each frame. Every line begins with valid image data. Dummy data may be used as padding at each line end if the current valid image data is less than the line width. The last two bytes of every line is valid data length.

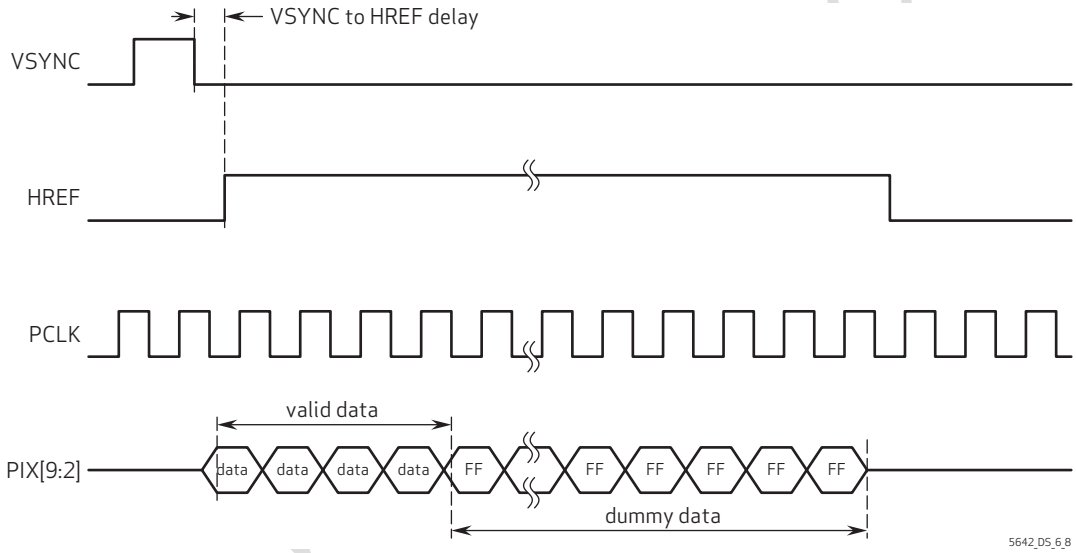
figure 6-7 compression mode 5 timing



6.1.6 compression mode 6 timing

The width and height are fixed in each frame. Every line begins with valid image data. Dummy data may be used as padding at each line end if the current valid image data less than the line width.

figure 6-8 compression mode 6 timing



6.1.7 compression mode control

table 6-1 compression control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3818	COMPRESSION ENABLE	0x80	RW	Bit[4]: Thumbnail enable Thumbnail data enable 0: Thumbnail mode disabled 1: Thumbnail mode enabled Bit[3]: Compression enable 0: Compression disabled 1: Compression enabled
0x4600	VFIFO CTRL 00	0x80	RW	Bit[5]: Compression output fixed height enable 0: In compression mode2, compression height is different in each frame 1: In compression mode2, compression height is fixed in each frame
0x4602	VFIFO HSIZE	0x04	RW	Bit[7:0]: Compression output width high byte
0x4603	VFIFO HSIZE	0x00	RW	Bit[7:0]: Compression output width low byte
0x4604	VFIFO VSIZE	0x03	RW	Bit[7:0]: Compression output height high byte
0x4605	VFIFO VSIZE	0x00	RW	Bit[7:0]: Compression output height low byte
0x4606	VFIFO CTRL 06	0x02	RW	Bit[4]: Compression oversize mask disable 0: When oversize occurs, the rest of the data will be masked 1: Disable oversize mask
0x460C	VFIFO CTRL 0C	0x20	RW	Bit[7:4]: Compression dummy data pad speed Bit[2]: Footer disable Compression footer disable 0: In compression mode2, footer will be added in the last six bytes of each frame 1: Disable footer
0x460D	VFIFO CTRL 0D	0x00	RW	Bit[7:0]: Compression pad dummy data

table 6-1 compression control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4713	COMPRESSION MODE SELECT	0x02	RW	Bit[2:0]: Compression mode select 001: Compression mode1 010: Compression mode2 011: Compression mode3 100: Compression mode4 101: Compression mode5 110: Compression mode6
0x471F	COMPRESSION BLK MIN	0x40	RW	Bit[7:0]: Compression mode2, 3 minimum blanking time between HREF
0x4723	COMPRESSION456 SKIP NUM	0x00	RW	Bit[7:0]: Compression mode4,5,6 line skip number
0x4400	COMPRESSION CTRL 00	0x81	RW	Bit[7]: input_format 0: YUV420 1: YUV422 Bit[6:0]: JFIFO read speed control
0x4401	COMPRESSION CTRL 01	0x01	RW	Bit[7:4]: SFIFO output buffer speed control Bit[1:0]: SFIFO read speed control
0x4404	COMPRESSION CTRL 04	0x24	RW	Bit[7]: jfifo_pwrdn Bit[6]: sfifo_pwrdn Bit[5]: Header output enable Bit[4]: Enable gated clock 0: Disable gated clock 1: Enable gated clock
0x4417	JFIFO OVERFLOW	–	R	Bit[0]: JFIFO overflow indicator

6.2 system control

System control registers include clock, reset control, and PLL configure. Individual modules can be reset or clock gated by setting the appropriate registers.

table 6-2 system control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3000	SYSTEM RESET00	0x20	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[6]: Reset MCU program memory Bit[5]: Reset MCU Bit[4]: Reset OTP memory Bit[3]: Reset STB Bit[1]: Reset timing control Bit[0]: Reset array control
0x3001	SYSTEM RESET01	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset AWB registers Bit[6]: Reset AFC Bit[5]: Reset ISP Bit[4]: Reset FC Bit[3]: Reset CIF Bit[2]: Reset BLC Bit[1]: Reset AEC registers Bit[0]: Reset AEC
0x3002	SYSTEM RESET02	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset VFIFO Bit[6]: Reset IFIFO Bit[5]: Reset format Bit[4]: Reset JFIFO Bit[3]: Reset SFIFO Bit[2]: Reset compression Bit[1]: Reset format mux Bit[0]: Reset average
0x3003	SYSTEM RESET03	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[2]: Reset ISP FC Bit[1]: Reset MIPI Bit[0]: Reset DVP

table 6-2 system control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3004	CLOCK ENABLE00	0xDF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[6]: Enable MCU program memory clock Bit[5]: Enable MCU clock Bit[4]: Enable OTP memory clock Bit[3]: Enable strobe clock Bit[1]: Enable timing control clock Bit[0]: Enable array control clock
0x3005	CLOCK ENABLE01	0xFF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable AWB register clock Bit[6]: Enable AFC clock Bit[5]: Enable ISP clock Bit[4]: Enable FC clock Bit[3]: Enable CIF clock Bit[2]: Enable BLC clock Bit[1]: Enable AEC register clock Bit[0]: Enable AEC clock
0x3006	CLOCK ENABLE02	0xFF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable IFIFO clock Bit[6]: Enable format clock Bit[5]: Enable JFIFO 2x clock Bit[4]: Enable JFIFO clock Bit[3]: Enable SFIFO clock Bit[2]: Enable compression 2x clock Bit[1]: Enable format mux clock Bit[0]: Enable average clock
0x3007	CLOCK ENABLE03	0x3F	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[4]: Enable MIPI PCLK clock Bit[3]: Enable MIPI clock Bit[2]: Enable DVP clock Bit[1]: Enable VFIFO PCLK clock Bit[0]: Enable VFIFO SCLK clock
0x3008	SYSTEM CONTROL00	0x02	RW	System Control Registers Bit[7]: System software reset 0: Normal work mode 1: Software reset mode Bit[6]: System sleep mode 0: Normal work mode 1: Software power down mode

table 6-2 system control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3009	PLL PRE DIVIDER STEP	0x00	RW	PLL Pre-divider Step Bit[7]: PLL pre-divider step 0: Bypass pre-divider step Bit[6:0]: Pre-divider step PLL input clock = pad clock × (step/mod)
0x300A	PLL PRE DIVIDER MOD	0x00	RW	PLL Pre-divider Mod Bit[7]: PLL pre-divider mod 0: Bypass pre-divider mod Bit[6:0]: Pre-divider mod PLL input clock = pad clock × (step/mod)

6.3 microcontroller unit (MCU)

The MCU firmware can be downloaded by writing to registers starting from 0x8000. A total of 6 KB of program memory can be used for program storage. Before downloading the firmware, the user must enable the MCU clock by setting register **0x3004**[5] to 1'b1. After downloading the firmware, set register **0x3000**[5] to 1'b0 to enable the MCU. The MCU interrupts are triggered by several internal signals for firmware development.

table 6-3 MCU control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3F00	MC CTRL 00	0x00	RW	Bit[0]: MCU soft reset 1: Reset MCU
0x3F01	MC INTERRUPT MASK0	0x00	RW	Mask0 for Interrupt Bit[5]: ISP EOF 0: Disable interrupt bit 1: Enable interrupt bit Bit[4]: ISP SOF 0: Disable interrupt bit 1: Enable interrupt bit Bit[2]: AWB done 0: Disable interrupt bit 1: Enable interrupt bit Bit[1]: VFIFO full 0: Disable interrupt bit 1: Enable interrupt bit Bit[0]: VFIFO empty 0: Disable interrupt bit 1: Enable interrupt bit
0x3F02	MC INTERRUPT MASK1	0x00	RW	Mask1 for Interrupt Bit[7]: AEC done 0: Disable interrupt bit 1: Enable interrupt bit Bit[6]: Average done 0: Disable interrupt bit 1: Enable interrupt bit Bit[5]: AEC trigger 0: Disable interrupt bit 1: Enable interrupt bit Bit[3]: MIPI turn around 0: Disable interrupt bit 1: Enable interrupt bit Bit[2]: MIPI low power contention detect 0: Disable interrupt bit 1: Enable interrupt bit Bit[0]: BLC SOF 0: Disable interrupt bit 1: Enable interrupt bit

table 6-3 MCU control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3F03	MC READ INTERRUPT ADDRESS	0x70	RW	Bit[7:0]: Set high byte for SCCB address that will trigger interrupt when read
0x3F04	MC READ INTERRUPT ADDRESS	0x00	RW	Bit[7:0]: Set low byte for SCCB address that will trigger interrupt when read
0x3F05	MC WRITE INTERRUPT ADDRESS	0x70	RW	Bit[7:0]: Set high byte for SCCB address that will trigger interrupt when written
0x3F06	MC WRITE INTERRUPT ADDRESS	0x04	RW	Bit[7:0]: Set low byte for SCCB address that will trigger interrupt when written
0x3F0C	MC INTERRUPT0 STATUS	–	R	Interrupt0 Status Indicator Bit[5]: ISP EOF Bit[4]: ISP SOF Bit[2]: AWB done Bit[1]: VFIFO full Bit[0]: VFIFO empty
0x3F0D	MC INTERRUPT1 STATUS	–	R	Interrupt1 Status Indicator Bit[7]: AEC done Bit[6]: Average done Bit[5]: AEC trigger Bit[3]: MIPI turn around Bit[2]: MIPI low power contention detect Bit[0]: BLC SOF

6.4 camera interface (CIF)

The camera interface (CIF) is used to receive external sensor image data through the DVP.

table 6-4 CIF control registers

address	register name	default value	R/W	description
0x4100	CIF CTRL 00	0x00	RW	Reverse External Sensor Input Polarity Bit[7]: Source select 0: From external DVP input 1: From MIPI RX Bit[5]: Reverse VSYNC polarity Bit[4]: Reverse HREF polarity Bit[3]: Reverse PCLK polarity

6.5 frame control (FC)

Frame control (FC) is used to mask some specified frame by setting the appropriate registers.

table 6-5 FC control registers

address	register name	default value	R/W	description
0x4201	FRAME CONTROL 00	0x00	RW	Control Passed Frame Number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode Bit[3:0]: Frame ON number
0x4202	FRAME CONTROL 01	0x00	RW	Control Masked Frame Number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode Bit[3:0]: Frame OFF number

6.6 format description

Format control converts the internal data format into the desired output format including YUV, RGB, or RAW.

table 6-6 FORMAT control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x4300	FORMAT CONTROL 00	0xF8	RW	Format Control 00 Bit[7:4]: Output format of formatter module 0x0: RAW Bit[3:0]: Output sequence 0x0: BGBG... / GRGR... 0x1: GBGB... / RGRG... 0x2: GRGR... / BGBG... 0x3: RGRG... / GBGB... 0x4~0xF: Not allowed 0x1: Y8 Bit[3:0]: Does not matter 0x2: YUV444/RGB888 (not available for full resolution) Bit[3:0]: Output sequence 0x0: YUVYUV..., or GBRGBR... 0x1: YVUYVU..., or GRBGRB... 0x2: UYVUYV..., or BGRBGR... 0x3: VYUVYU..., or RGBRGB... 0x4: UVYUVY..., or BRGBRG... 0x5: VUYVUY..., or RBGRBG... 0x6~0xE: Not allowed 0xF: UYVUYV..., or BGRBGR... 0x3: YUV422 Bit[3:0]: Output sequence 0x0: YUYV... 0x1: YVYU... 0x2: UYVY... 0x3: VYUY... 0x4~0xE: Not allowed 0xF: UYVY... 0x4: YUV420 Bit[3:0]: Output sequence 0x0: YYYY... / YUYV... 0x1: YYYY... / YVYU... 0x2: YYYY... / UYVY... 0x3: YYYY... / VYUY... 0x4: YUYV... / YYYY...

table 6-6 FORMAT control registers (sheet 2 of 5)

address	register name	default value	R/W	description
				0x5: YVYU... / YYYY... 0x6: UYVY... / YYYY... 0x7: VYUY... / YYYY... 0x8~0xE: Not allowed 0xF: YYYY... / UYVY... 0x5: YUV420 (for MIPI only) Bit[3:0]: Output sequence 0x0~0xD: Not allowed 0xE: VYYVYY... / UYYUYY... 0xF: UYYUYY... / VYYVYY... 0x6: RGB565 Bit[3:0]: Output sequence 0x0: {b[4:0],g[5:3]}, {g[2:0],r[4:0]} 0x1: {r[4:0],g[5:3]}, {g[2:0],b[4:0]} 0x2: {g[4:0],r[5:3]}, {r[2:0],b[4:0]} 0x3: {b[4:0],r[5:3]}, {r[2:0],g[4:0]} 0x4: {g[4:0],b[5:3]}, {b[2:0],r[4:0]} 0x5: {r[4:0],b[5:3]}, {b[2:0],g[4:0]} 0x6~0xE: Not allowed 0xF: {g[2:0],b[4:0]}, {r[4:0],g[5:3]} 0x7: RGB555 format 1 Bit[3:0]: Output sequence 0x0: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} 0x1: {r[4:0],g[4:2]}, {g[1:0],1'b0,b[4:0]} 0x2: {g[4:0],r[4:2]}, {r[1:0],1'b0,b[4:0]} 0x3: {b[4:0],r[4:2]}, {r[1:0],1'b0,g[4:0]} 0x4: {r[4:0],b[4:2]}, {b[1:0],1'b0,g[4:0]} 0x5: {g[4:0],b[4:2]}, {b[1:0],1'b0,r[4:0]} 0x6~0xE: Not allowed 0xF: {g[1:0],1'b0,b[4:0]}, {r[4:0],g[4:2]} 0x8: RGB555 format 2 Bit[3:0]: Output sequence 0x0: {1'b0,b[4:0],g[4:3]}, {g[2:0],r[4:0]}

table 6-6 FORMAT control registers (sheet 3 of 5)

address	register name	default value	R/W	description
				0x1: {1'b0,r[4:0],g[4:2]}, {g[2:0],b[4:0]} 0x2: {1'b0,g[4:0],r[4:2]}, {r[2:0],b[4:0]} 0x3: {1'b0,b[4:0],r[4:2]}, {r[2:0],g[4:0]} 0x4: {1'b0,r[4:0],b[4:2]}, {b[2:0],g[4:0]} 0x5: {1'b0,g[4:0],b[4:2]}, {b[2:0],r[4:0]} 0x6: {b[4:0],1'b0,g[4:3]}, {g[2:0],r[4:0]} 0x7: {r[4:0],1'b0,g[4:2]}, {g[2:0],b[4:0]} 0x8: {g[4:0],1'b0,r[4:2]}, {r[2:0],b[4:0]} 0x9: {b[4:0],1'b0,r[4:2]}, {r[2:0],g[4:0]} 0xA: {r[4:0],1'b0,b[4:2]}, {b[2:0],g[4:0]} 0xB: {g[4:0],1'b0,b[4:2]}, {b[2:0],r[4:0]} 0xC~0xF: Not allowed 0x9: RGB444 format 1 Bit[3:0]: Output sequence 0x0: {1'b0,b[3:0],2'h0,g[3]}, {g[2:0],1'b0,r[3:0]} 0x1: {1'b0,r[3:0],2'h0,g[3]}, {g[2:0],1'b0,b[3:0]} 0x2: {1'b0,g[3:0],2'h0,r[3]}, {r[2:0],1'b0,b[3:0]} 0x3: {1'b0,b[3:0],2'h0,r[3]}, {r[2:0],1'b0,g[3:0]} 0x4: {1'b0,r[3:0],2'h0,b[3]}, {b[2:0],1'b0,g[3:0]} 0x5: {1'b0,g[3:0],2'h0,b[3]}, {b[2:0],1'h0,r[3:0]} 0x6: {b[3:0],1'b0,g[3:1]}, {g[0],2'h0,r[3:0],1'b0} 0x7: {r[3:0],1'b0,g[3:1]}, {g[0],2'h0,b[3:0],1'b0} 0x8: {g[3:0],1'b0,r[3:1]}, {r[0],2'h0,b[3:0],1'b0} 0x9: {b[3:0],1'b0,r[3:1]}, {r[0],2'h0,g[3:0],1'b0} 0xA: {r[3:0],1'b0,b[3:1]}, {b[0],2'h0,g[3:0],1'b0} 0xB: {g[3:0],1'b0,b[3:1]}, {b[0],2'h0,r[3:0],1'b0} 0xC~0xE: Not allowed

table 6-6 FORMAT control registers (sheet 4 of 5)

address	register name	default value	R/W	description
				0xF: {g[0],2'h2,b[3:0],1'b1}, {r[3:0],1'b1,g[3:1]} 0xA: RGB444 format 2 Bit[3:0]: Output sequence 0x0: {4'b0,b[3:0]}, {g[3:0],r[3:0]} 0x1: {4'b0,r[3:0]}, {g[3:0],b[3:0]} 0x2: {4'b0,b[3:0]}, {r[3:0],g[3:0]} 0x3: {4'b0,r[3:0]}, {b[3:0],g[3:0]} 0x4: {4'b0,g[3:0]}, {b[3:0],r[3:0]} 0x5: {4'b0,g[3:0]}, {r[3:0],b[3:0]} 0x6: {b[3:0],g[3:0],2'h0}, {r[3:0],b[3:0],2'h0,g[3:0],r[3:0],2'h0} 0x7: {r[3:0],g[3:0],2'h0}, {b[3:0],r[3:0],2'h0,g[3:0],b[3:0],2'h0} 0x8: {b[3:0],r[3:0],2'h0}, {g[3:0],b[3:0],2'h0,r[3:0],g[3:0],2'h0} 0x9: {r[3:0],b[3:0],2'h0}, {g[3:0],r[3:0],2'h0,b[3:0],g[3:0],2'h0} 0xA: {g[3:0],b[3:0],2'h0}, {r[3:0],g[3:0],2'h0,b[3:0],r[3:0],2'h0} 0xB: {g[3:0],r[3:0],2'h0}, {b[3:0],g[3:0],2'h0,r[3:0],b[3:0],2'h0} 0xC~0xF: Not allowed 0xB~0xE: Not allowed 0xF: Bypass Formatter Module, not recommended. Bit[3:0]: Output format 0x8: Raw 0x9: YUV422 0xA: YUV444 0xE: VYYVYY.../UYYUYY 0xF: UYYUYY.../VYYVYY
0x4301	FORMAT CONTROL 01	0x00	RW	Format Control 01 Bit[1:0]: YUV422 UV control 00: U/V generated from average 01: U/V generated from first pixel 11: U/V generated from second pixel

table 6-6 FORMAT control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x4302	YMAX VALUE	0x03	RW	Bit[1:0]: Y Max Clip Value[9:8]
0x4303	YMAX VALUE	0xFF	RW	Bit[7:0]: Y Max Clip Value[7:0]
0x4304	YMIN VALUE	0x00	RW	Bit[1:0]: Y Min Clip Value[9:8]
0x4305	YMIN VALUE	0x00	RW	Bit[7:0]: Y Min Clip Value[7:0]
0x4306	UMAX VALUE	0x03	RW	Bit[1:0]: U Max Clip Value[9:8]
0x4307	UMAX VALUE	0xFF	RW	Bit[7:0]: U Max Clip Value[7:0]
0x4308	UMIN VALUE	0x00	RW	Bit[1:0]: U Min Clip Value[9:8]
0x4309	UMIN VALUE	0x00	RW	Bit[7:0]: U Min Clip Value[7:0]
0x430A	VMAX VALUE	0x03	RW	Bit[1:0]: V Max Clip Value[9:8]
0x430B	VMAX VALUE	0xFF	RW	Bit[7:0]: V Max Clip Value[7:0]
0x430C	VMIN VALUE	0x00	RW	Bit[1:0]: V Min Clip Value[9:8]
0x430D	VMIN VALUE	0x00	RW	Bit[7:0]: V Min Clip Value[7:0]

6.7 digital video port (DVP)

6.7.1 overview

The Digital Video Port (DVP) provides 10-bit parallel data output in all formats supported and extended features including compression mode, HSYNC mode, CCIR656 mode, and test pattern output. The DVP is also used to receive the video data from an external camera, which will be sent out through the OV5642 MIPI interface.

table 6-7 DVP control registers (sheet 1 of 2)

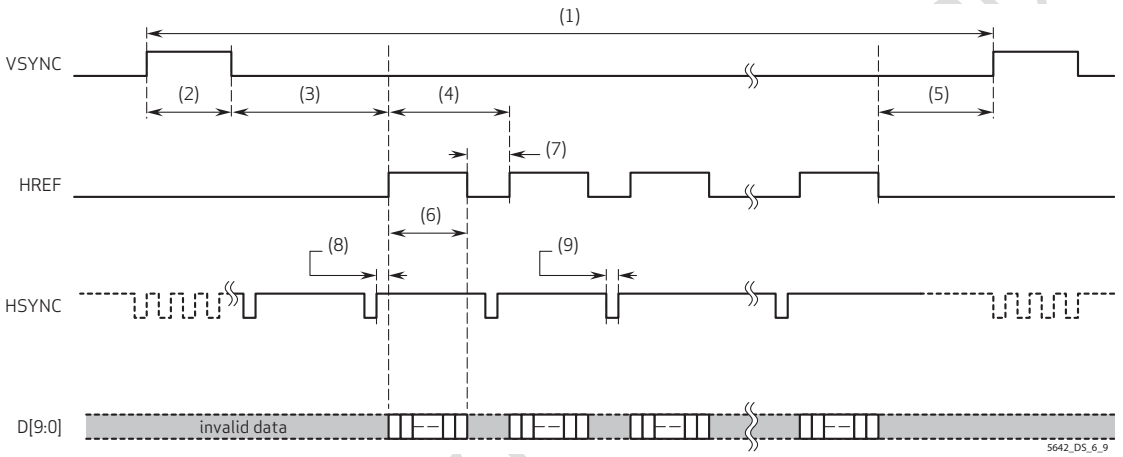
address	register name	default value	R/W	description
0x4711	PAD LEFT CONTROL	0x00	RW	HSYNC Mode Left Padding Pixel Count Add padding data at the start of a line
0x4712	PAD RIGHT CONTROL	0x00	RW	HSYNC Mode Right Padding Pixel Count Add padding data at the end of a line
0x4713	COMPRESSION MODE SELECT	0x02	RW	Bit[2:0]: Compression mode select 001: Compression mode 1 010: Compression mode 2 011: Compression mode 3 100: Compression mode 4 101: Compression mode 5 110: Compression mode 6
0x4715	656 DUMMY LINE	0x00	RW	Bit[3:0]: CCIR656 dummy line number Control dummy line number at the beginning of the frame
0x4719	CCIR656 V SEL	0x01	RW	Bit[1:0]: First sync code select 00: First sync code is SAV 01: First sync code is EAV 1x: Using this is not recommended
0x471B	HSYNC CONTROL 00	0x02	RW	Bit[0]: HSYNC mode enable
0x471D	DVP CONTROL 1D	0x00	RW	Bit[1:0]: VSYNC option 00: VSYNC extend when dummy line is inserted 01: Dummy line is inserted after VSYNC pulse 10: Dummy line is inserted before VSYNC pulse 11: Not allowed
0x4721	VERTICAL START OFFSET	0x01	RW	Bit[3:0]: Vertical start delay between video output and video input
0x4722	VERTICAL END OFFSET	0x00	RW	Bit[3:0]: Vertical end delay between video output and video input

table 6-7 DVP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4730	CCIR656 CONTROL 00	0x00	RW	Bit[0]: CCIR656 mode enable
0x4732	CCIR656 FS	0x01	RW	CCIR656 Sync Code Frame Start
0x4733	CCIR656 FE	0x0F	RW	CCIR656 Sync Code Frame End
0x4734	CCIR656 LS	0x00	RW	CCIR656 Sync Code Line Start
0x4735	CCIR656 LE	0x00	RW	CCIR656 Sync Code Line End
0x4740	POLARITY CTRL 00	0x20	RW	DVP Output Polarity Control Bit[5]: PCLK polarity 0: Latch at rising edge 1: Latch at falling edge Bit[3]: Gate PCLK under VSYNC Bit[2]: Gate PCLK under HREF Bit[1]: HREF polarity 0: Active low 1: Active high Bit[0]: VSYNC polarity 0: Active low 1: Active high
0x4741	TEST PATTERN	0x00	RW	Bit[2]: Test pattern enable Bit[1]: Test pattern (bit shift pattern) select 0: Output test pattern 0 1: Output test pattern 1 Bit[0]: Test pattern 8-bit / 10-bit 0: 10-bit test pattern 1: 8-bit test pattern
0x4745	DATA ORDER	0x00	RW	Bit[0]: Output data order 0: Normal output 1: Reverse output data bit order

6.7.2 DVP timing

figure 6-9 DVP timing diagram



note
The timing values shown in **table 6-8** may vary depending upon register settings.

table 6-8 DVP timing specifications (sheet 1 of 2)

mode	timing
5 megapixel 2592x1944	(1) 6132288 tp (2) 15776 tp (3) 12468 tp (4) 311 tp (5) 47064 tp (6) 2592 tp (7) 524 tp (8) 0 tp (9) 524 tp
1080p 1920x1080	(1) 6132288 tp (2) 16448 tp (3) 12468 tp (4) 3116 tp (5) 2739288 tp (6) 1920 tp (7) 1196 tp (8) 0 tp (9) 1196 tp
UXGA 1600x1200	(1) 6132288 tp (2) 16768 tp (3) 12468 tp (4) 3116 tp (5) 2739288 tp (6) 1600 tp (7) 1516 tp (8) 0 tp (9) 1516 tp

table 6-8 DVP timing specifications (sheet 2 of 2)

mode	timing
720p 1280x720	(1) 3066144 tp (2) 7904 tp (3) 6234 tp (4) 1558 tp (5) 1930524 tp (6) 1280 tp (7) 278 tp (8) 0 tp (9) 278 tp
XGA 1024x768	(1) 3066144 tp (2) 8160 tp (3) 6234 tp (4) 1558 tp (5) 1855740 tp (6) 1024 tp (7) 534 tp (8) 0 tp (9) 534 tp
VGA 640x480	(1) 1533072 tp (2) 3952 tp (3) 3117 tp (4) 779 tp (5) 1152222 tp (6) 640 tp (7) 139 tp (8) 0 tp (9) 139 tp
QVGA 320x240	(1) 766536 tp (2) 2959 tp (3) 1555 tp (4) 389 tp (5) 637611 tp (6) 320 tp (7) 69 tp (8) 0 tp (9) 69 tp
SQCIF 128x96	(1) 3066144 tp (2) 7904 tp (3) 6234 tp (4) 1558 tp (5) 1930524 tp (6) 1280 tp (7) 278 tp (8) 0 tp (9) 278 tp

6.8 mobile industry processor interface (MIPI)

MIPI provides a single uni-directional clock lane and two bi-directional data lane solution for communication links between components inside a mobile device. The two data lanes have full support for HS (uni-direction) and LP (bi-direction) data transfer mode. Contact your local OmniVision FAE for more details.

table 6-9 MIPI receiver registers

address	register name	default value	R/W	description
0x4A00	MIPI RX CTRL00	0x00	RW	Bit[1:0]: mipi_rx_vc MIPI RX virtual channel ID
0x4A01	MIPI RX CTRL01	0x06	RW	Bit[2:1]: ph_order Packet header options 00: {data_id, byte_num[7:0], byte_num[15:8]} 01: {data_id, byte_num} 10: {byte_num[7:0], byte_num[15:8], data_id} 11: {byte_num, data_id} Bit[0]: line_sync_sel 0: Input stream without line sync short packet 1: Input stream with line sync short packet
0x4A02	MIPI RX CTRL02	0x04	RW	Delay Between VSYNC Positive Edge and FE
0x4A03	MIPI RX CTRL03	0x04	RW	Delay Between VSYNC Negative Edge and FS

table 6-10 MIPI transmitter registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x4800	MIPI CTRL 00	0x04	RW	MIPI Control 00 Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Lane select 0: Use lane1 as default data lane 1: Use lane2 as default data lane Bit[2]: Idle status 0: MIPI bus will be LP00 when no packet to transmit 1: MIPI bus will be LP11 when no packet to transmit

table 6-10 MIPI transmitter registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x4801	MIPI CTRL 01	0x03	RW	MIPI Control 01 Bit[7]: Long packet data type manual enable 0: Use mipi_dt 1: Use dt_man_o as long pkt dt Bit[6]: Short packet data type manual enable 1: Use dt_spkt as short pkt dt Bit[5]: Short packet WORD COUNTER manual enable 0: Use frame counter or line counter 1: Select spkt_wc_reg_o Bit[4]: PH bit order for ECC 0: {DI[7:0],WC[7:0],WC[15:8]} 1: {DI[0:7],WC[0:7],WC[8:15]} Bit[3]: PH byte order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[2]: PH byte order2 for ECC 0: {DI,WC} 1: {WC,DI}
0x4803	MIPI CTRL 03	0x5F	RW	MIPI Control 03 Bit[3]: Enable LP CD when HS TX for lane1 0: Disable 1: Enable Bit[2]: Enable LP CD when HS TX for lane2 0: Disable 1: Enable Bit[1]: Enable LP CD when LP TX for lane2 0: Disable 1: Enable Bit[0]: Enable LP CD when LP TX for lane1 0: Disable 1: Enable
0x4804	MIPI CTRL 04	0x8D	RW	MIPI Control 04 Bit[4]: Enable MIPI LP RX to read/write registers 0: Disable - RX LP data will write to VFIFO 1: Enable Bit[3]: Address read/write register will auto add 1 1: Enable Bit[2]: LP TX lane select 0: Select lane1 to transmit LP data 1: Select lane2 to transmit LP data

table 6-10 MIPI transmitter registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x4805	MIPI CTRL 05	0x10	RW	MIPI Control 05 Bit[7]: MIPI lane1 disable 1: Disable MIPI data lane1, lane1 will be LP00 Bit[6]: MIPI lane1 disable 1: Disable MIPI data lane1, lane1 will be LP00 Bit[2]: MIPI read/write registers disable 1: Disable MIPI access to SRB
0x4810	MAX FCNT H	0xFF	RW	High Byte of Max Frame Counter of Frame Sync Short Packet
0x4811	MAX FCNT L	0xFF	RW	Low Byte of Max Frame Counter of Frame Sync Short Packet
0x4812	MIN SPKT WC REG H	0x00	RW	High Byte of Manual Short Packet Word Counter
0x4813	MIN SPKT WC REG L	0x00	RW	High Byte of Manual Short Packet Word Counter
0x4814	MIPI CTRL 14	0x2A	RW	Bit[7:6]: MIPI virtual channel Bit[5:0]: Data type manual
0x4815	MIPI SPKT DT	0x00	RW	Manual Data Type for Short Packet
0x4818	MIN HS ZERO H	0x00	RW	High Byte of Minimum Value of hs_zero, unit ns
0x4819	MIN HS ZERO L	0x96	RW	Low Byte of Minimum Value of hs_zero hs_zero_real = hs_zero_min_o + tui × ui_hs_zero_min_o
0x481A	MIN MIPI HS TRAIL H	0x00	RW	High Byte of Minimum Value of hs_trail, unit ns
0x481B	MIN MIPI HS TRAIL L	0x3C	RW	Low Byte of Minimum Value of hs_trail hs_trail_real = hs_trail_min_o + tui × ui_hs_trail_min_o
0x481C	MIN MIPI CLK ZERO H	0x01	RW	High Byte of Minimum Value of clk_zero, unit ns
0x481D	MIN MIPI CLK ZERO L	0x86	RW	Low Byte of Minimum Value of clk_zero clk_zero_real = clk_zero_min_o + tui × ui_clk_zero_min_o
0x481E	MIN MIPI CLK PREPARE H	0x00	RW	High Byte of Minimum Value of clk_prepare, unit ns
0x481F	MIN MIPI CLK PREPARE L	0x3C	RW	Low Byte of Minimum Value of clk_prepare clk_prepare_real = clk_prepare_min_o + tui × ui_clk_prepare_min_o
0x4820	MIN CLK POST H	0x00	RW	High Byte of Minimum Value of clk_post, unit ns
0x4821	MIN CLK POST L	0x56	RW	Low Byte of Minimum Value of clk_post clk_post_real = clk_post_min_o + tui × ui_clk_post_min_o

table 6-10 MIPI transmitter registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x4822	MIN CLK TRAIL H	0x00	RW	High Byte of Minimum Value of clk_trail, unit ns
0x4823	MIN CLK TRAIL L	0x3C	RW	Low Byte of Minimum Value of clk_trail clk_trail_real = clk_trail_min_o + tui × ui_clk_trail_min_o
0x4824	MIN LPX PCLK H	0x00	RW	High Byte of Minimum Value of lpx_p, unit ns
0x4825	MIN LPX PCLK L	0x32	RW	Low Byte of Minimum Value of lpx_p lpx_p_real = lpx_p_min_o + tui × ui_lpx_p_min_o
0x4826	MIN HS PREPARE H	0x00	RW	High Byte of Minimum Value of hs_prepare, unit ns
0x4827	MIN HS PREPARE L	0x32	RW	Low Byte of Minimum Value of hs_prepare hs_prepare_real = hs_prepare_min_o + tui × ui_hs_prepare_min_o
0x4828	MIN HS EXIT H	0x00	RW	High Byte of Minimum Value of hs_exit, unit ns
0x4829	MIN HS EXIT L	0x64	RW	Low Byte of Minimum Value of hs_exit hs_exit_real = hs_exit_min_o + tui × ui_hs_exit_min_o
0x482A	MIN HS ZERO/UI	0x05	RW	Minimum UI Value of hs_zero, unit UI
0x482B	MIN HS TRAIL/UI	0x04	RW	Minimum UI Value of hs_trail, unit UI
0x482C	MIN CLK ZERO/UI	0x00	RW	Minimum UI Value of clk_zero, unit UI
0x482D	MIN CLK PREPARE/UI	0x00	RW	Minimum UI Value of clk_prepare, unit UI
0x482E	MIN CLK POST/UI	0x34	RW	Minimum UI Value of clk_post, unit UI
0x482F	MIN CLK TRAIL/UI	0x00	RW	Minimum UI Value of clk_trail, unit UI
0x4830	MIN LPX PCLK/UI	0x00	RW	Minimum UI Value of lpx_p (pclk2x domain), unit UI
0x4831	MIN HS PREPARE/UI	0x04	RW	Minimum UI Value of hs_prepare, unit UI
0x4832	MIN HS EXIT/UI	0x00	RW	Minimum UI Value of hs_exit, unit UI
0x4833	MIN MIPI REG H	0x00	RW	High Byte of mipi_reg_min Address range of MIPI read/write registers is between mipi_reg_min and mipi_reg_max
0x4834	MIN MIPI REG L	0x00	RW	Low Byte of mipi_reg_min
0x4835	MAX MIPI REG H	0xFF	RW	High Byte of mipi_reg_max
0x4836	MAX MIPI REG L	0xFF	RW	Low Byte of mipi_reg_max
0x4837	PCLK PERIOD	0x10	RW	Period of pclk2x, pclk_div = 1, and 1-bit decimal
0x4838	WKUP DLY	0x02	RW	Wakeup delay for MIPI (Mark1 state) / 2^{12}

table 6-10 MIPI transmitter registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x483B	MIPI GPIO CTRL	0x33	RW	Bit[7]: Lane1 GPIO select 1: Select lane1 as GPIO Bit[6]: GPIO direction for lane1 0: Input 1: Output Bit[5]: Low power P value for lane1 Bit[4]: Low power N value for lane1 Bit[3]: Lane2 GPIO select 1: Select lane2 as GPIO Bit[2]: GPIO direction for lane2 0: Input 1: Output Bit[1]: Low power P value for lane2 Bit[0]: Low power N value for lane2
0x483C	MIPI CTRL 33	0x4F	RW	Bit[7:4]: Global timing for t_lpx Unit sclk cycle Bit[3:0]: Global timing for t_clk_pre Unit pixel clock cycle
0x483D	MIPI_T_TA_GO	0x10	RW	mipi_t_ta_go in unit of system clock cycle
0x483E	MIPI_T_TA_SURE	0x06	RW	mipi_t_ta_sure in unit of system clock cycle
0x483F	MIPI_T_TA_GET	0x14	RW	mipi_t_ta_get in unit of system clock cycle
0x4865	LP TX STATUS	0x00	R	Bit[5]: MIPI LP RX busy 1: MIPI_LP_RX receiving LP data Bit[4]: MIPI LP TX busy 0: Enable MIPI read/write registers 1: MIPI_LP_TX is busy to send LP data Bit[3]: MIPI low power input for lane1 P Bit[2]: MIPI low power input for lane1 N Bit[1]: MIPI low power input for lane2 P Bit[0]: MIPI low power input for lane2 N

7 register tables

The following tables provide descriptions of the device control registers contained in the OV5642. For all registers enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x78 for write and 0x79 for read.

table 7-1 system and IO pad control registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x3000	SYSTEM RESET00	0x20	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Debug mode Bit[6]: Reset MCU program memory Bit[5]: Reset MCU Bit[4]: Reset OTP memory Bit[3]: Reset STB Bit[2]: Debug mode Bit[1]: Reset timing control Bit[0]: Reset array control
0x3001	SYSTEM RESET01	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset AWB registers Bit[6]: Reset AFC Bit[5]: Reset ISP Bit[4]: Reset FC Bit[3]: Reset CIF Bit[2]: Reset BLC Bit[1]: Reset AEC registers Bit[0]: Reset AEC
0x3002	SYSTEM RESET02	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset VFIFO Bit[6]: Reset IFIFO Bit[5]: Reset format Bit[4]: Reset JFIFO Bit[3]: Reset SFIFO Bit[2]: Reset compression Bit[1]: Reset format mux Bit[0]: Reset average
0x3003	SYSTEM RESET03	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7:3]: Reserved Bit[2]: Reset ISP FC Bit[1]: Reset MIPI Bit[0]: Reset DVP

table 7-1 system and IO pad control registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x3004	CLOCK ENABLE00	0xDF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Debug mode Bit[6]: Enable MCU program memory clock Bit[5]: Enable MCU clock Bit[4]: Enable OTP memory clock Bit[3]: Enable strobe clock Bit[2]: Debug mode Bit[1]: Enable timing control clock Bit[0]: Enable array control clock
0x3005	CLOCK ENABLE01	0xFF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable AWB register clock Bit[6]: Enable AFC clock Bit[5]: Enable ISP clock Bit[4]: Enable FC clock Bit[3]: Enable CIF clock Bit[2]: Enable BLC clock Bit[1]: Enable AEC register clock Bit[0]: Enable AEC clock
0x3006	CLOCK ENABLE02	0xFF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable IFIFO clock Bit[6]: Enable format clock Bit[5]: Enable JFIFO 2x clock Bit[4]: Enable JFIFO clock Bit[3]: Enable SFIFO clock Bit[2]: Enable compression 2x clock Bit[1]: Enable format mux clock Bit[0]: Enable average clock
0x3007	CLOCK ENABLE03	0x3F	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7:5]: Not used Bit[4]: Enable MIPI PCLK clock Bit[3]: Enable MIPI clock Bit[2]: Enable DVP clock Bit[1]: Enable VFIFO PCLK clock Bit[0]: Enable VFIFO SCLK clock
0x3008	SC SYS0	0x02	RW	System Control Bit[7]: Software reset Bit[6]: Software power down Bit[5:0]: Debug mode

table 7-1 system and IO pad control registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x3009	MIPI PCLK DIVIDER CONTROL	0x01	RW	MIPI PCLK Divider Control Bit[7]: MIPI PCLK divider separate 1: MIPI PCLK divider separate setting from MIPI serial clock Bit[6]: Reserved Bit[5:0]: MIPI PCLK divider
0x300A	CHIP ID HIGH BYTE	0x56	R	Chip ID High Byte
0x300B	CHIP ID LOW BYTE	0x42	R	Chip ID Low Byte
0x300C	PLL_CTRL	–	RW	PLL Debug Mode
0x300D	ALFD_CTRL	0x02	RW	Auto Light Frequency Detection Control
0x300E	MIPI CONTROL 00	0x18	RW	MIPI Control 00 Bit[7:5]: Not used Bit[4]: MIPI TX PHY power down 1: Power down MIPI PHY HS TX module Bit[3]: MIPI RX PHY power down 1: Power down PHY LP RX module Bit[2]: MIPI enable 0: DVP enable 1: MIPI enable Bit[1]: MIPI system suspend control 1: Suspend MIPI Bit[0]: Lane disable option
0x300F	PLL CONTROL 00	0x06	RW	PLL Control 00 System clock frequency = PLL input clock x PLL DIVP / PLL DIVS / 4 PLL VCO frequency = PLL input clock x PLL DIVP x PLL SELD5 (PLL SELD5 = 1 or 4 or 5 Bit[7:3]: Debug mode Bit[2]: PLL DIVL divider Bit[1:0]: PLL SELD5 divider 0x: Bypass 10: Divide by 4 when in 8-bit mode 11: Divide by 5 when in 10-bit mode
0x3010	PLL CONTROL 01	0x00	RW	PLL Control 01 Bit[7:4]: PLL DIVS divider System divider ratio Bit[3:0]: PLL DIVM divider MIPI divider ratio

table 7-1 system and IO pad control registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x3011	PLL CONTROL 02	0x14	RW	PLL Control 02 Bit[7]: PLL bypass Bit[6]: Reserved Bit[5:0]: PLL DIVP divider
0x3012	PLL CONTROL 03	0x00	RW	PLL Control 03 Bit[7:3]: Reserved Bit[2:0]: PLL pre-divider ratio 000: 1 001: 1.5 010: 2 011: 2.5 100: 3 101: 4 110: 6 111: 8
0x3013~ 0x3015	SYSTEM CONTROL	–	RW	System Control Registers
0x3016	PAD OUTPUT ENABLE 00	0x00	RW	Input/Output Control (0: input; 1: output) Bit[7:3]: Not used Bit[2]: SDA output enable Bit[1]: STROBE output enable Bit[0]: Reserved
0x3017	PAD OUTPUT ENABLE 01	0x00	RW	Input/Output Control (0: input; 1: output) Bit[7]: FREX output enable Bit[6]: VSYNC output enable Bit[5]: HREF output enable Bit[4]: PCLK output enable Bit[3]: D9 output enable Bit[2]: D8 output enable Bit[1]: D7 output enable Bit[0]: D6 output enable
0x3018	PAD OUTPUT ENABLE 02	0x00	RW	Input/Output Control (0: input; 1: output) Bit[7]: D5 output enable Bit[6]: D4 output enable Bit[5]: D3 output enable Bit[4]: D2 output enable Bit[3]: D1 output enable Bit[2]: D0 output enable Bit[1]: GPIO1 output enable Bit[0]: GPIO0 output enable

table 7-1 system and IO pad control registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x3019	PAD OUTPUT VALUE 00	0x00	RW	GPIO Output Value 00 Bit[7:2]: Not used Bit[1]: STROBE Bit[0]: SDA
0x301A	PAD OUTPUT VALUE 01	0x00	RW	GPIO Output Value 01 Bit[7]: FREX Bit[6]: VSYNC Bit[5]: HREF Bit[4]: PCLK Bit[3]: D9 Bit[2]: D8 Bit[1]: D7 Bit[0]: D6
0x301B	PAD OUTPUT VALUE 02	0x00	RW	GPIO Output Value 02 Bit[7]: D5 Bit[6]: D4 Bit[5]: D3 Bit[4]: D2 Bit[3]: D1 Bit[2]: D0 Bit[1]: GPIO1 Bit[0]: GPIO0
0x301C	PAD OUTPUT SELECT 00	0x00	RW	Output Selection for GPIO Bit[7:2]: Not used Bit[1]: IO STROBE select Bit[0]: IO SDA select
0x301D	PAD OUTPUT SELECT 01	0x00	RW	Output Selection for GPIO Bit[7]: FREX select Bit[6]: VSYNC select Bit[5]: HREF select Bit[4]: PCLK select Bit[3]: D9 select Bit[2]: D8 select Bit[1]: D7 select Bit[0]: D6 select
0x301E	PAD OUTPUT SELECT 02	0x00	RW	Output Selection for GPIO Bit[7]: D5 select Bit[6]: D4 select Bit[5]: D3 select Bit[4]: D2 select Bit[3]: D1 select Bit[2]: D0 select Bit[1]: IO GPIO1 select Bit[0]: IO GPIO0 select
0x301F~ 0x302B	SYSTEM CONTROL	–	RW	System Control Registers

table 7-1 system and IO pad control registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x302C	PAD CONTROL 00	0x02	RW	Pad Control Bit[7:6]: Output drive capability 00: 1x 01: 2x 10: 3x 11: 4x Bit[5:2]: Debug mode Changing this value is not allowed Bit[1]: FREX enable Bit[0]: Debug mode Changing this value is not allowed
0x302D~ 0x302F	SYSTEM CONTROL	–	RW	System Control Registers Changing these values is not recommended
0x3030	SC A PWC PK O	0x0B	RW	PWC Control Bit[7:6]: Debug mode Changing this value is not allowed Bit[5]: bp_regulator Bit[4:0]: Debug mode Changing this value is not allowed
0x3031~ 0x303F	SYSTEM CONTROL	–	RW	System Control Registers Changing these values is not recommended
0x3040	PAD INPUT VALUE 00	–	R	Pad Input Status Bit[7:5]: Reserved Bit[3]: PWDN Bit[2]: PWUP Bit[1]: SCL Bit[0]: SDA
0x3041	PAD INPUT VALUE 01	–	R	Pad Input Status Bit[7]: OTP memory out Bit[6]: VSYNC Bit[5]: HREF Bit[4]: PCLK Bit[3]: D9 Bit[2]: D8 Bit[1]: D7 Bit[0]: D6

table 7-1 system and IO pad control registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x3042	PAD INPUT VALUE 02	–	R	Pad Input Status Bit[7]: D5 Bit[6]: D4 Bit[5]: D3 Bit[4]: D2 Bit[3]: D1 Bit[2]: D0 Bit[1]: GPIO1 Bit[0]: GPIO0

table 7-2 SCCB control registers

address	register name	default value	R/W	description
0x3100	SCCB ID	0x78	RW	SCCB Slave ID
0x3101~ 0x3102	SCCB CONTROL	–	RW	SCCB Control Registers Changing these values is not allowed
0x3103	PCLK CLOCK SELECT	0x01	RW	PLL Clock Select Bit[7:4]: Not used Bit[3:2]: Debug mode Changing this value is not allowed Bit[1]: Select PLL input clock 0: From pad clock 1: From pre-divider (clock modulator) Bit[0]: Debug mode Changing this value is not allowed
0x3104	SCCB PAD CLOCK DIVIDER	0x01	RW	Pad Clock Divider for SCCB Clock

table 7-3 group write control registers

address	register name	default value	R/W	description
0x3200	GROUP ADDR0	0x40	RW	Start Address for Group0 {group_addr0[7:0], 4'h0}
0x3201	GROUP ADDR1	0x4A	RW	Start Address for Group1 {group_addr1[7:0], 4'h0}
0x3202	GROUP ADDR2	0x54	RW	Start Address for Group2 {group_addr2[7:0], 4'h0}
0x3203	GROUP ADDR3	0x5E	RW	Start Address for Group3 {group_addr3[7:0], 4'h0}
0x3204~ 0x3211	GROUP WRITE CONTROL REGISTERS	–	RW	Group Write Registers Changing these values is not recommended
0x3212	GROUP ACCESS	0x00	RW	Bit[7]: group_launch_en Bit[6]: Debug mode (must be 0) Bit[5]: group_launch Bit[4]: group_hold_end Bit[3:0]: group_id 00~11: ID of the group to hold register
0x3213~ 0x3214	GROUP WRITE CONTROL REGISTERS	–	RW	Group Write Registers Changing these values is not recommended

table 7-4 AWB (for power keep domain in AWB gain) registers

address	register name	default value	R/W	description
0x3400	AWB R GAIN	0x04	RW	AWB R Gain High Byte
0x3401	AWB RGAIN	0x00	RW	AWB R Gain Low Byte
0x3402	AWB G GAIN	0x04	RW	AWB G Gain High Byte
0x3403	AWB G GAIN	0x00	RW	AWB G Gain Low Byte
0x3404	AWB B GAIN	0x04	RW	AWB B Gain High Byte
0x3405	AWB B GAIN	0x00	RW	AWB B Gain Low Byte
0x3406	AWB MANUAL	0x00	RW	Bit[7:1]: Not used Bit[0]: AWB manual enable 0: Auto 1: Manual

table 7-5 AEC/AGC (for power keep domain in AEC/AGC) registers

address	register name	default value	R/W	description
0x3500	AEC PK LONG EXPO	0x00	RW	Long Channel Exposure Output Bit[7:4]: Not used Bit[3:0]: Exposure[19:16]
0x3501	AEC PK LONG EXPO	0x00	RW	Long Channel Exposure Output Bit[7:0]: Exposure[15:8]
0x3502	AEC PK LONG EXPO	0x00	RW	Long Channel Exposure Output Bit[7:0]: Exposure[7:0]
0x3503	AEC PK MANUAL	0x00	RW	AEC Manual Mode Control Bit[7:3]: Not used Bit[2]: VTS manual 0: Auto enable 1: Manual enable Bit[1]: AGC manual 0: Auto enable 1: Manual enable Bit[0]: AEC manual 0: Auto enable 1: Manual enable
0x3504~ 0x3507	NOT USED	–	–	Not Used
0x3508	AEC PK LONG GAIN	0x00	RW	Long Channel Gain Output Bit[7:1]: Not used Bit[0]: Gain high bit
0x3509	AEC PK LONG GAIN	0x00	RW	Long Channel Gain Output Bit[7:0]: Gain low bits
0x350A	AEC PK AGC ADJ	0x00	RW	Gain Output to Sensor Bit[7:1]: Not used Bit[0]: Gain high bit
0x350B	AEC PK AGC ADJ	0x00	RW	Gain Output to Sensor Bit[7:0]: Gain low bits
0x350C	AEC PK VTS	0x06	RW	AEC VTS Output Bit[7:0]: VTS high bits[15:8]
0x350D	AEC PK VTS	0x18	RW	AEC VTS Output Bit[7:0]: VTS low bits[7:0]

table 7-6 sensor control registers

address	register name	default value	R/W	description
0x3600~ 0x3620	ANALOG CONTROL REGISTERS	–	RW	Analog Control Registers
0x3621	ARRAY CONTROL 01	0x10	RW	Array Control 01 Bit[7]: Horizontal binning enable Bit[6:0]: Reserved
0x3622~ 0x3634	ANALOG CONTROL REGISTERS	–	RW	Analog Control Registers
0x3700~ 0x370C	ANALOG CONTROL REGISTERS	–	RW	Analog Control Registers
0x370D	ANALOG CONTROL D	0x05	RW	Analog Control Bit[7]: Debug mode Changing this value is not allowed Bit[6]: Vertical binning enable Bit[5:0]: Debug mode Changing this value is not allowed
0x370E~ 0x3711	ANALOG CONTROL REGISTERS	–	RW	Analog Control Registers

table 7-7 timing control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3800	TIMING HS	0x01	RW	Bit[7:4]: Not used Bit[3:0]: HREF horizontal start point high byte[11:8]
0x3801	TIMING HS	0xB4	RW	Bit[7:0]: HREF horizontal start point low byte[7:0]
0x3802	TIMING VS	0x00	RW	Bit[7:4]: Not used Bit[3:0]: HREF vertical start point high byte[11:8]
0x3803	TIMING VS	0x0A	RW	Bit[7:0]: HREF vertical start point low byte[7:0]
0x3804	TIMING HW	0x08	RW	Bit[7:4]: Not used Bit[3:0]: HREF horizontal width high byte[11:8]

table 7-7 timing control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3805	TIMING HW	0x00	RW	Bit[7:0]: HREF horizontal width low byte[7:0]
0x3806	TIMING VH	0x06	RW	Bit[7:4]: Not used Bit[3:0]: HREF vertical height high byte[11:8]
0x3807	TIMING VH	0x00	RW	Bit[7:0]: HREF vertical height low byte[7:0]
0x3808	TIMING DVPHO	0x08	RW	Bit[7:4]: Not used Bit[3:0]: DVP output horizontal width high byte[11:8]
0x3809	TIMING DVPHO	0x00	RW	Bit[7:0]: DVP output horizontal width low byte[7:0]
0x380A	TIMING DVPVO	0x06	RW	Bit[7:4]: Not used Bit[3:0]: DVP output vertical height high byte[11:8]
0x380B	TIMING DVPVO	0x00	RW	Bit[7:0]: DVP output vertical height low byte[7:0]
0x380C	TIMING HTS	0x09	RW	Bit[7:4]: Not used Bit[3:0]: Total horizontal size high byte[11:8]
0x380D	TIMING HTS	0x48	RW	Bit[7:0]: Total horizontal size low byte[7:0]
0x380E	TIMING VTS	0x06	RW	Bit[7:4]: Not used Bit[3:0]: Total vertical size high byte[11:8]
0x380F	TIMING VTS	0x18	RW	Bit[7:0]: Total vertical size low byte[7:0]
0x3810	TIMING HVOFFS	0xC2	RW	Horizontal and Vertical Offset Setting Bit[7:4]: HOFF Bit[3:0]: VOFFS
0x3811	TIMING THNVH	0xF0	RW	Thumbnail Output Size Vertical
0x3812	TIMING THNHW	0x01	RW	Bit[7:1]: Not used Bit[0]: Thumbnail output size horizontal high byte[8]
0x3813	TIMING THNHW	0x40	RW	Bit[7:0]: Thumbnail output size horizontal low byte[7:0]

table 7-7 timing control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3818	TIMING CONTROL 18	0x80	RW	Timing Control Bit[6]: Mirror ON/OFF select 0: Mirror OFF 1: Mirror ON Bit[5]: Vertical flip ON/OFF select 0: Vertical flip OFF 1: Vertical flip ON Bit[4]: Thumbnail enable 0: Thumbnail mode disabled 1: Thumbnail mode enabled Bit[3]: Compression enable 0: Compression disabled 1: Compression enabled Bit[2]: Not used Bit[1]: Vertical subsample 1/4 Bit[0]: Vertical subsample 1/2

table 7-8 power down domain AEC/AGC registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3A00	AEC CTRL00	0x7C	RW	AEC System Control 0 (0: disable; 1: enable) Bit[7]: Not used Bit[6]: Less one line mode Bit[5]: Band function Bit[4]: Band low limit mode Bit[3]: Reserved Bit[2]: Night mode Bit[1]: Not used Bit[0]: Freeze
0x3A01	AEC CTRL01	0x04	RW	Minimum Exposure Output Limit Bit[7:0]: Min expo
0x3A02	AEC MAX EXPO (60Hz)	0x03	RW	60 Hz Maximum Exposure Output Limit Bit[7:4]: Not used Bit[3:0]: Max expo[19:16]
0x3A03	AEC MAX EXPO (60Hz)	0xD8	RW	60 Hz Maximum Exposure Output Limit Bit[7:0]: Max expo[15:8]
0x3A04	AEC MAX EXPO (60Hz)	0x00	RW	60 Hz Maximum Exposure Output Limit Bit[7:0]: Max expo[7:0]

table 7-8 power down domain AEC/AGC registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3A05	AEC CTRL05	0x30	RW	AEC System Control 2 Bit[7]: f50_reverse 0: Hold 50,60Hz detect input 1: Switch 50, 60Hz detect input Bit[6]: frame_insert 0: In night mode, insert frame disable 1: In night mode, insert frame enable Bit[5]: step_auto_en 0: Step manual mode 1: Step auto_mode Bit[4:0]: step_auto_ratio In step auto mode, step ratio setting to adjust speed
0x3A06	AEC CTRL06	0x10	RW	AEC System Control 3 Bit[7]: Not used Bit[6]: pclk_div4 0: Disabled 1: Vsub4, clock divided by 4 Bit[5]: pclk_div2 0: Disabled 1: Vsub2, clock divided by 2 Bit[4:0]: step_man1 Step manual, increase mode fast step
0x3A07	AEC CTRL07	0x18	RW	AEC Manual Step Bit[7:4]: step_man2 Step manual, slow step Bit[3:0]: step_man3 Step manual, decrease mode fast step
0x3A08	AEC B50 STEP	0x0E	RW	50 Hz Band Width Bit[7:6]: Not used Bit[5:0]: b50_step[13:8]
0x3A09	AEC B50 STEP	0xA0	RW	50 Hz Band Width Bit[7:0]: b50_step[7:0]
0x3A0A	AEC B60 STEP	0x0C	RW	60 Hz Band Width Bit[7:6]: Not used Bit[5:0]: b60_step[13:8]
0x3A0B	AEC B60 STEP	0x30	RW	60 Hz Band Width Bit[7:0]: b60_step[7:0]

table 7-8 power down domain AEC/AGC registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3A0C	AEC CTRL REGISTERS	–	RW	AEC Control Registers
0x3A0D	AEC CTRL0D	0x08	RW	60 Hz Max Bands in One Frame Bit[7:6]: Not used Bit[5:0]: b60_max
0x3A0E	AEC CTRL0E	0x06	RW	50 Hz Max Bands in One Frame Bit[7:6]: Not used Bit[5:0]: b50_max
0x3A0F	AEC CTRL0F	0x78	RW	Stable Range High Limit (enter) Bit[7:0] wpt
0x3A10	AEC CTRL10	0x68	RW	Stable Range Low Limit (enter) Bit[7:0] bpt
0x3A11	AEC CTRL11	0xD0	RW	Step Manual Mode, Fast Zone High Limit Bit[7:0] vpt_high
0x3A12	AEC CTRL12	0x00	RW	Manual Average Input Bit[7:0]: r_man_avg_i
0x3A13	AEC CTRL13	0x10	RW	AEC Control 13 Bit[7:6]: Not used Bit[5]: Pre-gain enable Bit[4:0]: Pre-gain value
0x3A14	AEC MAX EXPO (50Hz)	0x03	RW	50 Hz Maximum Exposure Output Limit Bit[7:4]: Not used Bit[3:0]: Max expo[19:16]
0x3A15	AEC MAX EXPO (50Hz)	0x75	RW	50 Hz Maximum Exposure Output Limit Bit[7:0]: Max expo[15:8]
0x3A16	AEC MAX EXPO (50Hz)	0x00	RW	50 Hz Maximum Exposure Output Limit Bit[7:0]: Max expo[7:0]
0x3A17	AEC CTRL17	0x89	RW	Gain Base When in Night Mode Bit[7:2]: Not used Bit[1:0]: gnight_thre 00: 0x00 01: 0x10 10: 0x30 11: 0x70
0x3A18	AEC GAIN CEILING	0x03	RW	Gain Output Top Limit Bit[7:1]: Not used Bit[0]: AEC gain ceiling high bit
0x3A19	AEC GAIN CEILING	0xE0	RW	Gain Output Top Limit Bit[7:0]: AEC gain ceiling low bits
0x3A1A	AEC CTRL REGISTERS	–	RW	AEC Control Registers

table 7-8 power down domain AEC/AGC registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3A1B	AEC CTRL1B	0x78	RW	Stable Range High Limit (go out) Bit[7:0]: wpt2
0x3A1C	LED ADD ROW	0x06	RW	Exposure Values Added When Strobe is ON Bit[7:0]: aec_led_add_row [15:8]
0x3A1D	LED ADD ROW	0x18	RW	Exposure Values Added When Strobe is ON Bit[7:0]: aec_led_add_row [7:0]
0x3A1E	AEC CTRL1E	0x68	RW	Stable Range Low Limit (go out) Bit[7:0]: bpt2
0x3A1F	AEC CTRL1F	0x40	RW	Step Manual Mode, Fast Zone Low Limit Bit[7:0]: vpt_low
0x3A20	AEC CONTROL 20	–	RW	AEC Debug Mode Changing these values is not allowed

table 7-9 FREX strobe registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Strobe Control Bit[7]: Strobe request ON/OFF 0: OFF/BLC 1: ON Bit[6]: Strobe pulse reverse Bit[5:4]: Debug mode Bit[3:2]: width_in_xenon Bit[1:0]: Strobe mode 00: Xenon 01: LED1 10: LED2 11: LED3
0x3B01~ 0x3B03	FREX CONTROL	–	RW	FREX Control Registers
0x3B04	FREX CONTROL 01	0x04	RW	FREX Exposure Time High Byte
0x3B05	FREX CONTROL 02	0x00	RW	FREX Exposure Time Low Byte
0x3B06	FREX CONTROL 03	0x04	RW	Bit[7:4]: FREX frame delay number Bit[3:0]: Reserved

table 7-9 FREX strobe registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B07	FREX CONTROL 04	0x08	RW	Bit[7:2]: Reserved Bit[1:0]: FREX mode select 0x: Rolling strobe 10: FREX strobe mode0 11: FREX strobe mode1
0x3B08	FREX CONTROL 05	0x00	RW	FREX Request

table 7-10 light frequency registers

address	register name	default value	R/W	description
0x3C00	ALFD_CTRL2	0x00	RW	Bit[7:6]: Not used Bit[5:3]: Light frequency detection control Changing these values is not allowed Bit[2]: Manual light frequency selection 0: 60 Hz 1: 50 Hz Bit[1:0]: Light frequency detection control Changing these values is not allowed
0x3C01	ALFD_CTRL1	0x00	RW	Bit[7]: Auto detection enable 0: Enable auto detection 1: Disable auto detection Bit[6:0]: Light frequency detection control Changing these values is not allowed
0x3C02~ 0x3C0B	ALFD_CTRL	–	–	Light Frequency Detection Control Changing these registers is NOT recommended.
0x3C0C	ALFD_CTRLC	–	R	Bit[7:1]: Debug information Bit[0]: Light frequency indicator 0: 60 Hz 1: 50 Hz
0x3C0D~ 0x3C1F	ALFD_CTRL	–	R	Light Frequency Detection Control Changing these registers is NOT recommended.

table 7-11 OTP registers

address	register name	default value	R/W	description
0x3D00	OTP DATA00	0x00	RW	OTP Dump/Load Data00
0x3D01	OTP DATA01	0x00	RW	OTP Dump/Load Data01
0x3D02	OTP DATA02	0x00	RW	OTP Dump/Load Data02
0x3D03	OTP DATA03	0x00	RW	OTP Dump/Load Data03
0x3D04	OTP DATA04	0x00	RW	OTP Dump/Load Data04
0x3D05	OTP DATA05	0x00	RW	OTP Dump/Load Data05
0x3D06	OTP DATA06	0x00	RW	OTP Dump/Load Data06
0x3D07	OTP DATA07	0x00	RW	OTP Dump/Load Data07
0x3D08	OTP DATA08	0x00	RW	OTP Dump/Load Data08
0x3D09	OTP DATA09	0x00	RW	OTP Dump/Load Data09
0x3D0A	OTP DATA0A	0x00	RW	OTP Dump/Load Data0a
0x3D0B	OTP DATA0B	0x00	RW	OTP Dump/Load Data0b
0x3D0C	OTP DATA0C	0x00	RW	OTP Dump/Load Data0c
0x3D0D	OTP DATA0D	0x00	RW	OTP Dump/Load Data0d
0x3D0E	OTP DATA0E	0x00	RW	OTP Dump/Load Data0e
0x3D0F	OTP DATA0F	0x00	RW	OTP Dump/Load Data0f
0x3D10	OTP CTRL	0x00	RW	OTP Control Bit[7:2]: Debug mode Bit[1:0]: OTP operation mode 00: OTP OFF 01: Load/dump OTP 10: Write/program OTP 11: OTP OFF

table 7-12 MCU registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3F00	MC CTRL00	0x00	RW	MC Control 00 Bit[7:1]: Control register bits for microcontroller Changing these values is not recommended Bit[0]: Soft reset of MCU 1: Reset MCU
0x3F01	MC INTERRUPT MASK0	0x00	RW	Mask0 for Interrupt Bit[7:6]: Reserved Bit[5]: ISP EOF 0: Disable interrupt bit 1: Enable interrupt bit Bit[4]: ISP SOF 0: Disable interrupt bit 1: Enable interrupt bit Bit[3]: Reserved Bit[2]: AWB done 0: Disable interrupt bit 1: Enable interrupt bit Bit[1]: VFIFO full 0: Disable interrupt bit 1: Enable interrupt bit Bit[0]: VFIFO empty 0: Disable interrupt bit 1: Enable interrupt bit
0x3F02	MC INTERRUPT MASK1	0x00	RW	Mask1 for Interrupt Bit[7]: AEC done 0: Disable interrupt bit 1: Enable interrupt bit Bit[6]: Average done 0: Disable interrupt bit 1: Enable interrupt bit Bit[5]: AEC trigger 0: Disable interrupt bit 1: Enable interrupt bit Bit[4]: Reserved Bit[3]: MIPI turn around 0: Disable interrupt bit 1: Enable interrupt bit Bit[2]: MIPI low power contention detect 0: Disable interrupt bit 1: Enable interrupt bit Bit[1]: Reserved Bit[0]: BLC SOF 0: Disable interrupt bit 1: Enable interrupt bit

table 7-12 MCU registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3F03	MC READ INTERRUPT ADDRESS	0x70	RW	Bit[7:0]: Set high byte for SCCB address that will trigger interrupt when read
0x3F04	MC READ INTERRUPT ADDRESS	0x00	RW	Bit[7:0]: Set low byte for SCCB address that will trigger interrupt when read
0x3F05	MC WRITE INTERRUPT ADDRESS	0x70	RW	Bit[7:0]: Set high byte for SCCB address that will trigger interrupt when written
0x3F06	MC WRITE INTERRUPT ADDRESS	0x04	RW	Bit[7:0]: Set low byte for SCCB address that will trigger interrupt when written
0x3F0C	MC INTERRUPT0 STATUS	–	R	Interrupt0 Status Indicator Bit[7:6]: Reserved Bit[5]: ISP EOF Bit[4]: ISP SOF Bit[3]: Reserved Bit[2]: AWB done Bit[1]: VFIFO full Bit[0]: VFIFO empty
0x3F0D	MC INTERRUPT1 STATUS	–	R	Interrupt1 Status Indicator Bit[7]: AEC done Bit[6]: Average done Bit[5]: AEC trigger Bit[4]: Reserved Bit[3]: MIPI turn around Bit[2]: MIPI low power contention detect Bit[1]: Reserved Bit[0]: BLC SOF
0x3F0E	MC INTERRUPT WIDTH	0x01	RW	Bit[7:0]: Interrupt signal width

table 7-13 BLC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x09	RW	BLC Control 00 Bit[7:5]: Reserved Bit[4]: Manual digital gain enable Bit[3:2]: Reserved Bit[1]: freeze_en 0: BLC will be updated in some cases 1: BLC will be keep original value Bit[0]: blc_en BLC is enabling signal
0x4001~ 0x4002	BLC RESERVED	0x00	RW	Bit[7:0]: Reserved
0x4003	BLC CTRL 03	0x80	RW	BLC Control 03 Bit[1:0]: dig_gain_man Manual digital gain 00: 1x 01: 2x 10: 3x 11: 4x
0x4004~ 0x4005	BLC RESERVED	0x00	RW	Bit[7:0]: Reserved
0x4006	LONG EXPOSURE BLACK LEVEL TARGET	0x00	RW	Black Level Target for Long Exposure Bit[7:2]: Not used Bit[1:0]: l_blacklevel_target[9:8] Black level target for long exposure
0x4007	LONG EXPOSURE BLACK LEVEL TARGET	0x20	RW	Black Level Target for Long Exposure Bit[7:0]: l_blacklevel_target[7:0] Black level target for long exposure
0x4008~ 0x4009	NOT USED	–	–	Not Used
0x400A~ 0x400B	BLC RESERVED	0x00	RW	Bit[7:0]: Reserved
0x400C	BLC CTRL03	0x00	RW	Bit[7:1]: Reserved Bit[0]: blc_offset01[8]
0x400D~ 0x401C	BLC RESERVED	0x00	RW	Reserved

table 7-13 BLC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x401D	BLC FRAME CTRL	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: blc_en_mode 00: BLC always updates 01: BLC will update when the lowest 4 bits of sensor gain are changed 10: BLC will update when the highest 5 bits of sensor gain are changed 11: BLC will update only when the frame number is less than max. frame Bit[3:2]: Reserved Bit[1]: format_change_en If enabled and when format_change_flag_i is active, the frame count is cleared to update the BLC Bit[0]: frames_up_flag Clears the frame count to update BLC
0x401E	BLC FRAME	0xFF	RW	BLC is updated when the current frame number is less than this value

table 7-14 CIF registers

address	register name	default value	R/W	description
0x4100	CIF CTRL00	0x00	RW	CIF Control 00 Bit[7]: Source select 0: From external DVP input 1: From MIPI receiver Bit[6]: Debug mode Bit[5]: Reverse VSYNC polarity Bit[4]: Reverse HREF polarity Bit[3]: Reverse PCLK polarity Bit[2:0]: Debug mode

table 7-15 frame control registers

address	register name	default value	R/W	description
0x4201	FRAME CTRL00	0x00	RW	Control Passed Frame Number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode Bit[7:4]: Not used Bit[3:0]: Frame ON number
0x4202	FRAME CTRL01	0x00	RW	Control Masked Frame Number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode Bit[7:4]: Not used Bit[3:0]: Frame OFF number

table 7-16 format registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x4300	FORMAT CONTROL 00	0xF8	RW	Format Control 00 Bit[7:4]: Output format of formatter module 0x0: RAW Bit[3:0]: Output sequence 0x0: BGBG... / GRGR... 0x1: GBGB... / RGRG... 0x2: GRGR... / BGBG... 0x3: RGRG... / GBGB... 0x4~0xF: Not allowed 0x1: Y8 Bit[3:0]: Does not matter 0x2: YUV444/RGB888 (not available for full resolution) Bit[3:0]: Output sequence 0x0: YUVYUV..., or GBRGBR... 0x1: YVUYVU..., or GRBGRB... 0x2: UYVUYV..., or BGRBGR... 0x3: VYUVYU..., or RGBRGB... 0x4: UVYUVY..., or BRGBRG... 0x5: VUYVUY..., or RBGRBG... 0x6~0xE: Not allowed 0xF: UYVUYV..., or BGRBGR... 0x3: YUV422 Bit[3:0]: Output sequence 0x0: YUYV... 0x1: YVYU... 0x2: UYVY... 0x3: VYUY... 0x4~0xE: Not allowed 0xF: UYVY... 0x4: YUV420 Bit[3:0]: Output sequence 0x0: YYYY... / YUYV... 0x1: YYYY... / YVYU... 0x2: YYYY... / UYVY... 0x3: YYYY... / VYUY... 0x4: YUYV... / YYYY... 0x5: YVYU... / YYYY... 0x6: UYVY... / YYYY... 0x7: VYUY... / YYYY... 0x8~0xE: Not allowed 0xF: YYYY... / UYVY...

table 7-16 format registers (sheet 2 of 5)

address	register name	default value	R/W	description
				0x5: YUV420 (for MIPI only) Bit[3:0]: Output sequence 0x0~0xD: Not allowed 0xE: VYYVYY... / UYYUYY... 0xF: UYYUYY... / VYYVYY... 0x6: RGB565 Bit[3:0]: Output sequence 0x0: {b[4:0],g[5:3]}, {g[2:0],r[4:0]} 0x1: {r[4:0],g[5:3]}, {g[2:0],b[4:0]} 0x2: {g[4:0],r[5:3]}, {r[2:0],b[4:0]} 0x3: {b[4:0],r[5:3]}, {r[2:0],g[4:0]} 0x4: {g[4:0],b[5:3]}, {b[2:0],r[4:0]} 0x5: {r[4:0],b[5:3]}, {b[2:0],g[4:0]} 0x6~0xE: Not allowed 0xF: {g[2:0],b[4:0]}, {r[4:0],g[5:3]} 0x7: RGB555 format 1 Bit[3:0]: Output sequence 0x0: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} 0x1: {r[4:0],g[4:2]}, {g[1:0],1'b0,b[4:0]} 0x2: {g[4:0],r[4:2]}, {r[1:0],1'b0,b[4:0]} 0x3: {b[4:0],r[4:2]}, {r[1:0],1'b0,g[4:0]} 0x4: {r[4:0],b[4:2]}, {b[1:0],1'b0,g[4:0]} 0x5: {g[4:0],b[4:2]}, {b[1:0],1'b0,r[4:0]} 0x6~0xE: Not allowed 0xF: {g[1:0],1'b0,b[4:0]}, {r[4:0],g[4:2]} 0x8: RGB555 format 2 Bit[3:0]: Output sequence 0x0: {1'b0,b[4:0],g[4:3]}, {g[2:0],r[4:0]} 0x1: {1'b0,r[4:0],g[4:2]}, {g[2:0],b[4:0]} 0x2: {1'b0,g[4:0],r[4:2]}, {r[2:0],b[4:0]}

table 7-16 format registers (sheet 3 of 5)

address	register name	default value	R/W	description
				0x3: {1'b0,b[4:0],r[4:2]}, {r[2:0],g[4:0]} 0x4: {1'b0,r[4:0],b[4:2]}, {b[2:0],g[4:0]} 0x5: {1'b0,g[4:0],b[4:2]}, {b[2:0],r[4:0]} 0x6: {b[4:0],1'b0,g[4:3]}, {g[2:0],r[4:0]} 0x7: {r[4:0],1'b0,g[4:2]}, {g[2:0],b[4:0]} 0x8: {g[4:0],1'b0,r[4:2]}, {r[2:0],b[4:0]} 0x9: {b[4:0],1'b0,r[4:2]}, {r[2:0],g[4:0]} 0xA: {r[4:0],1'b0,b[4:2]}, {b[2:0],g[4:0]} 0xB: {g[4:0],1'b0,b[4:2]}, {b[2:0],r[4:0]} 0xC~0xF: Not allowed 0x9: RGB444 format 1 Bit[3:0]: Output sequence 0x0: {1'b0,b[3:0],2'h0,g[3]}, {g[2:0],1'b0,r[3:0]} 0x1: {1'b0,r[3:0],2'h0,g[3]}, {g[2:0],1'b0,b[3:0]} 0x2: {1'b0,g[3:0],2'h0,r[3]}, {r[2:0],1'b0,b[3:0]} 0x3: {1'b0,b[3:0],2'h0,r[3]}, {r[2:0],1'b0,g[3:0]} 0x4: {1'b0,r[3:0],2'h0,b[3]}, {b[2:0],1'b0,g[3:0]} 0x5: {1'b0,g[3:0],2'h0,b[3]}, {b[2:0],1'h0,r[3:0]} 0x6: {b[3:0],1'b0,g[3:1]}, {g[0],2'h0,r[3:0],1'b0} 0x7: {r[3:0],1'b0,g[3:1]}, {g[0],2'h0,b[3:0],1'b0} 0x8: {g[3:0],1'b0,r[3:1]}, {r[0],2'h0,b[3:0],1'b0} 0x9: {b[3:0],1'b0,r[3:1]}, {r[0],2'h0,g[3:0],1'b0} 0xA: {r[3:0],1'b0,b[3:1]}, {b[0],2'h0,g[3:0],1'b0} 0xB: {g[3:0],1'b0,b[3:1]}, {b[0],2'h0,r[3:0],1'b0} 0xC~0xE: Not allowed 0xF: {g[0],2'h2,b[3:0],1'b1}, {r[3:0],1'b1,g[3:1]}

table 7-16 format registers (sheet 4 of 5)

address	register name	default value	R/W	description
				0xA: RGB444 format 2 Bit[3:0]: Output sequence 0x0: {4'b0,b[3:0]}, {g[3:0],r[3:0]} 0x1: {4'b0,r[3:0]}, {g[3:0],b[3:0]} 0x2: {4'b0,b[3:0]}, {r[3:0],g[3:0]} 0x3: {4'b0,r[3:0]}, {b[3:0],g[3:0]} 0x4: {4'b0,g[3:0]}, {b[3:0],r[3:0]} 0x5: {4'b0,g[3:0]}, {r[3:0],b[3:0]} 0x6: {b[3:0],g[3:0],2'h0}, {r[3:0],b[3:0],2'h0,g[3:0],r[3:0],2'h0} 0x7: {r[3:0],g[3:0],2'h0}, {b[3:0],r[3:0],2'h0,g[3:0],b[3:0],2'h0} 0x8: {b[3:0],r[3:0],2'h0}, {g[3:0],b[3:0],2'h0,r[3:0],g[3:0],2'h0} 0x9: {r[3:0],b[3:0],2'h0}, {g[3:0],r[3:0],2'h0,b[3:0],g[3:0],2'h0} 0xA: {g[3:0],b[3:0],2'h0}, {r[3:0],g[3:0],2'h0,b[3:0],r[3:0],2'h0} 0xB: {g[3:0],r[3:0],2'h0}, {b[3:0],g[3:0],2'h0,r[3:0],b[3:0],2'h0} 0xC~0xF: Not allowed 0xB~0xE: Not allowed 0xF: Bypass formatter module, not recommended. Bit[3:0]: Output format 0x8: Raw 0x9: YUV422 0xA: YUV444 0xE: VYYVYY.../UYYUYY 0xF: UYYUYY.../VYYVYY
0x4301	FORMAT CTRL01	0x00	RW	Format Control 01 Bit[7:2]: Not used Bit[1:0]: YUV422 UV control 00: U/V is generated from average 01: U/V is generated from first pixel 11: U/V is generated from second pixel
0x4302	YMAX VALUE	0x03	RW	Set Y Max Clip Value High 2 Bits

table 7-16 format registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x4303	YMAX VALUE	0xFF	RW	Set Y Max Clip Value Low Byte
0x4304	YMIN VALUE	0x00	RW	Set Y Min Clip Value High 2 Bits
0x4305	YMIN VALUE	0x00	RW	Set Y Min Clip Value Low Byte
0x4306	UMAX VALUE	0x03	RW	Set U Max Clip Value High 2 Bits
0x4307	UMAX VALUE	0xFF	RW	Set U Max Clip Value Low Byte
0x4308	UMIN VALUE	0x00	RW	Set U Min Clip Value High 2 Bits
0x4309	UMIN VALUE	0x00	RW	Set U Min Clip Value Low Byte
0x430A	VMAX VALUE	0x03	RW	Set V Max Clip Value High 2 Bits
0x430B	VMAX VALUE	0xFF	RW	Set V Max Clip Value Low Byte
0x430C	VMIN VALUE	0x00	RW	Set V Min Clip Value High 2 Bits
0x430D	VMIN VALUE	0x00	RW	Set V Min Clip Value Low Byte

table 7-17 compression registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4400	COMPRESSION CTRL00	0x81	RW	Compression Control 00 Bit[7]: Input_format 0: YUV420 1: YUV422; Bit[6:0]: JFIFO read speed control
0x4401	COMPRESSION CTRL01	0x01	RW	Compression Control 01 Bit[7:4]: SFIFO output buffer speed control Bit[3]: Read SRAM enable when blanking 0: Disable 1: Enable Bit[2]: Read SRAM at first blanking 0: Disable 1: Enable Bit[1:0]: SFIFO read speed control
0x4402	COMPRESSION CTRL02	0x10	RW	Compression Control 02 Bit[7]: SFIFO output control mode 0: Controlled by HREF and valid data before scaled down 1: Controlled by input HREF and valid data Bit[6:4]: SOF control 001: Start at the first valid HREF 010: Start at the eighth valid HREF Bit[3:0]: SFIFO output buffer speed control at last stripe
0x4403	COMPRESSION CTRL03	0x33	RW	Compression Control 03 Bit[7]: Memory select 0: Select ROM QT 1: Select SRAM QT Bit[6]: Reserved Bit[5]: Enable zero stuff Bit[4]: Enable Huffman table output Bit[3]: Rounding enable for C Bit[2]: Rounding enable for Y Bit[1]: Input shift 128 select for C Bit[0]: Input shift 128 select for Y

table 7-17 compression registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4404	COMPRESSION CTRL04	0x24	RW	Compression Control 04 Bit[7]: jfifo_pwrdn Bit[6]: sfifo_pwrdn Bit[5]: Header output enable Bit[4]: Enable gated clock 0: Disable gated clock 1: Enable gated clock Bit[3]: Substitute 0xFF to 0xFE in QT Bit[2:0]: Quantization rounding bias Set value = Bias/8
0x4405	COMPRESSION CTRL05	0x40	RW	Compression Control 05 Bit[7:0]: QZ out truncate for Y
0x4406	COMPRESSION CTRL06	0x40	RW	Compression Control 06 Bit[7:0]: QZ out truncate for C
0x4407	COMPRESSION CTRL07	0x0C	RW	Compression Control 07 Bit[7]: Enable read QTA auto increment Bit[6]: Reserved Bit[5:0]: QS Quantization scale
0x4408	COMPRESSION ISI CTRL	0x00	RW	Bit[7]: Scalado mode enable 0: Normal 1: Insert 0xFFFF after EOB
0x4409	COMPRESSION CONTROL 09	0x4E	RW	Debug Mode
0x440A	COMPRESSION CTRL0A	0x4E	RW	Compression Control 0A Bit[7:0]: JFIFO output delay
0x440B~ 0x440C	COMPRESSION CONTROL 0B~0C	–	RW	Debug Mode
0x440D~ 0x440F	NOT USED	–	–	Not Used
0x4410	COMPRESSION QT DATA	0x00	RW	Bit[7:0]: QT data
0x4411	COMPRESSION QT ADDR	0x00	RW	Bit[7:0]: QT address
0x4412~ 0x4413	COMPRESSION ISI DATA	–	RW	Manual Control for Microcontroller Changing this value is not allowed
0x4414	COMPRESSION LENGTH	–	R	Compression Length High Byte
0x4415	COMPRESSION LENGTH	–	R	Compression Length Middle Byte
0x4416	COMPRESSION LENGTH	–	R	Compression Length Low Byte
0x4417	JFIFO OVERFLOW	–	R	Bit[7:1]: Not used Bit[0]: JFIFO overflow indicator

table 7-18 IFIFO control registers

address	register name	default value	R/W	description
0x4500	JPEG_CTRL00	0x7E	RW	Bit[7]: Reserved Bit[6]: smk_header_en Enable/disable the start marker header Bit[5]: length_header_en Enable/disable the length header Bit[4]: emk_header_en Enable/disable the end marker header Bit[3]: emk_header_en 0: Number will be data number of the data which comes before ififo_eoi 1: Number will be data number which comes before jpg_eoi Bit[2]: isi_bf_emb_en 0: isi data is output after embedding data 1: isi data is output before embedding data Bit[1]: smkd_mode Start marker header mode 0: Bit[15:8] of the start marker data is set by register and Bit[7:0] of the start marker data is the line counter 1: Start marker data is set by the register Bit[0]: thmbpt_mode Thumbnail packet point mode 0: Thumbnail packet point will follow the normal data 1: Thumbnail packet point will be before the footer
0x4501	IFIFO_RAMRD_OFF	0x00	RW	Bit[7:0]: Offset of the start read address of SRAM
0x4502	IFIFO_SMARKER	0xFF	RW	Bit[7:0]: 8 MSB of start marker
0x4503	IFIFO_SMARKER	0xFE	RW	Bit[7:0]: 8 LSB of start marker
0x4504	IFIFO_EMARKER	0xFF	RW	Bit[7:0]: 8 MSB of end marker
0x4505	IFIFO_EMARKER	0xFD	RW	Bit[7:0]: 8 LSB of end marker

table 7-19 VFIFO registers

address	register name	default value	R/W	description
0x4600	VFIFO CTRL00	0x80	RW	VFIFO Control 00 Bit[7:6]: Reserved Bit[5]: Compression output fixed height enable 0: In Compression mode2, compression height is different in each frame 1: In Compression mode2, compression height is fixed in each frame
0x4602	VFIFO HSIZE	0x04	RW	Compression Output Width High Byte
0x4603	VFIFO HSIZE	0x00	RW	Compression Output Width Low Byte
0x4604	VFIFO VSIZE	0x03	RW	Compression Output Height High Byte
0x4605	VFIFO HSIZE	0x00	RW	Compression Output Height Low Byte
0x4606	VFIFO CTRL06	0x02	RW	VFIFO Control 06 Bit[7:5]: Reserved Bit[4]: Compression oversize mask disable 0: When oversize occurs, the rest of the data will be masked 1: Disable oversize mask Bit[3:0]: Reserved
0x460C	VFIFO CTRL0C	0x20	RW	VFIFO Control 0C Bit[7:4]: Compression dummy data pad speed Bit[3]: Reserved Bit[2]: Footer disable Compression footer disable 0: In Compression mode2, a footer will be added in the last six bytes of each frame 1: Disable footer Bit[1]: PCLK manual enable 0: DVP PCLK divider is controlled by auto mode 1: DVP PCLK divider is controlled by 0x3815[4:0] Bit[0]: Reserved

table 7-20 DVP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4700~ 0x4710	DVP CONTROL	–	RW	DVP Control Registers
0x4711	PAD LEFT CTRL	0x00	RW	HSYNC Mode Left Padding Pixel Count Adds padding data at start of a line
0x4712	PAD RIGHT CTRL	0x00	RW	HSYNC Mode Right Padding Pixel Count Adds padding data at end of a line
0x4713	JPG MODE SELECT	0x02	RW	Bit[7:3]: Reserved Bit[2:0]: Compression mode select 001: Compression mode 1 010: Compression mode 2 011: Compression mode 3 100: Compression mode 4 101: Compression mode 5 110: Compression mode 6
0x4714	DVP CONTROL	–	RW	DVP Control Register
0x4715	656 DUMMY LINE	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: CCIR656 dummy line number Controls dummy line number at beginning of the frame
0x4716~ 0x471A	DVP CONTROL	–	RW	DVP Control Registers
0x471B	HSYNC CTRL00	0x02	RW	Bit[7:1]: Reserved Bit[0]: HSYNC mode enable
0x471C	DVP CONTROL 1C	0xD0	RW	Debug Mode Changing this value is not allowed
0x471D	DVP CONTROL 1D	0x00	RW	Bit[7:6]: Not used Bit[5:2]: Debug mode Changing this value is not recommended Bit[1:0]: VSYNC option 00: VSYNC extend when dummy line is inserted 01: Dummy line is inserted after VSYNC pulse 10: Dummy line is inserted before VSYNC pulse 11: Not allowed
0x471E~ 0x472F	DVP CONTROL	–	RW	DVP Control Registers
0x4730	CCIR656 CTRL00	0x00	RW	Bit[7:1]: Reserved Bit[0]: CCIR656 mode enable

table 7-20 DVP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4731	DVP CONTROL	–	RW	DVP Control Registers
0x4732	CCIR656 FS	0x01	RW	CCIR656 Sync Code Frame start
0x4733	CCIR656 FE	0x0F	RW	CCIR656 Sync Code Frame end
0x4734	CCIR656 LS	0x00	RW	CCIR6656 Sync Code Line start
0x4735	CCIR656 LE	0x00	RW	CCIR656 Sync Code Line end
0x4740	POLARITY CTRL00	0x20	RW	DVP Output Polarity Control Bit[7:6]: Reserved Bit[5]: PCLK polarity 0: Latch at rising edge 1: Latch at falling edge Bit[4]: Reserved Bit[3]: Gate PCLK under VSYNC Bit[2]: Gate PCLK under HREF Bit[1]: HREF polarity 0: Active low 1: Active high Bit[0]: VSYNC polarity 0: Active low 1: Active high
0x4741	TEST PATTERN	0x00	RW	Bit[7:5]: Not used Bit[4:3]: Debug mode Changing this value is not recommended Bit[2]: Test pattern enable Bit[1]: Test pattern select 0: Output test pattern 0 1: Output test pattern 1 Bit[0]: test pattern 8 bit/10bit 0: 10-bit test pattern 1: 8-bit test pattern
0x4742~ 0x4744	DVP CONTROL 42~44	–	RW	Debug Mode Changing these values is not allowed
0x4745	DATA ORDER	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Output data order 00: DATA[9:0] output to pin D[9:0] 01: DATA[9:0] output to pin {D[7:0], D[9:8]} 10: DATA[9:0] output to pin {D[1:0], D[9:2]} 11: Not allowed

table 7-21 MIPI transmitter (TX) registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x4800	MIPI CTRL 00	0x04	RW	MIPI Control 00 Bit[7]: Not used Bit[6]: Debug mode Changing this value is not allowed Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Lane select 0: Use lane1 as default data lane 1: Use lane2 as default data lane Bit[2]: Idle status 0: MIPI bus will be LP00 when no packet to transmit 1: MIPI bus will be LP11 when no packet to transmit Bit[1:0]: Debug mode Changing this value is not allowed
0x4801	MIPI CTRL 01	0x03	RW	MIPI Control 01 Bit[7]: Long packet data type manual enable 0: Use mipi_dt 1: Use dt_man_o as long pkt dt Bit[6]: Short packet data type manual enable 1: Use dt_spkt as short pkt dt Bit[5]: Short packet WORD COUNTER manual enable 0: Use frame counter or line counter 1: Select spkt_wc_reg_o Bit[4]: PH bit order for ECC 0: {DI[7:0],WC[7:0],WC[15:8]} 1: {DI[0:7],WC[0:7],WC[8:15]} Bit[3]: PH byte order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[2]: PH byte order2 for ECC 0: {DI,WC} 1: {WC,DI} Bit[1:0]: Debug mode Changing this value is not allowed
0x4802	MIPI CTRL 02	0x00	RW	MIPI Control 02 Bit[7:0]: Reserved

table 7-21 MIPI transmitter (TX) registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x4803	MIPI CTRL 03	0x5F	RW	MIPI Control 03 Bit[7:4]: Debug mode Changing this value is not allowed Bit[3]: Enable LP CD when HS TX for lane1 0: Disable 1: Enable Bit[2]: Enable LP CD when HS TX for lane2 0: Disable 1: Enable Bit[1]: Enable LP CD when LP TX for lane2 0: Disable 1: Enable Bit[0]: Enable LP CD when LP TX for lane1 0: Disable 1: Enable
0x4804	MIPI CTRL 04	0x8D	RW	MIPI Control 04 Bit[7:5]: Debug mode Changing this value is not allowed Bit[4]: Enable MIPI LP RX to read/write registers 0: Disable - RX LP data will write to VFIFO 1: Enable Bit[3]: Address read/write register will auto add 1 1: Enable Bit[2]: LP TX lane select 0: Select lane1 to transmit LP data 1: Select lane2 to transmit LP data Bit[1:0]: Debug mode Changing this value is not allowed
0x4805	MIPI CTRL 05	0x10	RW	MIPI Control 05 Bit[7]: MIPI lane1 disable 1: Disable MIPI data lane1, lane1 will be LP00 Bit[6]: MIPI lane1 disable 1: Disable MIPI data lane1, lane1 will be LP00 Bit[5:3]: Reserved Bit[2]: MIPI read/write registers disable 1: Disable MIPI access to SRB Bit[1:0]: Debug mode Changing this value is not allowed
0x4806~ 0x480F	NOT USED	–	–	Not Used
0x4810	MAX FCNT H	0xFF	RW	High Byte of Max Frame Counter of Frame Sync Short Packet
0x4811	MAX FCNT L	0xFF	RW	Low Byte of Max Frame Counter of Frame Sync Short Packet

table 7-21 MIPI transmitter (TX) registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x4812	MIN SPKT WC REG H	0x00	RW	High Byte of Manual Short Packet Word Counter
0x4813	MIN SPKT WC REG L	0x00	RW	Low Byte of Manual Short Packet Word Counter
0x4814	MIPI CTRL 14	0x2A	RW	MIPI Control 14 Bit[7:6]: Virtual channel of MIPI packet Bit[5:0]: Data type manual
0x4815	MIPI SPKT DT	0x00	RW	Manual Data Type for Short Packet
0x4816~ 0x4817	NOT USED	–	–	Not Used
0x4818	MIN HS ZERO H	0x00	RW	High Byte of Minimum Value of hs_zero Unit: ns
0x4819	MIN HS ZERO L	0x96	RW	Low Byte of Minimum Value of hs_zero hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	MIN MIPI HS TRAIL H	0x00	RW	High Byte of Minimum Value of hs_trail Unit: ns
0x481B	MIN MIPI HS TRAIL L	0x3C	RW	Low Byte of Minimum Value of hs_trail hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	MIN MIPI CLK ZERO H	0x01	RW	High Byte of Minimum Value of clk_zero
0x481D	MIN MIPI CLK ZERO L	0x86	RW	Low Byte of Minimum Value of clk_zero clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	MIN MIPI CLK PREPARE H	0x00	RW	High Byte of Minimum Value of clk_prepare Unit: ns
0x481F	MIN MIPI CLK PREPARE L	0x3C	RW	Low Byte of Minimum Value of clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	MIN CLK POST H	0x00	RW	High Byte of Minimum Value of clk_post Unit: ns
0x4821	MIN CLK POST L	0x56	RW	Low Byte of Minimum Value of clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x4822	MIN CLK TRAIL H	0x00	RW	High Byte of Minimum Value of clk_trail Unit: ns
0x4823	MIN CLK TRAIL L	0x3C	RW	Low Byte of Minimum Value of clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	MIN LPX PCLK H	0x00	RW	High Byte of Minimum Value of lpx_p, unit ns

table 7-21 MIPI transmitter (TX) registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x4825	MIN LPX PCLK L	0x32	RW	Low Byte of Minimum Value of lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	MIN HS PREPARE H	0x00	RW	High Byte of Minimum Value of hs_prepare Unit: ns
0x4827	MIN HS PREPARE L	0x32	RW	Low Byte of Minimum Value of hs_prepare hs_prepare_real = hs_prepare_min_o + Tui*ui_hs_prepare_min_o
0x4828	MIN HS EXIT H	0x00	RW	High Byte of Minimum Value of hs_exit Unit: ns
0x4829	MIN HS EXIT L	0x64	RW	Low Byte of Minimum Value of hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	MIN HS ZERO/UI	0x05	RW	Minimum UI Value of hs_zero Unit: UI
0x482B	MIN HS TRAIL/UI	0x04	RW	Minimum UI Value of hs_trail Unit: UI
0x482C	MIN CLK ZERO/UI	0x00	RW	Minimum UI Value of clk_zero Unit: UI
0x482D	MIN CLK PREPARE/UI	0x00	RW	Minimum UI Value of clk_prepare Unit: UI
0x482E	MIN CLK POST/UI	0x34	RW	Minimum UI Value of clk_post Unit: UI
0x482F	MIN CLK TRAIL/UI	0x00	RW	Minimum UI Value of clk_trail Unit: UI
0x4830	MIN LPX PCLK/UI	0x00	RW	Minimum UI Value of lpx_p (pclk2x domain) Unit: UI
0x4831	MIN HS PREPARE/UI	0x04	RW	Minimum UI Value of hs_prepare Unit: UI
0x4832	MIN HS EXIT/UI	0x00	RW	Minimum UI Value of hs_exit Unit: UI
0x4833	MIN MIPI REG H	0x00	RW	High byte of mipi_reg_min Address range of MIPI read/write registers is between mipi_reg_min and mipi_reg_max
0x4834	MIN MIPI REG L	0x00	RW	Low byte of mipi_reg_min
0x4835	MAX MIPI REG H	0xFF	RW	High byte of mipi_reg_max
0x4836	MAX MIPI REG L	0xFF	RW	Low byte of mipi_reg_max
0x4837	PCLK PERIOD	0x10	RW	Period of Pixel Clock pclk_div=1 and 1-bit decimal

table 7-21 MIPI transmitter (TX) registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x4838	WKUP DLY	0x02	RW	Wakeup Delay for MIPI (MARK1 state)/2^{12}
0x4839	NOT USED	–	–	Not Used
0x483A	DIR DELAY	0x08	RW	Debug Mode Changing this value is not allowed
0x483B	MIPI GPIO CTRL	0x33	RW	Bit[7]: Lane1 GPIO select 1: Select lane1 as GPIO Bit[6]: GPIO direction for lane1 0: Input 1: Output Bit[5]: Low power P value for lane1 Bit[4]: Low power N value for lane1 Bit[3]: Lane2 GPIO select 1: Select lane2 as GPIO Bit[2]: GPIO direction for lane2 0: Input 1: Output Bit[1]: Low power P value for lane2 Bit[0]: Low power N value for lane2
0x483C	MIPI CTRL 33	0x4F	RW	Bit[7:4]: Global timing for t_lpx Unit: sclk cycle Bit[3:0]: Global timing for t_clk_pre Unit: pixel clock cycle
0x483D	TA GO/Tp	0x10	RW	Unit: sclk cycle
0x483E	TA SURE/Tp	0x06	RW	Unit: sclk cycle
0x483F	TA GET/Tp	0x14	RW	Unit: sclk cycle
0x4840~ 0x484F	NOT USED	–	–	Not Used
0x4850~ 0x4854	MIPI CONTROL 50~54	–	RW	Debug Mode Changing these values is not allowed
0x4855~ 0x485F	NOT USED	–	–	Not Used
0x4860	MIPI CTRL 60	–	R	Bit[7:1]: Not used Bit[0]: MIPI read/write register enable (this register is MIPI access only) 0: Enable MIPI read/write registers 1: Disable MIPI read/write registers
0x4861~ 0x4864	MIPI CONTROL 61~64	–	RW	Debug Mode Changing these values is not allowed

table 7-21 MIPI transmitter (TX) registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x4865	LP TX STATUS	–	R	Bit[7:6]: Not used Bit[5]: MIPI LP RX busy 1: MIPI_LP_RX receiving LP data Bit[4]: MIPI LP TX busy 1: MIPI_TX_LP_TX is busy to send LP data Bit[3]: MIPI low power input for lane1 P Bit[2]: MIPI low power input for lane1 N Bit[1]: MIPI low power input for lane2 P Bit[0]: MIPI low power input for lane2 N

table 7-22 ISP frame control registers

address	register name	default value	R/W	description
0x4901	FRAME CTRL00	0x00	RW	Control passed frame number When both on and off number set to 0x00, frame control is in bypass mode. Bit[7:4]: Reserved Bit[3:0]: Frame ON number
0x4902	FRAME CTRL01	0x00	RW	Control masked frame number When both on and off number set to 0x00, frame control is in bypass mode. Bit[7:4]: Reserved Bit[3:0]: Frame OFF number

table 7-23 MIPI receiver (RX) registers

address	register name	default value	R/W	description
0x4A00	MIPI RX CTRL00	0x00	RW	MIPI RX Control 00 Bit[7:2]: Reserved Bit[1:0]: mipi_rx_vc MIPI RX virtual channel ID
0x4A01	MIPI RX CTRL01	0x06	RW	MIPI RX Control 01 Bit[7:3]: Reserved Bit[2:1]: ph_order Packet header options 00: {data_id, byte_num[7:0], byte_num[15:8]} 01: {data_id, byte_num} 10: {byte_num[7:0], byte_num[15:8], data_id} 11: {byte_num, data_id} Bit[0]: line_sync_sel 0: Input stream without line sync short packet 1: Input stream with line sync short packet
0x4A02	MIPI RX CTRL02	0x04	RW	Delay Between VSYNC Positive Edge and FE
0x4A03	MIPI RX CTRL03	0x04	RW	Delay Between VSYNC Negative Edge and FS
0x4A04	MIPI CONTROL	–	RW	MIPI Control Registers
0x4A05	MIPI RX PHY CTRL00	0x10	RW	MIPI RX PHY Control 1 Bit[7:6]: Reserved Bit[5]: mipi_rx_ihalf Bit[4:2]: Reserved Bit[1:0]: cmrx_max
0x4A06	MIPI RX PHY CTRL01	0x00	RW	MIPI RX PHY Control 2 Bit[7:6]: dtm_dly Bit[5:4]: dst_dly Bit[3:2]: ctm_dly Bit[1:0]: cst_dly

table 7-24 ISP top control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0xDF	RW	ISP Control 00 (0: disable; 1: enable) Bit[7]: LENC correction enable Bit[6]: Gamma (in YUV domain) enable Bit[5]: Raw gamma enable Bit[4]: Even odd removing enable Bit[3]: De-noise enable Bit[2]: Black pixel cancellation enable Bit[1]: White pixel cancellation enable Bit[0]: Color interpolation enable
0x5001	ISP CONTROL 01	0x4F	RW	ISP Control 01 (0: disable; 1: enable) Bit[7]: Special digital effect enable Bit[6]: UV adjust enable Bit[5]: Scale vertical enable Bit[4]: Scale horizontal enable Bit[3]: Line stretch enable Bit[2]: UV average enable Bit[1]: Color matrix enable Bit[0]: Auto white balance enable
0x5002	ISP CONTROL 02	0xE0	RW	ISP Control 02 (0: disable; 1: enable) Bit[7]: Scale for thumbnail enable Bit[6:5]: Reserved Bit[4]: Dither enable Bit[3]: YUV to RGB enable Bit[2]: Subsample at horizontal enable Bit[1:0]: Not used
0x5003	ISP CONTROL 03	0xA8	RW	ISP Control 03 Bit[7:4]: Reserved Bit[3]: YUV to YCbCr for YUVCLIP enable 0: Disable 1: Enable Bit[2]: YUV422 input enable 0: Disable 1: Enable Bit[1]: Draw window for AFC enable 0: Disable 1: Enable Bit[0]: Reserved
0x5004	ISP RESERVED	0x08	RW	Reserved

table 7-24 ISP top control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x5005	ISP CONTROL 05	0xDC	RW	ISP Control 05 Bit[7]: Raw gamma bias plus enable 0: Disable 1: Enable Bit[6]: Raw gamma bias ON enable 0: Disable 1: Enable Bit[5]: UV average old style enable 0: Disable 1: Enable Bit[4]: Auto white balance bias ON enable 0: Disable 1: Enable Bit[3]: LENC correction bias plus enable 0: Disable 1: Enable Bit[2]: LENC correction bias ON enable 0: Disable 1: Enable Bit[1]: UV swap enable for YUV422 to YUV444 0: Do not swap 1: Swap Bit[0]: Y swap enable for YUV422 to YUV444 0: Do not swap 1: Swap
0x5006~ 0x501B	ISP RESERVED	–	RW	Reserved
0x501C	HORIZON SUBSAMPLE MODE	0x00	RW	Mode Selection for Horizontal Subsampling when 0x5002[2]=1 Bit[7:6]: B channel mode 00: Average mode x1: Not allowed 10: Skip mode Bit[5:4]: Gb channel mode 00: Average mode x1: Not allowed 10: Skip mode Bit[3:2]: Gr channel mode 00: Average mode x1: Not allowed 10: Skip mode Bit[1:0]: R channel mode 00: Average mode x1: Not allowed 10: Skip mode

table 7-24 ISP top control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x501D	ISP RESERVED	0x02	RW	Reserved
0x501E	RGB DITHER CONTROL	0x40	RW	RGB Dither Control Bit[7]: Debug mode Changing this value is not allowed Bit[6]: Dither register control selection enable 0: From register control 1: From system control Bit[5:4]: R channel register control when 0x501E[6]=0 00: Not allowed 01: RGB444 10: RGB565/555 11: Not allowed Bit[3:2]: G channel register control when 0x501E[6]=0 00: Not allowed 01: RGB444 10: RGB565/555 11: Not allowed Bit[1:0]: B channel register control when 0x501E[6]=0 00: Not allowed 01: RGB444 10: RGB565/555 11: Not allowed
0x501F	FORMAT MUX CONTROL	0x04	RW	Format Mux Control Bit[7:6]: Format option Changing this value is not recommended Bit[5]: External Y swap enable Bit[4]: UV selection Bit[3]: UV fixed enable Bit[2:0]: Format selection 000: ISP YUV 001: ISP RGB 010: ISP YUV 011: ISP raw 100: Internal cif raw 101: External CIF raw 110: External CIF YUV422 bypass enable
0x5020~ 0x5024	ISP RESERVED	–	RW	Reserved

table 7-24 ISP top control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x5025	ISP CONTROL 37	0x80	RW	ISP Control 37 Bit[7:3]: Debug mode Changing this value is not allowed Bit[2]: AFC statistic selection 0: After even 1: snr_input Bit[1:0]: Avg statistic selection 00: raw_i 01: rawgma 10: yuvgma 11: isp_y
0x5026	ISP RESERVED	–	RW	Reserved
0x5027	DRAW WINDOW CONTROL 00	0x02	RW	Draw Window Control 00 Bit[7:1]: Debug mode Changing this value is not allowed Bit[0]: Draw window control 0: No fix 1: Fixed Y
0x5028	DRAW WINDOW LEFT POSITION CONTROL	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Draw window left[11:8] high byte
0x5029	DRAW WINDOW LEFT POSITION CONTROL	0x6C	RW	Bit[7:0]: Draw window left[7:0] low byte
0x502A	DRAW WINDOW RIGHT POSITION CONTROL	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Draw window right[11:8] high byte
0x502B	DRAW WINDOW RIGHT POSITION CONTROL	0xAC	RW	Bit[7:0]: Draw window right[7:0] low byte
0x502C	DRAW WINDOW TOP POSITION CONTROL	0x02	RW	Bit[7:4]: Not used Bit[2:0]: Draw window top[10:8] high byte
0x502D	DRAW WINDOW TOP POSITION CONTROL	0x91	RW	Bit[7:0]: Draw window top[7:0] low byte
0x502E	DRAW WINDOW BOTTOM POSITION CONTROL	0x03	RW	Bit[7:4]: Not used Bit[2:0]: Draw window bottom[10:8] high byte
0x502F	DRAW WINDOW BOTTOM POSITION CONTROL	0x81	RW	Bit[7:0]: Draw window bottom[7:0] low byte
0x5030	DRAW WINDOW HORIZONTAL BOUNDARY WIDTH CONTROL	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Draw window horizontal boundary width[11:8] high byte

table 7-24 ISP top control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x5031	DRAW WINDOW HORIZONTAL BOUNDARY WIDTH CONTROL	0x14	RW	Bit[7:0]: Draw window horizontal boundary width[7:0] low byte
0x5032	DRAW WINDOW VERTICAL BOUNDARY WIDTH CONTROL	0x00	RW	Bit[7:4]: Not used Bit[2:0]: Draw window vertical boundary width[10:8] high byte
0x5033	DRAW WINDOW VERTICAL BOUNDARY WIDTH CONTROL	0x14	RW	Bit[7:0]: Draw window vertical boundary width[7:0] low byte
0x5034	DRAW WINDOW Y CONTROL	0x80	RW	Bit[7:0]: Fixed Y for draw window
0x5035	DRAW WINDOW U CONTROL	0x2A	RW	Bit[7:0]: Fixed U for draw window
0x5036	DRAW WINDOW V CONTROL	0x14	RW	Bit[7:0]: Fixed V for draw window
0x5037~ 0x503C	ISP RESERVED	–	RW	Reserved
0x503D	PRE ISP TEST SETTING 1	0x00	RW	Bit[7]: pre_isp_test_en_i 0: Test disable 1: Color bar enable Bit[6]: Reserved Bit[5:4]: pre_isp_bar_style_i 00: Standard 8 color bar 01: Gradual change at vertical mode 1 10: Gradual change at horizontal 11: Gradual change at vertical mode 2 Bit[3]: Reserved Bit[2]: pre_isp_rolling_i 0: Disable rolling 1: Rolling enable Bit[1]: pre_isp_isp_test_i 0: Normal 1: Fixed low 2 bits to 2'b0 Bit[0]: pre_isp_squ_size_i 0: Disable 1: Test pattern square size enable

table 7-24 ISP top control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x503E	PRE ISP TEST SETTING 2	0x00	RW	Bit[7]: Reserved Bit[6:4]: pre_isp_seed_i 001: Random data pattern generated seed enable Bit[3]: pre_isp_squ_bw_i 1: Test pattern square black/white mode enable Bit[2]: pre_isp_trans_i 1: Add test pattern on image data Bit[1:0]: pre_isp_test_sel_i 00: Color bar 01: Random data 10: Square data 11: Black image
0x503F	PRE ISP TEST SETTING 3	0x00	RW	Bit[7:5]: Reserved Bit[4]: pre_isp_sw_en 0: Disable 1: Data sequence switch enable Bit[3]: pre_isp_sw_b_en 0: Disable 1: B1G2B3G4 is changed to B3G2B1G4 Bit[2]: pre_isp_sw_gb_en 0: Disable 1: B1G2B3G4 is changed to B1G4B3G2 Bit[1]: pre_isp_sw_gr_en 0: Disable 1: G1R2G3R4 is changed to G3R2G1R4 Bit[0]: pre_isp_sw_r_en 0: Disable 1: G1R2G3R4 is changed to G1R4G3R2
0x5080	EVEN CTRL 00	0x40	RW	Bit[7:0]: Threshold Threshold for the difference between the adjacent pixel in the same channel.

table 7-25 AWB registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5180	AWB CONTROL 00	0xFF	RW	AWB Control 00 Bit[7:0]: awb_b_block
0x5181	AWB CONTROL 01	0x58	RW	AWB Control 01 Bit[7:6]: step_local Bit[5:4]: step_fast Bit[3]: slop_8x Bit[2]: slop_4x Bit[1]: one_zone Bit[0]: avg_all
0x5182	AWB CONTROL 02	0x11	RW	AWB Control 02 Bit[7:4]: max_local_cnt Bit[3:0]: max_fast_cnt
0x5183	AWB CONTROL 03	0x90	RW	AWB Control 03 Bit[7]: awb_simple_enable 0: awb_advanced 1: awb_simple Bit[6]: Debug mode Changing this value is not recommended Bit[5]: awb_preset Bit[4]: awb_simf Bit[3:0]: Debug mode Changing this value is not recommended
0x5184	AWB CONTROL 04	0x25	RW	AWB Control 04 Bit[7:6]: count_area_selection Bit[5]: g_en Bit[4:2]: count_limit_control Bit[1:0]: cnt_th
0x5185	AWB CONTROL 05	0x24	RW	AWB Control 05 Bit[7:4]: stable_range_us Threshold for unstable to stable change Bit[3:0]: stable_range_s Threshold for stable to unstable change
0x5186	AWB CONTROL 06	0x10	RW	AWB Control 06 Bit[7:0]: awb_s
0x5187	AWB CONTROL 07	0x10	RW	AWB Control 07 Bit[7:0]: awb_ec
0x5188	AWB CONTROL 08	0x10	RW	AWB Control 08 Bit[7:0]: awb_fc
0x5189	AWB CONTROL 09	0x40	RW	AWB Control 09 Bit[7:0]: awb_x0

table 7-25 AWB registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x518A	AWB CONTROL 10	0x40	RW	AWB Control 10 Bit[7:0]: awb_y0
0x518B	AWB CONTROL 11	0x00	RW	AWB Control 11 Bit[7:0]: awb_kx
0x518C	AWB CONTROL 12	0x00	RW	AWB Control 12 Bit[7:0]: awb_ky
0x518D	AWB CONTROL 13	0x00	RW	AWB Control 13 Bit[7:0]: day_limit
0x518E	AWB CONTROL 14	0x00	RW	AWB Control 14 Bit[7:0]: a_limit
0x518F	AWB CONTROL 15	0x20	RW	AWB Control 15 Bit[7:0]: day_split
0x5190	AWB CONTROL 16	0x20	RW	AWB Control 16 Bit[7:0]: a_split
0x5191	AWB CONTROL 17	0xFF	RW	AWB Control 17 Bit[7:0]: awb_top_limit
0x5192	AWB CONTROL 18	0x00	RW	AWB Control 18 Bit[7:0]: awb_bot_limit
0x5193	AWB CONTROL 19	0xF0	RW	AWB Control 19 Bit[7:0]: red_limit
0x5194	AWB CONTROL 20	0xF0	RW	AWB Control 20 Bit[7:0]: green_limit
0x5195	AWB CONTROL 21	0xF0	RW	AWB Control 21 Bit[7:0]: blue_limit
0x5196	AWB CONTROL 22	0x03	RW	AWB Control 22 Bit[7]: AWB gain manual enable Bit[6]: Reserved Bit[5]: awb_freeze Bit[4]: Debug mode Changing this value is not recommended Bit[3:2]: awb_sim_selection 00: awb_simple from after awb_gain 01: awb_simple from after raw_gma 10: Not allowed 11: awb_simple from after awb_gain Bit[1]: fast_enable Bit[0]: awb_bias_stat
0x5197	AWB CONTROL 23	0x02	RW	AWB Control 23 Bit[7:0]: local_limit

table 7-25 AWB registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5198	AWB R GAIN MANUAL	0x00	RW	Bit[7:4]: Not used Bit[3:0]: awb_r_gain_m[11:8] high byte (functions when 0x5196[7]=1)
0x5199	AWB R GAIN MANUAL	0x00	RW	Bit[7:0]: awb_r_gain_m[7:0] low byte (functions when 0x5196[7]=1)
0x519A	AWB G GAIN MANUAL	0x00	RW	Bit[7:4]: Not used Bit[3:0]: awb_g_gain_m[11:8] high byte (functions when 0x5196[7]=1)
0x519B	AWB G GAIN MANUAL	0x00	RW	Bit[7:0]: awb_g_gain_m[7:0] low byte (functions when 0x5196[7]=1)
0x519C	AWB B GAIN MANUAL	0x00	RW	Bit[7:4]: Not used Bit[3:0]: awb_b_gain_m[11:8] high byte (functions when 0x5196[7]=1)
0x519D	AWB B GAIN MANUAL	0x00	RW	Bit[7:0]: awb_b_gain_m[7:0] low byte (functions when 0x5196[7]=1)
0x519E	AWB CONTROL 30	0x00	RW	AWB Control 30 Bit[7:4]: Reserved Bit[3]: local_limit_sel Bit[2]: simple_stable_sel Bit[1:0]: awb_reg_read_sel 00: awb finish 01: vsync_i 10: Anytime 11: Anytime
0x519F	AWB CURRENT R GAIN	–	R	Bit[7:4]: Not used Bit[3:0]: current_r_setting[11:8] high byte
0x51A0	AWB CURRENT R GAIN	–	R	Bit[7:0]: current_r_setting[7:0] low byte
0x51A1	AWB CURRENT G GAIN	–	R	Bit[7:4]: Not used Bit[3:0]: current_g_setting[11:8] high byte
0x51A2	AWB CURRENT G GAIN	–	R	Bit[7:0]: current_g_setting[7:0] low byte
0x51A3	AWB CURRENT B GAIN	–	R	Bit[7:4]: Not used Bit[3:0]: current_b_setting[11:8]
0x51A4	AWB CURRENT B GAIN	–	R	Bit[7:0]: current_b_setting[7:0]
0x51A5	AWB AVERAGE B	–	R	Bit[7:0]: average r[9:2]
0x51A6	AWB AVERAGE B	–	R	Bit[7:0]: average g[9:2]
0x51A7	AWB AVERAGE B	–	R	Bit[7:0]: average b[9:2]

table 7-26 de-noise (DNS) registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5280	DNS CONTROL 10	0x04	RW	DNS Control 10 Bit[3:0]: noise y_a De-noise weight for Y
0x5281	DNS CONTROL 11	0x08	RW	DNS Control 11 Bit[4:0]: noise uv_a De-noise weight for UV
0x5282	DNS CONTROL 12	0x00	RW	DNS Control 12 Bit[0]: De-noise manual setting enable
0x5283	NOISE Y	0x02	RW	Noise Y De-noise level for Y when **0x5282**[0]=1
0x5284	NOISE U	0x00	RW	Noise U High Byte De-noise level for U when **0x5282**[0]=1
0x5285	NOISE U	0x02	RW	Noise U High Byte De-noise level for U when **0x5282**[0]=1
0x5286	NOISE V	0x00	RW	Noise V High Byte De-noise level for V when **0x5282**[0]=1
0x5287	NOISE V	0x02	RW	Noise V High Byte De-noise level for V when **0x5282**[0]=1
0x5288	DNS EDGETHRE	0x06	RW	DNS Edge Threshold Edge threshold for DNS when **0x5282**[0]=1
0x5289	DNS GBGR EXTRA	0x04	RW	DNS GbGr Extra GbGr extra level for DNS
0x528A	NOISE Y LIST 0	0x02	RW	Noise Y List 0 Noise Y curve position 0 for automatic noise Y computation according sensor gain
0x528B	NOISE Y LIST 1	0x04	RW	Noise Y List 1 Noise Y curve position 1 for automatic noise Y computation according sensor gain
0x528C	NOISE Y LIST 2	0x08	RW	Noise Y List 2 Noise Y curve position 2 for automatic noise Y computation according sensor gain
0x528D	NOISE Y LIST 3	0x14	RW	Noise Y List 3 Noise Y curve position 3 for automatic noise Y computation according sensor gain

table 7-26 de-noise (DNS) registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x528E	NOISE Y LIST 4	0x1E	RW	Noise Y List 4 Noise Y curve position 4 for automatic noise Y computation according sensor gain
0x528F	NOISE Y LIST 5	0x28	RW	Noise Y List 5 Noise Y curve position 5 for automatic noise Y computation according sensor gain
0x5290	NOISE Y LIST 6	0x32	RW	Noise Y List 6 Noise Y curve position 6 for automatic noise Y computation according sensor gain
0x5291	DNS DUMMY	0x00	RW	DNS Dummy
0x5292	NOISE UV LIST 0	0x00	RW	Noise UV List 0 Noise UV curve position 0 for automatic noise U / noise V computation according to sensor gain
0x5293	NOISE UV LIST 0	0x02	RW	Noise UV List 0 Noise UV curve position 0 for automatic noise U / noise V computation according to sensor gain
0x5294	NOISE UV LIST 1	0x00	RW	Noise UV List 1 Noise UV curve position 1 for automatic noise U / noise V computation according to sensor gain
0x5295	NOISE UV LIST 1	0x04	RW	Noise UV List 1 Noise UV curve position 1 for automatic noise U / noise V computation according to sensor gain
0x5296	NOISE UV LIST 2	0x00	RW	Noise UV List 2 Noise UV curve position 2 for automatic noise U / noise V computation according to sensor gain
0x5297	NOISE UV LIST 2	0x0C	RW	Noise UV List 2 Noise UV curve position 2 for automatic noise U / noise V computation according to sensor gain
0x5298	NOISE UV LIST 3	0x00	RW	Noise UV List 3 Noise UV curve position 3 for automatic noise U / noise V computation according to sensor gain

table 7-26 de-noise (DNS) registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5299	NOISE UV LIST 3	0x28	RW	Noise UV List 3 Noise UV curve position 3 for automatic noise U / noise V computation according to sensor gain
0x529A	NOISE UV LIST 4	0x00	RW	Noise UV List 4 Noise UV curve position 4 for automatic noise U / noise V computation according to sensor gain
0x529B	NOISE UV LIST 4	0x32	RW	Noise UV List 4 Noise UV curve position 4 for automatic noise U / noise V computation according to sensor gain
0x529C	NOISE UV LIST 5	0x00	RW	Noise UV List 5 Noise UV curve position 5 for automatic noise U / noise V computation according to sensor gain
0x529D	NOISE UV LIST 5	0x3C	RW	Noise UV List 5 Noise UV curve position 5 for automatic noise U / noise V computation according to sensor gain
0x529E	NOISE UV LIST 6	0x00	RW	Noise UV List 6 Noise UV curve position 6 for automatic noise U / noise V computation according to sensor gain
0x529F	NOISE UV LIST 6	0x4C	RW	Noise UV List 6 Noise UV curve position 6 for automatic noise U / noise V computation according to sensor gain
0x52A0	DNS NOISEY READ OUT	0x00	R	DNS NoiseY Read Out
0x52A1	DNS EDGETHRE READ OUT	0x00	R	DNS Edgethre Read Out
0x52A2	DNS NOISEU READ OUT	0x00	R	DNS NoiseU Read Out
0x52A3	DNS NOISEU READ OUT	0x00	R	DNS NoiseU Read Out
0x52A4	DNS NOISEV READ OUT	0x00	R	DNS NoiseV Read Out
0x52A5	DNS NOISEV READ OUT	0x00	R	DNS NoiseV Read Out
0x52A6	REAL GAIN	0x00	R	Real Gain Read Out
0x52A7	REAL GAIN	0x00	R	Real Gain Read Out

table 7-27 CIP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5300	CIP MIN GAIN	0x00	RW	Bit[1:0]: cip_mingain[9:8] Minimum real gain for calculation of CIP parameters normalized by 0x10.
0x5301	CIP MIN GAIN	0x10	RW	Bit[7:0]: cip_mingain[7:0] Minimum real gain for calculation of CIP parameters normalized by 0x10.
0x5302	CIP MAX GAIN	0x00	RW	Bit[1:0]: cip_maxgain[9:8] Maximum real gain for calculation of CIP parameters normalized by 0x10.
0x5303	CIP MAX GAIN	0x80	RW	Bit[7:0]: cip_maxgain[7:0] Maximum real gain for calculation of CIP parameters normalized by 0x10.
0x5304	CIP MIN INTNOISE	0x00	RW	Bit[1:0]: cip_min_intnoise[8] CIP de-noise at CIP MIN GAIN. The larger the value, the blurrier the image.
0x5305	CIP MIN INTNOISE	0x30	RW	Bit[7:0]: cip_min_intnoise[7:0] CIP de-noise at CIP MIN GAIN. The larger the value, the blurrier the image.
0x5306	CIP MAX INTNOISE	0x01	RW	Bit[1:0]: cip_max_intnoise[8] CIP de-noise at CIP MAX GAIN. The larger the value, the blurrier the image.
0x5307	CIP MAX INTNOISE	0x20	RW	Bit[7:0]: cip_max_intnoise[7:0] CIP de-noise at CIP MAX GAIN. The larger the value, the blurrier the image.
0x5308	CIP SHARPEN MASK 0	0x10	RW	Bit[7:0]: cip punsharpen mask0[7:0] (sign + abs) Weight for position 0 and 4 in the 5-point filter when evaluating edge effect.

table 7-27 CIP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5309	CIP SHARPEN MASK 1	0x30	RW	Bit[7:0]: cip punsharpen mask1[7:0] (sign + abs) Weight for position 1 and 3 in the 5-point filter when evaluating edge effect.
0x530A	CIP CONTROL10	0x01	RW	CIP Control 10 Bit[7:4]: Not used Bit[3]: Sharpen manual enable Bit[2:1]: Debug mode Changing this value is not recommended Bit[0]: Anti-aliasing enable 0: Anti-aliasing mode disable 1: Anti-aliasing mode enable
0x530B~ 0x531D	CIP CONTROL REGISTERS	–	RW	CIP Control Registers
0x531E	CIP MANUAL SHARPENP	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: CIP sharpenp[5:0] manual setting when **0x530A**[3]=1
0x531F	CIP MANUAL SHARPENM	0x0C	RW	Bit[7]: Not used Bit[6:0]: CIP sharpenm[6:0] manual setting when **0x530A**[3]=1
0x5320	CIP MANUAL SHARPENTP	0x20	RW	Bit[7:0]: CIP sharpentp[7:0] manual setting when **0x530A**[3]=1
0x5321	CIP MANUAL SHARPENTM	0x20	RW	Bit[7:0]: CIP sharpentm[7:0] manual setting when **0x530A**[3]=1

table 7-28 CMX registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5380	CMX 00	0x01	RW	Bit[7:2]: Not used Bit[1:0]: cmx 00[9:8]
0x5381	CMX 00	0x00	RW	Bit[7:0]: cmx 00[7:0]
0x5382	CMX 01	0x00	RW	Bit[7:2]: Not used Bit[1:0]: cmx 01[9:8]
0x5383	CMX 01	0x17	RW	Bit[7:0]: cmx 01[7:0]
0x5384	CMX 02	0x00	RW	Bit[7:2]: Not used Bit[1:0]: cmx 02[9:8]
0x5385	CMX 02	0x01	RW	Bit[7:0]: cmx 02[7:0]
0x5386	CMX 10	0x00	RW	Bit[7:2]: Not used Bit[1:0]: cmx 10[9:8]
0x5387	CMX 10	0x00	RW	Bit[7:0]: cmx 10[7:0]
0x5388	CMX 11	0x01	RW	Bit[7:2]: Not used Bit[1:0]: cmx 11[9:8]
0x5389	CMX 11	0x35	RW	Bit[7:0]: cmx 11[7:0]
0x538A	CMX 12	0x00	RW	Bit[7:2]: Not used Bit[1:0]: cmx 12[9:8]
0x538B	CMX 12	0x3E	RW	Bit[7:0]: cmx 12[7:0]
0x538C	CMX 20	0x00	RW	Bit[7:2]: Not used Bit[1:0]: cmx 20[9:8]
0x538D	CMX 20	0x00	RW	Bit[7:0]: cmx 20[7:0]
0x538E	CMX 21	0x0A	RW	Bit[7:2]: Not used Bit[1:0]: cmx 21[9:8]
0x538F	CMX 21	0x00	RW	Bit[7:0]: cmx 21[7:0]
0x5390	CMX 22	0x00	RW	Bit[7:2]: Not used Bit[1:0]: cmx 22[9:8]
0x5391	CMX 22	0xCD	RW	Bit[7:0]: cmx 22[7:0]
0x5392	CMX CMXSIGN	0x00	RW	CMX Sign High Byte Bit[7:1]: Not used Bit[0]: cmx 22 sign

table 7-28 CMX registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5393	CMX CMXSIGN	0x20	RW	CMX Sign Low Byte Bit[7]: cmx 21 sign Bit[6]: cmx 20 sign Bit[5]: cmx 12 sign Bit[4]: cmx 11 sign Bit[3]: cmx 10 sign Bit[2]: cmx 02 sign Bit[1]: cmx 01 sign Bit[0]: cmx 00 sign
0x5394	CMX CONTROL20	0x08	RW	CMX Control 20 Bit[7:4]: Not used Bit[3:0]: cmx shift

table 7-29 stretch registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5400~ 0x5401	STRETCH RESERVED	–	RW	Reserved
0x5402	STRETCH MIN HIGH LEVEL	0x3C	RW	Bit[7]: Not used Bit[6:0]: Minimum high level high byte[14:8] Minimum high level threshold.
0x5403	STRETCH MIN HIGH LEVEL	0x00	RW	Bit[7:0]: Minimum high level low byte[7:0] Minimum high level threshold
0x5404	STRETCH MAX LOW LEVEL	0x02	RW	Bit[7]: Not used Bit[6:0]: Maximum low level high byte[14:8] Maximum low level threshold.
0x5405	STRETCH MAX LOW LEVEL	0x00	RW	Bit[7:0]: Maximum low level low byte[7:0] Maximum low level threshold.
0x5406~ 0x540B	STRETCH RESERVED	–	RW	Reserved
0x540C~ 0x540D	NOT USED	–	–	Not Used

table 7-29 stretch registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x540E	STRETCH THRES1	0x00	RW	Bit[7]: Not used Bit[6:0]: Thres1[22:16] high 2 byte Threshold1 for stretch algorithm
0x540F	STRETCH THRES1	0x3A	RW	Bit[7:0]: Thres1[15:8] low 1 byte Threshold1 for stretch algorithm
0x5410	STRETCH THRES1	0x98	RW	Bit[7:0]: Thres1[7:0] low 2 byte Threshold1 for stretch algorithm
0x5411	NOT USED	–	–	Not Used
0x5412	STRETCH THRES2	0x00	RW	Bit[7]: Not used Bit[6:0]: Thres2[22:16] high 2 byte Threshold2 for stretch algorithm
0x5413	STRETCH THRES2	0x3A	RW	Bit[7:0]: Thres2[15:8] low 1 byte Threshold2 for stretch algorithm
0x5414	STRETCH THRES2	0x98	RW	Bit[7:0]: Thres2[7:0] low 2 byte Threshold2 for stretch algorithm
0x5415~ 0x541C	DEBUG MODE	–	–	Debug Mode Changing these values is not allowed
0x541D	STRETCH STEP	0x20	RW	Bit[7:0]: Stretch step[7:0] Step for stretch control

table 7-30 raw gamma / Y gamma registers

address	register name	default value	R/W	description
0x5480	GAMMA CONTROL00	0x1A	RW	Bit[7:0]: Y list 00
0x5481	GAMMA CONTROL01	0x28	RW	Bit[7:0]: Y list 01
0x5482	GAMMA CONTROL02	0x3E	RW	Bit[7:0]: Y list 02
0x5483	GAMMA CONTROL03	0x5E	RW	Bit[7:0]: Y list 03
0x5484	GAMMA CONTROL04	0x6B	RW	Bit[7:0]: Y list 04
0x5485	GAMMA CONTROL05	0x77	RW	Bit[7:0]: Y list 05
0x5486	GAMMA CONTROL06	0x81	RW	Bit[7:0]: Y list 06
0x5487	GAMMA CONTROL07	0x8B	RW	Bit[7:0]: Y list 07
0x5488	GAMMA CONTROL08	0x94	RW	Bit[7:0]: Y list 08
0x5489	GAMMA CONTROL09	0x9C	RW	Bit[7:0]: Y list 09
0x548A	GAMMA CONTROL0A	0xAB	RW	Bit[7:0]: Y list 0a
0x548B	GAMMA CONTROL0B	0xB8	RW	Bit[7:0]: Y list 0b
0x548C	GAMMA CONTROL0C	0xCE	RW	Bit[7:0]: Y list 0c
0x548D	GAMMA CONTROL0D	0xDF	RW	Bit[7:0]: Y list 0d
0x548E	GAMMA CONTROL0E	0xEC	RW	Bit[7:0]: Y list 0e
0x548F	GAMMA CONTROL0F	00xD	RW	Bit[7:0]: Y list 0f

table 7-31 UV gamma registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5490	GAMMA GAIN LIST 00	0x07	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 00 high byte
0x5491	GAMMA GAIN LIST 00	0x81	RW	Bit[7:0]: Gain list 00 low byte
0x5492	GAMMA GAIN LIST 01	0x05	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 01 high byte
0x5493	GAMMA GAIN LIST 01	0xF5	RW	Bit[7:0]: Gain list 01 low byte
0x5494	GAMMA GAIN LIST 02	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 02 high byte
0x5495	GAMMA GAIN LIST 02	0xC8	RW	Bit[7:0]: Gain list 02 low byte
0x5496	GAMMA GAIN LIST 03	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 03 high byte
0x5497	GAMMA GAIN LIST 03	0x96	RW	Bit[7:0]: Gain list 03 low byte
0x5498	GAMMA GAIN LIST 04	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 04 high byte
0x5499	GAMMA GAIN LIST 04	0x3B	RW	Bit[7:0]: Gain list 04 low byte
0x549A	GAMMA GAIN LIST 05	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 05 high byte
0x549B	GAMMA GAIN LIST 05	0xF5	RW	Bit[7:0]: Gain list 05 low byte
0x549C	GAMMA GAIN LIST 06	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 06 high byte
0x549D	GAMMA GAIN LIST 06	0xB9	RW	Bit[7:0]: Gain list 06 low byte
0x549E	GAMMA GAIN LIST 07	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 07 high byte
0x549F	GAMMA GAIN LIST 07	0x84	RW	Bit[7:0]: Gain list 07 low byte
0x54A0	GAMMA GAIN LIST 08	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 08 high byte
0x54A1	GAMMA GAIN LIST 08	0x59	RW	Bit[7:0]: Gain list 08 low byte
0x54A2	GAMMA GAIN LIST 09	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 09 high byte
0x54A3	GAMMA GAIN LIST 09	0x31	RW	Bit[7:0]: Gain list 09 low byte
0x54A4	GAMMA GAIN LIST 10	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 10 high byte
0x54A5	GAMMA GAIN LIST 10	0xED	RW	Bit[7:0]: Gain list 10 low byte

table 7-31 UV gamma registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x54A6	GAMMA GAIN LIST 11	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 11 high byte
0x54A7	GAMMA GAIN LIST 11	0xB3	RW	Bit[7:0]: Gain list 11 low byte
0x54A8	GAMMA GAIN LIST 12	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 12 high byte
0x54A9	GAMMA GAIN LIST 12	0x59	RW	Bit[7:0]: Gain list 12 low byte
0x54AA	GAMMA GAIN LIST 13	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 13 high byte
0x54AB	GAMMA GAIN LIST 13	0x11	RW	Bit[7:0]: Gain list 13 low byte
0x54AC	GAMMA GAIN LIST 14	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 14 high byte
0x54AD	GAMMA GAIN LIST 14	0xD4	RW	Bit[7:0]: Gain list 14 low byte
0x54AE	GAMMA GAIN LIST 15	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 15 high byte
0x54AF	GAMMA GAIN LIST 15	0x1D	RW	Bit[7:0]: Gain list 15 low byte
0x54B0	GAMMA CONTROL30	0x01	RW	Bit[7:2]: Not used Bit[1]: Debug mode Changing this value is not allowed Bit[0]: UV dark enable 0: Do not apply 1: Apply UV process in dark area controlled by UV dark threshold
0x54B1	GAMMA CONTROL31	0x20	RW	Bit[7:0]: UV dark threshold Threshold for UV process in dark area
0x54B2	GAMMA CONTROL32	0x01	RW	Bit[7:1]: Not used Bit[0]: H dark enable 0: Do not apply 1: Apply h process in dark area controlled by UV dark threshold
0x54B3	GAMMA CONTROL33	0x40	RW	Bit[7:0]: H dark threshold Threshold for h process in dark area
0x54B4~ 0x54B7	GAMMA CONTROL	–	RW	Gamma Control Registers

table 7-32 UV adjust registers

address	register name	default value	R/W	description
0x5500	UV UVADJUST CONTROL0	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Adjust offset UV adjust in value mimimum threshold
0x5501	UV UVADJUST CONTROL3	0x1F	RW	UV Adjust Control 3 Bit[7:6]: Not used Bit[5]: UV adjust manual enable 0: Auto mode 1: Manual mode Bit[4:0]: UV adjust in manual UV adjust manual setting when 0x5501[5]=1
0x5502	UV ADJ TH1	0x00	RW	Bit[7:1]: Not used Bit[0]: UV adj th1[8] Real gain threshold for UV adjust in which will be limited to 31 if real gain is smaller than UV adj th1.
0x5503	UV ADJ TH1	0x00	RW	Bit[7:0]: UV adj th1 Real gain threshold for UV adjust in which will be limited to 31 if real gain is smaller than UV adj th1.
0x5504	UV ADJ TH2	0x01	RW	Bit[7:1]: Not used Bit[0]: UV adj th2[8] Real gain threshold for UV adjust in which will be limited to UV offset (UV UVADJUST CTRL0[4:0] (**0x5500**)) if real gain is larger than UV adj th1.
0x5505	UV ADJ TH2	0xFF	RW	Bit[7:0]: UV adj th2 Real gain threshold for UV adjust in which will be limited to UV offset (UV UVADJUST CTRL0[4:0] (**0x5500**)) if real gain is larger than UV adj th1.
0x5506	UV ADJUST IN AUTO	–	R	Bit[7:5]: Not used Bit[4:0]: UV adjust in read out

table 7-33 SDE registers

address	register name	default value	R/W	description
0x5580	SDE CONTROL0	0x00	RW	Bit[7]: Fixed Y enable Bit[6]: Negative enable Bit[5]: Gray enable Bit[4]: Fixed V enable Bit[3]: Fixed U enable Bit[2]: Contrast enable Bit[1]: Satuation enable Bit[0]: Hue enable
0x5581	SDE CONTROL1	0x80	RW	Bit[7:0]: Hue cos Controlled by: hue_angle_en (**0x558A**[6]) hue_angle_en=1'b0: hue cos[7:0] hue_angle_en=1'b1: angle[7:0]
0x5582	SDE CONTROL2	0x00	RW	Bit[7:0]: hue sin Controlled by: hue_angle_en (**0x558A**[6]) hue_angle_en=1'b0: hue sin[7:0] hue_angle_en=1'b1: angle[8]
0x5583	SDE CONTROL3	0x40	RW	Bit[7:0]: Saturation U
0x5584	SDE CONTROL4	0x40	RW	Bit[7:0]: Saturation V
0x5585	SDE CONTROL5	0x80	RW	Bit[7:0]: Ureg for fixed U
0x5586	SDE CONTROL6	0x80	RW	Bit[7:0]: Vreg for fixed V
0x5587	SDE CONTROL7	0x00	RW	Bit[7:0]: Yoffset for contrast or Y value for fixed Y
0x5588	SDE CONTROL8	0x20	RW	Bit[7:0]: Ygain for contrast
0x5589	SDE CONTROL9	0x00	RW	Bit[7:0]: Ybright for contrast
0x558A	SDE CONTROL10	0x01	RW	Bit[7]: Solarize enable Bit[6]: Hue angle enable Bit[5]: Sign COS for Cr Bit[4]: Sign COS for Cb Bit[3]: Sign offset for contrast Bit[2]: Sign bright for contrast Bit[1]: Sign SIN for Cb Bit[0]: Sign SIN for Cr

table 7-34 scale/average registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5600	SCALE CONTROL 00	0x00	RW	Scale Control 00 Bit[7]: Not used Bit[6]: YUV422 man 0: From system 1: Manually Bit[5]: YUV422 sel 0: From scale h YUV422 1: From DCW scale YUV422 output Bit[4]: UV drop for YUV444to422 Bit[3]: Vfirst for YUV444to422 Bit[2]: UV swap for YUV422to444 Bit[1]: Y swap for YUV422to444 Bit[0]: Debug mode Changing this value is not allowed
0x5680	AVG X START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Avg x start[11:8] Horizontal start position for average window
0x5681	AVG X START	0x00	RW	Bit[7:0]: Avg x start[7:0] Horizontal start position for average window
0x5682	AVG X END	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Avg x end[11:8] Horizontal end position for average window
0x5683	AVG X END	0x00	RW	Bit[7:0]: Avg x end[7:0] Horizontal end position for average window
0x5684	AVG Y START	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Avg y start[10:8] Vertical start position for average window
0x5685	AVG Y START	0x00	RW	Bit[7:0]: Avg y start[7:0] Vertical start position for average window
0x5686	AVG Y END	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Avg y end[10:8] Vertical end position for average window

table 7-34 scale/average registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5687	AVG Y END	0x00	RW	Bit[7:0]: avg y end[7:0] Vertical end position for average window
0x5688	AVG R8	0xFF	RW	Bit[7:4]: Window1 weight Bit[3:0]: Window0 weight
0x5689	AVG R9	0xFF	RW	Bit[7:4]: Window3 weight Bit[3:0]: Window2 weight
0x568A	AVG RA	0xFF	RW	Bit[7:4]: Window5 weight Bit[3:0]: Window4 weight
0x568B	AVG RB	0xFF	RW	Bit[7:4]: Window7 weight Bit[3:0]: Window6 weight
0x568C	AVG RC	0xFF	RW	Bit[7:4]: Window9 weight Bit[3:0]: Window8 weight
0x568D	AVG RD	0xFF	RW	Bit[7:4]: Window11 weight Bit[3:0]: Window10 weight
0x568E	AVG RE	0xFF	RW	Bit[7:4]: Window13 weight Bit[3:0]: Window12 weight
0x568F	AVG RF	0xFF	RW	Bit[7:4]: Window15 weight Bit[3:0]: Window14 weight
0x5690	AVG R10	–	R	Bit[7:0]: Average value
0x5691	AVG R11	–	R	Bit[7:1]: Not used Bit[0]: Average done read out

table 7-35 DCW and DPC registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5700	THUMBNAIL CONTROL 00	0x10	RW	Bit[7]: Not used Bit[6]: v_first YUV444 to YUV422 output U or V first 0: U first 1: V first Bit[5]: uv_drop YUV444 to YUV422 drop mode versus averge mode selection 0: Average mode 1: Drop mode Bit[4]: auto_mode Scale auto mode versus manual mode selection 0: Manual mode 1: Auto mode Bit[3] Hround dcw_hrounding 0: No horizontal rounding 1: Horizontal rounding Bit[2] Hdrop dcw_drop_mode 0: Horizontal average mode 1: Horizontal drop mode Bit[1] Vround dcw_vrounding 0: No vertical rounding 1: Vertical rounding Bit[0] Vdrop dcw_drop_mode 0: Vertical average mode 1: Vertical drop mode

table 7-35 DCW and DPC registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5701	THUMBNAIL TIMES CONTROL	0x00	RW	Bit[7]: Not used Bit[6:4]: Hdiv dcw_scale_times 000: dcw_1_time 001: dcw_2_time 010: dcw_4_time 011: dcw_8_time 100: dcw_16_time Others: dcw_16_time Bit[2:0]: Vdiv dcw_scale_times 000: dcw_1_time 001: dcw_2_time 010: dcw_4_time 011: dcw_8_time 100: dcw_16_time Others: dcw_16_time
0x5702	THUMBNAIL XSC	0x02	RW	Bit[7:2]: Not used Bit[1:0]: DCW XSC reg Horizontal output size for thumbnail
0x5703	THUMBNAIL XSC	0x00	RW	Bit[7:0]: DCW XSC reg Horizontal output size for thumbnail
0x5704	THUMBNAIL YSC	0x02	RW	Bit[7:2]: Not used Bit[1:0]: DCW YSC reg Vertical output size for thumbnail
0x5705	THUMBNAIL YSC	0x00	RW	Bit[7:0]: DCW YSC reg Vertical output size for thumbnail
0x5706	THUMBNAIL OFFSET	0x00	RW	Bit[7:4]: Not used Bit[3:0]: voffset_4bits
0x5707~ 0x577F	THUMBNAIL CONTROL	–	RW	Thumbnail Control Registers
0x5780	DPC CTRL 00	0x77	RW	DPC Control 00 Bit[7]: Not used Bit[6]: Detail enable Bit[5:4]: Boundary selection Bit[3]: Debug mode Changing this value is not allowed Bit[2]: Smooth enable Bit[1]: Differenct channel enable Bit[0]: Single channel enable

table 7-35 DCW and DPC registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5781	DPC THRESHOLD	0x30	RW	Bit[7:0]: Threshold for DPC
0x5782	DPC CTRL 02	0x20	RW	DPC Control 02 Bit[7]: Bypass select enable Bit[6:0]: White threshold for DPC
0x5783	DPC B THRESHOLD	0x40	RW	Bit[7:0]: Black threshold for DPC
0x5784	DPC CTRL 04	0x03	RW	DPC Control 04 Bit[7:4]: Not used Bit[3]: Debug mode Changing this value is not allowed Bit[2:0]: gainbd_pwr
0x5785	DPC RESERVED	0x02	RW	Reserved
0x5786	DPC GAIN LIST1	0x08	RW	Bit[7:0]: Gain list 1
0x5787	DPC GAIN LIST2	0x20	RW	Bit[7:0]: Gain list 2
0x5788	DPC WHITE THRESHOLD LIST0	0x20	RW	Bit[7:0]: White threshold list 0
0x5789	DPC WHITE THRESHOLD LIST1	0x18	RW	Bit[7:0]: White threshold list 1
0x578A	DPC WHITE THRESHOLD LIST2	0x08	RW	Bit[7:0]: White threshold list 2
0x578B	DPC WHITE THRESHOLD LIST3	0x04	RW	Bit[7:0]: White threshold list 3
0x578C	DPC BLACKTHRESHOLD LIST0	0x40	RW	Bit[7:0]: Black threshold list 0
0x578D	DPC BLACK THRESHOLD LIST1	0x20	RW	Bit[7:0]: Black threshold list 1
0x578E	DPC BLACK THRESHOLD LIST2	0x08	RW	Bit[7:0]: Black threshold list 2
0x578F	DPC BLACK THRESHOLD LIST3	0x04	RW	Bit[7:0]: Black threshold list 3
0x5790	DPC READ OUT	–	R	Bit[7]: Detail enable Bit[6:0]: White threshold

table 7-36 LENC registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x5800	LENC PARA G00	0x30	RW	Bit[7:0]: LENC PARA G00
0x5801	LENC PARA G01	0x30	RW	Bit[7:0]: LENC PARA G01
0x5802	LENC PARA G02	0x30	RW	Bit[7:0]: LENC PARA G02
0x5803	LENC PARA G03	0x30	RW	Bit[7:0]: LENC PARA G03
0x5804	LENC PARA G04	0x30	RW	Bit[7:0]: LENC PARA G04
0x5805	LENC PARA G05	0x30	RW	Bit[7:0]: LENC PARA G05
0x5806	LENC PARA G06	0x30	RW	Bit[7:0]: LENC PARA G06
0x5807	LENC PARA G07	0x30	RW	Bit[7:0]: LENC PARA G07
0x5808	LENC PARA G08	0x30	RW	Bit[7:0]: LENC PARA G08
0x5809	LENC PARA G09	0x18	RW	Bit[7:0]: LENC PARA G09
0x580A	LENC PARA G10	0x18	RW	Bit[7:0]: LENC PARA G10
0x580B	LENC PARA G11	0x18	RW	Bit[7:0]: LENC PARA G11
0x580C	LENC PARA G12	0x18	RW	Bit[7:0]: LENC PARA G12
0x580D	LENC PARA G13	0x18	RW	Bit[7:0]: LENC PARA G13
0x580E	LENC PARA G14	0x18	RW	Bit[7:0]: LENC PARA G14
0x580F	LENC PARA G15	0x30	RW	Bit[7:0]: LENC PARA G15
0x5810	LENC PARA G16	0x30	RW	Bit[7:0]: LENC PARA G16
0x5811	LENC PARA G17	0x18	RW	Bit[7:0]: LENC PARA G17
0x5812	LENC PARA G18	0x0A	RW	Bit[7:0]: LENC PARA G18
0x5813	LENC PARA G19	0x0A	RW	Bit[7:0]: LENC PARA G19
0x5814	LENC PARA G20	0x0A	RW	Bit[7:0]: LENC PARA G20
0x5815	LENC PARA G21	0x0A	RW	Bit[7:0]: LENC PARA G21
0x5816	LENC PARA G22	0x18	RW	Bit[7:0]: LENC PARA G22
0x5817	LENC PARA G23	0x30	RW	Bit[7:0]: LENC PARA G23
0x5818	LENC PARA G24	0x30	RW	Bit[7:0]: LENC PARA G24
0x5819	LENC PARA G25	0x18	RW	Bit[7:0]: LENC PARA G25
0x581A	LENC PARA G26	0x0A	RW	Bit[7:0]: LENC PARA G26
0x581B	LENC PARA G27	0x00	RW	Bit[7:0]: LENC PARA G27
0x581C	LENC PARA G28	0x00	RW	Bit[7:0]: LENC PARA G28

table 7-36 LENC registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x581D	LENC PARA G29	0x0A	RW	Bit[7:0]: LENC PARA G29
0x581E	LENC PARA G30	0x18	RW	Bit[7:0]: LENC PARA G30
0x581F	LENC PARA G31	0x30	RW	Bit[7:0]: LENC PARA G31
0x5820	LENC PARA G32	0x30	RW	Bit[7:0]: LENC PARA G32
0x5821	LENC PARA G33	0x18	RW	Bit[7:0]: LENC PARA G33
0x5822	LENC PARA G34	0x0A	RW	Bit[7:0]: LENC PARA G34
0x5823	LENC PARA G35	0x00	RW	Bit[7:0]: LENC PARA G35
0x5824	LENC PARA G36	0x00	RW	Bit[7:0]: LENC PARA G36
0x5825	LENC PARA G37	0x0A	RW	Bit[7:0]: LENC PARA G37
0x5826	LENC PARA G38	0x18	RW	Bit[7:0]: LENC PARA G38
0x5827	LENC PARA G39	0x30	RW	Bit[7:0]: LENC PARA G39
0x5828	LENC PARA G40	0x30	RW	Bit[7:0]: LENC PARA G40
0x5829	LENC PARA G41	0x18	RW	Bit[7:0]: LENC PARA G41
0x582A	LENC PARA G42	0x0A	RW	Bit[7:0]: LENC PARA G42
0x582B	LENC PARA G43	0x0A	RW	Bit[7:0]: LENC PARA G43
0x582C	LENC PARA G44	0x0A	RW	Bit[7:0]: LENC PARA G44
0x582D	LENC PARA G45	0x0A	RW	Bit[7:0]: LENC PARA G45
0x582E	LENC PARA G46	0x18	RW	Bit[7:0]: LENC PARA G46
0x582F	LENC PARA G47	0x30	RW	Bit[7:0]: LENC PARA G47
0x5830	LENC PARA G48	0x30	RW	Bit[7:0]: LENC PARA G48
0x5831	LENC PARA G49	0x18	RW	Bit[7:0]: LENC PARA G49
0x5832	LENC PARA G50	0x18	RW	Bit[7:0]: LENC PARA G50
0x5833	LENC PARA G51	0x18	RW	Bit[7:0]: LENC PARA G51
0x5834	LENC PARA G52	0x18	RW	Bit[7:0]: LENC PARA G52
0x5835	LENC PARA G53	0x18	RW	Bit[7:0]: LENC PARA G53
0x5836	LENC PARA G54	0x18	RW	Bit[7:0]: LENC PARA G54
0x5837	LENC PARA G55	0x30	RW	Bit[7:0]: LENC PARA G55
0x5838	LENC PARA G56	0x30	RW	Bit[7:0]: LENC PARA G56
0x5839	LENC PARA G57	0x30	RW	Bit[7:0]: LENC PARA G57
0x583A	LENC PARA G58	0x30	RW	Bit[7:0]: LENC PARA G58

table 7-36 LENC registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x583B	LENC PARA G59	0x30	RW	Bit[7:0]: LENC PARA G59
0x583C	LENC PARA G60	0x30	RW	Bit[7:0]: LENC PARA G60
0x583D	LENC PARA G61	0x30	RW	Bit[7:0]: LENC PARA G61
0x583E	LENC PARA G62	0x30	RW	Bit[7:0]: LENC PARA G62
0x583F	LENC PARA G63	0x30	RW	Bit[7:0]: LENC PARA G63
0x5840	LENC PARA BR00	0x14	RW	Bit[7:0]: LENC PARA BR00
0x5841	LENC PARA BR01	0x14	RW	Bit[7:0]: LENC PARA BR01
0x5842	LENC PARA BR02	0x14	RW	Bit[7:0]: LENC PARA BR02
0x5843	LENC PARA BR03	0x14	RW	Bit[7:0]: LENC PARA BR03
0x5844	LENC PARA BR04	0x14	RW	Bit[7:0]: LENC PARA BR04
0x5845	LENC PARA BR05	0x14	RW	Bit[7:0]: LENC PARA BR05
0x5846	LENC PARA BR06	0x14	RW	Bit[7:0]: LENC PARA BR06
0x5847	LENC PARA BR07	0x12	RW	Bit[7:0]: LENC PARA BR07
0x5848	LENC PARA BR08	0x12	RW	Bit[7:0]: LENC PARA BR08
0x5849	LENC PARA BR09	0x12	RW	Bit[7:0]: LENC PARA BR09
0x584A	LENC PARA BR10	0x12	RW	Bit[7:0]: LENC PARA BR10
0x584B	LENC PARA BR11	0x14	RW	Bit[7:0]: LENC PARA BR11
0x584C	LENC PARA BR12	0x14	RW	Bit[7:0]: LENC PARA BR12
0x584D	LENC PARA BR13	0x12	RW	Bit[7:0]: LENC PARA BR13
0x584E	LENC PARA BR14	0x10	RW	Bit[7:0]: LENC PARA BR14
0x584F	LENC PARA BR15	0x10	RW	Bit[7:0]: LENC PARA BR15
0x5850	LENC PARA BR16	0x12	RW	Bit[7:0]: LENC PARA BR16
0x5851	LENC PARA BR17	0x14	RW	Bit[7:0]: LENC PARA BR17
0x5852	LENC PARA BR18	0x14	RW	Bit[7:0]: LENC PARA BR18
0x5853	LENC PARA BR19	0x12	RW	Bit[7:0]: LENC PARA BR19
0x5854	LENC PARA BR20	0x10	RW	Bit[7:0]: LENC PARA BR20
0x5855	LENC PARA BR21	0x10	RW	Bit[7:0]: LENC PARA BR21
0x5856	LENC PARA BR22	0x12	RW	Bit[7:0]: LENC PARA BR22
0x5857	LENC PARA BR23	0x14	RW	Bit[7:0]: LENC PARA BR23
0x5858	LENC PARA BR24	0x14	RW	Bit[7:0]: LENC PARA BR24

table 7-36 LENC registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x5859	LENC PARA BR25	0x12	RW	Bit[7:0]: LENC PARA BR25
0x585A	LENC PARA BR26	0x12	RW	Bit[7:0]: LENC PARA BR26
0x585B	LENC PARA BR27	0x12	RW	Bit[7:0]: LENC PARA BR27
0x585C	LENC PARA BR28	0x12	RW	Bit[7:0]: LENC PARA BR28
0x585D	LENC PARA BR29	0x14	RW	Bit[7:0]: LENC PARA BR29
0x585E	LENC PARA BR30	0x14	RW	Bit[7:0]: LENC PARA BR30
0x585F	LENC PARA BR31	0x14	RW	Bit[7:0]: LENC PARA BR31
0x5860	LENC PARA BR32	0x14	RW	Bit[7:0]: LENC PARA BR32
0x5861	LENC PARA BR33	0x14	RW	Bit[7:0]: LENC PARA BR33
0x5862	LENC PARA BR34	0x14	RW	Bit[7:0]: LENC PARA BR34
0x5863	LENC PARA BR35	0x14	RW	Bit[7:0]: LENC PARA BR35
0x5864	LENC PARA BR36	0x14	RW	Bit[7:0]: LENC PARA BR36
0x5865	LENC PARA BR37	0x14	RW	Bit[7:0]: LENC PARA BR37
0x5866	LENC PARA BR38	0x14	RW	Bit[7:0]: LENC PARA BR38
0x5867	LENC PARA BR39	0x14	RW	Bit[7:0]: LENC PARA BR39
0x5868	LENC PARA BR40	0x14	RW	Bit[7:0]: LENC PARA BR40
0x5869	LENC PARA BR41	0x14	RW	Bit[7:0]: LENC PARA BR41
0x586A	LENC PARA BR42	0x14	RW	Bit[7:0]: LENC PARA BR42
0x586B	LENC PARA BR43	0x12	RW	Bit[7:0]: LENC PARA BR43
0x586C	LENC PARA BR44	0x12	RW	Bit[7:0]: LENC PARA BR44
0x586D	LENC PARA BR45	0x12	RW	Bit[7:0]: LENC PARA BR45
0x586E	LENC PARA BR46	0x12	RW	Bit[7:0]: LENC PARA BR46
0x586F	LENC PARA BR47	0x14	RW	Bit[7:0]: LENC PARA BR47
0x5870	LENC PARA BR48	0x14	RW	Bit[7:0]: LENC PARA BR48
0x5871	LENC PARA BR49	0x12	RW	Bit[7:0]: LENC PARA BR49
0x5872	LENC PARA BR50	0x10	RW	Bit[7:0]: LENC PARA BR50
0x5873	LENC PARA BR51	0x10	RW	Bit[7:0]: LENC PARA BR51
0x5874	LENC PARA BR52	0x12	RW	Bit[7:0]: LENC PARA BR52
0x5875	LENC PARA BR53	0x14	RW	Bit[7:0]: LENC PARA BR53
0x5876	LENC PARA BR54	0x14	RW	Bit[7:0]: LENC PARA BR54

table 7-36 LENC registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x5877	LENC PARA BR55	0x12	RW	Bit[7:0]: LENC PARA BR55
0x5878	LENC PARA BR56	0x10	RW	Bit[7:0]: LENC PARA BR56
0x5879	LENC PARA BR57	0x10	RW	Bit[7:0]: LENC PARA BR57
0x587A	LENC PARA BR58	0x12	RW	Bit[7:0]: LENC PARA BR58
0x587B	LENC PARA BR59	0x14	RW	Bit[7:0]: LENC PARA BR59
0x587C	LENC PARA BR60	0x14	RW	Bit[7:0]: LENC PARA BR60
0x587D	LENC PARA BR61	0x12	RW	Bit[7:0]: LENC PARA BR61
0x587E	LENC PARA BR62	0x12	RW	Bit[7:0]: LENC PARA BR62
0x587F	LENC PARA BR63	0x12	RW	Bit[7:0]: LENC PARA BR63
0x5880	LENC PARA BR64	0x12	RW	Bit[7:0]: LENC PARA BR64
0x5881	LENC PARA BR65	0x14	RW	Bit[7:0]: LENC PARA BR65
0x5882	LENC PARA BR66	0x14	RW	Bit[7:0]: LENC PARA BR66
0x5883	LENC PARA BR67	0x14	RW	Bit[7:0]: LENC PARA BR67
0x5884	LENC PARA BR68	0x14	RW	Bit[7:0]: LENC PARA BR68
0x5885	LENC PARA BR69	0x14	RW	Bit[7:0]: LENC PARA BR69
0x5886	LENC PARA BR70	0x14	RW	Bit[7:0]: LENC PARA BR70
0x5887	LENC PARA BR71	0x14	RW	Bit[7:0]: LENC PARA BR71
0x5888	LENC BRV SCALE	0x01	RW	Bit[7:1]: Reserved Bit[0]: LENC_BRV_SCALE[8] Reciprocal of vertical step for B/R channel. B/R channel in whole image is divided into 4x4 blocks. The step is used to point to the border of the adjacent block. BRVScale = ((4<<17) + (nHeight>>1)) / nHeight
0x5889	LENC BRV SCALE	0x0C	RW	Bit[7:0]: LENC_BRV_SCALE[7:0] Reciprocal of vertical step at B/R channel. B/R channel in whole image is divided into 4x4 blocks. The step is used to point to the border of the adjacent block. BRVScale = ((4<<17) + (nHeight>>1)) / nHeight

table 7-36 LENC registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x588A	LENC BRH SCALE	0x00	RW	Bit[7:1]: Reserved Bit[0]: LENC_BRH_SCALE[8] Reciprocal of horizontal step for B/R channel. B/R channel in whole image is divided into 4x4 blocks. The step is used to point to the border of the adjacent block. BRHScale = ((4<<17) + (nWidth>>1)) / nWidth
0x588B	LENC BRH SCALE	0xC8	RW	Bit[7:0]: LENC_BRH_SCALE[7:0] Reciprocal of horizontal step for B/R channel. B/R channel in whole image is divided into 4x4 blocks. The step is used to point to the border of the adjacent block. BRHScale = ((4<<17) + (nWidth>>1)) / nWidth
0x588C	LENC GV SCALE	0x00	RW	Bit[7:1]: Reserved Bit[0]: LENC_GV_SCALE[8] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block. GVScale = ((4<<17) + (nHeight>>1)) / nHeight
0x588D	LENC GV SCALE	0xC9	RW	Bit[7:0]: LENC_GV_SCALE[7:0] Reciprocal of vertical step at G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block. GVScale = ((4<<17) + (nHeight>>1)) / nHeight

table 7-36 LENC registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x588E	LENC GH_SCALE	0x01	RW	Bit[7:1]: Reserved Bit[0]: LENC_GH_SCALE[8] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block. GHScale = ((4<<17) + (nWidth>>1)) / nWidth
0x588F	LENC GH_SCALE	0x2D	RW	Bit[7:0]: LENC_GH_SCALE[7:0] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block. GHScale = ((4<<17) + (nWidth>>1)) / nWidth
0x5890	LENC X OFFSET	0x00	RW	Bit[7:0]: LENC_X_OFFSET
0x5891	LENC X OFFSET	0x00	RW	Bit[7:0]: LENC_X_OFFSET
0x5892	LENC Y OFFSET	0x00	RW	Bit[7:0]: LENC_Y_OFFSET
0x5893	LENC Y OFFSET	0x00	RW	Bit[7:0]: LENC_Y_OFFSET
0x5894	LENC NGAIN	0xFF	RW	Bit[7:0]: LENC_NGAIN

table 7-37 AFC control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x6000	AFC CTRL00	0xFF	RW	AFC Control 00 Bit[7:5]: Not used Bit[4]: Edge filter enable 1: afc_edge module will update 0: afc_edge module will not update Bit[3]: Edge filter b select Edge b filters select 0: Edge selects b2 1: Edge selects b1 Bit[2:0]: Edge filter a select Edge a filters select 001: edge selects a1 010: edge selects a2 100: edge selects a4 101: edge selects a5
0x6001	AFC CTRL01	0xFF	RW	AFC Control 01 Bit[7:0]: Edge window0 left This window coordinate Others: Edge selects a1
0x6002	AFC CTRL02	0xFF	RW	AFC Control 02 Bit[7:0]: Edge window0 top This window coordinate
0x6003	AFC CTRL03	0xFF	RW	AFC Control 03 Bit[7:0]: Edge window0 right This window coordinate
0x6004	AFC CTRL04	0xFF	RW	AFC Control 04 Bit[7:0]: edge window0 bottom This window coordinate This bottom must be larger than any other
0x6005	AFC CTRL05	0xFF	RW	AFC Control 05 Bit[7:0]: Edge window1 left This window coordinate
0x6006	AFC CTRL06	0xFF	RW	AFC Control 06 Bit[7:0]: Edge window1 top This window coordinate
0x6007	AFC CTRL07	0xFF	RW	AFC Control 07 Bit[7:0]: Edge window1 right This window coordinate
0x6008	AFC CTRL08	0xFF	RW	AFC Control 08 Bit[7:0]: Edge window1 bottom This window coordinate

table 7-37 AFC control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x6009	AFC CTRL09	0xFF	RW	AFC Control 09 Bit[7:0]: Edge window2 left This window coordinate
0x600A	AFC CTRL10	0xFF	RW	AFC Control 10 Bit[7:0]: Edge window2 top This window coordinate
0x600B	AFC CTRL11	0xFF	RW	AFC Control 11 Bit[7:0]: Edge window2 right This window coordinate
0x600C	AFC CTRL12	0xFF	RW	AFC Control 12 Bit[7:0]: Edge window2 bottom This window coordinate
0x600D	AFC CTRL13	0xFF	RW	AFC Control 13 Bit[7:0]: Edge window3 left This window coordinate
0x600E	AFC CTRL14	0xFF	RW	AFC Control 14 Bit[7:0]: edge window3 top This window coordinate
0x600F	AFC CTRL15	0xFF	RW	AFC Control 15 Bit[7:0]: Edge window3 right This window coordinate
0x6010	AFC CTRL16	0xFF	RW	AFC Control 16 Bit[7:0]: Edge window3 bottom This window coordinate
0x6011	AFC CTRL17	0xFF	RW	AFC Control 17 Bit[7:0]: Edge window4 left This window coordinate
0x6012	AFC CTRL18	0xFF	RW	AFC Control 18 Bit[7:0]: Edge window4 top This window coordinate
0x6013	AFC CTRL19	0xFF	RW	AFC Control 19 Bit[7:0]: Edge window4 right This window coordinate
0x6014	AFC CTRL20	0xFF	RW	AFC Control 20 Bit[7:0]: Edge window4 bottom This window coordinate
0x6015	AFC CTRL21	–	R	AFC Control 21 Bit[7:6]: Not used Bit[5:0]: Window0 filter a[29:24]
0x6016	AFC CTRL22	–	R	AFC Control 22 Bit[7:0]: Window0 filter a[23:16]

table 7-37 AFC control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x6017	AFC CTRL23	–	R	AFC Control 23 Bit[7:0]: Window0 filter a[15:8]
0x6018	AFC CTRL24	–	R	AFC Control 24 Bit[7:0]: Window0 filter a[7:0]
0x6019	AFC CTRL25	–	R	AFC Control 25 Bit[7:6]: Not used Bit[5:0]: Window0 filter b[29:24]
0x601A	AFC CTRL26	–	R	AFC Control 26 Bit[7:0]: Window0 filter b[23:16]
0x601B	AFC CTRL27	–	R	AFC Control 27 Bit[7:0]: Window0 filter b[15:8]
0x601C	AFC CTRL28	–	R	AFC Control 28 Bit[7:0]: Window0 filter b[7:0]
0x601D	AFC CTRL29	–	R	AFC Control 29 Bit[7:6]: Not used Bit[5:0]: Window1 filter a[29:24]
0x601E	AFC CTRL30	–	R	AFC Control 30 Bit[7:0]: Window1 filter a[23:16]
0x601F	AFC CTRL31	–	R	AFC Control 31 Bit[7:0]: Window1 filter a[15:8]
0x6020	AFC CTRL32	–	R	AFC Control 32 Bit[7:0]: Window1 filter a[7:0]
0x6021	AFC CTRL33	–	R	AFC Control 33 Bit[7:6]: Not used Bit[5:0]: Window1 filter b[29:24]
0x6022	AFC CTRL34	–	R	AFC Control 34 Bit[7:0]: Window1 filter b[23:16]
0x6023	AFC CTRL35	–	R	AFC Control 35 Bit[7:0]: Window1 filter b[15:8]
0x6024	AFC CTRL36	–	R	AFC Control 36 Bit[7:0]: Window1 filter b[7:0]
0x6025	AFC CTRL37	–	R	AFC Control 37 Bit[7:6]: Not used Bit[5:0]: Window2 filter a[29:24]
0x6026	AFC CTRL38	–	R	AFC Control 38 Bit[7:0]: Window2 filter a[23:16]
0x6027	AFC CTRL39	–	R	AFC Control 39 Bit[7:0]: Window2 filter a[15:8]

table 7-37 AFC control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x6028	AFC CTRL40	–	R	AFC Control 40 Bit[7:0]: Window2 filter a[7:0]
0x6029	AFC CTRL41	–	R	AFC Control 41 Bit[7:6]: Not used Bit[5:0]: Window2 filter b[29:24]
0x602A	AFC CTRL42	–	R	AFC Control 42 Bit[7:0]: Window2 filter b[23:16]
0x602B	AFC CTRL43	–	R	AFC Control 43 Bit[7:0]: Window2 filter b[15:8]
0x602C	AFC CTRL44	–	R	AFC Control 44 Bit[7:0]: Window2 filter b[7:0]
0x602D	AFC CTRL45	–	R	AFC Control 45 Bit[7:6]: Not used Bit[5:0]: Window3 filter a[29:24]
0x602E	AFC CTRL46	–	R	AFC Control 46 Bit[7:0]: Window3 filter a[23:16]
0x602F	AFC CTRL47	–	R	AFC Control 47 Bit[7:0]: Window3 filter a[15:8]
0x6030	AFC CTRL48	–	R	AFC Control 48 Bit[7:0]: Window3 filter a[7:0]
0x6031	AFC CTRL49	–	R	AFC Control 49 Bit[7:6]: Not used Bit[5:0]: Window3 filter b[29:24]
0x6032	AFC CTRL50	–	R	AFC Control 50 Bit[7:0]: Window3 filter b[23:16]
0x6033	AFC CTRL51	–	R	AFC Control 51 Bit[7:0]: Window3 filter b[15:8]
0x6034	AFC CTRL52	–	R	AFC Control 52 Bit[7:0]: Window3 filter b[7:0]
0x6035	AFC CTRL53	–	R	AFC Control 53 Bit[7:6]: Not used Bit[5:0]: Window4 filter a[29:24]
0x6036	AFC CTRL54	–	R	AFC Control 54 Bit[7:0]: Window4 filter a[23:16]
0x6037	AFC CTRL55	–	R	AFC Control 55 Bit[7:0]: Window4 filter a[15:8]
0x6038	AFC CTRL56	–	R	AFC Control 56 Bit[7:0]: Window4 filter a[7:0]

table 7-37 AFC control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x6039	AFC CTRL57	–	R	AFC Control 57 Bit[7:6]: Not used Bit[5:0]: Window4 filter b[29:24]
0x603A	AFC CTRL58	–	R	AFC Control 58 Bit[7:0]: Window4 filter b[23:16]
0x603B	AFC CTRL59	–	R	AFC Control 59 Bit[7:0]: Window4 filter b[15:8]
0x603C	AFC CTRL60	–	R	AFC Control 60 Bit[7:0]: Window4 filter b[7:0]

8 electrical specifications

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
operating temperature range[b]		-30°C to +70°C
stable image temperature range[c]		0°C to +50°C
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-C}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		±200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

b. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

c. image quality remains stable throughout this temperature range

table 8-2 DC characteristics (-30°C < T_A < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-D}[a]	supply voltage (digital core)	1.425	1.5	1.575	V
V_{DD-IO}	supply voltage (digital I/O)	1.71	1.8	3.0	V
I_{DD-A}	active (operating) current	TBD	TBD	TBD	mA
I_{DD-IO}[b, c]		TBD	TBD	TBD	mA
$I_{DDS-SCCB}$	standby current	TBD	TBD	TBD	mA
$I_{DDS-PWDN}$		TBD	TBD	TBD	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs[d]					
V_{IL}	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}	SIOC and SIOD	1.26	1.8	2.3	V

a. using the internal DVDD regulator is strongly recommended for minimum power down current

b. active current is based on sensor resolution at full size and at full speed in compression format

c. with MIPI function, the active current needs an additional 20mA

d. based on DOVDD = 1.8V.

table 8-3 AC characteristics (T_A = 25°C, V_{DD-A} = 2.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		30		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	settling time for hardware reset			<1	ms
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 8-4 timing characteristics

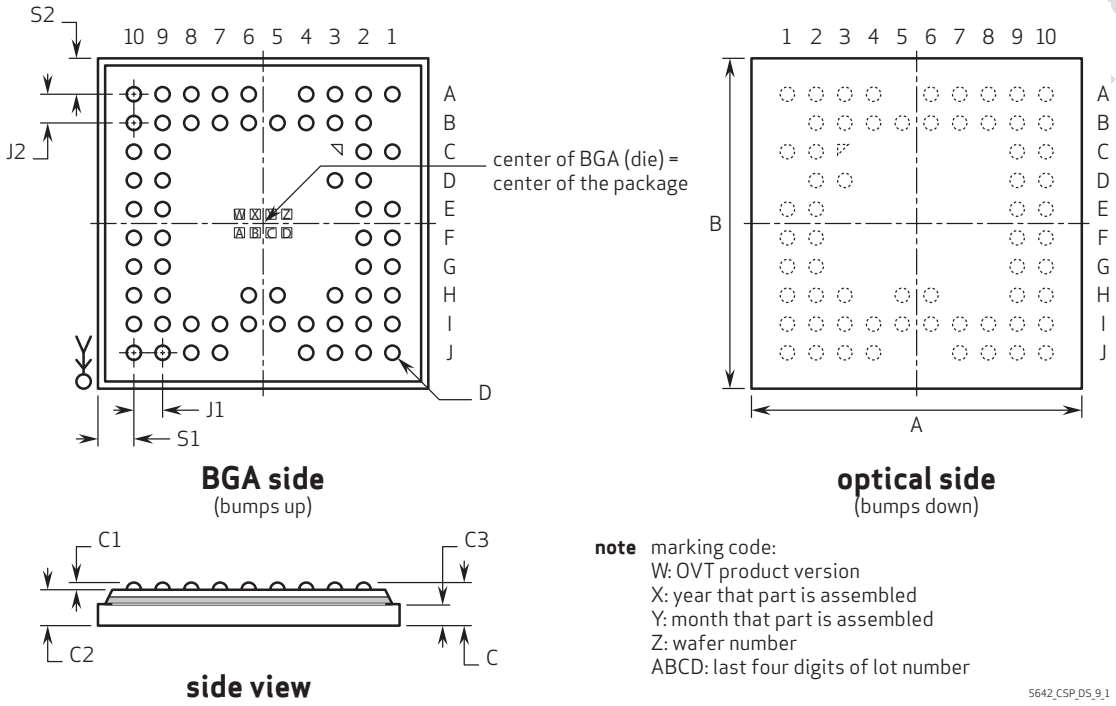
symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a. if using the internal PLL

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications



note marking code:
W: OVT product version
X: year that part is assembled
Y: month that part is assembled
Z: wafer number
ABCD: last four digits of lot number

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table 9-1 package dimensions (sheet 1 of 2)

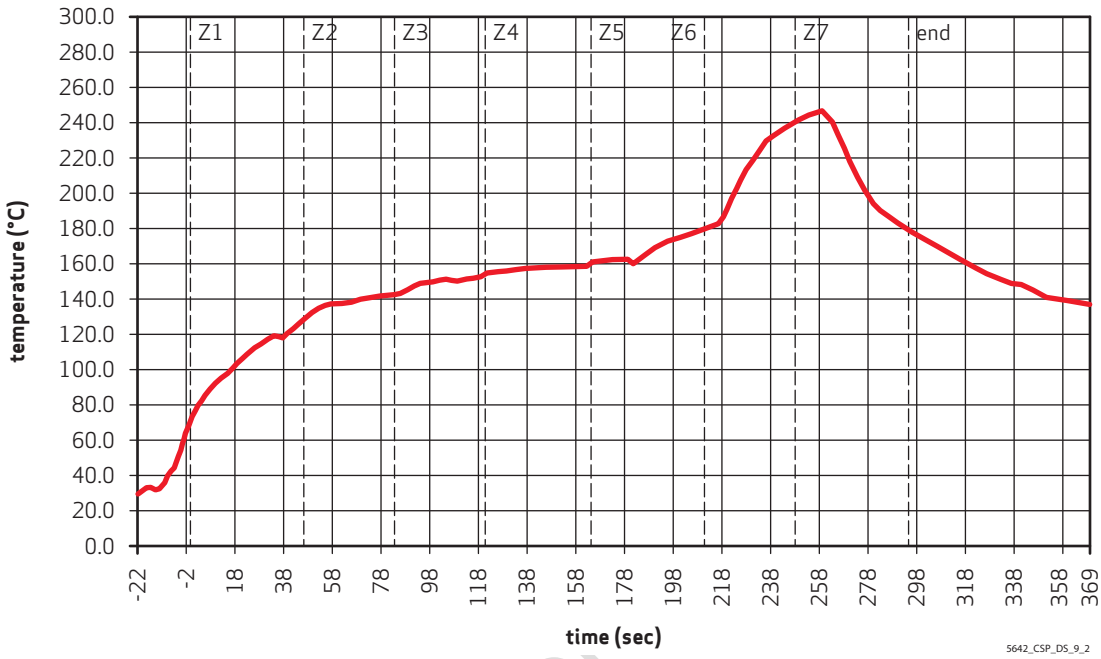
parameter	symbol	min	typ	max	unit
package body dimension x	A	6920	6945	6970	µm
package body dimension y	B	6670	6695	6720	µm
package height	C	720	780	840	µm
ball height	C1	130	160	190	µm
package body thickness	C2	575	620	665	µm
cover glass thickness	C3	425	445	465	µm
ball diameter	D	270	300	330	µm
total pin count	N		63 (8 NC)		

table 9-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
pin count x-axis	N1		10		
pin count y-axis	N2		10		
pins pitch x-axis	J1		640		µm
pins pitch y-axis	J2		630		µm
edge-to-pin center distance analog x	S1	563	593	623	µm
edge-to-pin center distance analog y	S2	483	513	543	µm

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note

The OV5642 uses a lead-free package.

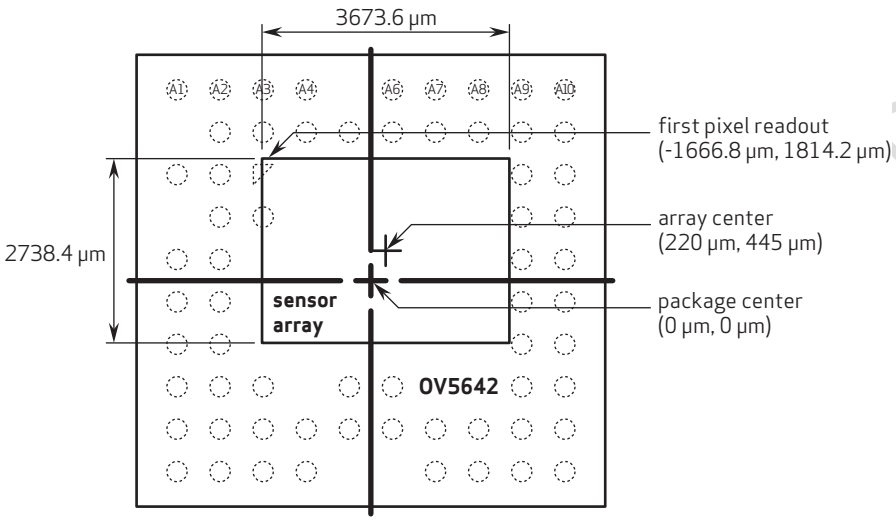
table 9-2 reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A10 oriented down on the PCB.

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10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

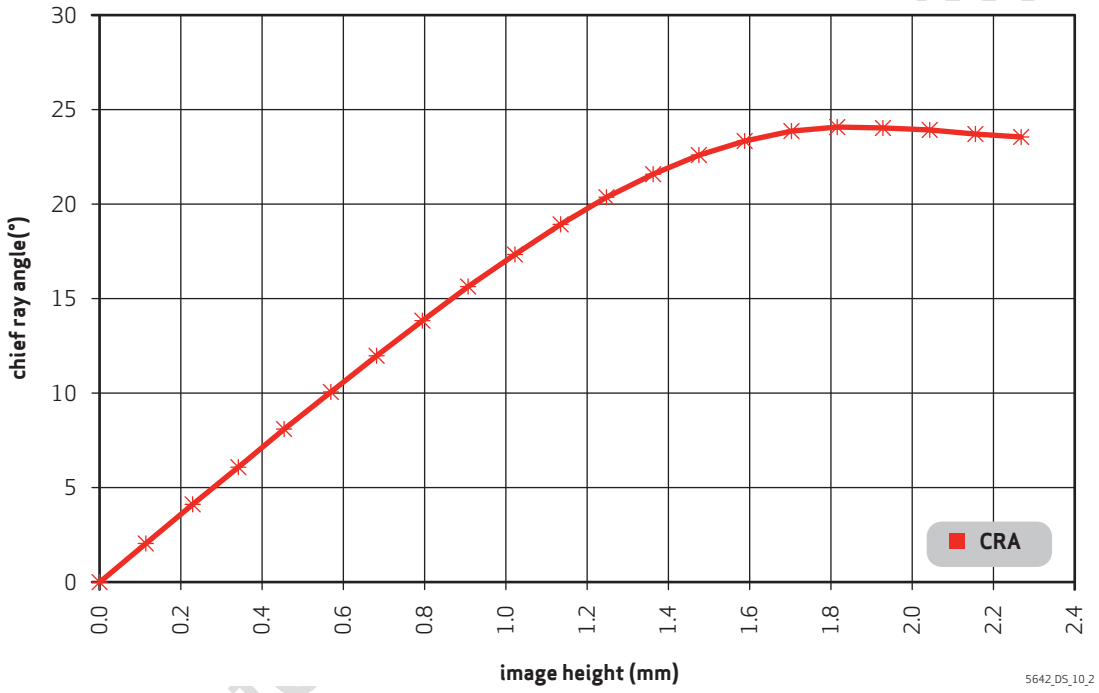

table 10-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0	0	0
0.05	0.114	2.0
0.1	0.227	4.1
0.15	0.341	6.1
0.2	0.454	8.1
0.25	0.568	10.1
0.3	0.681	12.0
0.35	0.795	13.8
0.4	0.908	15.6
0.45	1.022	17.3

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.5	1.135	18.9
0.55	1.249	20.4
0.6	1.362	21.6
0.65	1.476	22.6
0.7	1.589	23.4
0.75	1.703	23.9
0.8	1.816	24.1
0.85	1.930	24.1
0.9	2.043	23.9
0.95	2.157	23.7
1	2.270	23.6

revision history

version 1.0 07.15.2008

- initial release

version 1.1 11.19.2008

- made major revisions (too many to document) to whole datasheet

version 1.11 01.08.2009

- revised the ordering information from OV05642-V63A changed to OV05642-A63A
- revised table 9-1 in the package dimensions and removed symbol C4

the clear advantage™

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