TMS87C510 524 288-BIT UV ERASABLE MULTIPLEXED EPROM
TMS87PC510 524 288-BIT MULTIPLEXED PROM

SMLS851–JANUARY 1993

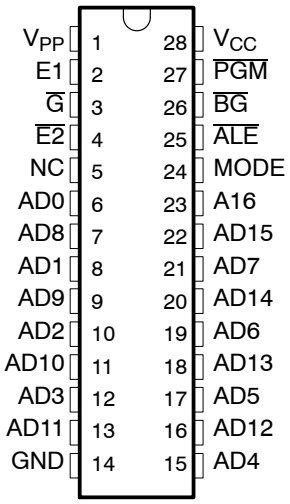
PRODUCT PREVIEW

- **Organization . . . 64K × 8 or 32K × 16**
- **Single 5-V Power Supply**
- **JEDEC Approved Pin Assignment (STD 21-C)**
- **Industry Standard 28-Pin Plastic and Ceramic Dual-In-Line Package, 32-Lead Plastic and Ceramic Chip Carrier**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

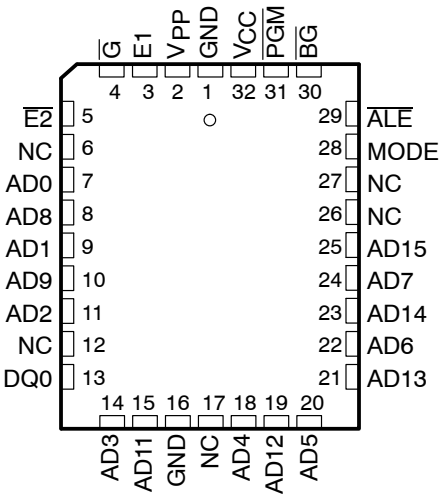
V_{CC} ± 5%	V_{CC} ± 10%	
’87C510-100		100 ns
’87PC510-100		100 ns
’87C510-120	’87C510-12	120 ns
’87PC510-120	’87PC510-12	120 ns
’87C510-150	’87C510-15	150 ns
’87PC510-150	’87PC510-15	150 ns
’87C510-200	’87C510-20	200 ns
’87PC510-200	’87PC510-20	200 ns

- **8-Bit or 16-Bit Output For Use in Microprocessor Based Systems**
- **On Chip Latches for Address and Data**
- **No Interface Needed to Most Microcontrollers**
- **TI Proprietary Novel Features**
  - **ON BOARD Programming**
  - **GLUE-LESS BUS INTERFACE™**
  - **FRIENDLY WRITE INTERFACE™**
- **Very High-Speed SNAP! Pulse Programming**
- **2 Byte or 1 Word Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **Differentiated Chip Enables:**
  - **E1 for Fast Access,**
  - **$\overline{E2}$ for Low Power Consumption**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 165 mW Worst Case**
  - **Economy . . . 55 mW (CMOS-Input Levels)**
  - **Power Down . . . 1.1 mW (CMOS-Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In and Choices of Operating Temperature Ranges**

J AND N PACKAGES†
(TOP VIEW)



FN AND FM PACKAGES†
(TOP VIEW)



† Packages are shown for pinout reference only.
‡ Pin 1 and Pin 16 must be externally connected to ground.

PIN NOMENCLATURE	
AD15–AD0	Address/Data Inputs/Outputs
$\overline{E1}$, E2	Chip Enable Inputs
$\overline{G}$	Output Enable
$\overline{PGM}$	Program Enable
$\overline{ALE}$	Address Latch Enable
$\overline{BG}$	Byte Mode Select
MODE	Bus Mode Select
NC	No Internal Conections
V_{CC}	5-V Power Supply
GND	Ground
V_{PP}	13-V Power Supply§

§ Only in program mode, 5-V or open in read mode.

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description

The TMS87C510 series are 524 288-bit, ultraviolet-light erasable, electrically programmable read-only memories. The TMS87PC510 series are 524 288-bit, one time, electrically programmable read-only memories. Address and data are fully multiplexed on the same pins (AD0–AD15). This allows minimizing the number of interconnection lines between the memory and industry standard microprocessors with time multiplexed address and data bus.

A bus mode control pin (MODE) allows the memory to be directly interfaced to either any Intel-like multiplexed bus or to any Motorola-like multiplexed bus without need of glue logic (GLUE-LESS BUS INTERFACE™).

A byte mode control pin $\overline{BG}$, in conjunction with AD0, allows the device to be used either as a byte wide (8 bit data input/output) or as a word wide (16 bit data input/output) memory. In particular no interface is required to 80C48/51, 80C88/98, 70C20/40/42, 68H05/11 8-bit families and 80C86/186, 80C96/196 16-bit families of microprocessors/microcontrollers.

The TMS87C510 and TMS87PC510 can be programmed using V_{PP} = 13 V, V_{CC} = 5 V (SNAP! Pulse programming algorithm) for a minimum programming time of 7 sec. and a maximum programming time of 70 sec. An internal voltage reference allows the memory to be programmed without changing the 5-V supply available at the P.C. board level. In this way the chip can be programmed without removing it from the board. This facility, not available on standard EPROMs, is called *ON BOARD* Programming.

Unlike any other EPROM, THE TMS87C510 and TMS87PC510 are internally provided with a write interface that allows the microprocessor to control programming of the memory by using short pulse signals at the beginning and at the end of each program operation (FRIENDLY WRITE INTERFACE™), this avoids keeping the $\overline{PGM}$ line and the address and data lines steady throughout the program operation.

The TMS87C510 and TMS87PC510 are provided with two enable pins: active high E1 and active low $\overline{E2}$. The memory is enabled only when both enable pins are active. The availability of two enable pins increases flexibility in using this memory in systems where either the response speed, or low power consumption is a key concern. E1 allows the memory to respond quickly and therefore can be activated just before strobing data in or out whereas $\overline{E2}$ needs to be asserted earlier, but guarantees the lowest power consumption while inactive.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS87C510 EPROM is offered in both 28 pin dual in-line ceramic package (J suffix) and 32-lead chip-carrier ceramic package (FN suffix).
The TMS87PC510 OTP PROM is offered in both 28 pin dual in-line plastic package (N suffix) and 32-lead chip-carrier plastic package (FM suffix).
The TMS87C510 and TM87PC510 are offered with three choices of temperature ranges of 0°C to 70°C, – 40°C to 85°C and – 40°C to 110°C.
The TMS87C510 is also offered with 168-Hour Burn-in for all temperature ranges. (See table below).

EPROM AND OTP PROM	SUFFIC FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN			SUFFIX FOR PEP4 168-HOUR BURN-IN VS TEMPERATURE RANGES		
	0°C TO 70°C	– 40°C TO 85°C	– 40°C TO 110°C	0°C TO 70°C	– 40°C TO 85°C	– 40°C TO 110°C
TMS87C510_xxx	JL/FNL	JE/FNE	JQ/FNQ	JL4/FNL4	JE4/FNE4	JQ4/FNQ4
TMS87PC510_xxx	NL/FML	NE/FME	NQ/FMQ			

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These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming. All programming signals are TTL level. These devices are programmable using the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 5 V for a nominal programming time of seven seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

A key feature of this family of devices is the direct interfaceability to either of the two standard microprocessor control busses widely known as Intel-like and Motorola-like busses.

When the MODE pin is tied to V_{CC}, the TMS87C510 and TMS87PC510 are directly compatible with the Intel- mode bus scheme.

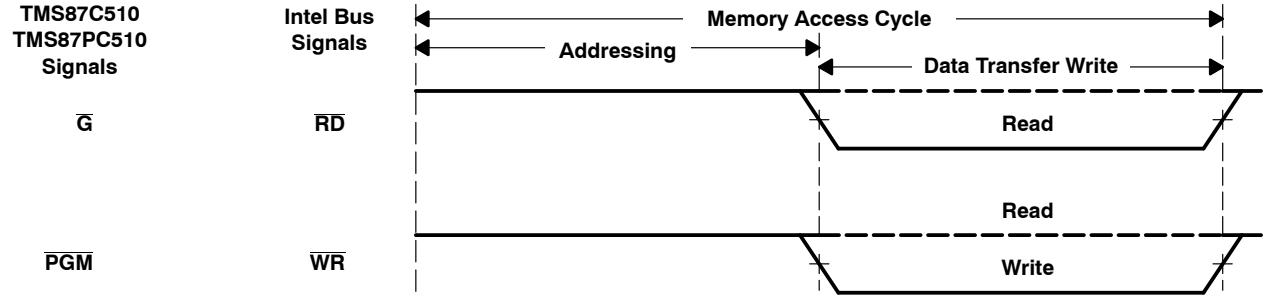

Figure 1. Intel-Mode Control Bus

When the MODE pin is tied to GND, the TMS87C510 and TMS87PC510 are directly compatible with the Motorola- mode bus scheme.

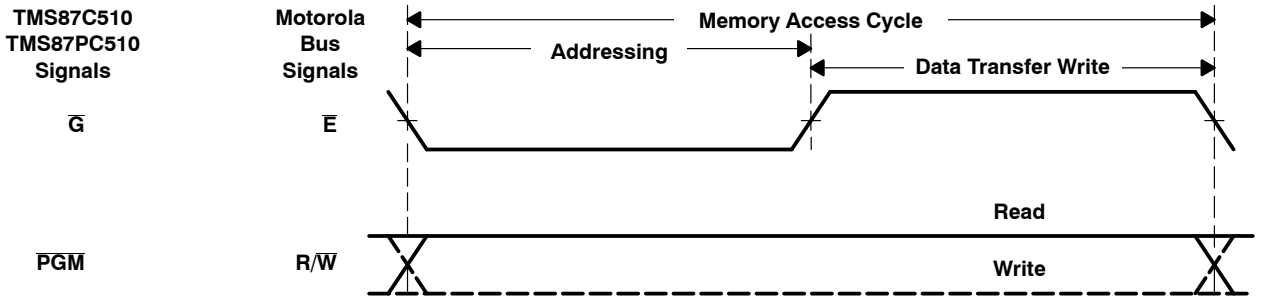

Figure 2. Motorola-Mode Control Bus

operation

Intel-mode (MODE = V_{CC})

The ten device-level modes of operation are listed in the following table. The read mode requires a single 5 V supply. All inputs are TTL level except V_{PP} during programming is 13 V, MODE in all modes is 5 V and $\overline{E2}$ in signature mode is 12 V.

MODE / FORMAT	READ				WRITE				STAND BY	POWER DOWN
	ADDR IN	READ DATA	OUTPUT DISABLE	SIGNATURE MODE	ADDR IN	PROGRAM DATA	PROGRAM VERIFY	PROGRAM INHIBIT		
E1	X	V_{IH}	V_{IL} or V_{IH} or V_{IH}	V_{IH}	X	V_{IH}	V_{IH}	V_{IL} or V_{IH}	V_{IL}	X
$\overline{E2}$	V_{IL}	V_{IL}		HV†	V_{IL}	V_{IL}	V_{IL}		V_{IL}	V_{IH}
$\overline{G}$	V_{IH}	V_{IL}		V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	X
$\overline{PGM}$	V_{IH}	V_{IH}	X	V_{IH}	V_{IH}	V_{IL}§	V_{IH}	X	X	X
$\overline{ALE}$	V_{IH}	V_{IL}	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	X	X	X
$\overline{BG}$	AIN‡	X	X	X	AIN	X	X	X	X	X
V_{PP}	5 V or open	5 V or open	5 V or open	5 V or open	13 V	13 V	13 V	13 V	5 V or open	5 V or open
V_{CC}	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V
AD0	AIN‡	DOUT/Z‡	Z	MFG/DEV CODE	AIN‡	DIN/X‡	DOUT/Z‡	Z	Z	Z
AD1–AD7	AIN	DOUT/Z‡	Z		AIN	DIN/X‡	DOUT/Z‡	Z	Z	Z
AD8–AD15	AIN	DOUT/Z‡	Z	00	AIN	DIN/X‡	DOUT/Z‡	Z	Z	Z
MODE	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V

X = Don't care input
Z = High impedance output
† High voltage = 12 V ± 0.5 V
‡ See Input/Output Truth Table
§ Data loaded when asserted and programmed when deasserted until dummy read is executed

INPUT/OUTPUT TRUTH TABLE				
$\overline{BG}$	AD0	D 15:8	D 7:0	WIDTH
LOW	LOW	UPPER BYTE	LOWER BYTE	WORD
LOW	HIGH	UPPER BYTE	X / HIGH-Z	BYTE
HIGH	LOW	X / HIGH-Z	LOWER BYTE	BYTE
HIGH	HIGH	X / HIGH-Z	UPPER BYTE	BYTE

Below is the functional table for the MOTOROLA-mode. (MODE = GND).

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operation

Motorola-mode (MODE = GND)

The ten device-level modes of operation are listed in the in the following table. The read mode requires a single 5 V supply. All inputs are TTL level except V_{PP} during programming is 13 V, MODE in all modes is 0 V and $\overline{E2}$ in signature mode is 12 V.

MODE / FORMAT	READ				WRITE				STAND BY	POWER DOWN
	ADDR IN	READ DATA	OUTPUT DISABLE	SIGNATURE MODE	ADDR IN	PROGRAM DATA	PROGRAM VERIFY	PROGRAM INHIBIT		
E1	X	V_{IH}	V_{IL} or V_{IH} or V_{IH}	V_{IH}	X	V_{IH}	V_{IH}	V_{IL} or V_{IH}	V_{IL}	X
$\overline{E2}$	V_{IL}	V_{IL}		HV†	V_{IL}	V_{IL}	V_{IL}		V_{IL}	V_{IH}
$\overline{G}$	V_{IH}	V_{IH}		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X
$\overline{PGM}$	V_{IH}	V_{IH}	X	V_{IH}	V_{IL}	V_{IL}§	V_{IH}	X	X	X
$\overline{ALE}$	V_{IH}	V_{IL}	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	X	X	X
$\overline{BG}$	AIN‡	X	X	X	AIN‡	X	X	X	X	X
V_{PP}	5 V or open	5 V or open	5 V or open	5 V or open	13 V	13 V	13 V	13 V	5 V or open	5 V or open
V_{CC}	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V
AD0	AIN‡	DOUT/Z‡	Z	MFG/DEV CODE	AIN‡	DIN/X‡	DOUT/Z‡	Z	Z	Z
AD1–AD7	AIN	DOUT/Z‡	Z		AIN	DIN/X‡	DOUT/Z‡	Z	Z	Z
AD8–AD15	AIN	DOUT/Z‡	Z	00	AIN	DIN/X‡	DOUT/Z‡	Z	Z	Z
MODE	0 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V

X = Don't care input
Z = High impedance output
† High voltage = 12 V ± 0.5 V
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§ Data loaded when asserted and programmed when deasserted until dummy read is executed

INPUT/OUTPUT TRUTH TABLE				
$\overline{BG}$	AD0	D 15:8	D 7:0	WIDTH
LOW	LOW	UPPER BYTE	LOWER BYTE	WORD
LOW	HIGH	UPPER BYTE	X / HIGH-Z	BYTE
HIGH	LOW	X / HIGH-Z	LOWER BYTE	BYTE
HIGH	HIGH	X / HIGH-Z	UPPER BYTE	BYTE

address latching

Multiplexing of address and data consists of issuing a set of valid values on address lines AD0–AD15, and signal $\overline{BG}$, at the beginning of every memory access cycle along with a valid address strobe $\overline{ALE}$.

The address values are latched onto a set of static registers internal to the memory by using the $\overline{ALE}$ signal as transparent address latch enable. The described operation is called address latching. After this phase, lines AD0–AD15 are made available for data transfer.

Multiplexing of address and data on the same line implies that on the bus AD0–AD15 will be present at different times either information related to the address (indicated specifically with A0–A15 and generally with AIN) or information related to the data (indicated specifically with D0–D15 and generally with DIN or DOUT).

During the address latching phase it is not required to have both E1, $\overline{E2}$ chip enables active. In particular the access time is not affected by delays in the external decoding used to enable the memory chip with E1, if $\overline{E2}$ has been asserted since the beginning of the current memory access cycle or earlier (see economy mode).

During address latching the signals $\overline{BG}$ and AD0 are latched and decoded to configure the memory chip input/output data width to be either a word (16 bit data), or a byte (8 bit data). (See input/output truth tables, pages 4, 5).

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Configurations are as follows:

- $\overline{BG}$ = low, AD0 = low: data width is a word. The lower byte (i.e., the even address byte, AD0 = 0) and the upper byte (the odd address byte, AD0 = 1) are simultaneously transferred on address/data lines with lower byte on lower half of address/data lines and upper byte on upper half of address/data lines.
- $\overline{BG}$ = low, AD0 = high: data width is a byte. The upper byte (the odd address byte AD0 = 1) is transferred on upper half of address/data lines.
- Cases with $\overline{BG}$ = high correspond to standard byte wide memory operation. Data is always transferred on the lower half of address/data lines. AD0 has the usual meaning of least significant bit of the byte address.

The address latch operation is the same in both read and write modes except for V_{PP} value.

output disable

When the outputs of two or more TMS87C510 or TMS87PC510 are connected in parallel on the same bus, the output of any particular device can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low-level is applied to the $\overline{E2}$ and $\overline{G}$ pins and a high level is applied to E1 pin. All other devices in the circuit should have their outputs disabled by applying a high level signal to either $\overline{E2}$ or $\overline{G}$ pins or a low level to E1 pin.

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latchup immunity

Latchup immunity on the TMS87C510 and TMS87PC510 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, "*Design Considerations; Latchup Immunity of the HVCMOS EPROM Family*", available through TI Sales Offices.

power down and economy/standby modes

Active I_{CC} supply current can be reduced from 30 mA to 200 μA for a high CMOS input on $\overline{E2}$ (power down mode) or to 10 mA for a low CMOS input on both E1, and $\overline{E2}$ (economy or standby mode). All other inputs are supposed to be steady CMOS level (for TTL input levels the power consumption is higher). In either mode, all outputs are in the high-impedance state.

erasure (TMS87C510)

Before programming, the TMS87C510 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W-s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS87C510, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

inititalizing (TMS87PC510)

The one-time programmable TMS87PC510 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS87C510 and TMS87PC510 PROM are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 3, which programs in a minimum time of seven seconds. Actual programming time will vary as a function of the programmer used.

The SNAP! Pulse programming algorithm uses internal pulse of t_{pw} = 100 µs followed by a data verification to determine when the addressed location has been successfully programmed. Up to ten 100-µs pulses per location are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 5 V, E1 = V_{IH}, $\overline{E2}$ = V_{IL} and $\overline{G}$ = V_{IH} in Intel-mode ($\overline{PGM}$ = V_{IL} in Motorola-mode). Once addresses are latched and data are issued, $\overline{PGM}$ is pulsed low ($\overline{G}$ is pulsed high) for a minimum time of 50 nsec. Depending on the data transfer mode the memory is operating in (see input/output truth table, pages 4, 5) the data to be programmed is handled, before the actual program operation can start, in the way reported below.

- $\overline{BG}$ = low, AD0 = low: data width is a word. Rising edge of $\overline{PGM}$ (falling edge of $\overline{G}$) latches the 16 bit data into the internal 16 bit data register and an internal programming operation is started.
- $\overline{BG}$ = low, AD0 = high: data width is a byte. Rising edge of $\overline{PGM}$ (falling edge of $\overline{G}$) latches the 8 bit data present on lines AD8–AD15 into the upper byte of the internal data register and an internal programming operation is started.
- $\overline{BG}$ = high, AD0 = high: data width is a byte. Rising edge of $\overline{PGM}$ (falling edge of $\overline{G}$) latches the 8 bit data present on lines AD0–AD7 into the upper byte of the internal data register and an internal programming operation is started.
- $\overline{BG}$ = high, AD0 = high: data width is a byte. Rising edge of $\overline{PGM}$ (falling edge of $\overline{G}$) latches the 8 bit data present on lines AD0–AD7 into the lower byte of the internal data register. After this data latch, another data latch operation must be executed for upper byte ($\overline{BG}$ = high, AD0 = high); the second $\overline{PGM}$ ($\overline{G}$ pulse) will latch the 8 bit data into the upper byte of the internal data register and will start the internal programming operation.

Two byte latching allows to reduce programming time since two bytes are programmed with only one internal programming operation. In case only one byte program operation is required, a dummy write of FF (Hex) into the other byte of the internal 16 bit data register must be done.

Once activated, the internal programming operation prevents the latched address from being modified by bus data transfer activity until programming is complete. However it is recommended not to reiterate write cycles to the memory since this may result in corruption of the data being programmed.

The internal programming operation enables the contents of the internal 16 bit data register to be permanently stored into the memory array at the desired location.

The internal programming operation is terminated (after 100 µs min) when a dummy read is executed, with $\overline{G}$ pulsed low (pulsed high) for a minimum time of 50 nsec, and the device is enabled.

This technique to generate the internal enable signal for program operation is called FRIENDLY WRITE™ and allows the microprocessor to easily control program operation with the simplest interfacing possible.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{PP} = V_{CC} or open.

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ON BOARD Programming

Unlike a standard EPROM, the TMS87C510 and TMS87PC510 need not raise V_{CC} to 6.5 V since this voltage is generated internally when V_{PP} = 12.5 V. This provision is called ON BOARD Programming and simplifies the design of systems featuring in-field programming.

program inhibit

Programming may be inhibited by maintaining a high level input on $\overline{E2}$ or $\overline{PGM}$, or a low level input on E1.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, E1 = V_{IH}, $\overline{E2} = V_{IL}$ and $\overline{PGM} = V_{IH}$. This assures that adequate read margin is used to obtain the same data retention as standard devices.

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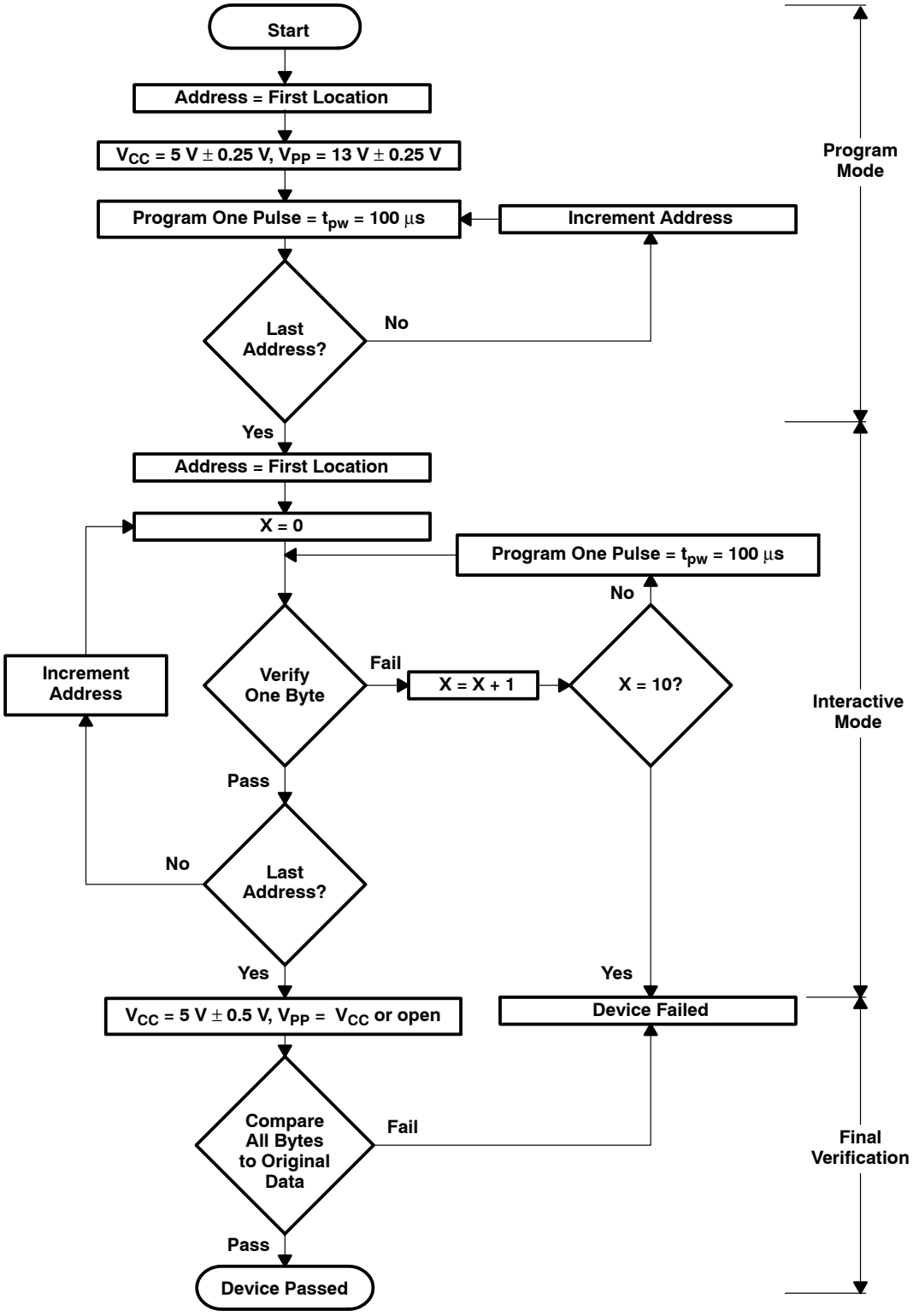

Figure 3. SNAP! Pulse Programming Flowchart

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signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when $\overline{E2}$ is forced to 12 V (word width only is allowed). Two identifier bytes are accessed by different values of AD0. All other addresses must be helf low. The signature code for these devices is 97 B0. AD0 low selectes the manufacturere's code 97 (Hex), and AD0 high selects the device code B0 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	AD0	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	1	0	1	1	0	0	0	0	B0

† E1 = V_{IH}, $\overline{G}$ pulsed low when readinig out, $\overline{E2}$ = HV, A1–A15 = V_{IL}, V_{PP} = V_{CC} or open.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.6 V to 7 V
Supply voltage range, V_{PP} . . . . . –0.6 V to 14 V
Input voltage range: All inputs except $\overline{E2}$ . . . . . –0.6 V to V_{CC} + 1 V
$\overline{E2}$ . . . . . –0.6 V to 13.5 V
Output voltage range, with respect to GND (see Note 1) . . . . . –0.6 V to V_{CC} + 1 V
Operating free-air temperature range (’87C510-_ _JL/FNL/FNL4 and
’87PC510-_ _NL/FML) . . . . . –0°C to 70°C
Operating free-air temperature range (’87C510-_ _JE/FNE/JE4/FNE4 and
’87PC510-_ _NE/FME) . . . . . –40° C to 85°C
Operating free-air temperature range (’87C510-_ _JQ/FNQ/FQ4/FNQ4 and
’87PC510-_ _NQ/FMQ) . . . . . –40° C to 110°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			’87C510/PC510-100 ’87C510/PC510-120 ’87C510/PC510-150 ’87C510/PC510-200			’87C510/PC510-12 ’87C510/PC510-15 ’87C510/PC510-20			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage (see Note 2)		4.75	5	5.25	4.75	5	5.5	V
V_{PP}	Supply voltage	Read Mode (see Note 3)	V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V
		SNAP! Pulse Programming Algorithm	12.75	13	13.25	12.75	13	13.25	V
V_{IH}	High-level input voltage	TLL	2.0		V_{CC} + 0.5	2.0		V_{CC} + 0.5	V
		CMOS	V_{CC} – 0.2		V_{CC} + 0.5	V_{CC} – 0.2		V_{CC} + 0.5	
V_{IL}	Low-level input voltage	TTL	– 0.5		0.8	– 0.5		0.8	V
		CMOS	– 0.5		GND + 0.2	– 0.5		GND + 0.2	
T_A	Operating free-air temperature	’87C510__JL/FNL/FNL4 ’87PC510__NL/FML	0		70	0		70	°C
T_A	Operating free-air temperature	’87C510__JE/FNE/FNE4 ’87PC510__NE/FME	– 40		85	– 40		85	°C
T_A	Operating free-air temperature	’87C510__JQ/FNQ/FNQ4 ’87PC510__NQ/FMQ	– 40		110	– 40		110	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly or left open (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

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electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 20 mA	V_{CC} – 0.2			V
			I_{OH} = – 2 mA	2.4			
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 µA			0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V			±1	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V			10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V			50	mA
I_{CC1}	V_{CC} supply current (power down)	TTL-input level	$\overline{E2}$ = V_{IH}, V_{CC} = 5 V, V_{PP} open			450	µA
		CMOS-input level	$\overline{E2}$ = V_{CC} = 5.5 V, V_{PP} open			200	
I_{CC2}	V_{CC} supply current (economy)	TTL-input level	E1 = $\overline{E2}$ = V_{IL}, V_{CC} = 5 V, V_{PP} open			10	mA
		CMOS-input level	E1 = $\overline{E2}$ = GND, V_{CC} = 5.5 V, V_{PP} open			10	
I_{CC2}	V_{CC} supply current (active)		E1 = V_{IH}, $\overline{E2}$ = V_{IL}, V_{CC} = 5.5 V t_{cycle} = minimum cycle time†, outputs open			30	mA

† Minimum cycle time = maximum address access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		4	8	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		6	10	pF

‡ Capacitance measurements are made on a sample basis only.
§ All typical values are at T_A = 25°C and nominall voltages.

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switching characteristics over full ranges of recommended operating conditions (see Notes 4)

PARAMETER		TEST CONDITIONS	'87C510-100 '87PC510-100		'87C510-120 '87PC510-120 '87C510-12 '87PC510-12		'87C510-150 '87PC510-150 '87C510-15 '87PC510-15		'87C510-200 '87PC510-200 '87C510-20 '87PC510-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns,		100		120		150		200	ns
$t_{a(E1)}$	Access time from chip enable E1			50		60		75		100	ns
$t_{a(E2)}$	Access time from chip enable $\overline{E2}$			100		120		150		200	ns
$t_{en(G)}$	Enable time, output from $\overline{G}$			50		55		75		75	ns
t_{dis}	Disable time, output from $\overline{G}$ or E1 or $\overline{E2}$, whichever occurs first†		0	50	0	50	0	60	0	60	ns
$t_{w(AL)des}$	Address latch deselect duration		25		30		50		50		ns
$t_{su(ALE)}$	Setup time, address to latch enable		6		10		30		30		ns
$t_{h(LEA)}$	Hold time, address from latch enable		10		10		20		20		ns
$t_{t(DLE)}$	Data transfer to latch enable		10		10		10		10		ns

† Value calculated from 0.5 V delta to measured level.

recommended timing requirements for programming: VCC = 5 V and VPP = 13 V (SNAP! Pulse programming), TA = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{w(P)}$	Internal program operation duration	95	100	105	µs
$t_{w(W)}$	Pulse duration, write	50			ns
$t_{w(R)}$	Pulse duration, read	50			ns
$t_{su(E1)}$	Setup time, E1	80			ns
$t_{su(E2)}$	Setup time, $\overline{E2}$	25			ns
$t_{su(D)}$	Setup time, data	40			ns
$t_{h(D)}$	Hold time, data				ns
$t_{su(VPP)}$	Setup time, V_{PP}	800			µs
$t_{c(ALE)}$	Cycle time, $\overline{ALE}$				

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2.0 V for logic high and 0.8 V for logic low (reference AC Testing Wave Form).

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PARAMETER MEASUREMENT INFORMATION

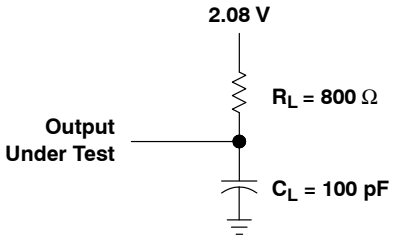
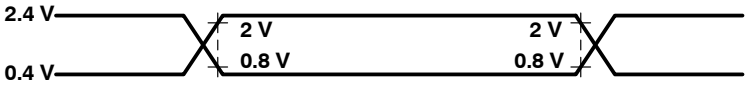


Figure 4. AC Testing Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

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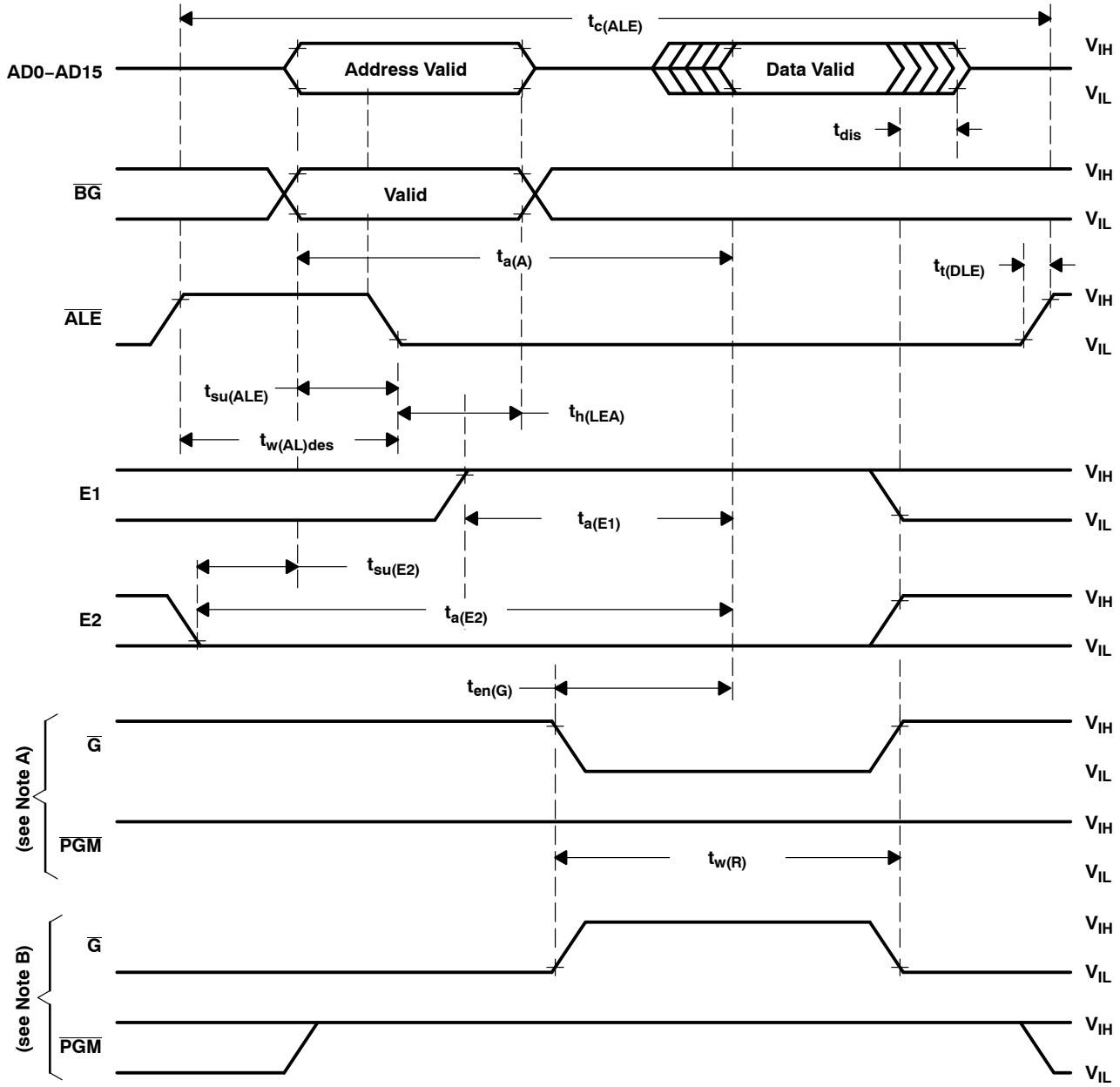
PARAMETER MEASUREMENT INFORMATION



NOTES: A. INTEL mode, MODE = V_{CC}.
B. MOTOROLA mode, MODE = GND.

Figure 5. Read Cycle Timing

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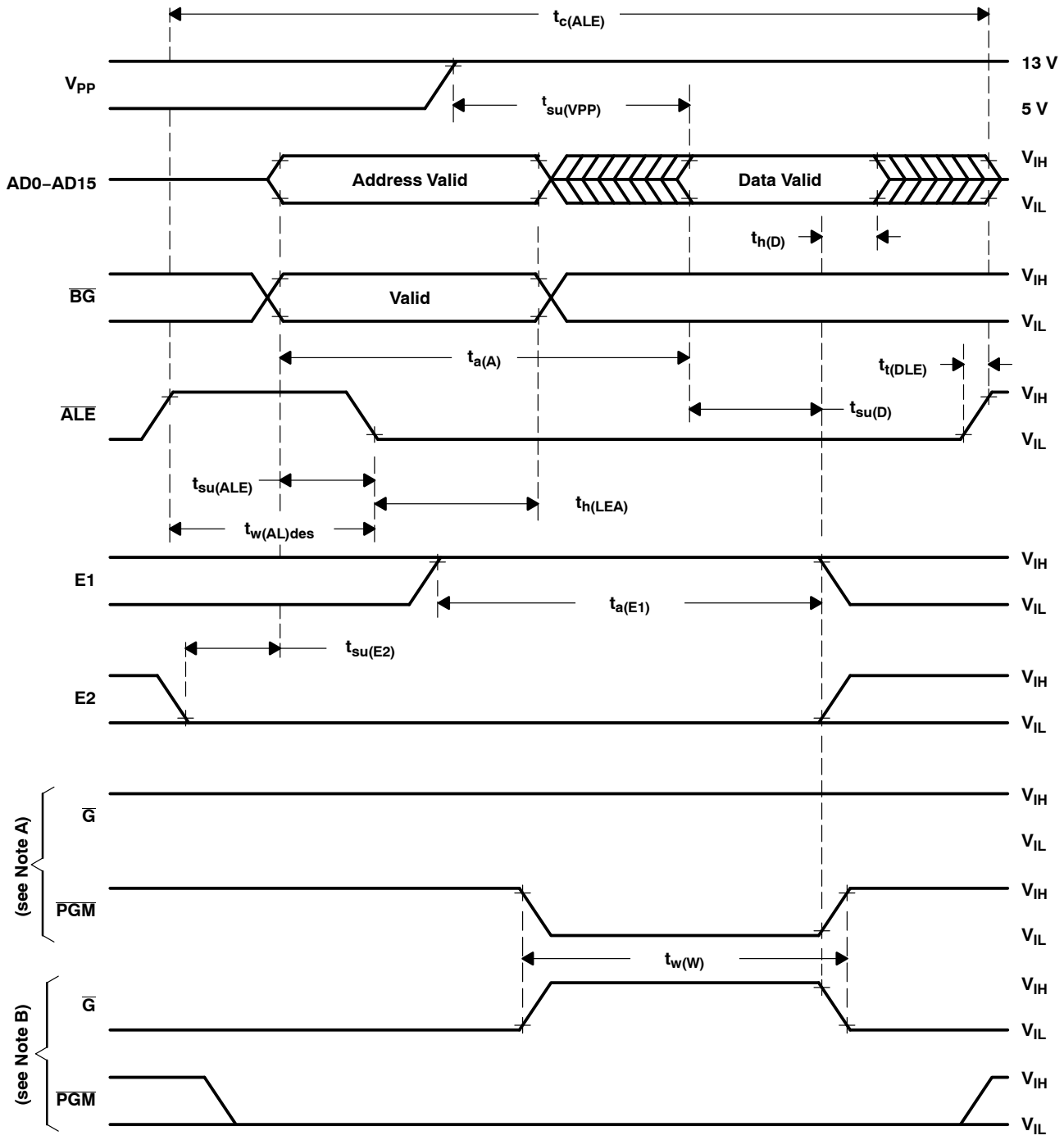
PARAMETER MEASUREMENT INFORMATION



NOTES: A. INTEL mode, MODE = V_{CC}.
B. MOTOROLA mode, MODE = GND.

Figure 6. Write Cycle Timing

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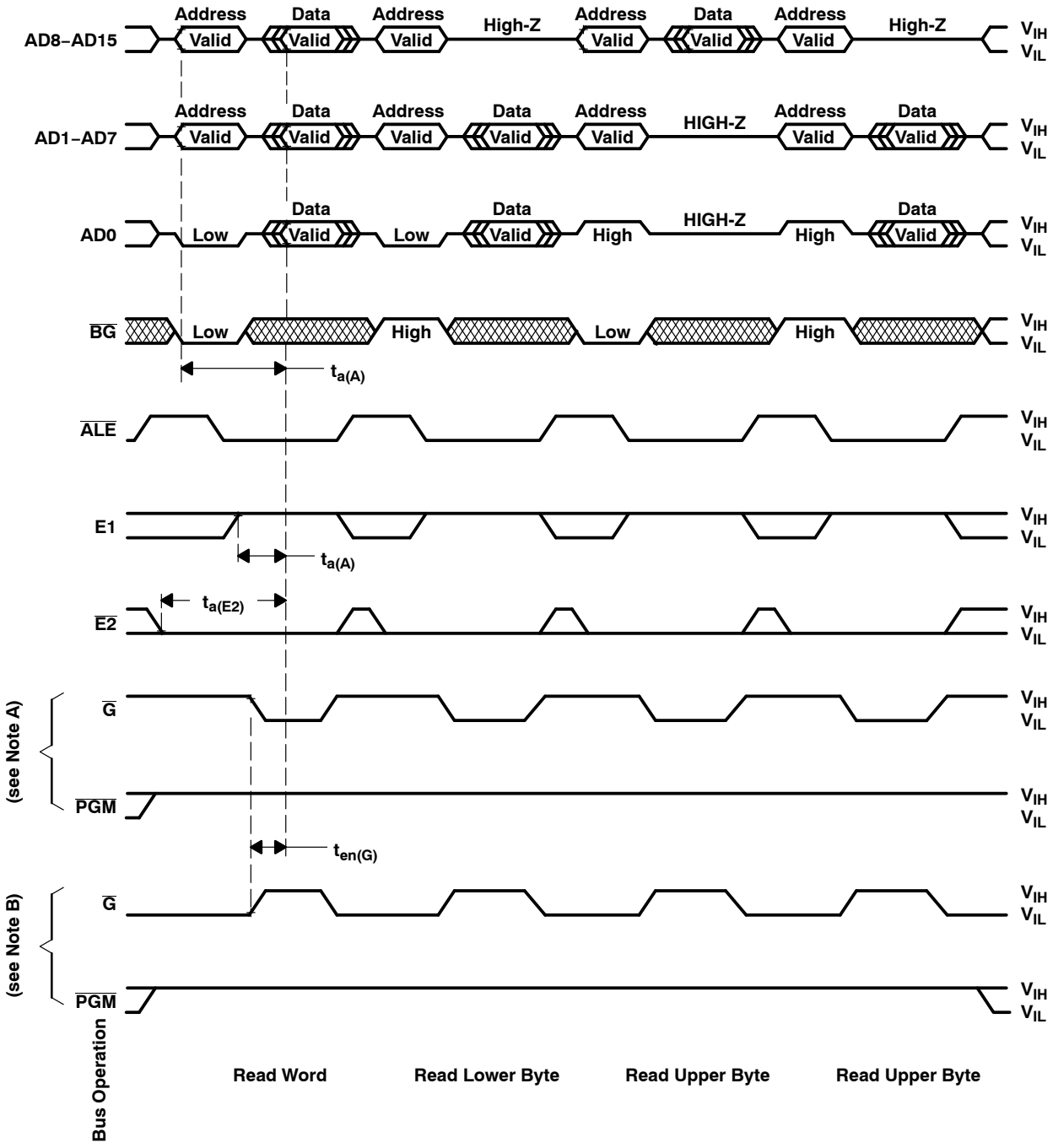
PARAMETER MEASUREMENT INFORMATION



NOTES: A. INTEL mode, MODE = V_{CC}.
B. MOTOROLA mode, MODE = GND.

Figure 7. Word/Byte Read Cycle Timing

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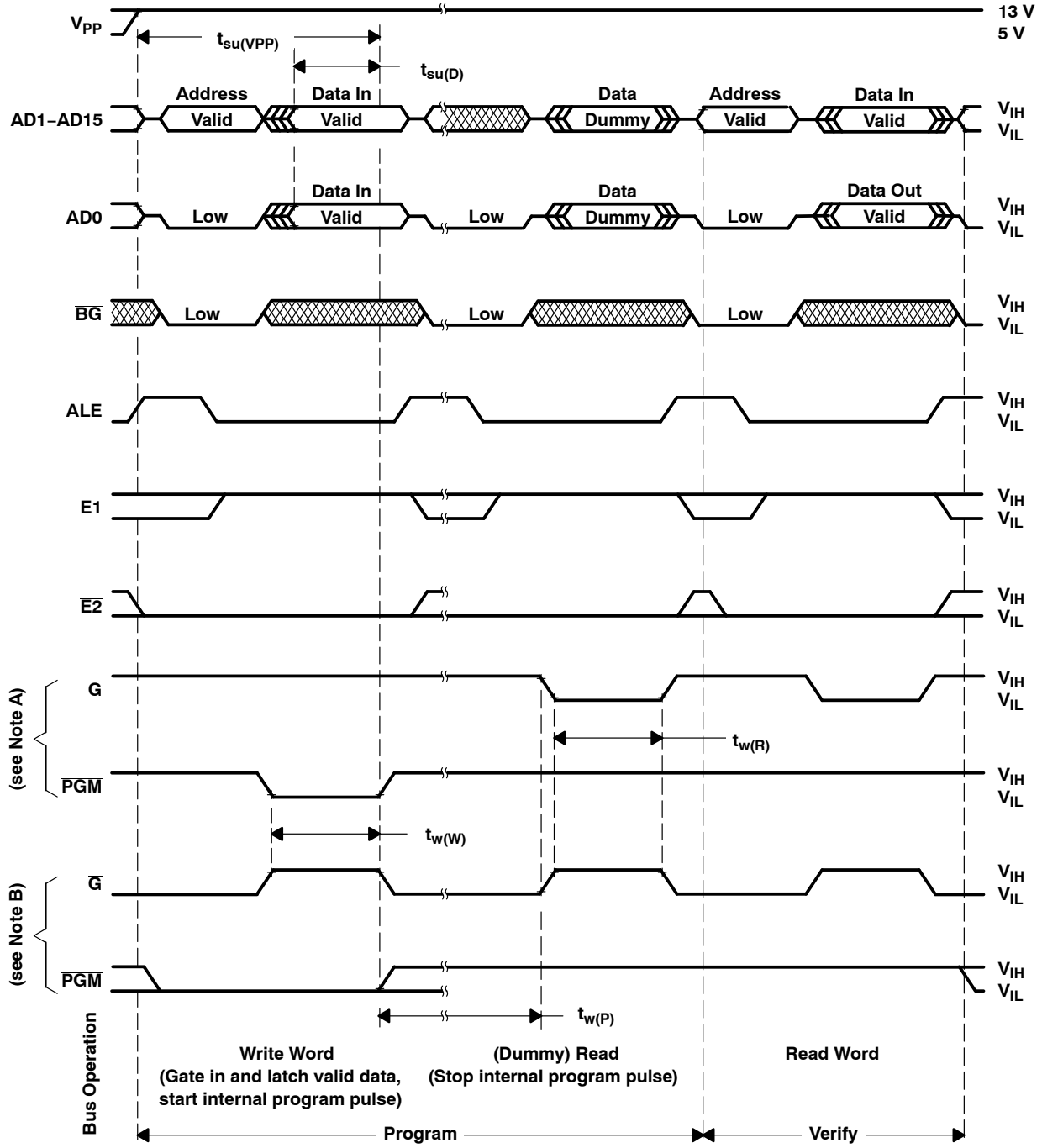
PARAMETER MEASUREMENT INFORMATION



NOTES: A. INTEL mode, MODE = V_{CC}.
B. MOTOROLA mode, MODE = GND.

Figure 8. Program Cycle Timing—One 16 Bit Data (Word)

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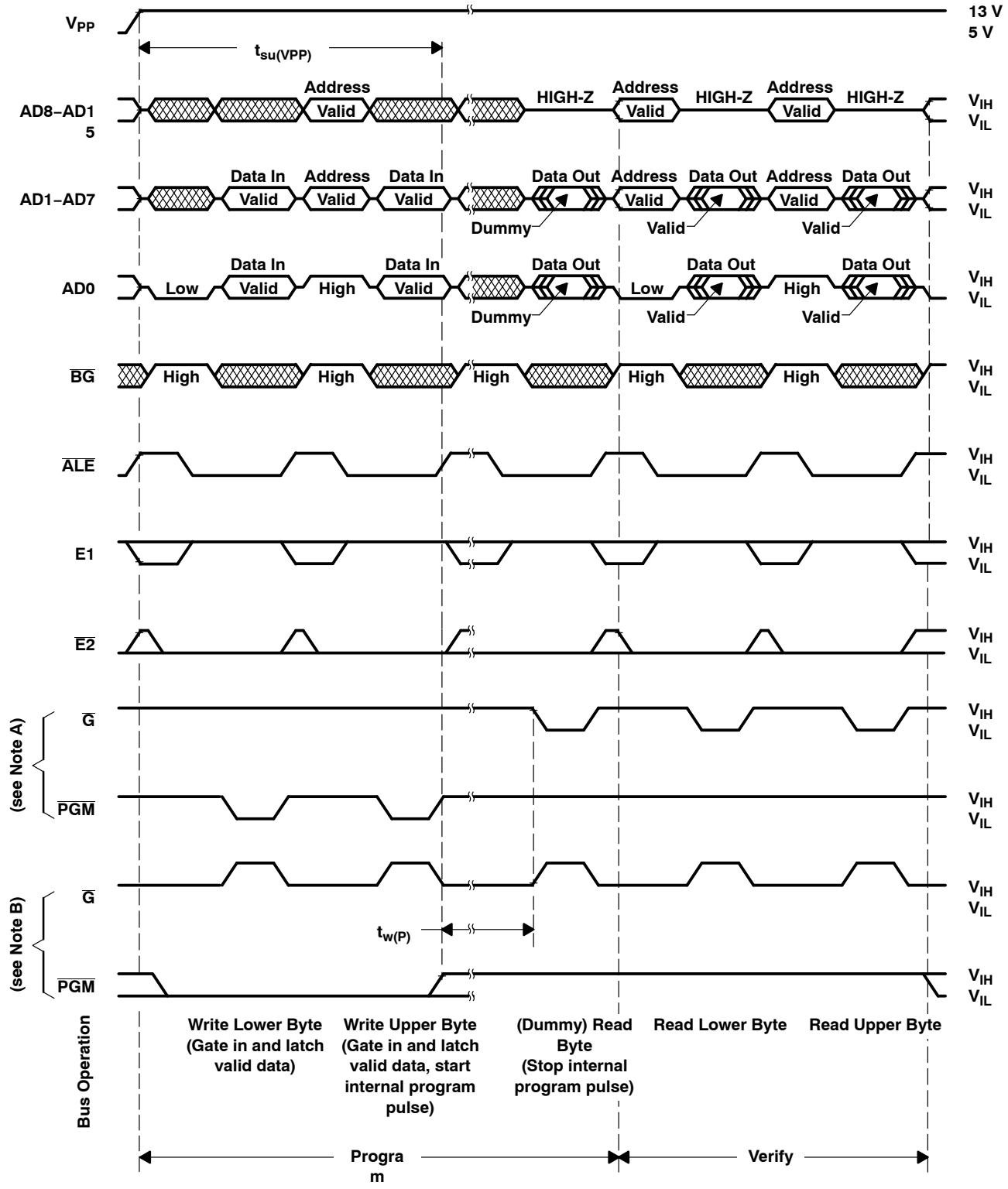
PARAMETER MEASUREMENT INFORMATION



NOTES: A. INTEL mode, MODE = V_{CC}.
B. MOTOROLA mode, MODE = GND.

Figure 9. Programming Waveform—Two 8 Bit Data (Bytes) in 16 Bit Data Bus

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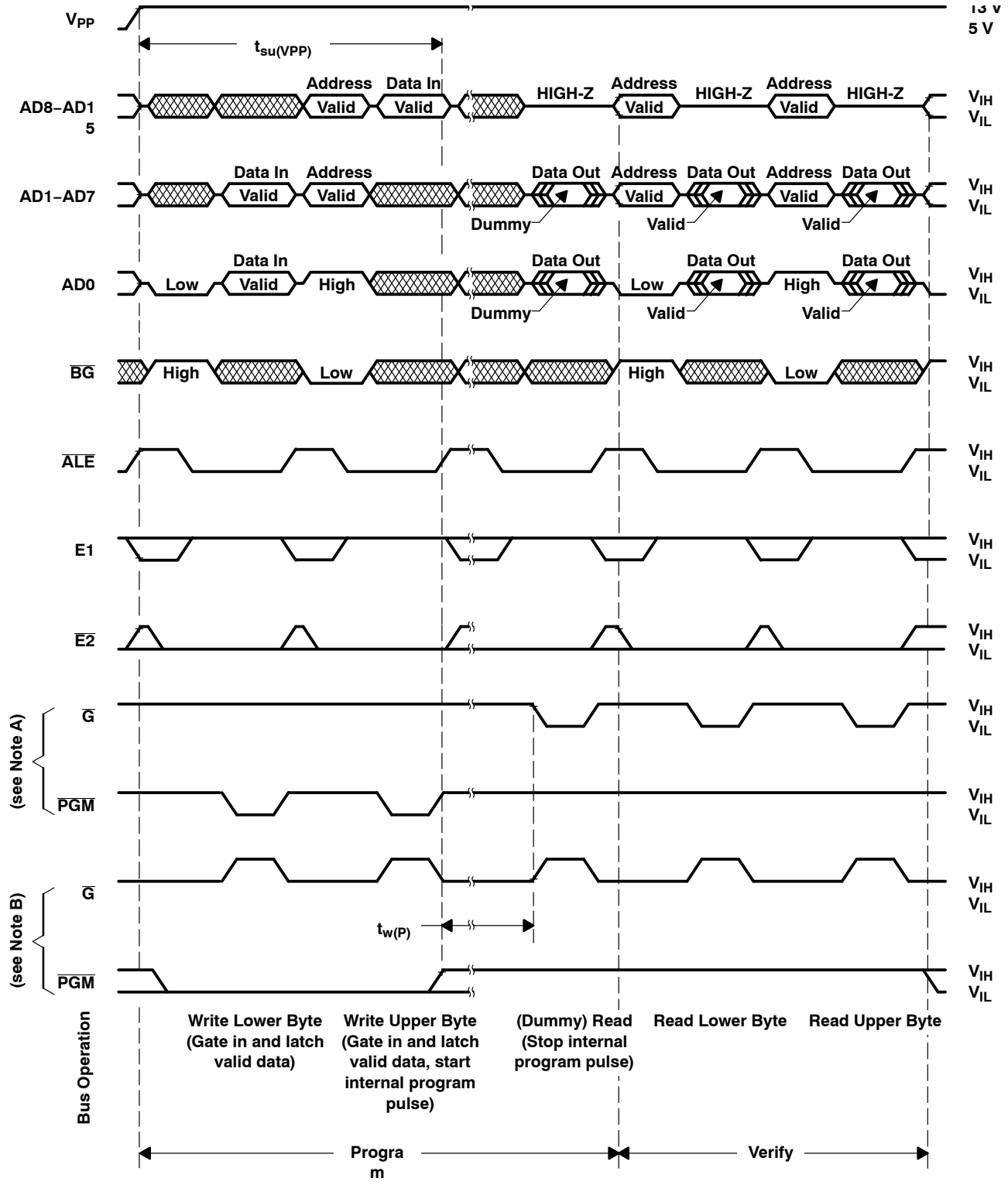
PARAMETER MEASUREMENT INFORMATION



NOTES: A. INTEL mode, MODE = V_{CC}.
B. MOTOROLA mode, MODE = GND.

Figure 10. Programming Waveform—Two 8 Bit Data (Bytes) in 16 Bit Data Bus

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