AD7124Library

1.0.0

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Namespace Documentation

2.1 Ad7124 Namespace Reference

General namespace.

Enumerations

- enum BurnoutCurrent { BurnoutOff = 0, Burnout500nA, Burnout2uA, Burnout4uA }

  These bits select the magnitude of the sensor burnout detect current source.
- enum ClkSel { InternalClk = 0, InternalWithOutputClk, ExternalClk, ExternalDiv4Clk }

  These bits select the clock source for the ADC Either the on-chip 614.4 kHz clock can be used or an external clock can be used. The ability to use an external clock allows several AD7124 devices to be synchronized. Also, 50 Hz and 60 Hz rejection is improved when an accurate external clock drives the ADC.
- enum FilterType {
  Sinc4Filter = 0, Sinc3Filter = 2, Sinc4FastFilter = 4, Sinc3FastFilter = 5,
  PostFilter = 7 }

  Filter type select bits. These bits select the filter type.
- enum InputSel {
  AIN0Input = 0, AIN1Input, AIN2Input, AIN3Input,
  AIN4Input, AIN5Input, AIN6Input, AIN7Input,
  TEMPInput = 16, AVSSInput, REFInput, DGNDInput,
  AVDD6PInput, AVDD6MInput, IOVDD6PInput, IOVDD6MInput,
  ALDO6PInput, ALDO6MInput, DLDO6PInput, DLDO6MInput,
  V20mVPInput, V20mVMInput }

  Analog input AIN input select.
- enum IoutCh {
  IoutCh0 = 0, IoutCh1 = 1, IoutCh2 = 4, IoutCh3 = 5,
  IoutCh4 = 10, IoutCh5 = 11, IoutCh6 = 14, IoutCh7 = 15 }

  Channel select bits for the excitation current for IOUT.
- enum IoutCurrent {
  CurrentOff = 0, Current50uA, Current100uA, Current250uA,
  Current500uA, Current750uA, Current1000uA }

  These bits set the value of the excitation current for IOUT.
- enum OperatingMode {
  ContinuousMode = 0, SingleConvMode, StandbyMode, PowerDownMode,
  IdleMode, InternalOffsetCalibrationMode, InternalGainCalibrationMode, SystemOffsetCalibrationMode,
  SystemGainCalibrationMode }

Control the mode of operation for ADC.

- enum PgaSel {
  Pga1 = 0, Pga2, Pga4, Pga8,
  Pga16, Pga32, Pga64, Pga128 }

  Gain select bits. These bits select the gain to use when converting on any channels using this configuration register.

- enum PostFilterType { dB47PostFilter = 2, dB62PostFilter = 3, dB86PostFilter = 5, dB92PostFilter = 6 }

  Post filter type select bits. When the filter bits are set to 1, the sinc 3 filter is followed by a post filter which offers good 50 Hz and 60 Hz rejection at output data rates that have zero latency approximately.

- enum PowerMode { LowPower = 0, MidPower, FullPower }

  Power Mode Select These bits select the power mode. The current consumption and output data rate ranges are dependent on the power mode.

- enum RefSel { RefIn1 = 0, RefIn2, RefInternal, RefAVdd }

  Reference source select bits. These bits select the reference source to use when converting on any channels using this configuration register.

2.1.1 Detailed Description

General namespace.

2.1.2 Enumeration Type Documentation

2.1.2.1 enum Ad7124::BurnoutCurrent

These bits select the magnitude of the sensor burnout detect current source.

Enumerator

BurnoutOff burnout current source off (default).

Burnout500nA burnout current source on, 0.5 A.

Burnout2uA burnout current source on, 2 A.

Burnout4uA burnout current source on, 4 A.

Definition at line 150 of file ad7124.h.

```
150                     {
151     BurnoutOff = 0,
152     Burnout500nA,
153     Burnout2uA,
154     Burnout4uA
155   };
```

2.1.2.2 enum Ad7124::ClkSel

These bits select the clock source for the ADC Either the on-chip 614.4 kHz clock can be used or an external clock can be used. The ability to use an external clock allows several AD7124 devices to be synchronized. Also, 50 Hz and 60 Hz rejection is improved when an accurate external clock drives the ADC.

Enumerator

InternalClk internal 614.4 kHz clock. The internal clock is not available at the CLK pin.

InternalWithOutputClk internal 614.4 kHz clock. This clock is available at the CLK pin.

ExternalClk external 614.4 kHz clock.

ExternalDiv4Clk external clock. The external clock is divided by 4 within the AD7124.

Definition at line 58 of file ad7124.h.

```
58              {
59     InternalClk = 0,
60     InternalWithOutputClk,
61     ExternalClk,
62     ExternalDiv4Clk
63   };
```

2.1.2.3 enum Ad7124::FilterType

Filter type select bits. These bits select the filter type.

Enumerator

Sinc4Filter sinc4 filter (default).

Sinc3Filter sinc 3 filter.

Sinc4FastFilter fast settling filter using the sinc 4 filter. The sinc 4 filter is followed by an averaging block, which results in a settling time equal to the conversion time. In full power and mid power modes, averaging by 16 occurs whereas averaging by 8 occurs in low power mode.

Sinc3FastFilter fast settling filter using the sinc 3 filter. The sinc 3 filter is followed by an averaging block, which results in a settling time equal to the conversion time. In full power and mid power modes, averaging by 16 occurs whereas averaging by 8 occurs in low power mode.

PostFilter post filter enabled. The AD7124 includes several post filters, selectable using the POST_FILTER bits. The post filters have single cycle settling, the settling time being considerably better than a simple sinc 3 /sinc 4 filter. These filters offer excellent 50 Hz and60 Hz rejection.

Definition at line 161 of file ad7124.h.

```
161                 {
162     Sinc4Filter = 0,
163     Sinc3Filter = 2,
164     Sinc4FastFilter = 4,
165     Sinc3FastFilter = 5,
166     PostFilter = 7
167   };
```

2.1.2.4 enum Ad7124::InputSel

Analog input AIN input select.

Enumerator

AIN0Input AIN0

AIN1Input AIN1

AIN2Input AIN2

AIN3Input AIN3

AIN4Input AIN4

AIN5Input AIN5

AIN6Input AIN6

AIN7Input AIN7

TEMPInput Temperature sensor (internal)

AVSSInput AVss

REFInput Internal reference

DGNDInput DGND.

AVDD6PInput (AVdd AVss)/6+. Use in conjunction with (AVdd AVss)/6 to monitor supply AVdd AVss .

AVDD6MInput (AVdd AVss)/6. Use in conjunction with (AVdd AVss)/6+ to monitor supply AVdd AVss .

IOVDD6PInput (IOVdd DGND)/6+. Use in conjunction with (IOVdd DGND)/6 to monitor IOVdd DGND.

IOVDD6MInput (IOVdd DGND)/6. Use in conjunction with (IOVdd DGND)/6+ to monitor IOVdd DGND.

ALDO6PInput (ALDO AVss)/6+. Use in conjunction with (ALDO AVss)/6 to monitor the analog LDO.

ALDO6MInput (ALDO AVss)/6. Use in conjunction with (ALDO AVss)/6+ to monitor the analog LDO.

DLDO6PInput (DLDO DGND)/6+. Use in conjunction with (DLDO DGND)/6 to monitor the digital LDO.

DLDO6MInput (DLDO DGND)/6. Use in conjunction with (DLDO DGND)/6+ to monitor the digital LDO.

V20mVPInput V_20MV_P. Use in conjunction with V_20MV_M to apply a 20 mV p-p signal to the ADC.

V20mVMInput V_20MV_M. Use in conjunction with V_20MV_P to apply a 20 mV p-p signal to the ADC.

Definition at line 95 of file ad7124.h.

```
95                {
96     AIN0Input = 0,
97     AIN1Input,
98     AIN2Input,
99     AIN3Input,
100     AIN4Input,
101     AIN5Input,
102     AIN6Input,
103     AIN7Input,
104     TEMPInput = 16,
105     AVSSInput,
106     REFInput,
107     DGNDInput,
108     AVDD6PInput,
109     AVDD6MInput,
110     IOVDD6PInput,
111     IOVDD6MInput,
112     ALDO6PInput,
113     ALDO6MInput,
114     DLDO6PInput,
115     DLDO6MInput,
116     V20mVPInput,
117     V20mVMInput
118   };
```

2.1.2.5 enum Ad7124::IoutCh

Channel select bits for the excitation current for IOUT.

Enumerator

IoutCh0 IOUT is available on the AIN0 pin.

IoutCh1 IOUT is available on the AIN1 pin.

IoutCh2 IOUT is available on the AIN2 pin.

IoutCh3 IOUT is available on the AIN3 pin.

IoutCh4 IOUT is available on the AIN4 pin.

IoutCh5 IOUT is available on the AIN5 pin.

IoutCh6 IOUT is available on the AIN6 pin.

IoutCh7 IOUT is available on the AIN7 pin.

Definition at line 81 of file ad7124.h.

```
81              {
82     IoutCh0 = 0,
83     IoutCh1 = 1,
84     IoutCh2 = 4,
85     IoutCh3 = 5,
86     IoutCh4 = 10,
87     IoutCh5 = 11,
88     IoutCh6 = 14,
89     IoutCh7 = 15
90   };
```

2.1.2.6 enum Ad7124::IoutCurrent

These bits set the value of the excitation current for IOUT.

Enumerator

CurrentOff Off

Current50uA 50 A

Current100uA 100 A

Current250uA 250 A

Current500uA 500 A

Current750uA 750 A

Current1000uA 1 mA

Definition at line 68 of file ad7124.h.

```
68                  {
69     CurrentOff = 0,
70     Current50uA,
71     Current100uA,
72     Current250uA,
73     Current500uA,
74     Current750uA,
75     Current1000uA
76   };
```

2.1.2.7 enum Ad7124::OperatingMode

Control the mode of operation for ADC.

Enumerator

ContinuousMode Continuous conversion mode (default). In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register.

SingleConvMode Single conversion mode. When single conversion mode is selected, the ADC powers up and performs a single conversion on the selected channel.

StandbyMode Standby mode. In standby mode, all sections of the AD7124 can be powered down except the LDOs.

PowerDownMode Power-down mode. In power-down mode, all the AD7124 circuitry is powered down, including the current sources, power switch, burnout currents, bias voltage generator, and clock circuitry.

IdleMode Idle mode. In idle mode, the ADC filter and modulator are held in a reset state even though the modulator clocks continue to be provided.

InternalOffsetCalibrationMode Internal zero-scale (offset) calibration. An internal short is automatically connected to the input. RDY goes high when the calibration is initiated and returns low when the calibration is complete.

InternalGainCalibrationMode Internal full-scale (gain) calibration. A full-scale input voltage is automatically connected to the selected analog input for this calibration.

SystemOffsetCalibrationMode System zero-scale (offset) calibration. Connect the system zero-scale input to the channel input pins of the selected channel. RDY goes high when the calibration is initiated and returns low when the calibration is complete.

SystemGainCalibrationMode System full-scale (gain) calibration. Connect the system full-scale input to the channel input pins of the selected channel. RDY goes high when the calibration is initiated and returns low when the calibration is complete.

Definition at line 29 of file ad7124.h.

```
29                      {
30     ContinuousMode = 0,
31     SingleConvMode,
32     StandbyMode,
33     PowerDownMode,
34     IdleMode,
35     InternalOffsetCalibrationMode,
36     InternalGainCalibrationMode,
37     SystemOffsetCalibrationMode,
38     SystemGainCalibrationMode
39   };
```

2.1.2.8 enum Ad7124::PgaSel

Gain select bits. These bits select the gain to use when converting on any channels using this configuration register.

Enumerator

Pga1 Gain 1, Input Range When VREF = 2.5 V: ±2.5 V

Pga2 Gain 2, Input Range When VREF = 2.5 V: ±1.25 V

Pga4 Gain 4, Input Range When VREF = 2.5 V: ± 625 mV

Pga8 Gain 8, Input Range When VREF = 2.5 V: ±312.5 mV

Pga16 Gain 16, Input Range When VREF = 2.5 V: ±156.25 mV

Pga32 Gain 32, Input Range When VREF = 2.5 V: ±78.125 mV

Pga64 Gain 64, Input Range When VREF = 2.5 V: ±39.06 mV

Pga128 Gain 128, Input Range When VREF = 2.5 V: ±19.53 mV

Definition at line 124 of file ad7124.h.

```
124               {
125     Pga1 = 0,
126     Pga2,
127     Pga4,
128     Pga8,
129     Pga16,
130     Pga32,
131     Pga64,
132     Pga128
133   };
```

2.1.2.9 enum Ad7124::PostFilterType

Post filter type select bits. When the filter bits are set to 1, the sinc 3 filter is followed by a post filter which offers good 50 Hz and 60 Hz rejection at output data rates that have zero latency approximately.

Enumerator

dB47PostFilter Rejection at 50 Hz and 60 Hz ± 1 Hz: 47 dB, Output Data Rate (SPS): 27.27 Hz

dB62PostFilter Rejection at 50 Hz and 60 Hz ± 1 Hz: 62 dB, Output Data Rate (SPS): 25 Hz

dB86PostFilter Rejection at 50 Hz and 60 Hz ± 1 Hz: 86 dB, Output Data Rate (SPS): 20 Hz

dB92PostFilter Rejection at 50 Hz and 60 Hz ± 1 Hz: 92 dB, Output Data Rate (SPS): 16.7 Hz

Definition at line 174 of file ad7124.h.

```
174                     {
175     dB47PostFilter = 2,
176     dB62PostFilter = 3,
177     dB86PostFilter = 5,
178     dB92PostFilter = 6
179   };
```

2.1.2.10 enum Ad7124::PowerMode

Power Mode Select These bits select the power mode. The current consumption and output data rate ranges are dependent on the power mode.

Enumerator

LowPower low power

MidPower mid power

FullPower full power

Definition at line 46 of file ad7124.h.

```
46                {
47     LowPower = 0,
48     MidPower,
49     FullPower
50   };
```

2.1.2.11 enum Ad7124::RefSel

Reference source select bits. These bits select the reference source to use when converting on any channels using this configuration register.

Enumerator

RefIn1 REFIN1(+)/REFIN1().

RefIn2 REFIN2(+)/REFIN2().

RefInternal internal reference.

RefAVdd AVDD

Definition at line 140 of file ad7124.h.

```
140             {
141     RefIn1 = 0,
142     RefIn2,
143     RefInternal,
144     RefAVdd
145   };
```

Chapter 3

Class Documentation

3.1 Ad7124Chip Class Reference

ADC device.

`#include <ad7124.h>`

Public Member Functions

- int begin (int slave_select)

  Initializes the AD7124.
- int channelConfig (uint8_t ch)

  Returns the setup number used by the channel.
- int currentChannel ()

  Returns the last sampling channel.
- int enableChannel (uint8_t ch, bool enable=true)

  Enable/Disable channel.
- long getData ()

  Returns the last sample.
- long getRegister (Ad7124::RegisterId id)

  Reads the value of the specified register.
- int internalCalibration (uint8_t ch)

  Proceed to Internal zero-scale and full-scale calibration.
- long read (uint8_t ch)

  Sampling a channel The channel is enabled in single mode, then the conversion is started and the value of the sample is returned.
- int reset ()

  Resets the device.
- int setAdcControl (Ad7124::OperatingMode mode, Ad7124::PowerMode power_mode, bool ref_en=true, Ad7124::ClkSel clk_sel=Ad7124::InternalClk)

  Sets the ADC Control register.
- int setChannel (uint8_t ch, uint8_t cfg, Ad7124::InputSel ainp, Ad7124::InputSel ainm, bool enable=false)

  Setup channel.
- int setConfig (uint8_t cfg, Ad7124::RefSel ref, Ad7124::PgaSel pga, bool bipolar, Ad7124::BurnoutCurrent burnout=Ad7124::BurnoutOff)

Sets a setup.

- int setConfigFilter (uint8_t cfg, Ad7124::FilterType filter, Ad7124::PostFilterType postfilter, uint16_t fs, bool rej60, bool single)

  Sets the filter type and output word rate for a setup.
- int setConfigGain (uint8_t cfg, uint32_t value)

  Set gain for a setup The gain registers are 24-bit registers and hold the full-scale calibration coefficient for the ADC. The AD7124 is factory calibrated to a gain of 1. The gain register contains this factory generated value on power-on and after a reset.
- int setConfigOffset (uint8_t cfg, uint32_t value)

  Set offset for a setup The offset registers are 24-bit registers and hold the offset calibration coefficient for the ADC and its power-on reset value is 0x800000.
- int setMode (Ad7124::OperatingMode mode)

  Control the mode of operation for ADC.
- int setRegister (Ad7124::RegisterId id, long value)

  Writes the value of the specified register.
- void setTimeout (uint32_t ms)

  set IO timeout in milliseconds
- int startSingleConversion (uint8_t ch)

  Start conversion in single mode.
- int status ()

  Returns the status register.
- uint32_t timeout () const

  return IO timeout in milliseconds (default is 1000ms)
- int waitEndOfConversion (uint32_t timeout_ms)

  Waits until a new conversion result is available.

Static Public Member Functions

- static double toVoltage (long value, int gain, double vref, bool bipolar=true)

  Converts sample to voltage.

3.1.1 Detailed Description

ADC device.

Definition at line 186 of file ad7124.h.

3.1.2 Member Function Documentation

3.1.2.1 int Ad7124Chip::begin (int *slave_select*)

Initializes the AD7124.

Parameters

slave_select	The Slave Chip Select Id to be passed to the SPI calls

Returns

0 for success or negative error code

3.1.2.2 int Ad7124Chip::channelConfig (uint8_t *ch*)

Returns the setup number used by the channel.

Parameters

ch	channel number 0 to 15

Returns

setup number (0 to 7), or negative error code

3.1.2.3 int Ad7124Chip::currentChannel ( )

Returns the last sampling channel.

Returns

channel or negative error code

3.1.2.4 int Ad7124Chip::enableChannel (uint8_t *ch*, bool *enable* = `true`)

Enable/Disable channel.

Parameters

ch	channel number 0 to 15
enable	true for enabled

Returns

0 for success or negative error code

3.1.2.5 long Ad7124Chip::getData ( )

Returns the last sample.

Returns

sample or negative error code

3.1.2.6 long Ad7124Chip::getRegister (Ad7124::RegisterId *id*)

Reads the value of the specified register.

Parameters

id	register identifier

Returns

8 to 24 bits register value, negative for error.

3.1.2.7 int Ad7124Chip::internalCalibration (uint8_t *ch*)

Proceed to Internal zero-scale and full-scale calibration.

Parameters

ch	channel number

Returns

0 for success or negative error code

3.1.2.8 long Ad7124Chip::read (uint8_t *ch*)

Sampling a channel The channel is enabled in single mode, then the conversion is started and the value of the sample is returned.

Parameters

ch	channel number

Returns

sample or negative error code

3.1.2.9 int Ad7124Chip::reset ( )

Resets the device.

Returns

Returns true for success, AD7124_TIMEOUT for timeout

3.1.2.10 int Ad7124Chip::setAdcControl (Ad7124::OperatingMode *mode,* Ad7124::PowerMode *power_mode,* bool *ref_en* = `true`, Ad7124::ClkSel *clk_sel* = Ad7124::InternalClk)

Sets the ADC Control register.

Parameters

mode	Control the mode of operation for ADC
power_mode	Power mode
ref_en	Internal reference voltage enable. When this bit is set, the internal reference is enabled and available at the REFOUT pin. When this bit is cleared, the internal reference is disabled.
clk_sel	select the clock source for the ADC

Returns

0 for success or negative error code

3.1.2.11 int Ad7124Chip::setChannel (uint8_t *ch,* uint8_t *cfg,* Ad7124::InputSel *ainp,* Ad7124::InputSel *ainm,* bool *enable* = `false`)

Setup channel.

Parameters

ch	channel number 0 to 15
cfg	Setup select. These bits identify which of the eight setups are used to configure the ADC for this channel.
ainp	Positive analog input AINP input select.
ainm	Negative analog input AINM input select.
enable	Channel enable bit. Setting this bit enables the device channel for the conversion sequence.

Returns

0 for success or negative error code

3.1.2.12 int Ad7124Chip::setConfig (uint8_t *cfg,* Ad7124::RefSel *ref,* Ad7124::PgaSel *pga,* bool *bipolar,* Ad7124::BurnoutCurrent *burnout* = Ad7124::BurnoutOff)

Sets a setup.

Parameters

cfg	Setup select.
ref	Reference source select bits.
pga	Gain select bits.
bipolar	Polarity select bit. When this bit is set, bipolar operation is selected. When this bit is cleared, unipolar operation is selected.
burnout	These bits select the magnitude of the sensor burnout detect current source.

Returns

0 for success or negative error code

3.1.2.13 int Ad7124Chip::setConfigFilter (uint8_t *cfg*, Ad7124::FilterType *filter*, Ad7124::PostFilterType *postfilter*, uint16_t *fs*, bool *rej60*, bool *single*)

Sets the filter type and output word rate for a setup.

Parameters

cfg	Setup select.
filter	Filter type
postfilter	Post filter type
fs	Filter output data rate select bits. These bits set the output data rate of the sinc 3 and sinc 4 filters as well as the fast settling filters. In addition, they affect the position of the first notch of the filter and the cutoff frequency. In association with the gain selection, they also determine the output noise and, therefore, the effective resolution of the device (see noise tables). FS can have a value from 1 to 2047.
rej60	When this bit is set, a first order notch is placed at 60 Hz when the first notch of the sinc filter is at 50 Hz. This allows simultaneous 50 Hz and 60 Hz rejection.
single	Single cycle conversion enable bit. When this bit is set, the AD7124 settles in one conversion cycle so that it functions as a zero latency ADC. This bit has no effect when multiple analog input channels are enabled or when the single conversion mode is selected. When the fast filters are used, this bit has no effect.

Returns

0 for success or negative error code

3.1.2.14 int Ad7124Chip::setConfigGain (uint8_t *cfg*, uint32_t *value*)

Set gain for a setup The gain registers are 24-bit registers and hold the full-scale calibration coefficient for the ADC. The AD7124 is factory calibrated to a gain of 1. The gain register contains this factory generated value on power-on and after a reset.

Parameters

cfg	Setup select.
value	gain

Returns

0 for success or negative error code

3.1.2.15 int Ad7124Chip::setConfigOffset (uint8_t *cfg*, uint32_t *value*)

Set offset for a setup The offset registers are 24-bit registers and hold the offset calibration coefficient for the ADC and its power-on reset value is 0x800000.

Parameters

cfg	Setup select.
value	offset

Returns

0 for success or negative error code

3.1.2.16 int Ad7124Chip::setMode (Ad7124::OperatingMode *mode*)

Control the mode of operation for ADC.

Parameters

mode	mode of operation

Returns

0 for success or negative error code

3.1.2.17 int Ad7124Chip::setRegister (Ad7124::RegisterId *id,* long *value*)

Writes the value of the specified register.

Parameters

id	register identifier
value	8 to 24 bits register value

Returns

0, negative for error.

3.1.2.18 void Ad7124Chip::setTimeout (uint32_t *ms*) [inline]

set IO timeout in milliseconds

3.1.2.19 int Ad7124Chip::startSingleConversion (uint8_t *ch*)

Start conversion in single mode.

Parameters

ch	channel number

Returns

0 for success or negative error code

3.1.2.20 int Ad7124Chip::status ( )

Returns the status register.

3.1.2.21 uint32_t Ad7124Chip::timeout ( ) const [inline]

return IO timeout in milliseconds (default is 1000ms)

3.1.2.22 static double Ad7124Chip::toVoltage (long *value*, int *gain*, double *vref*, bool *bipolar* = true) [static]

Converts sample to voltage.

Parameters

value	sample
gain	gain
vref	full scale voltage
bipolar	

Returns

voltage

3.1.2.23 int Ad7124Chip::waitEndOfConversion (uint32_t *timeout_ms*)

Waits until a new conversion result is available.

Parameters

timeout_ms	timeout delay

Returns

0 for success or negative error code