ICN6201/02 User Guide

MIPI® DSI BRIDGE TO FLATLINK™ LVDS

Revision 0.4

Chipone Technology (Beijing) Co., Ltd
13th Floor, Test Tower, Building 4, 31 Middle North Third Ring Rd.,
Haidian District, Beijing, 100088
PRC
Contact: Simon Liu
Email: simon_liu@chiponeic.com

Revision History

Rev	Date	Author	Description
0.1	2013-07-31	Simon_Liu WangGang	Initial version
0.2	2013-08-30	Simon_Liu WangGang	Change figure format of reference schematic to fit Zoom in/out
0.3	2013-10-30	Simon_Liu WangGang	Add Hardware layout guide
0.4	2014-01-06	Simon Liu WangGang	Add ICN6202

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1 Overview

ICN6201/02 is a bridge chip which receives MIPI® DSI inputs and sends LVDS outputs.

ICN6201/02 is primarily targeted for portable applications such as tablets and smart phones that utilize the MIPI DSI video format.

ICN6201/02 supports up to 4 lanes and each lane operates at 1Gbps maximum; the totally maximum input bandwidth is 4Gbps; The LVDS output 18 or 24 bits pixel with 25MHz to 154MHz, by VESA or JEIDA format.

ICN6201 adopts QFN48 package and ICN6202 adopts QFN 40pins package.

2 Implementation Guidelines

2.1 MIPI signal pins

DA0P/N, DA1P/N, DA2P/N, DA3P/N, DACP/N are MIPI high speed signals, which max bit rate is 1Gbps.Each pair *P/N should be routed together with controlled-differential 100-Ω impedance. Keep away from other high speed signals. Keep lengths within 5 mil of each other. Keep traces on layers adjacent to ground plane. The number of VIAS should be kept to a minimum. Each pair should be separated at least by 3 times the signal trace width. Route all differential pairs on the same group of layers (outer layers or inner layers) if not on the same layer. The unused MIPI pins can be left unconnected or driven to LP11 or LP00.

2.2 LVDS signal pins

A_Y0P/N, A_Y1P/N, A_Y2P/N, A_Y3P/N, A_CLKP/N are LVDS output high speed signals, so it is preferred to avoid via when routing. Each pair *P/N should be routed together with controlled-differential 100-Ω impedance. Keep away from other high speed signals. Keep lengths within 5 mil of each other. Keep traces on layers adjacent to ground plane. Each pair should be separated at least by 3 times the signal trace width. Route all differential pairs on the same group of layers (outer layers or inner layers) if not on the same layer. When power down the unused LVSD channel, the output is pull down to GND with internal 2K resister. The polarity of each pair of LVDS signals can be swapped by control registers. Each pair of LVDS can also be swapped by control registers. The unused LVDS pins should be left unconnected.

2.3 REFCLK PIN

For package ICN6201, there is only one REFCLK pin (#22), but for ICN6202, there are 2 REFCLK pin (#11 and #26), each REFCLK can be as the reference CLK of LVDS output. These pins receive AC coupled clock signals, which frequency is typical 26MHz. Ref CLK trace should be routed as short as possible.

Please note: if any one REFCLK pin is not used, this pin should be connected to GND.

2.4 VCORE PIN

This pin outputs 1.2V from the internal voltage regulator. This pin MUST have at least one 1uF and at least one 0.01uF external capacitor to GND.

2.5 EN PIN

ICN6201/02 is reset by control pin EN to Low. It is critical to transition the EN input from a low to a high level after the Vcc supply has reached the minimum operating voltage as following figure 2-1.

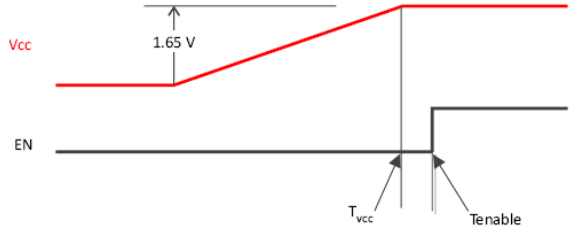


Figure 2-1 timing between EN and VCC

To achieve the required timing, an approximately 200nF capacitor as a reasonable first estimate is needed. The internal pull-up resister is about 200K.

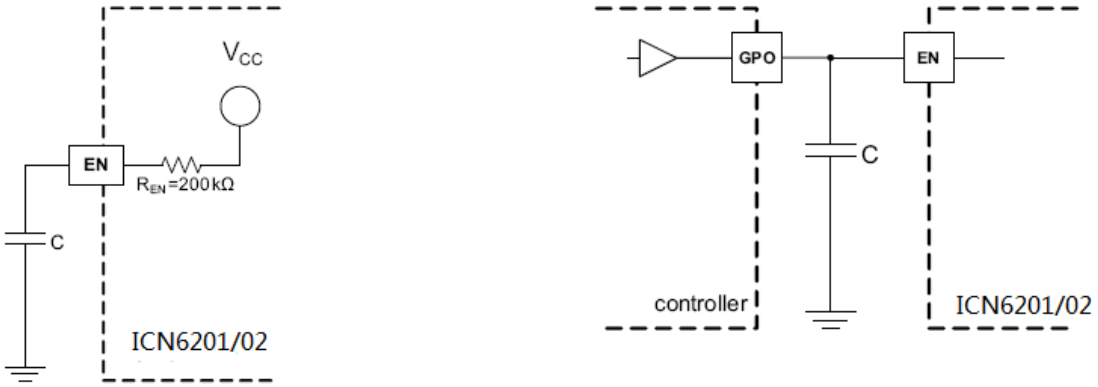


Figure 2-2 EN implement with external capacitor

2.6 ADDR_SEL PIN

The pin ADDR_SEL control the I2C slave's device address.

When this pin is connected to GND, the I2C device address is 0x2C;

When this pin is connected to VDD, the I2C device address is 0x2D.

2.7 TEST_EN & BIST_EN PIN

These two pins are not used for normal function. They can be connected to GND or left unconnected.

2.8 GPIO_0 & GPIO_1 & ATEST PIN

These three pins are reserved for debug function. They can be left unconnected.

2.9 IRQ

This pin is interrupt pin. If it is not used, it can be left unconnected.

2.10 SCL & SDA PIN

These two pins are I2C signals. They should be connected to I2C master with pull-up resister if I2C function is used. If these two pins are not used, they can be left unconnected.

2.11 Decoupling Capacitors

Decoupling capacitors should be placed near the power plane and power rails for the ICN6201. The trace length between decoupling capacitors must be minimized to avoid large current loops and trace inductance. The use of four ceramic capacitors (two 0.1 μF and two 0.01 μF) near the ICN6201 is recommended.

2.12 EXPOSED PAD

For ICN6201, the EXPOSED PAD should be connected to GND.

For ICN6202, the EXPOSED PAD can be connected to GND or left unconnected.

3 Reference schematics

3.1 Reference Schematics for ICN6201

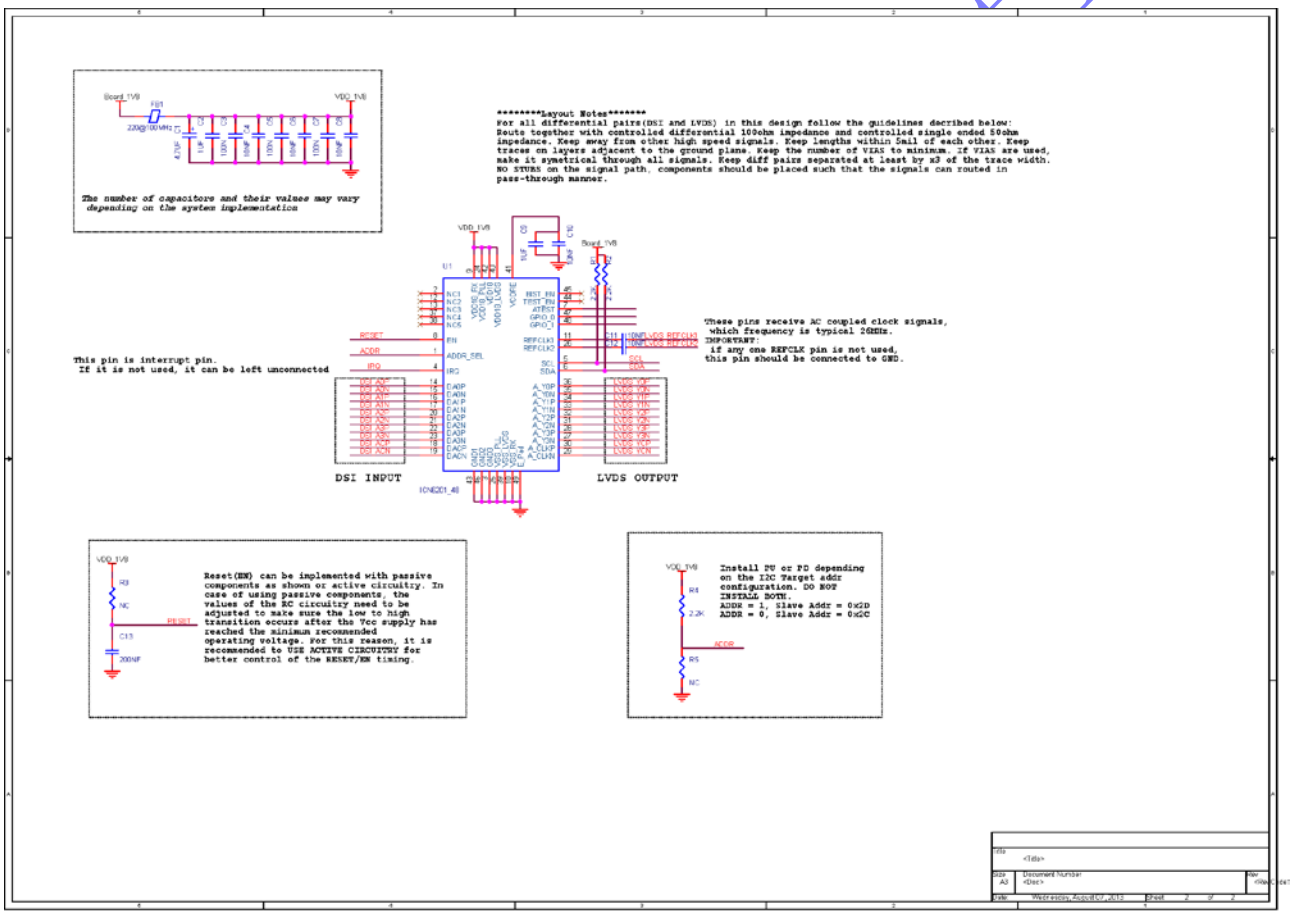


Figure 3-1 Reference schematic for ICN6201

3.2 Reference Schematics for ICN6202

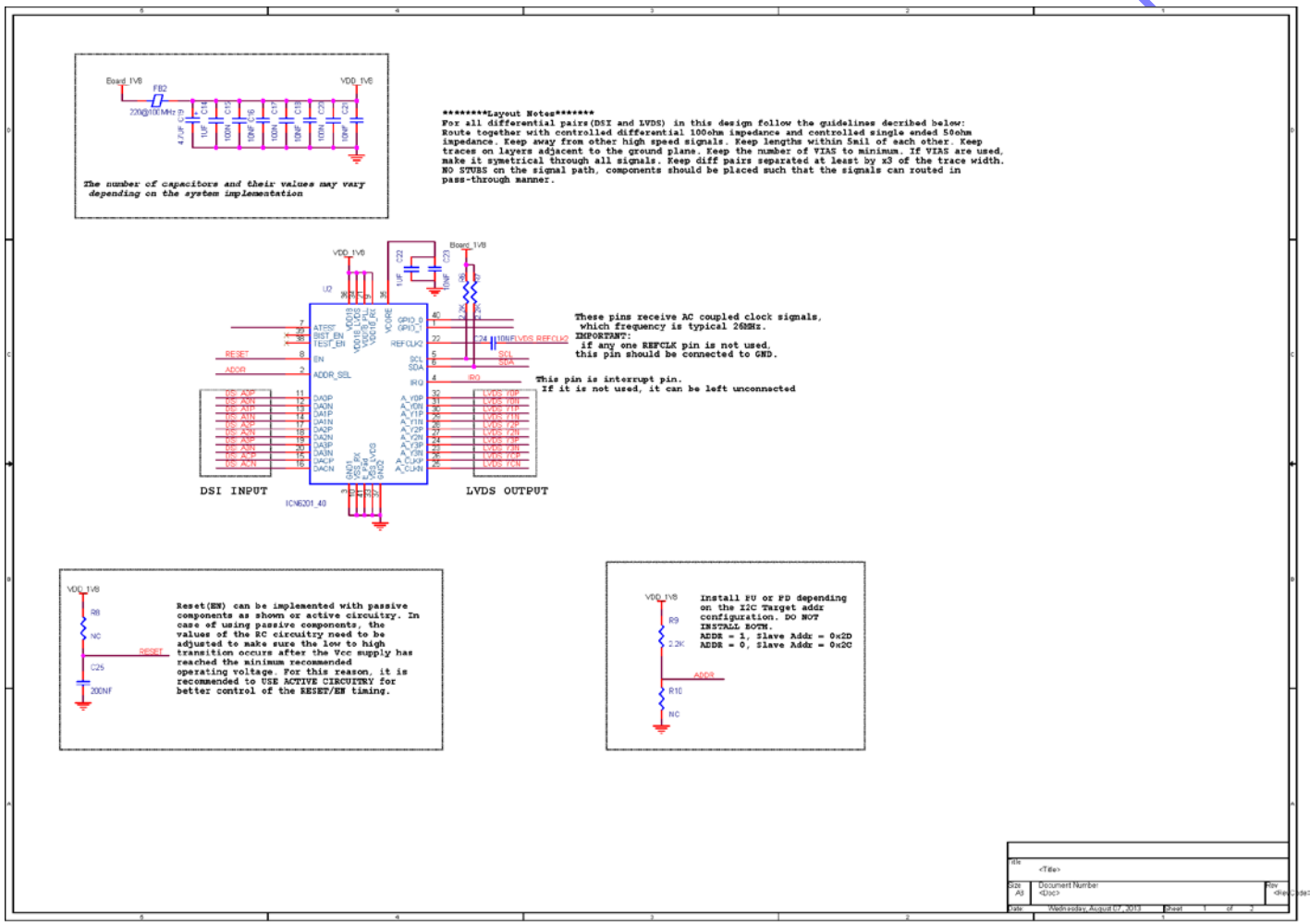


Figure 3-2 Reference schematic for ICN6202

4 Reference Layout

4.1 Reference Layout for ICN6201

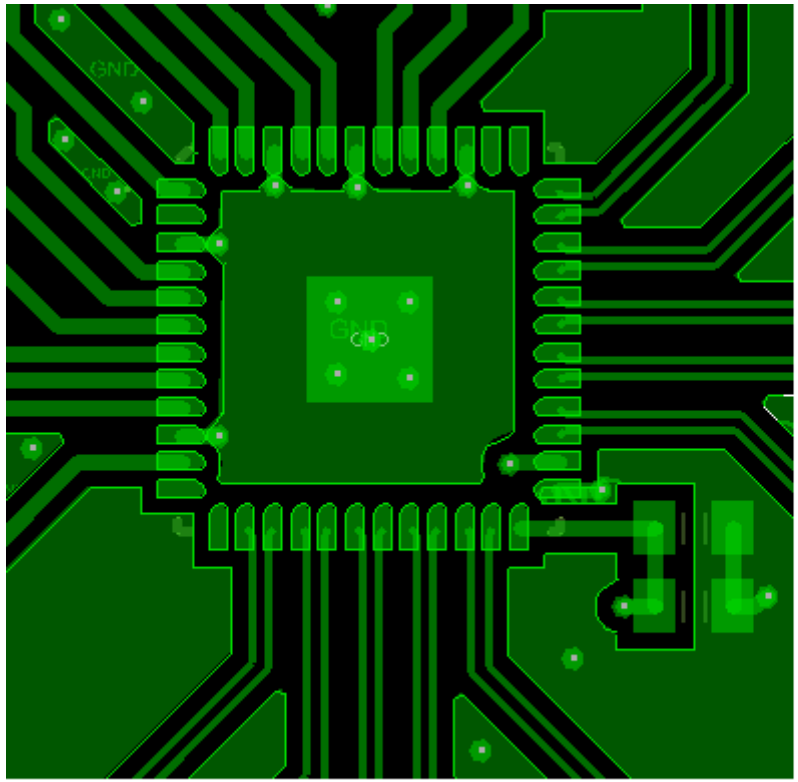
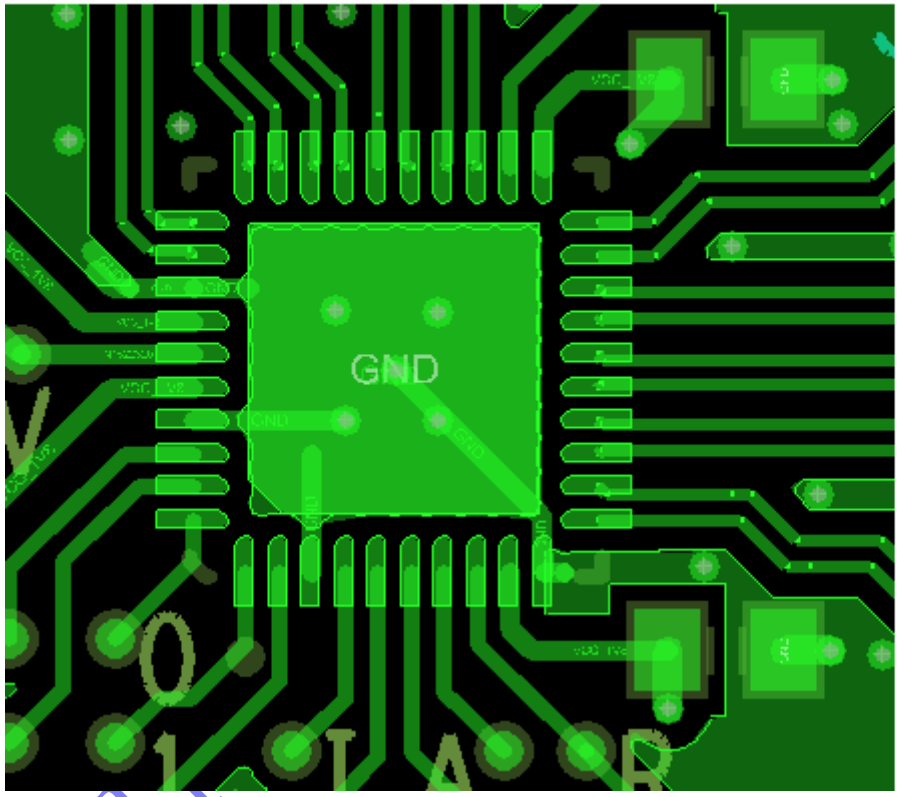


Figure 4-1 Reference Layout for ICN6202

4.2 Reference Layout for ICN6202

LVDS Signals



MIPI Signals

Figure 4-2 Reference Layout for ICN6202