ICN6201_6202 Specification
MIPI ® DSI BRIDGE TO FLATLINK TM LVDS
Revision 1.0

1 Introduction

ICN6201_6202 is a bridge chip which receives MIPI ® DSI inputs and sends LVDS outputs. MIPI ® DSI supports up to 4 lanes and each lane operates at 1Gbps maximum; the totally maximum input bandwidth is 4Gbps; and the MIPI defined ULPS(ultra-low-power state) is also supported. ICN6201 decodes MIPI ® DSI 18bepp RGB666 and 24bpp RGB888 packets. The LVDS output 18 or 24 bits pixel with 25MHz to 154MHz, by VESA or JEIDA format. ICN6201/02 support video resolution up to FHD (1920x1080) and WUXGA (1920x1200). ICN6201 adopts QFN48 package and ICN6202 adopts QFN40 package.

1.1 Feature List

- Supports MIPI ® D-PHY Version 1.00.00 and MIPI ® DSI Version 1.02.00.
- Single Channel DSI Receiver with One, Two, Three and Four lanes configurable, each lanes operates up to 1Gbps.
- Receives 18bpp RGB666 and 24bpp RGB888 packets defined by DSI.
- Supports MIPI Low State, Ultra-Low Power State, Shut Down mode.
- Single Channel LVDS with output clock range of 25MHz to 154MHz.
- LVDS can be generated from MIPI HS clock or external reference clock.
- Support LVDS clock with center spreading up to 2%, modulation 30KHz ~ 60KHz.
- LVDS output with VESA or JEIDA format.
- LVDS output pin order can be swapped flexible.
- Supply voltage: 1.8V.
- Provide I2C slave interface.
- Package: ICN6201 QFN48-pins with e-pad.
- Package: ICN6202 QFN40-pins with e-pad.

2 Functional Block Diagram

Following figure shows a functional block diagram of the ICN6201/02.

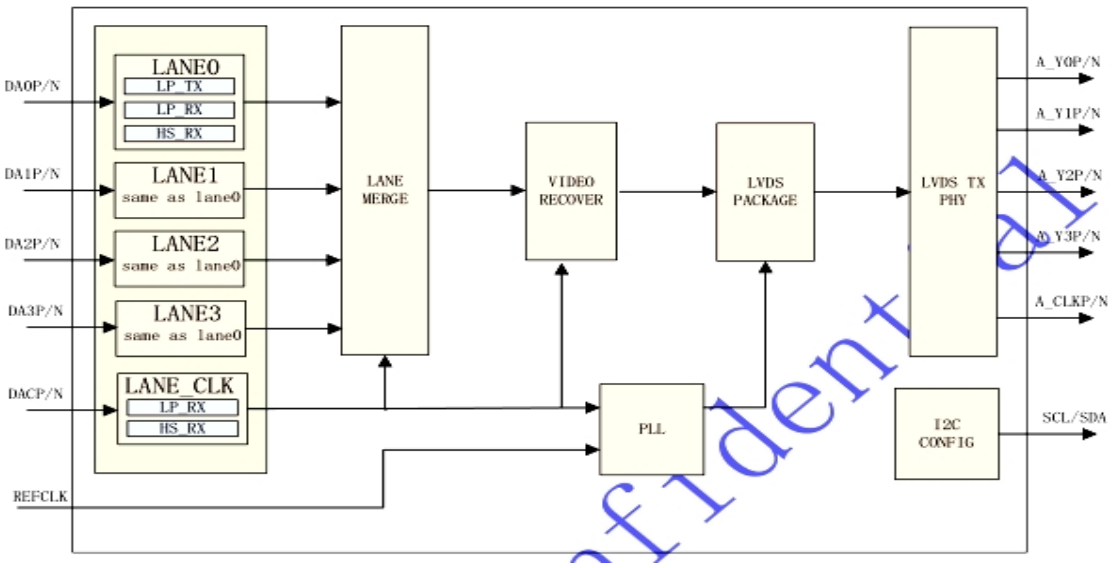

Figure 2-1 ICN6201/02 function block diagram

3 System Application Diagram

In the diagram below shows the ICN6201/02's system application.

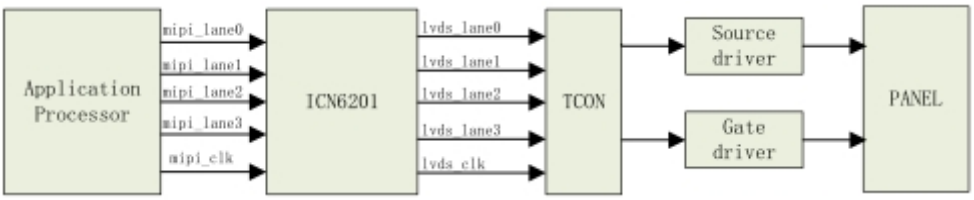

Figure 3-1 ICN6201/02 system application diagram

4 Pin Diagram

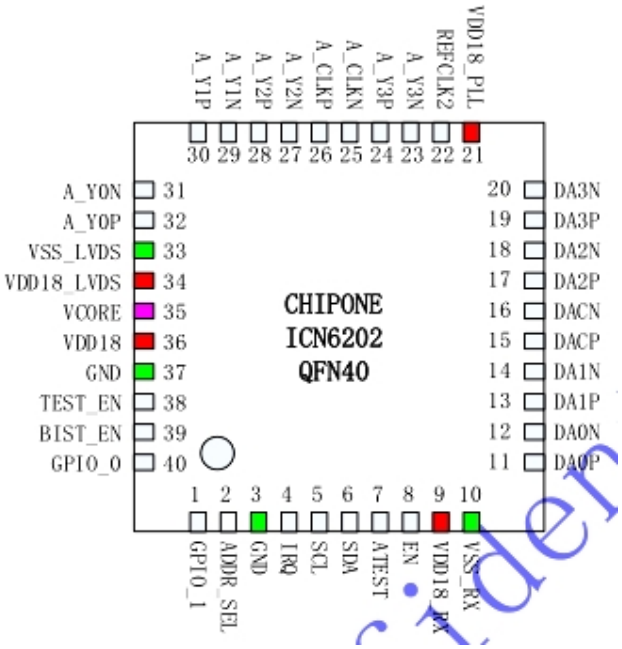

Figure 4-1 ICN6202 diagram (Top View)

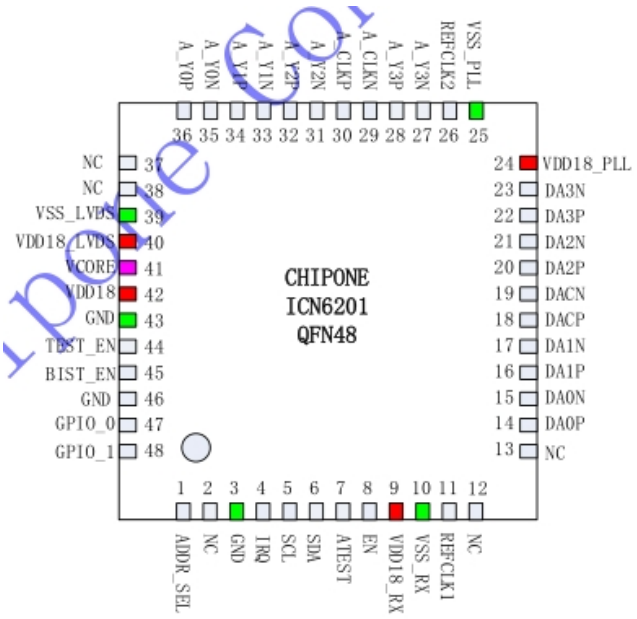

Figure 4-2 ICN6201 diagram (Top View)

5 Pin Description

Name	ICN6201	ICN6202	I/O	Description
MIPI interface				
DA0P/DA0N	14/15	11/12	Input	MIPI® D-PHY, data LANE0.
DA1P/DA1N	16/17	13/14	Input	MIPI® D-PHY, data LANE1.
DA2P/DA2N	20/21	17/18	Input	MIPI® D-PHY, data LANE2.
DA3P/DA3N	22/23	19/20	Input	MIPI® D-PHY, data LANE3.
DACP/DACN	18/19	15/16	Input	MIPI® D-PHY, clock LANE.
LVDS interface				
A_Y0P/A_Y0N	36/35	32/31	Output	LVDS data lane0
A_Y1P/A_Y1N	34/33	30/29	Output	LVDS data lane1
A_Y2P/A_Y2N	32/31	28/27	Output	LVDS data lane2
A_Y3P/A_Y3N	28/27	24/23	Output	LVDS data lane3
A_CLKP/A_CLKN	30/29	26/25	Output	LVDS clock lane
MISC				
ATEST	7	7	output	Analog test pin.
EN	8	8	input	When EN is low, this chip is reset.
ADDR_SEL	1	2	input	Local I2c address select.
REFCLK1	11	--	input	Optional reference clock for LVDS output clock.
REFCLK2	26	22	input	Optional reference clock for LVDS output clock.
SCL	5	5	input	Local I2C bus
SDA	6	6	inout	Local I2C bus
IRQ	4	4	output	Interrupt signal
TEST_EN	44	38	input	For ATE test, when work, connect to GND.
BIST_EN	45	39	input	For ATE test, when work, connect to GND.
GPIO_0	47	40	inout	Reserved.
GPIO_1	48	1	inout	Reserved.
Power/Ground				
GND	3, 10, 25, 39,	3, 10, 33,37		Ground

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	43, 46			
VDD18	9, 24, 40, 42	9, 21, 34, 36		1.8V input
VCORE	41	35		Output from voltage regulator for digital core.
Other				
NC	2, 12, 13, 37, 38	--		Not used pins, left unconnected

NOTE:

1. The use of four ceramic capacitors (2 x 1uF and 2 x 0.01uF) with pin VCORE provides good performance.At least, one 1uF and one 0.01uF capacitor is necessary. Also, the trace between the decoupling capacitor and pin should minimized.
2. Any one of REFCLK1 and REFCLK2 can be used as the reference clock for LVDS output. If one or two is not used, the unused pin should connect to GND. For ICN6202, only REFCLK2 is available.
3. TEST_EN & BIST_EN should be connected to GND when normal working.

6 Function Description

6.1 MIPI Receiver

6.1.1 DSI Lane Merging

ICN6201/02 support four DSI data lanes, and may be configured to one, two or three DSI data lanes. Unused DSI input lanes should be left unconnected or driven to LP11 state.Following figure illustrates the lane merging function for 4-lane, 3-lane, 2-lane and 1-lane separately.

Figure 6-1 DSI multi-lanes HS Transmission Example

6.1.2 DSI Pixel Stream Packets

ICN6201/02 receives and interpret 18bpp (RGB666), 24bpp (RGB888) DSI packets and translates to video stream.

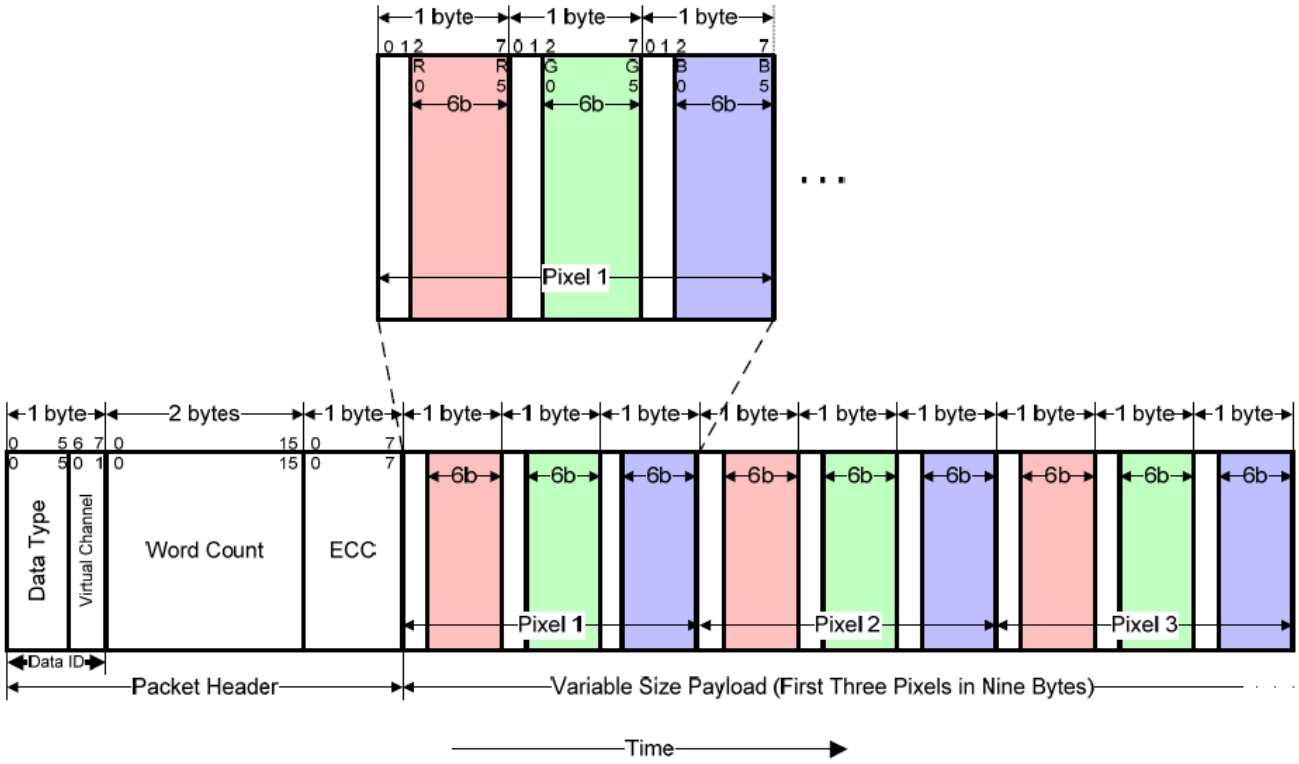

Figure 6-2 DSI RGB666 Color format, Loosely Long Packet

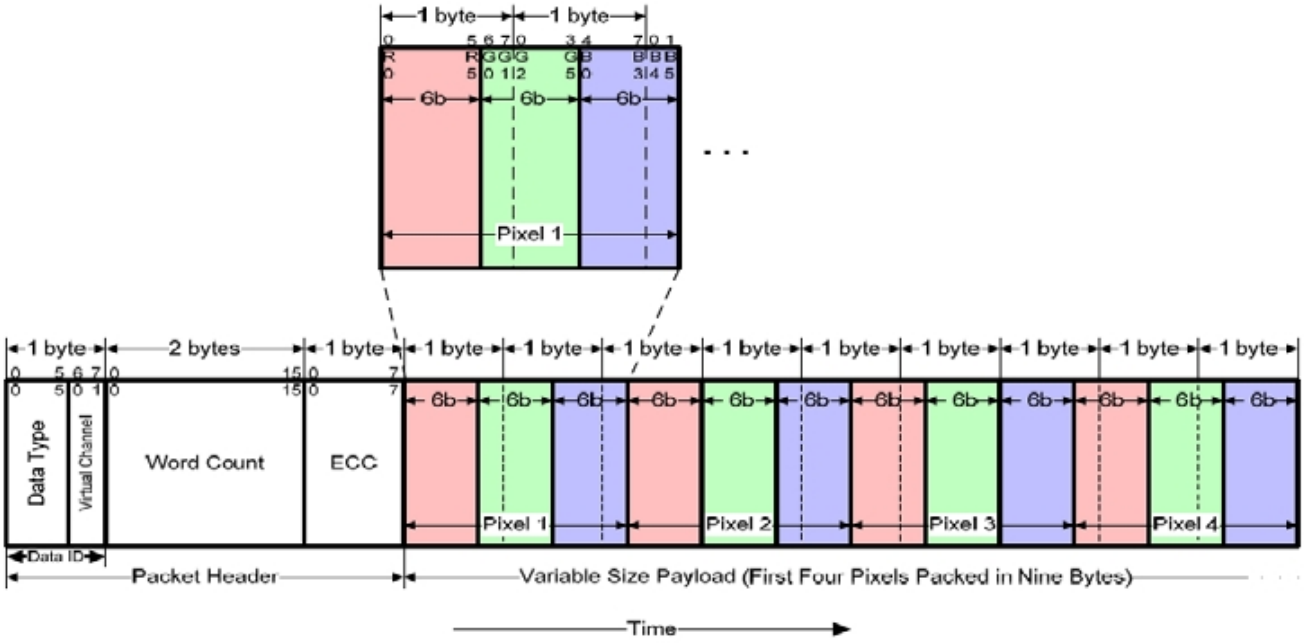

Figure 6-3 DSI RGB666 Color format, Tightly Long Packet

For the RGB666 tightly packet, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

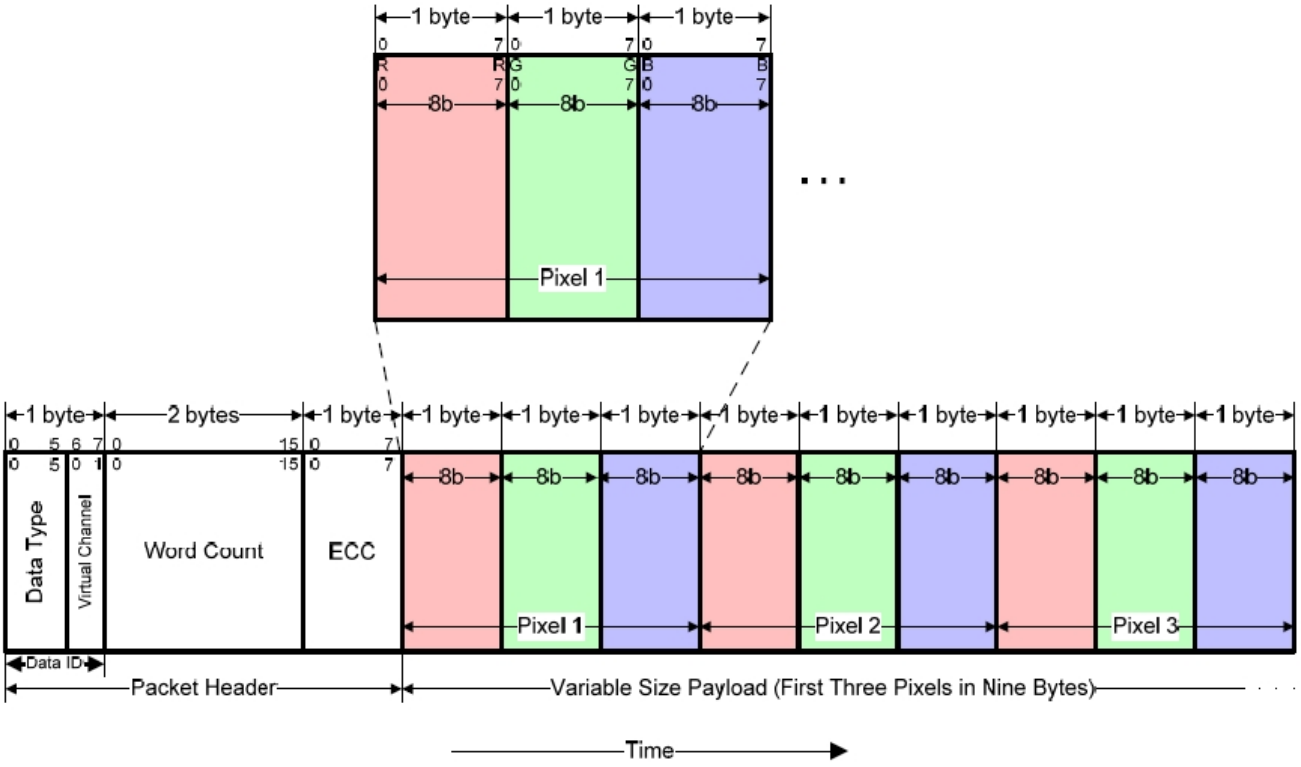

Figure 6-4 DSI RGB888 Color format, Long Packet

6.1.3 DSI Video Transmission sequence

ICN6201/02 supports Non-Burst Mode with Sync Pulses, Non-Burst Mode with Sync Events and Burst mode.

- Non-Burst Mode with Sync Pulses: enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events: similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode: RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power).

For all three sequences, the first line of a video frame shall start with a VSS packet, and all other lines start with VSE or HSS. The position of the synchronization packets in time is of utmost importance since this has a direct impact on the visual performance of the display panel; that is, the LVDS output video timing (HS-Horizontal sync and VS-Vertical sync) are generated based on the synchronization.

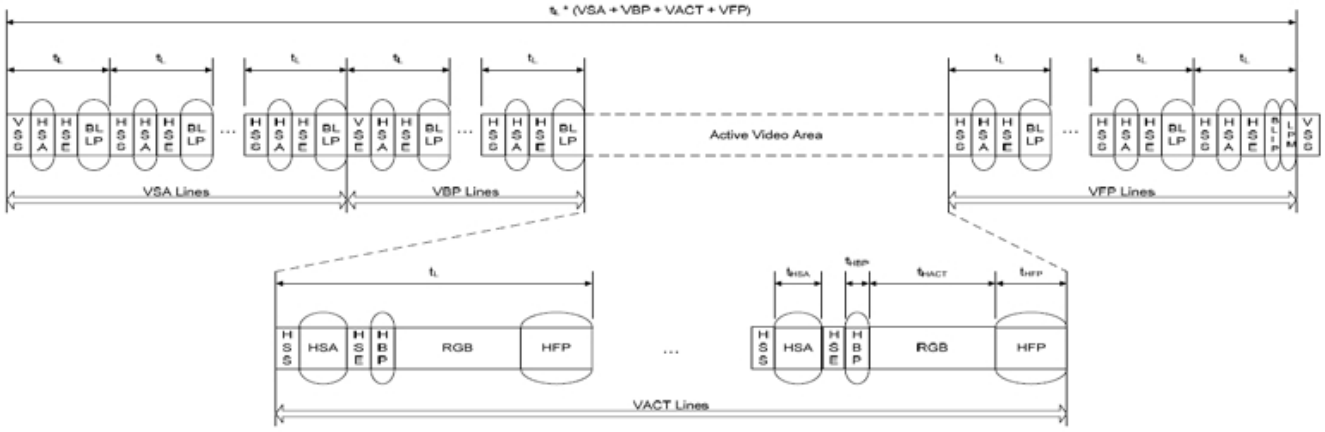

Figure 6-5 Non-Burst Mode with Sync Pulses

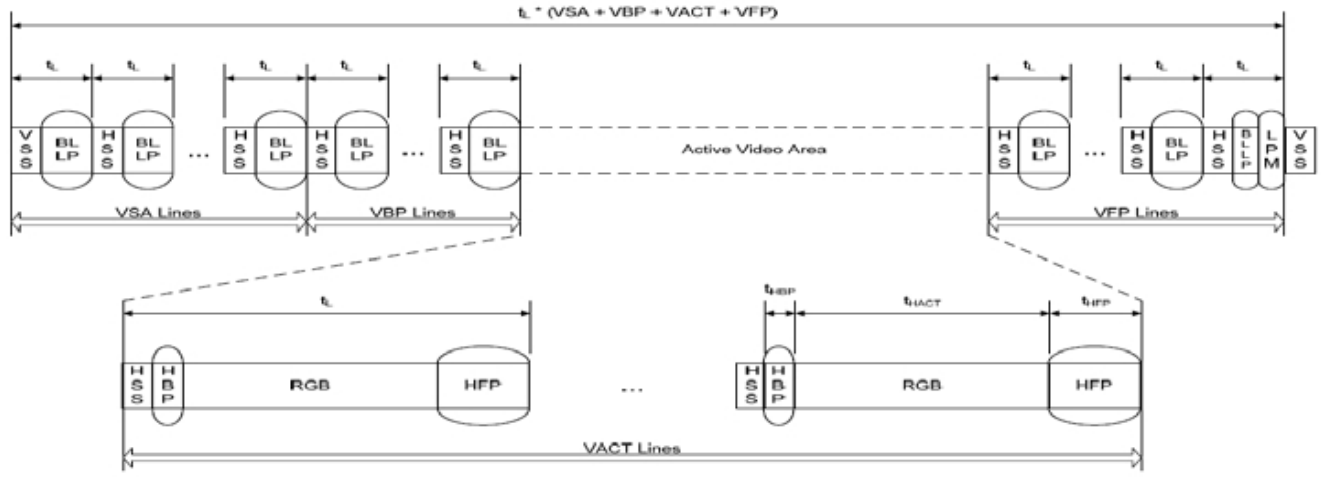

Figure 6-6 Non-Burst Mode with Sync Events

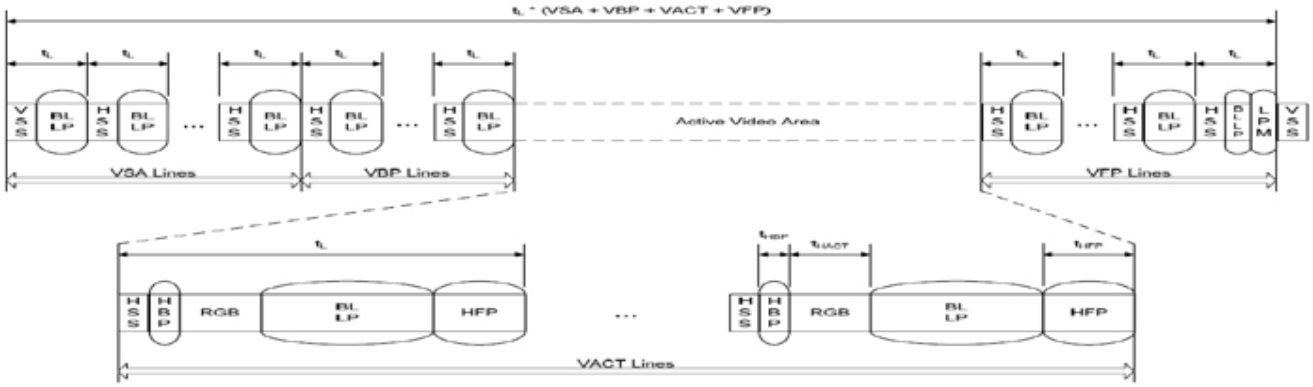

Figure 6-7 Burst mode

6.2 LVDS Transmitter

ICN6201/02 supports both JEIDA/VESA 6/8bits data format. Each format is as below diagram.

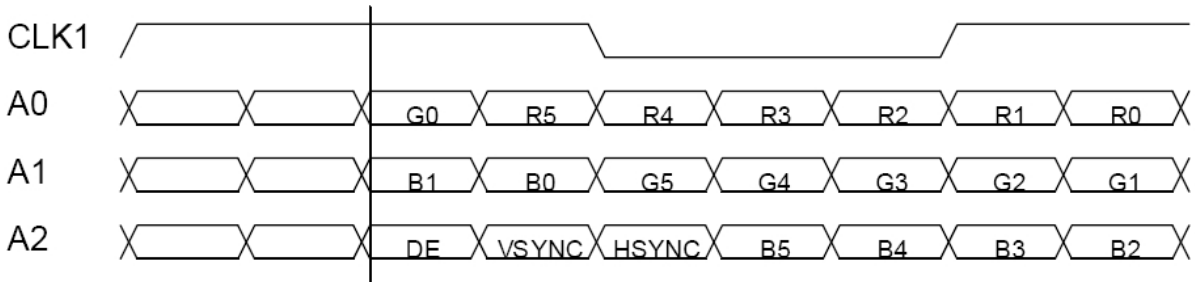

Figure 6-8 LVDS, 18-bit single port, VESA or JEIDA format

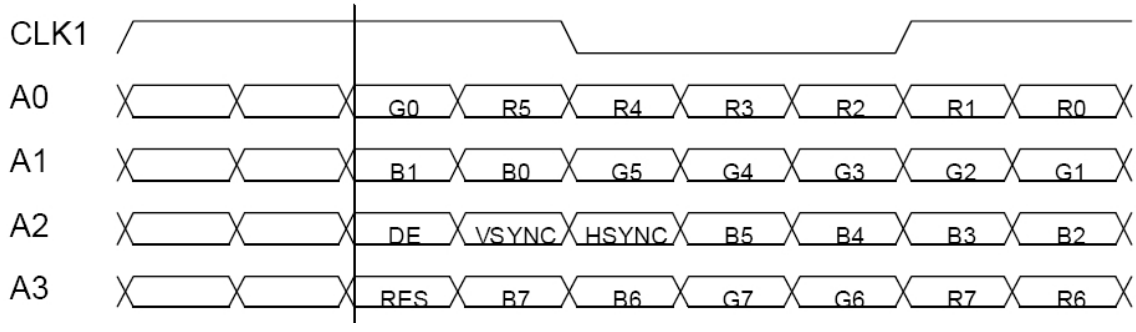

Figure 6-9 LVDS, 24-bit single port, VESA format

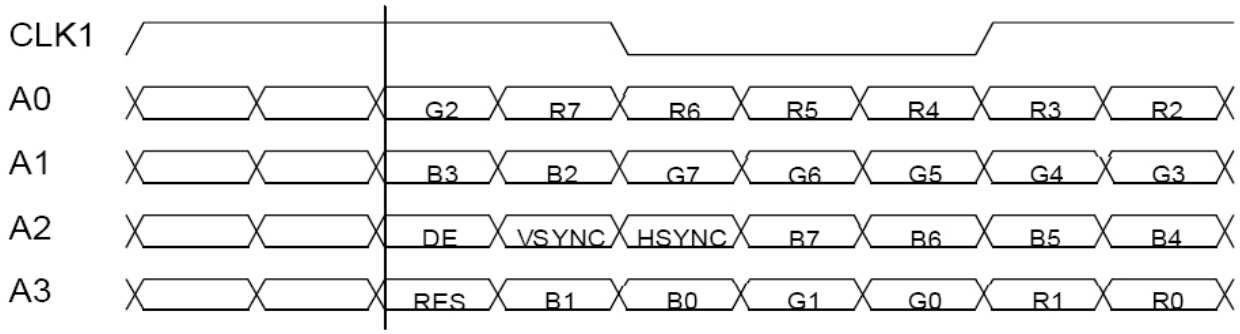

Figure 6-10 24-bit single port, JEIDA format

6.3 Bist mode

ICN6201/02 goes into bist mode when configure register is enabled, five built-in images as below are displayed sequentially; and the interval time can be set (default is about 2ms).

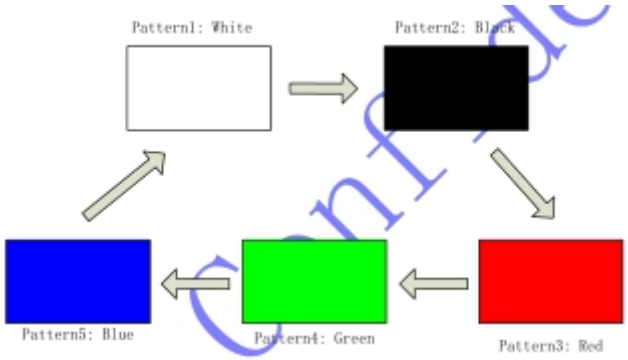

Figure 6-11 Bist mode pattern sequence

6.4 DSI access local registers

6.4.1 Write local registers

There are two methods to write local registers.These two method must be used under ESCAPE mode.

●Use Generic Short WRITE with 2 parameters(DI = 0x23)

The format is as below：DI(0x23) + offset[7:0] + data + ECC.

Please note that the offset is only 8bits.Also, this method can write only one data in each packet.

●Use Generic Long Write(DI = 0x29)

The format is as below：

DI(0x29) + WC[7:0] + WC[15:8] + ECC + offset[7:0] + data(1) + data(2) + …… + data(n) + CHKSUM[7:0] + CHKSUM[15:8].

Where： n = WC[15:0] – 1..

In this case, the data length can be 65535 maximum.

6.4.2 Read local registers

Use Generic READ with 2 parameters (0x24), this method can be used under HS mode or ESCAPE MODE.

The format is as below:

DI(0x24) + offset[7:0] + length[7:0] + ECC.

Please note that the offset is only 8bits.

The read length can be 255 maximum.

6.5 I2C access local registers

ICN6201/02 support standard I2C protocol with speed up to 400K.

The chip device address is determined by the pin “ADDR” as below table:

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(W/R)
0	1	0	1	1	0	ADDR	0/1

When ADDR = 1, device address is 0x5A(Write) and 0x5B(Read);

When ADDR = 0, device address is 0x58(Write) and 0x59(Read).

Following example is operation procedure with ADDR = 0.

- Write one byte to certain offset：ST→0x58→ACK→OFFSET→ACK→DATA→ACK→STOP.
- Write more bytes to successive address： ST→0x58→ACK→OFFSET→ACK→DATA0→ACK→DATA1→……→DATAn→ACK→STOP.
- Read data from certain offset： ST→0x58→ACK→OFFSET→ACK→RESTART→0X59→ACK→DATA0→ACK→DATA1→……→DATAn→NACK→STOP.

7 DC and AC Electrical Characteristics

7.1 ABSOLUTE MAXIMUM RATING

		MIN	MAX	UNIT
Supply Voltage Range	VCC	-0.3	2.175	V
Input Voltage Range	CMOS Input	-0.5	2.175	V
	DSI input	-0.4	1.4	V
Storage Temperature	Ts	-65	105	℃
Electrostatic discharge	Human Body Model		±2	KV
	Charged-device model		±500	V

Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.

7.2 RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	VCC power supply	1.65	1.8	1.95	V
V_{PSN}	Supply noise on any V_{CC} pin	f(noise) > 1MHz		0.05	V
T_A	Operating free-air temperature	-40		85	℃
T_{CASE}	Case temperature			92.2	℃
V_{DSI_PIN}	DSI input pin voltage range	-50		1350	mV
$f_{(I2C)}$	Local I2C input frequency			400	KHz
f_{HS_CLK}	DSI HS clock input frequency	40		500	MHz
t_{setup}	DSI HS data to clock setup time(Figure 7-1)	0.15			UI
t_{hold}	DSI HS data to clock hold time(Figure 7-1)	0.15			UI
Z_L	LVDS output differential impedance	90		132	Ω

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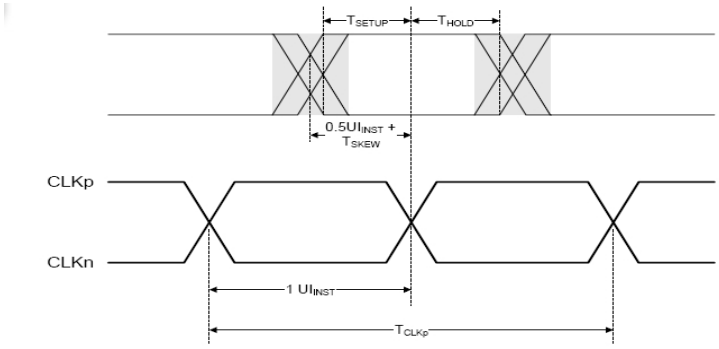

Figure 7-1 DSI HS UI timing definition

7.3 Electrical Characteristics

7.3.1 MIPI DSI INTERFACE

Refer to Figure 7-2.

parameter	Description	MIN	TYP	MAX	UNIT
V_{IL}	Low Power logic 1 input voltage	880			mV
V_{IH}	Low Power logic 0 input voltage			550	mV
$\|V_{ID}\|$	HS differential input voltage: $\|V_{dp} - V_{dn}\|$	70	200	270	mV
|VIDT|	HS differential input voltage threshold			50	mV
$V_{IL-ULPS}$	Low Power receiver logic 0 voltage, ULP state			300	mV
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70		330	mV
$\triangle V_{CMRX(HF)}$	HS common-mode interference			100	mV
V_{IHHS}	HS single-ended input high voltage			460	mV
V_{ILHS}	HS single-ended input low voltage	-40			mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable			450	mV
Z_{ID}	Differential input impedance	80	100	124	Ω

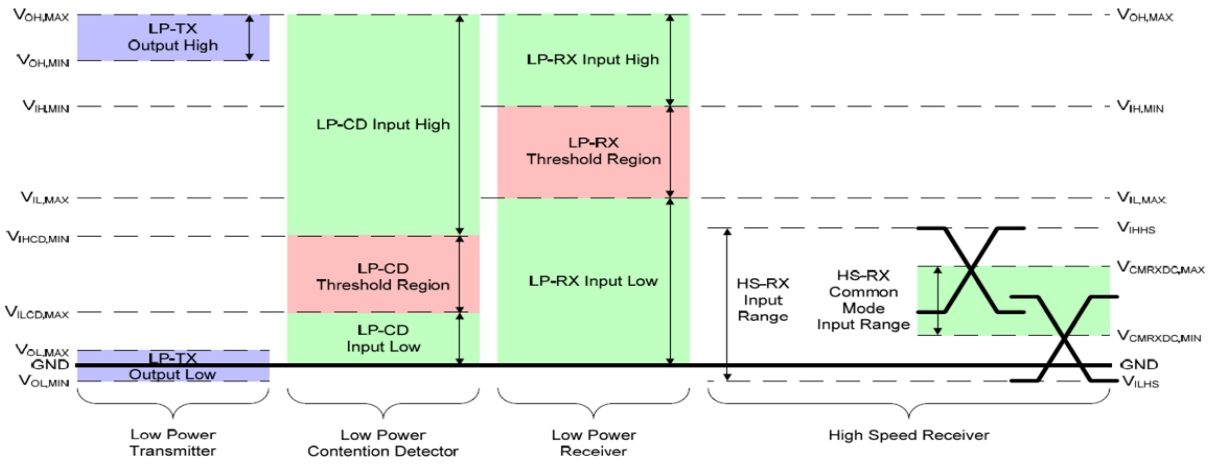

Figure 7-2 DSI HS/LP signaling and Contention Voltage

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7.3.2 LVDS output

Refer to Figure 7-3.

parameter	Description	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Steady-state differential output voltage	140		500	mV
$\triangle\|V_{OD}\|$	Change in steady-state differential output voltage between opposite bnary state			35	mV
$V_{OC(SS)}$	.Steady state common-mode output voltage	0.8	0.9	1.0	V
		1.15	1.25	1.35	V
$V_{OC(PP)}$	Peak-to-Peak common-mode output voltage			35	mV
R_{LVDS_DIS}	Pull-down resistance for disabled LVDS outputs		1		K Ω

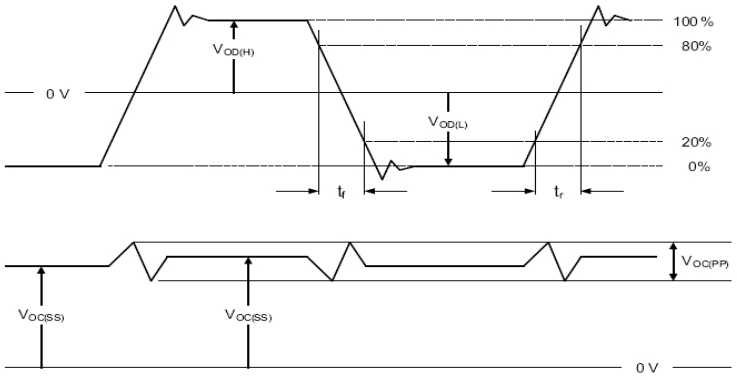

Figure 7-3 LVDS output signaling

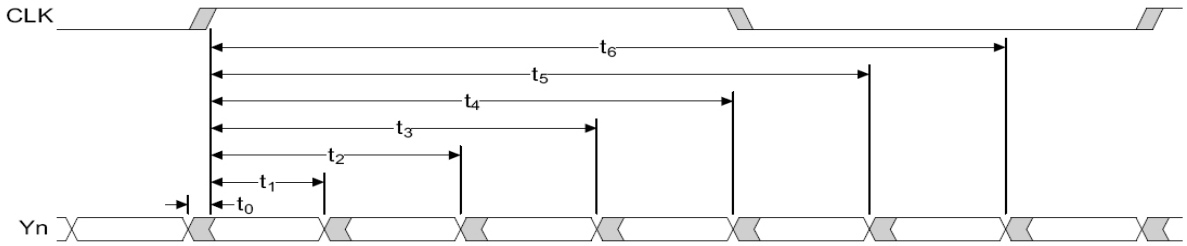

Figure 7-4 LVDS output data and clock timing

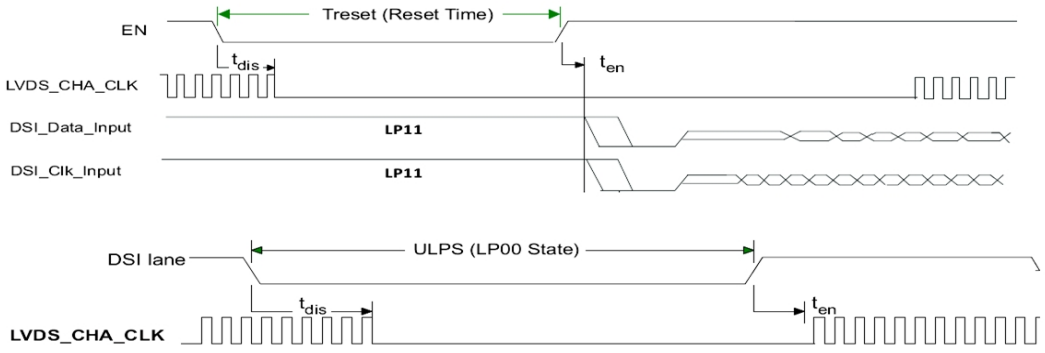

Figure 7-5 Power on and RESET and ULPS timing

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7.4 SWITCHING CHARACTERISTICS

Parameter	Description	MIN	TYP	MAX	UNIT
DSI					
t_{GS}	DSI LP input pulse rejection			300	ps
LVDS (refer to Figure 7-4)					
t_C	Output clock period	6.49		40	ns
t_W	High-Level output clock pulse duration		4/7 t_C		ns
t0	Delay time, CLK ↑ to 1st serial bit position	-0.15		+0.15	ns
t1	Delay time, CLK ↑ to 2nd serial bit position	1/7 t_C – 0.15		1/7 t_C + 0.15	ns
t2	Delay time, CLK ↑ to 3rd serial bit position	2/7 t_C – 0.15		2/7 t_C + 0.15	ns
t3	Delay time, CLK ↑ to 4th serial bit position	3/7 t_C – 0.15		3/7 t_C + 0.15	ns
t4	Delay time, CLK ↑ to 5th serial bit position	4/7 t_C – 0.15		4/7 t_C + 0.15	ns
t5	Delay time, CLK ↑ to 6th serial bit position	5/7 t_C – 0.15		5/7 t_C + 0.15	ns
t6	Delay time, CLK ↑ to 7th serial bit position	6/7 t_C – 0.15		6/7 t_C + 0.15	ns
tr	Differential output rise-time	180		500	ps
tf	Differential output fall-time	180		500	ps
REFCLK					
F_{REFCLK}	REFCLK Frequency	25		154	MHz
tr, tf	REFCLK rise and fall time	0.1		1	ns
t_{pj}	REFCLK peak-to-peak phase jitter			50	ps
Duty	REFCLK duty cycle	40%	50%	60%	
EN, ULPS, RESET (refer to Figure 7-5)					
t_{en}	Enable time from EN or ULPS			1	ms
t_{dis}	Disable time to standby			0.1	ms
t_{reset}	Reset time	10			ms

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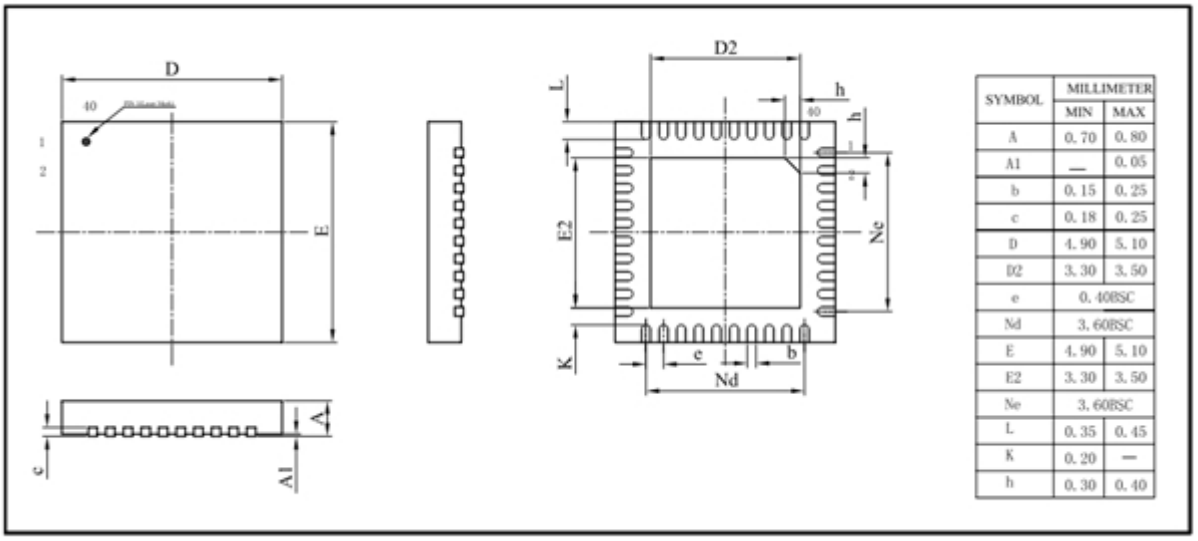
8 Package information

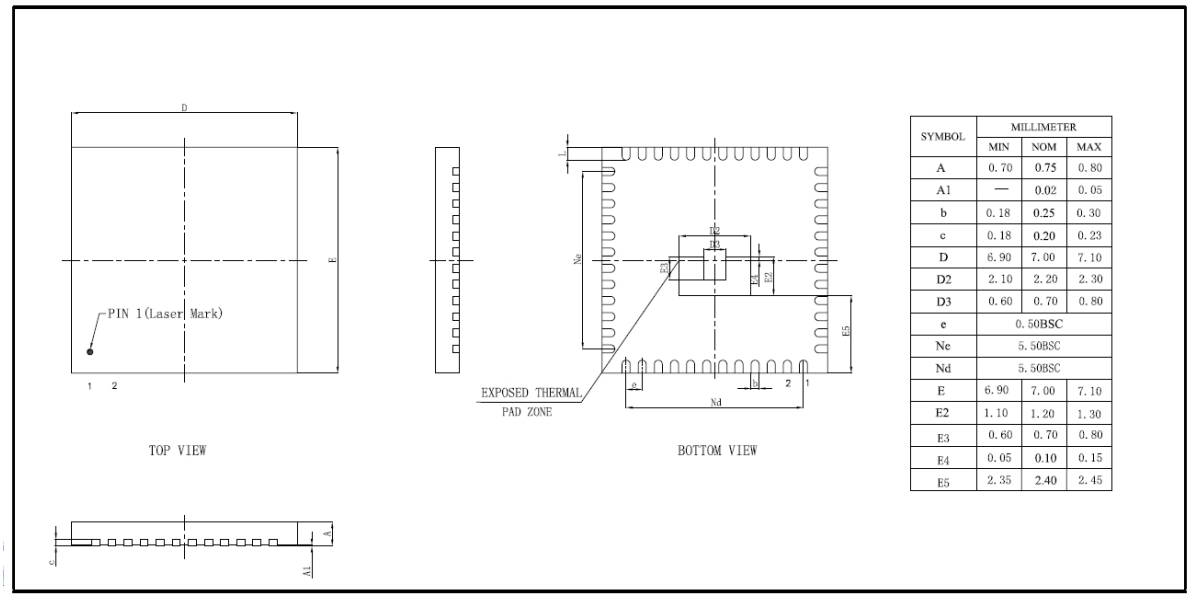
8.1 ICN6202 QFN40 package



SYMBOL	MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	—	0.05
b	0.15	0.25
c	0.18	0.25
D	4.90	5.10
D2	3.30	3.50
e	0.40BSC	
Nd	3.60BSC	
E	4.90	5.10
E2	3.30	3.50
Ne	3.60BSC	
L	0.35	0.45
K	0.20	—
h	0.30	0.40

Figure 8-1 ICN6202 QFN40 pin dimension

8.2 ICN6201 QFN48 package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.23
D	6.90	7.00	7.10
D2	2.10	2.20	2.30
D3	0.60	0.70	0.80
e	0.50BSC		
Ne	5.50BSC		
Nd	5.50BSC		
E	6.90	7.00	7.10
E2	1.10	1.20	1.30
E3	0.60	0.70	0.80
E4	0.05	0.10	0.15
E5	2.35	2.40	2.45

Figure 8-2 ICN6201 QFN48 pin with special shape e-pad dimension