# ICN6201

## Register Specification

### Revision 0.2



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# Revision History

| Rev | Date | Author | Description |
|---|---|---|---|
| 0.1 | 2013-07-22 | Simon_Liu | Initial |
| 0.2 | 2013-08-31 | Simon_Liu | Add register description |
| | | | |
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# 1 Register Set

## 1.1 Access Keys

**Table 1-1 Access Keys**

| Key | Description |
|---|---|
| R/W | Readable & Writable |
| RO | Read Only |
| WO | Write Only |
| RC | ReadClear |
| RW1TC | Readable & Write 1 to clear |
| RW0TC | Readable & Write 0 to clear |

## 1.2 Interrupt Controller Part (0x0100 ~ 0x01FF)

**Table 1-2 Interrupt Controller Register Map**

***Base Address: 0x0100***

| Register Name | Offset Address | SFR Address | Size(bits) | Description |
|---|---|---|---|---|
| IRQ_OUT_SEL | 0x007d | NA | 8 | Select IRQ pin output signals |
| REG_DBG_SEL | 0x007e | NA | 8 | Select Register debug signals |
| MIPI_REV_FORCE | 0x00c8 | | | Force the reverse transaction |
| MIPI_REG_DBG_SEL | 0x00e0 | | | Select MIPI register debug signals |
| | | | | |

**Table 1-3 VENDER_ID register**

**(Offset 0x0000)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| VENDER_ID | 7-0 | The ID of vender | RO | 8'hc1 | | | |

**Table 1-4 DEVICE_ID_H register**

**(Offset 0x0001)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| DEVICE_ID_H | 7-0 | The ID of device | RO | 8'h62 | | | |

**Table 1-5 DEVICE_ID_L register**

**(Offset 0x0002)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| DEVICE_ID_L | 7-0 | The ID of device | RO | 8'h01 | | | |

**Table 1-6 VERSION_ID register**

**(Offset 0x0003)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| VERSION_ID | 7-0 | The ID of version | RO | 8'hff | | | |

**Table 1-7 FIRMWARE_VERSION register**

**(Offset 0x0008)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| FIRMWARE_VERSION | 7-0 | The version of firmware | R/W | 8'h00 | | | |

**Table 1-8 CONFIG_FINISH register**

**(Offset 0x0009)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-5 | | -/- | -- | | | |
| CONFIG_FINISH | 4 | After set to 1'b1, the chip begins to work | R/W | 1'b0 | | | |
| Reserved | 3-1 | | -/- | -- | | | |
| SOFT_RESET | 0 | When set to 1'b1, reset the LVDS function | SC | 1'b0 | | | |

**Table 1-9 PD_CTRL_0 register**

**(Offset 0x000a)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PD_CTRL_0 | 7-0 | When one bit is set to 1'b1, power down related funcion's clk.<br>[0]: 216M for mipi lane0;<br>[1]: 216M for mipi lane1;<br>[2]: 216M for mipi lane2;<br>[3]: 216M for mipi lane3;<br>[4]: 216M for mipi lane clk;<br>[5]: 216M for others;<br>[6]: 216M for test;<br>[7]: hs clk for mipi test | R/W | 8'h00 | | | |

**Table 1-10 PD_CTRL_1 register**

**(Offset 0x000b)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PD_CTRL_1 | 7-0 | When one bit is set to 1'b1, power down related funcion's clk.<br>[0]: hs_clk for mipi lane0;<br>[1]: hs_clk for mipi lane1;<br>[2]: hs_clk for mipi lane2;<br>[3]: hs_clk for mipi lane3;<br>[4]: hs_clk for mipi RW;<br>[5]: hs_clk for mipi chksum;<br>[6]: hs_clk for mipi function;<br>[7]: hs_clk for bridge. | R/W | 8'h00 | | | |

**Table 1-11 PD_CTRL_2 register**

**(Offset 0x000c)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PD_CTRL_2 | 7-0 | When one bit is set to 1'b1, power down related funcion's clk.<br>[0]: lvds_clk for lvds lvds function<br>[1]: lvds_clk for bridge<br>[2]: clk for bist_gen<br>[3]: refclk_dig<br>[4]: pll_fbclk;<br>[5]: osc_cali<br>[6]: gold_clk. | R/W | 8'h00 | | | |

**Table 1-12 RST_CTRL_0 register**
**(Offset 0x000d)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| RST_CTRL_0 | 7-0 | When one bit is set to 1'b1, reset related function<br>[0]:reset LVDS(bridge, package,bist)<br>[7:1]: not used | R/W | 8'h00 | | | |

**Table 1-13 RST_CTRL_1 register**
**(Offset 0x000e)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| RST_CTRL_1 | 7-0 | When one bit is set to 1'b1, reset related function<br>[0]: i2c_slave;<br>[1]: arbiter;<br>[7:2]: not used. | R/W | 8'h00 | | | |

**Table 1-14 RST_CTRL_2 register**
**(Offset 0x000f)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| RST_CTRL_2 | 7-0 | When one bit is set to 1'b1, reset related function<br>[0]: lvds package<br>[1]: lvds bridge<br>[2]: bist_gen | R/W | 8'h00 | | | |

**Table 1-15 SYS_CTRL_0 register**
**(Offset 0x00010)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7 | | -/- | -- | | | |
| MIPI_XOR | 6 | Invert the mipi hs_clk | R/W | 1'b0 | | | |
| LVDS_XOR | 5 | Invert the lvds clk | R/W | 1'b0 | | | |
| DSM_XOR | 4 | Invert the dsm_clk | R/W | 1'b0 | | | |
| RST_WR_ADDR | 3 | 1'b1: reset address of line fifo for every line | R/W | 1'b0 | | | |
| VSW_MODE | 2 | 1: use register[0x28] to control the Vsync width | R/W | 1'b1 | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0: wait mipi “vse” | | | | | |
| HSW_MODE | 1 | 1: use register[0x24] to control the Hsync width<br>0: wait mipi “HSE” | R/W | 1’b1 | | | |
| BIST_GEN_EN | 0 | | R/W | 1’b1 | | | |

**Table 1-16 LVDS_CTRL_0 register**
**(Offset 0x00013)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| LVDS_LSB_MSB | 7 | 1: swap the 7bit sequence<br>0: normal sequence | R/W | 1’b0 | | | |
| LVDS_CLK_PN_SWAP | 6 | Lvds clock PN swap | R/W | 1’b0 | | | |
| LVDS_JEIDA_EN | 5 | 0: VESA; 1: JEIDA | R/W | 1’b0 | | | |
| LVDS_BIT_SEL | 4 | 0: 6bits; 1: 8bits | R/W | 1’b0 | | | |
| LVDS_DATA_PN_SWAP | 3-0 | Each bit controls one LVDS lane | R/W | 1’b0 | | | |

**Table 1-17 LVDS_CTRL_1 register**
**(Offset 0x00014)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7 | | -/- | -- | | | |
| LVDS_CLK_PATTERN | 6-0 | Set the LVDS clock lane pattern | R/W | 7’h63 | | | |

**Table 1-18 LVDS_CTRL_2 register**
**(Offset 0x00015)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| LVDS_LANE2_SEL[1:0] | 7-6 | LVDS lane2 select the packet pair | R/W | 2’b10 | | | |
| LVDS_LANE1_SEL | 5-3 | LVDS lane1 select the packet pair | R/W | 3’b001 | | | |
| LVDS_LANE0_SEL | 2-0 | LVDS lane0 select the packet pair | R/W | 3’b000 | | | |

**Table 1-19 LVDS_CTRL_3 register**
**(Offset 0x00016)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| LVDS_CHKSUM_EN | 7 | Enable LVDS checksum, just for test | R/W | 1’b0 | | | |
| LVDS_LANECK_SEL | 6-4 | LVDS lane clock select the packet pair | R/W | 3’b100 | | | |
| LVDS_LANE3_SEL | 3-1 | LVDS lane3 select the packet pair | R/W | 3’b011 | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| LVDS_LANE2_SEL[2] | 0 | LVDS lane2 select the packet pair | R/W | 1'b0 | | | |

**Table 1-20 LVDS_CTRL_4 register**
**(Offset 0x00017)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| LVDS_TEST_EN | 7 | Enable LVDS test | R/W | 1'h0 | | | |
| LVDS_TEST_TYPE | 6-5 | 00: low; 01: high; 10: clk; 11:prbs7 | R/W | 2'h0 | | | |
| LVDS_TEST_LANE | 4-0 | For each LVDS lane,<br>0: PRBS7 for MIPI Rx<br>1: set by LVDS_TEST_TYPE | R/W | 5'h0 | | | |

**Table 1-21 LOGIC RESET NUMBER register**
**(Offset 0x00018)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| LOGIC_RST_NUM | 7-0 | Set the reset time after PLL lock for digital logic function | R/W | 8'h10 | | | |

**Table 1-22 ATE PLL EN register**
**(Offset 0x0001f)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| ATE_PLL_EN | 7-0 | Enable PLL ATE | R/W | 8'h00 | | | |

**Table 1-23 HACTIVE_L register**
**(Offset 0x0020)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| HACTIVE[7:0] | 7-0 | Set the horizontal active pixl number | R/W | 8'h00 | | | |

**Table 1-24 VACTIVE_L register**
**(Offset 0x0021)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| VACTIVE[7:0] | 7-0 | Set the vertical active line number | R/W | 8'h58 | | | |

**Table 1-25 VACTIVE_HACTIVE_H register**
**(Offset 0x0022)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| VACTIVE[11:8] | 7-4 | Set the vertical active line number | R/W | 4'h2 | | | |
| HACTIVE[11:8] | 3-0 | Set the horizontal active pixel number | R/W | 4'h4 | | | |

**Table 1-26 HFP_L register**

**(Offset 0x0023)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| HFP[7:0] | 7-0 | Set the horizontal front port | R/W | 8'h54 | | | |

**Table 1-27 HSW_L register**

**(Offset 0x0024)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| HSW[7:0] | 7-0 | Set the horizontal sync width | R/W | 8'h64 | | | |

**Table 1-28 HBP_L register**

**(Offset 0x0025)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| HBP[7:0] | 7-0 | Set the horizontal back porch | R/W | 8'h38 | | | |

**Table 1-29 HFP_HSW_HBP_H register**

**(Offset 0x0026)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-6 | | -/- | -- | | | |
| HFP[9:8] | 5-4 | Set the horizontal front portch | R/W | 2'h0 | | | |
| HSW[9:8] | 3-2 | Set the horizontal sync width | R/W | 2'h0 | | | |
| HBP[9:8] | 1-0 | Set the horizontal back porch | R/W | 2'h0 | | | |

**Table 1-30 VFP register**

**(Offset 0x0027)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| VFP[7:0] | 7-0 | Set the vertical front porch | R/W | 8'h4 | | | |

**Table 1-31 VSW register**

**(Offset 0x0028)**

| Name | Bit | Description | R/W | Reset | CM | WM | RM |
|---|---|---|---|---|---|---|---|

| | | | | Value | | | |
|---|---|---|---|---|---|---|---|
| VSW[7:0] | 7-0 | Set the vertical sync width | R/W | 8'h4 | | | |

**Table 1-32 VBP register**

**(Offset 0x0029)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| VBP[7:0] | 7-0 | Set the vertical back porch | R/W | 8'h14 | | | |

**Table 1-33 BIST POL register**

**(Offset 0x002a)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| BIST_MODE | 7-4 | Select the bist mode<br>4'h0 : BIST mode is disabled<br>4'h1: Monochrome is enabled<br>4'h2 : Monochrome with colored border is enabled<br>4'h3: Chess board is enabled<br>4'h4 : Color bar is enabled<br>4'h5: Color switching is enabled<br>Others : reserved | R/W | 4'h0 | | | |
| BIST_FORCE | 3 | Force thei LVDS to send out bist_gen pattern | R/W | 1'h0 | | | |
| HS_POL | 2 | Set the hsync polarity | R/W | 1'h0 | | | |
| VS_POL | 1 | Set the vsync polarity | R/W | 1'h0 | | | |
| DE_POL | 0 | Set the de polarity | R/W | 1'h1 | | | |

**Table 1-34 BIST RED register**

**(Offset 0x002b)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| BIST_RED | 7-0 | Set the red color of bist_pattern. | R/W | 8'hff | | | |

**Table 1-35 BIST GREEN register**

**(Offset 0x002c)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| BIST_GREEN | 7-0 | Set the green color of bist_pattern. | R/W | 8'hff | | | |

**Table 1-36 BIST BLUE register**

**(Offset 0x002d)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| BIST_BLUE | 7-0 | Set the blue color of bist_pattern. | R/W | 8'hff | | | |

**Table 1-37 BIST CHESS X register**

**(Offset 0x002e)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| CHESS_X[7:0] | 7-0 | Set the chess width | R/W | 8'h01 | | | |

**Table 1-38 BIST CHESS Y register**

**(Offset 0x002f)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| CHESS_Y[7:0] | 7-0 | Set the chess height | R/W | 8'h01 | | | |

**Table 1-39 BIST CHESS XY_H register**

**(Offset 0x0030)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| CHESS_Y[11:8] | 7-4 | Set the chess heigth | R/W | 4'h0 | | | |
| CHESS_X[11:8] | 7-4 | Set the chess width | R/W | 4'h0 | | | |

**Table 1-40 BIST FRAME TIME L register**

**(Offset 0x0031)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| FRM_TIME[7:0] | 7-0 | Set the auto display frame time. | R/W | 8'h78 | | | |

**Table 1-41 BIST FRAME TIME H register**

**(Offset 0x0032)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SYNC_EVENT_DLY[11:8] | 7-4 | Set the delay number of MIPI event | R/W | 4'h0 | | | |
| FIFO_MAX_ADDR[9:8] | 3-2 | Set the fifo max address | R/W | 2'h3 | | | |
| FRM_TIME[9:8] | 1-0 | Set the auto display frame time | R/W | 2'h0 | | | |

**Table 1-42 FIFO MAX ADDR LOW register**

**(Offset 0x0033)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FIFO_MAX_ADDR[7:0] | 7-0 | Set the fifo max address | R/W | 8'hbf | | | |

**Table 1-43 SYNC EVENT DLY LOW register**
**(Offset 0x0034)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SYNC_EVENT_DLY[7:0] | 7-0 | Set the delay number of MIPI event | R/W | 8'h40 | | | |

**Table 1-44 HSW MIN register**
**(Offset 0x0035)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| HSW_MIN | 7-0 | Set the minimum pixel of HSW | R/W | 8'h8 | | | |

**Table 1-45 HFP MIN register**
**(Offset 0x0036)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| HFP_MIN | 7-0 | Set the minimum pixel of HFP | R/W | 8'h8 | | | |

**Table 1-46 TX_PHY_CTRL_0 register**
**(Offset 0x0040)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7 | | -/- | -- | | | |
| PD_TX_LOCK | 6 | 1: auto power down tx when pll is not done | R/W | 1'h1 | | | |
| PD_TX | 5 | 1: power down tx | R/W | 1'h0 | | | |
| PD_TX_CK | 4 | 1: power down lvds clock lane | R/W | 1'h0 | | | |
| PD_TX_CH3 | 3 | 1: power down lvds lane3 | R/W | 1'h0 | | | |
| PD_TX_CH2 | 2 | 1: power down lvds lane2 | R/W | 1'h0 | | | |
| PD_TX_CH1 | 1 | 1: power down lvds lane1 | R/W | 1'h0 | | | |
| PD_TX_CH0 | 0 | 1: power down lvds lane0 | R/W | 1'h0 | | | |

**Table 1-47 TX_PHY_CTRL_1 register**
**(Offset 0x0041)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TX_RTERM | 7 | LVDS near end differential terminal resistance:<br>0 for 100Ω ; 1 for 200Ω | R/W | 1'h0 | | | |
| TX_VOCM | 6 | LVDS data/clock output common mode<br>0 for 1.2V; 1 for 0.9V | R/W | 1'h1 | | | |
| TX_BYP_RSTDIV7 | 5 | Bypass DIV7 reset block | R/W | 1'h0 | | | |
| TX_CK_SWAP | 4 | Swap 7x clock polarity | R/W | 1'h0 | | | |
| TX_VOD_DATA | 3-0 | LVDS data output differential swing control<br>output swing=<3>*100m+<2:0>*50m+50m | R/W | 4'h3 | | | |

**Table 1-48 TX_PHY_CTRL_2 register**
**(Offset 0x0042)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| TX_VOD_CK | 7-4 | LVDS clock output differential swing control<br>output swing=<3>*100m+<2:0>*50m+50m | R/W | 4'h3 | | | |
| TX_VOCM_AD | 3-2 | LVDS data/clock output common mode fine adjust<br>TX_VOCM=0, 00: 1.12V, 01: 1.16V, 10: 1.2V, 11: 1.24V<br>TX_VOCM=1, 00: 0.86V, 01: 0.9V, 10: 0.94V, 11: 0.98V | R/W | 2'h1 | | | |
| Reserved | 1-0 | | -/- | -- | | | |

**Table 1-49 TX_PHY_CTRL_3 register**
**(Offset 0x0043)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7 | | -/- | -- | | | |
| TX_VOSL | 6-4 | LVDS data/clock output slew rate control | R/W | 3'h0 | | | |
| TX_SW_DATA | 3-2 | LVDS data driver switch strength<br>11: >=350mV, 10:200~350mV, 01:<200mV | R/W | 2'h2 | | | |
| TX_SW_CK | 1-0 | LVDS clock driver switch strength<br>11: >=350mV, 10:200~350mV, 01:<200mV | R/W | 2'h2 | | | |

**Table 1-50 TX_PHY_CTRL_4 register**
**(Offset 0x0044)**

| Name | Bit | Description | R/W | Reset | CM | WM | RM |
|---|---|---|---|---|---|---|---|

| | | | | Value | | | |
|---|---|---|---|---|---|---|---|
| TX_DCP_DATA | 7-6 | LVDS PMOS driver duty cycle control<br>for 0.9V VCM, recommend 3,<br>for 1.2V VCM, recommend 1 | R/W | 2'h3 | | | |
| TX_DCN_DATA | 5-4 | LVDS NMOS driver duty cycle control<br>for 0.9V VCM, recommend 3,<br>for 1.2V VCM, recommend 1 | R/W | 2'h3 | | | |
| TX_DCP_CK | 3-2 | LVDS PMOS driver duty cycle control<br>for 0.9V VCM, recommend 3,<br>for 1.2V VCM, recommend 1 | R/W | 2'h3 | | | |
| TX_DCN_CK | 1-0 | LVDS NMOS driver duty cycle control<br>for 0.9V VCM, recommend 3,<br>for 1.2V VCM, recommend 1 | R/W | 2'h3 | | | |

**Table 1-51 TX_PHY_CTRL_5 register**
**(Offset 0x0045)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| TX_TEST_EN | 7 | TX test enable | R/W | 1'h0 | | | |
| TX_TEST_SEL | 6-4 | TX test selection | R/W | 3'h0 | | | |
| Reserved | 3-0 | | -/- | -- | | | |

**Table 1-52 TX_PHY_CTRL_6 register**
**(Offset 0x0046)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| TX_RESERVE | 7-0 | reserve regesiter | R/W | 8'h00 | | | |

**Table 1-53 OSC_CTRL_0 register**
**(Offset 0x0048)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-5 | | -/- | -- | | | |
| CALI_SEQ_SET | 6 | 1: cali pll after osc cali finish;<br>0: cali pll directly | R/W | 1'h0 | | | |
| CALI_ULPS | 5 | 1: cali pll & osc again after ULPS<br>0: not cali pll & osc after ULPS | R/W | 1'h1 | | | |
| PLL_CALI_SIGN | 4 | Set PLL cali value sign(direction) | R/W | 1'h0 | | | |
| OSC_CALI_SIGN | 3 | Set OSC cali value sign(direction) | R/W | 1'h0 | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| OSC_CALI_REQ | 2 | Set 1 to request cali osc again | R/W | 1'h0 | | | |
| GOLD_CLK_SEL | 1-0 | Bit[1]=0: sel reference clk;<br>Bit[1]=1: sel mipi hs clk | R/W | 2'h0 | | | |

**Table 1-54 OSC_CTRL_1 register**
**(Offset 0x0049)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| OSC_CALI_EN | 7 | 1: cali osc;<br>0: not cali oscc, use OSC_FREQ | R/W | 1'h0 | | | |
| OSC_FREQ | 6-0 | Set the osc freq value when not cali osc | R/W | 7'h40 | | | |

**Table 1-55 OSC_CTRL_2 register**
**(Offset 0x004a)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| OSC_CALI_GOAL[7:0] | 7-0 | OSC cali goal value | R/W | 8'h00 | | | |

**Table 1-56 OSC_CTRL_3 register**
**(Offset 0x004b)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| OSC_CALI_GD_TIME[7:0] | 7-0 | Set the osc cali time window | R/W | 8'h00 | | | |

**Table 1-57 OSC_CTRL_4 register**
**(Offset 0x004c)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| OSC_CALI_GOAL[11:8] | 7-4 | OSC cali goal value | R/W | 4'h0 | | | |
| OSC_CALI_GD_TIME[11:8] | 3-0 | Set the osc cali time window | R/W | 4'h0 | | | |

**Table 1-58 OSC_CTRL_5 register**
**(Offset 0x004d)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| OSC_CALI_WT_TIME | 7-0 | Set the settle time for OSC each cali | R/W | 8'h1a | | | |

**Table 1-59 BG_CTRL register**

(Offset 0x004e)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| BG_TEST_EN | 7 | Bandgap test enable | R/W | 1'b0 | | | |
| Reserved | 6-2 | | -/- | -- | | | |
| LDODIG_REF | 1-0 | RX LDO reference voltage control<br>00:0.5V, 01:0.55V, 10:0.6V, 11:0.65V | R/W | 2'h2 | | | |

**Table 1-60 LDO_PLL register**

**(Offset 0x004f)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PD_LDOPLL_FORCE | 7 | When 1, use PD_LDOPLL | R/W | 1'b0 | | | |
| PD_LDOPLL | 6 | When 1, power down LDOPLL | R/W | 1'b0 | | | |
| Reserved | 5 | | -/- | -- | | | |
| LDOPLL_IDC | 4 | Control constant current for LDO | R/W | 1'b1 | | | |
| LDOPLL_REF | 3-2 | RX LDO reference voltage control<br>00:0.5V, 01:0.55V, 10:0.6V, 11:0.65V | R/W | 2'h2 | | | |
| LDOPLL_VO | 1-0 | RX LDO feedback ratio<br>00:1.85, 01:1.92, 10:2, 11:2.09 | R/W | 2'h2 | | | |

**Table 1-61 PLL_CTRL_0 register**

**(Offset 0x0050)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PD_PLL_FORCE | 7 | When 1, use PD_PLL | R/W | 1'b0 | | | |
| PD_PLL | 6 | When 1, power down PLL | R/W | 1'b0 | | | |
| Reserved | 5 | | -/- | -- | | | |
| PD_VCO | 4 | Power down VCO | R/W | 1'b1 | | | |
| PD_PFDCP | 3 | PD signal for PFD and charge pump | R/W | 1'b0 | | | |
| PD_FBDV | 2 | PD signal for feedback divider | R/W | 1'b0 | | | |
| Reserved | 1 | | -/- | -- | | | |
| PD_PLLDV | 0 | PD signal for PLL output divider | R/W | 1'b0 | | | |

**Table 1-62 PLL_CTRL_1 register**

(Offset 0x0051)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_CALI_EN | 7 | When 1, enable PLL cali | R/W | 1'b0 | | | |
| PLL_CALI_REQ | 6 | When 1, request PLL cali again | R/W | 1'b0 | | | |
| PLL_VCO_ISEL | 5-0 | Set the PLL_VCO_ISEL(default or force value) | R/W | 6'h8 | | | |

**Table 1-63 PLL_CTRL_2 register**

(Offset 0x0052)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_CALI_GOAL[7:0] | 7-0 | Set the goal value of PLL cali | R/W | 8'h00 | | | |

**Table 1-64 PLL_CTRL_3 register**

(Offset 0x0053)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_CALI_GD_TIME[7:0] | 7-0 | Set PLL cali time window | R/W | 8'h00 | | | |

**Table 1-65 PLL_CTRL_4 register**

(Offset 0x0054)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_CALI_GOAL[11:8] | 7-4 | Set the goal value of PLL cali | R/W | 4'h0 | | | |
| PLL_CALI_GD_TIME[11:8] | 3-0 | Set PLL cali time window | R/W | 4'h0 | | | |

**Table 1-66 PLL_CTRL_5 register**

(Offset 0x0055)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_CALI_WT_TIME[7:0] | 7-0 | Set PLL settle time before each cali. | R/W | 8'h1a | | | |

**Table 1-67 PLL_CTRL_6 register**

(Offset 0x0056)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_LPF_C | 7-5 | Loop filter capacitance control | R/W | 3'h4 | | | |
| PLL_LPF_R | 4-2 | Loop filter resistance control | R/W | 3'h4 | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PLL_REFSEL | 1-0 | PLL reference clock source:<br>00: from reference clock<br>10: from mipi high speed byte clock<br>11: from oscillator | R/W | 2'h0 | | | |

**Table 1-68 PLL_CTRL_7 register**
**(Offset 0x0057)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-4 | | -/- | -- | | | |
| PLL_TEST_EN | 3 | PLL test enable | R/W | 1'h0 | | | |
| PLL_TEST_SEL | 2-0 | PLL test selection | R/W | 3'h0 | | | |

**Table 1-69 PLL_CTRL_8 register**
**(Offset 0x0058)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7 | | -/- | -- | | | |
| PLL_OPEN | 6 | PLL open loop control<br>0: close loop, 1:open loop | R/W | 1'h0 | | | |
| PLL_LKDET_EN | 5 | PLL lock detection enable | R/W | 1'h1 | | | |
| PLL_ICP | 4-0 | Charge pump current default : 6uA and step = 3uA<br>Charge pump current=(PLL_ICP<2:0>+1)*step<br>step=2uA @ PLL_ICP<4:3>=00<br>step=3uA @ PLL_ICP<4:3>=01<br>step=4uA @ PLL_ICP<4:3>=10<br>step=6uA @ PLL_ICP<4:3>=11<br>suggested current = 9uA (PLL_ICP=5'ha) @ REFCLK_DIG<=18MHz<br>suggested current = 12uA (PLL_ICP=5'hb) @ REFCLK_DIG<=12MHz | R/W | 5'h9 | | | |

**Table 1-70 PLL_CTRL_9 register**
**(Offset 0x0059)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_DITHER_EN | 7-5 | Set PLL dither type | R/W | 3'h0 | | | |
| PLL_C_DLY_EN | 4 | When 1, delay DSM C value | R/W | 1'h0 | | | |
| PLL_INT_DLY_NUM | 3-2 | Set the integer delay number for DSM | R/W | 2'h0 | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PLL_DSM_TYPE | 1-0 | 00: 1 order; 01: 2 order; 10: 3 order | R/W | 2'h1 | | | |

**Table 1-71 PLL_CTRL_A register**
**(Offset 0x005a)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_DLY_LDO[7:0] | 7-0 | Set PLL wait LDO time | R/W | 8'he | | | |

**Table 1-72 PLL_CTRL_B register**
**(Offset 0x005b)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_DLY_UP[7:0] | 7-0 | Set PLL power up time | R/W | 8'h1e | | | |

**Table 1-73 PLL_CTRL_C register**
**(Offset 0x005c)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_WT_LOCK[7:0] | 7-0 | Set wait PLL lock time | R/W | 8'h64 | | | |

**Table 1-74 PLL_CTRL_D register**
**(Offset 0x005d)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_DLY_LDO[9:8] | 7-6 | Set PLL wait LDO time | R/W | 2'h1 | | | |
| PLL_DLY_UP[9:8] | 5-4 | Set PLL power up time | R/W | 2'h2 | | | |
| PLL_WT_LOCK[11:8] | 3-0 | Set wait PLL lock time | R/W | 4'h0 | | | |

**Table 1-75 PLL_CTRL_E register**
**(Offset 0x005e)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_TX_RST | 7-0 | Set tx rst time after PLL lock | R/W | 8'h1b | | | |

**Table 1-76 PLL_CTRL_F register**
**(Offset 0x005f)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Reserved | 7 | | -/- | -- | | | |
| PLL_AFCREF | 6-4 | PLL AFC reference voltage selection, 0.55+PLL_AFCREF*0.03 | R/W | 3'h4 | | | |
| PLL_PREDIV2 | 3 | FBDV pre divide by 2, 0: div1, 1: div2 | R/W | 1'h0 | | | |
| PLL_VGAIN | 2-0 | VCO bias select, PMOS finger=PLL_VGAIN*2+2 | R/W | 3'h3 | | | |

**Table 1-77 PLL_REM_0 register**
**(Offset 0x0060)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_REM[7:0] | 7-0 | PLL remainder[7:0] | R/W | 8'h00 | | | |

**Table 1-78 PLL_REM_1 register**
**(Offset 0x0061)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_REM[15:8] | 7-0 | PLL remainder[15:8] | R/W | 8'h00 | | | |

**Table 1-79 PLL_REM_2 register**
**(Offset 0x0062)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_REM[23:16] | 7-0 | PLL remainder[23:16] | R/W | 8'h00 | | | |

**Table 1-80 PLL_DIV_0 register**
**(Offset 0x0063)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_DIV[7:0] | 7-0 | Set the divisor[7:0] | R/W | 8'hff | | | |

**Table 1-81 PLL_DIV_1 register**
**(Offset 0x0064)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_DIV[15:8] | 7-0 | Set the divisor[15:8] | R/W | 8'h00 | | | |

**Table 1-82 PLL_DIV_2 register**
**(Offset 0x0065)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PLL_DIV[23:16] | 7-0 | Set the divisor[23:16] | R/W | 8'h00 | | | |

**Table 1-83 PLL_FRAC_0 register**
**(Offset 0x0066)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_FRAC[7:0] | 7-0 | Set the fraction[7:0] | R/W | 8'h00 | | | |

**Table 1-84 PLL_FRAC_1 register**
**(Offset 0x0067)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_FRAC[15:8] | 7-0 | Set the fraction[15:8] | R/W | 8'h00 | | | |

**Table 1-85 PLL_FRAC_2 register**
**(Offset 0x0068)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_FRAC[23:16] | 7-0 | Set the fraction[23:16] | R/W | 8'h00 | | | |

**Table 1-86 PLL_INT_0 register**
**(Offset 0x0069)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PLL_INT[7:0] | 7-0 | Set integer[7:0] | R/W | 8'h16 | | | |

**Table 1-87 PLL_INT_1 register**
**(Offset 0x006a)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-4 | | -/- | -- | | | |
| SSC_ENABLE | 3 | When 1, enable ssc | R/W | 1'h0 | | | |
| DET_LOCK_SEL | 2 | 1: sel lockb; 0:sel locka. | R/W | 1'h0 | | | |
| PLL_INT[9:8] | 1-0 | Set integer[9:8] | R/W | 2'h0 | | | |

**Table 1-88 PLL_REF_DIV register**
**(Offset 0x006b)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7 | | -/- | -- | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PLL_DV | 6-5 | PLL output divide ratio:<br>00: 1; 01: 2<br>10: 4; 11: 8 | R/W | 2'h0 | | | |
| PLL_REFDIV | 4-0 | Reference clock divide ratio<br>PLL_REFDIV<3:0> : 1~15: divide by 1~15, 0: divide by 16<br>PLL_REFDIV<4> , 0: no extra divide, 1: extra divide by 2 | R/W | 5'h1 | | | |

**Table 1-89 PLL_SSC_P0 register**
**(Offset 0x006c)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SSC_PERIOD[7:0] | 7-0 | Set SSC period[7:0] | R/W | 8'h0 | | | |

**Table 1-90 PLL_SSC_P1 register**
**(Offset 0x006d)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SSC_PERIOD[15:8] | 7-0 | Set SSC period[15:8] | R/W | 8'h0 | | | |

**Table 1-91 PLL_SSC_P2 register**
**(Offset 0x006e)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SSC_PERIOD[23:16] | 7-0 | Set SSC period[23:16] | R/W | 8'h0 | | | |

**Table 1-92 PLL_SSC_STEP0 register**
**(Offset 0x006f)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SSC_STEP[7:0] | 7-0 | Set SSC step[7:0] | R/W | 8'h0 | | | |

**Table 1-93 PLL_SSC_STEP1 register**
**(Offset 0x0070)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SSC_STEP[15:8] | 7-0 | Set SSC step[15:8] | R/W | 8'h0 | | | |

**Table 1-94 PLL_SSC_STEP2 register**
**(Offset 0x0071)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SSC_STEP[23:16] | 7-0 | Set SSC step[23:16] | R/W | 8'h0 | | | |

**Table 1-95 PLL_SSC_OFFSET0 register**
**(Offset 0x0072)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SSC_OFFSET[7:0] | 7-0 | Set SSC offset[7:0] | R/W | 8'h0 | | | |

**Table 1-96 PLL_SSC_OFFSET1 register**
**(Offset 0x0073)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SSC_OFFSET[15:8] | 7-0 | Set SSC offset[15:8] | R/W | 8'h0 | | | |

**Table 1-97 PLL_SSC_OFFSET2 register**
**(Offset 0x0074)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SSC_OFFSET[23:16] | 7-0 | Set SSC offset[23:16] | R/W | 8'h0 | | | |

**Table 1-98 PLL_SSC_OFFSET3 register**
**(Offset 0x0075)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SSC_OFFSET[31:24] | 7-0 | Set SSC offset[31:24] | R/W | 8'h0 | | | |

**Table 1-99 GPIO_OEN register**
**(Offset 0x0079)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| GPIO_1_OEN | 7 | Not used | R/W | 1'h0 | | | |
| GPIO_0_OEN | 6 | Not used | R/W | 1'h0 | | | |
| Reserved | 5-1 | | -/- | -- | | | |
| ARBITER_CONFLICT | 0 | Not used | RW1TC | 1'h0 | | | |

**Table 1-100 MIPI_CFG_PW register**
**(Offset 0x007a)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MIPI_CFG_PW | 7-0 | When 8'hc1, mipi can config local regs | R/W | 8'h3e | | | |

**Table 1-101 GPIO_0_SEL register**
**(Offset 0x007b)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| GPIO_0_SEL | 7-0 | Select gpio_0 output signals | R/W | 8'hff | | | |

**Table 1-102 GPIO_1_SEL register**
**(Offset 0x007c)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| GPIO_1_SEL | 7-0 | Select gpio_1 output signals | R/W | 8'hf1 | | | |

**Table 1-103 IRQ_SEL register**
**(Offset 0x007d)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| IRQ_SEL | 7-0 | Select irq output signals | R/W | 8'h01 | | | |

**Table 1-104 DBG_SEL register**
**(Offset 0x007e)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| GPIO_1_IN | 7 | Not used | RO | 1'h0 | | | |
| GPIO_0_IN | 6 | Not used | RO | 1'h0 | | | |
| DBG_SEL | 5-0 | Select the debug signals for [0x7f] | R/W | 6'h00 | | | |

**Table 1-105 DBG_SIGNAL register**
**(Offset 0x007f)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| DBG_SIGNAL | 7-0 | Debug signals. | R/W | 8'h00 | | | |

**Table 1-106 MIPI_ERR_VECTOR_L register**
**(Offset 0x0080)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| SOT_ERR | 0 | SoT error | R/W | 1'h0 | | | |
| SOT_SYNC_ERR | 1 | SoT sync Error | R/W | 1'h0 | | | |
| EOT_SYNC_ERR | 2 | EoT sync error | R/W | 1'h0 | | | |
| EMEC_ERR | 3 | Escape Mode Entry Command Error | R/W | 1'h0 | | | |
| LPT_SYNC_ERR | 4 | Low-Power Transmit sync error | R/W | 1'h0 | | | |
| PERIPHERAL_ERR | 5 | Peripheral timeout error | R/W | 1'h0 | | | |
| FALSE_CTRL_ERR | 6 | False control Error | R/W | 1'h0 | | | |
| CONTENTION_ERR | 7 | Contention Detected | R/W | 1'h0 | | | |

**Table 1-107 MIPI_ERR_VECTOR_H register**
**(Offset 0x0081)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| ECC_SINGLE_ERR | 0 | ECC error, single-bit | R/W | 1'h0 | | | |
| ECC_MULTI_ERR | 1 | ECC error, multi-bit | R/W | 1'h0 | | | |
| CHKSUM_ERR | 2 | Checksum Error | R/W | 1'h0 | | | |
| DDTNR_ERR | 3 | DSI Data type Not Recoginized | R/W | 1'h0 | | | |
| DSI_VC_ERR | 4 | DSI VC ID invalid | R/W | 1'h0 | | | |
| TRAN_LEN_ERR | 5 | Invalid Transmission Length | R/W | 1'h0 | | | |
| RESERVED_ERR | 6 | Reserved | R/W | 1'h0 | | | |
| PROT_VIO_ERR | 7 | DSI Protocol Violation | R/W | 1'h0 | | | |

**Table 1-108 MIPI_ERR_VECTOR_EN_L register**
**(Offset 0x0082)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| ERR_VECT_EN[7:0] | 7-0 | Error enable | R/W | 8'hff | | | |

**Table 1-109 MIPI_ERR_VECTOR_EN_H register**
**(Offset 0x0083)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| ERR_VECT_EN[15:8] | 7-0 | Error enable | R/W | 8'hff | | | |

**Table 1-110 MIPI_MAX_SIZE_L register**
**(Offset 0x0084)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| MAX_SIZE[7:0] | 7-0 | The maximum return packet size | R/W | 8'h01 | | | |

**Table 1-111 MIPI_MAX_SIZE_H register**
**(Offset 0x0085)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| MAX_SIZE[15:8] | 7-0 | The maximum return packet size | R/W | 8'h00 | | | |

**Table 1-112 DSI_CTRL register**
**(Offset 0x0086)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| MIPI_LINE_DIV_EN | 7 | 1: enable one line divided into multi packdet | R/W | 1'h0 | | | |
| MIPI_BIT_SWAP | 6 | 1: enable mipi rx 8bits MSB/LSB swap | R/W | 1'h0 | | | |
| MIPI_CHKSUM_EN | 5 | 1: enabler reverse transition with checksum | R/W | 1'h1 | | | |
| MIPI_8B9B_EN | 4 | Not used | R/W | 1'h0 | | | |
| MIPI_VIDEO_MODE | 3-2 | Not used | R/W | 2'h2 | | | |
| MIPI_LANE_NUM | 1-0 | 00: 1 lane; 01: 2 lane<br>10: 3 lane; 11: 4 lane | R/W | 2'h3 | | | |

**Table 1-113 MIPI_PN_SWAP register**
**(Offset 0x0087)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-6 | | -/- | -- | | | |
| AUTO_LPX_EN | 5 | 1: enable auto check LPX time for reverse transition. | R/W | 1'b0 | | | |
| MIPI_CLK_PN_SWAP | 4 | 1: enable mipi clock lane p/n swap | R/W | 1'h0 | | | |
| MIPI_DATA_PN_SWAP | 3-0 | 1: enable mipi data lane p/n swap | R/W | 4'h0 | | | |

**Table 1-114 MIPI_SOT_SYNC_BIT register**
**(Offset 0x0088)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| CLR_ERR_VECT | 7 | Write 1 to self clear | WSC | 1'b0 | | | |
| MIPI_SYNC_FOREVER | 6 | 1: enable find the sync pattern 011101 | R/W | 1'b0 | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | forever | | | | | |
| MIPI_SOT_SYNC_BIT | 5:0 | When one bit is 1, then the sync pattern can be error. | R/W | 6'h00 | | | |

**Table 1-115 MIPI_SOT_SYNC_BIT register**
**(Offset 0x0089)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-4 | | -/- | -- | | | |
| USE_LOCK_DET | 3 | 1: use hs_ck_det from analog<br>0: use digital detect logic | R/W | 1'b0 | | | |
| CON_DET_EN | 2 | 1: enable contention detect when reverse transsition | R/W | 1'b0 | | | |
| TIME_OUT_EN | 1-0 | bit[0]: enable HS_RX timeout check<br>bit[1]: not used | R/W | 2'b00 | | | |

**Table 1-116 MIPI_ULPS_CTRL register**
**(Offset 0x008a)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-6 | | -/- | -- | | | |
| ULPS_AND_OR | 5 | 0: use and logic with used lanes to set ULPS;<br>1: use or logic with used lanes to set ULPS | R/W | 1'b0 | | | |
| ULPS_EN | 4-0 | Enable related lanes to check ULPS | R/W | 5'h00 | | | |

**Table 1-117 MIPI_CLK_CHK_VAR register**
**(Offset 0x008e)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| CHK_CLK_EN | 7 | check MIPI RX clock stable or not | R/W | 1'b0 | | | |
| CHK_CLK_VAR | 6-0 | Set the variable when check MIPI RX clock | R/W | 7'h00 | | | |

**Table 1-118 MIPI_CLK_CHK_INI register**
**(Offset 0x008f)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| CHK_CLK_INI | 7-0 | Set the mipi rx clock check time | R/W | 8'h00 | | | |

**Table 1-119 MIPI_T_TERM_EN register**
**(Offset 0x0090)**

| Name | Bit | Description | R/W | Reset | CM | WM | RM |
|---|---|---|---|---|---|---|---|

| | | | | Value | | | |
|---|---|---|---|---|---|---|---|
| T_D_TERM_EN | 7-0 | Time for the data lane receiver to enable the HS line termination | R/W | 8'h05 | | | |

**Table 1-120 MIPI_T_HS_SETTLE register**
**(Offset 0x0091)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| T_HS_SETTLE | 7-0 | Time interval during which the HS receiver shall ignore any data lane HS transitions | R/W | 8'h0a | | | |

**Table 1-121 MIPI_T_TA_SURE_PRE register**
**(Offset 0x0092)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-5 | | | | | | |
| T_TA_SURE_PRE | 4-0 | Set the factor the TA_SURE time with T_LPX.<br>Bit[4]: integer;<br>[3:0]: fraction; | R/W | 5'h18 | | | |

**Table 1-122 MIPI_T_LPX_SET register**
**(Offset 0x0094)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| T_LPX_SET | 7-0 | When r_auto_lpx_en = 0, set the transmitted length of any low-power state period. | R/W | 8'h0d | | | |

**Table 1-123 MIPI_T_CLK_MISS register**
**(Offset 0x0095)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| T_CLK_MISS | 7-0 | Timeout for receiver to detect absence of clock transitions and disable the clock lane HS-RX | R/W | 8'h04 | | | |

**Table 1-124 MIPI_INIT_TIME_L register**
**(Offset 0x0096)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| T_INIT_TIME[7:0] | 7-0 | Set the initial time after power on | R/W | 8'h64 | | | |

**Table 1-125 MIPI_INIT_TIME_H register**
**(Offset 0x0097)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-4 | | -/- | -- | | | |
| T_INIT_TIME[11:8] | 3-0 | Set the initial time after power on | R/W | 4'h0 | | | |

**Table 1-126 MIPI_T_CLK_TERM_EN register**
**(Offset 0x0099)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| T_CLK_TERM_EN | 7-0 | Time for the clock lane receiver to enable the HS line termination. | R/W | 8'h05 | | | |

**Table 1-127 MIPI_T_CLK_SETTLE register**
**(Offset 0x009a)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| T_CLK_SETTLE | 7-0 | Time interval during which the HS receiver shall ignore any Clock Lane HS transitions. | R/W | 8'h96 | | | |

**Table 1-128 MIPI_TO_HS_RX_L register**
**(Offset 0x009e)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| HS_RX_TIMEOUT[7:0] | 7-0 | Set the HS-RX max time | R/W | 8'h00 | | | |

**Table 1-129 MIPI_TO_HS_RX_H register**
**(Offset 0x009f)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| HS_RX_TIMEOUT[15:8] | 7-0 | Set the HS-RX max time | R/W | 8'h00 | | | |

**Table 1-130 MIPI_PHY_0 register**
**(Offset 0x00a0)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| RX_RT_CTRL | 7-6 | RX terminal resistor value control<br>00:90ohm, 01:100ohm,<br>10:110ohm, 11:120ohm | R/W | 2'b01 | | | |
| RX_EQ_CTRL | 5-4 | RX equalization gain control | R/W | 2'b00 | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | 00:0dB; 01:1dB; 10:2dB; 11:3dB | | | | | |
| Reserved | 3 | | -/- | -- | | | |
| RX_CK_SWP | 2 | Swap deserializer clock polarity | R/W | 1'b0 | | | |
| RX_SKEW_CK | 1-0 | RX high speed output clock skew control | R/W | 2'b00 | | | |

**Table 1-131 MIPI_PHY_1 register**
**(Offset 0x00a1)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| RX_SKEW_CH3 | 7-6 | RX high speed output clock skew control | R/W | 2'b00 | | | |
| RX_SKEW_CH2 | 5-4 | RX high speed output clock skew control | R/W | 2'b00 | | | |
| RX_SKEW_CH1 | 3-2 | RX high speed output clock skew control | R/W | 2'b00 | | | |
| RX_SKEW_CH0 | 1-0 | RX high speed output clock skew control | R/W | 2'b00 | | | |

**Table 1-132 MIPI_PHY_2 register**
**(Offset 0x00a2)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| RX_HS_COMP | 7-6 | RX high speed mode comparator current control. bias current: 00:12uA, 01:18uA, 10:24uA, 11:30uA | R/W | 2'b10 | | | |
| RX_LPRX_COMP | 5-4 | RX LPRX comparator current control bias current: 00:12uA, 01:18uA, 10:24uA, 11:30uA | R/W | 2'b00 | | | |
| RX_LPCD_COMP | 3-2 | RX LPCD comparator current control bias current: 00:12uA, 01:18uA, 10:24uA, 11:30uA | R/W | 2'b00 | | | |
| RX_LP_LOAD | 1-0 | Low power reverse mode output load control for slew rate 00:0p, 01:2p, 10:4p, 11: 6p | R/W | 2'b01 | | | |

**Table 1-133 MIPI_PHY_3 register**
**(Offset 0x00a3)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| RX_REF_LPRX | 7-6 | RX low power receiver reference voltage control 00:690mV, 01:715mV, 10:740mV, 11:765mV | R/W | 2'b01 | | | |
| RX_REF_LPCD | 5-4 | RX low power contention detector reference voltage control | R/W | 2'b0 | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | 00:295mV, 01:320mV, 10:345mV, 11:370mV | | | | | |
| Reserved | 3-2 | | -/- | -- | | | |
| RX_REF_BYP | 1 | RX reference voltage bypass | R/W | 1'b1 | | | |
| RX_HSPLL_SEL | 0 | HSCLK_PLL selection, 0: div4, 1:div1, for <100MHz, no divide | R/W | 1'b0 | | | |

**Table 1-134 MIPI_PHY_4 register**
**(Offset 0x00a4)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-5 | | -/- | -- | | | |
| LDORX_IDC | 4 | Control constant current for LDO | R/W | 1'b0 | | | |
| LDORX_REF | 3-2 | RX LDO reference voltage control 00:0.5V, 01:0.55V, 10:0.6V, 11:0.65V | R/W | 2'b10 | | | |
| LDORX_VO | 1-0 | RX LDO feedback ratio 00:1.85, 01:1.92, 10:2, 11:2.09 | R/W | 2'b10 | | | |

**Table 1-135 MIPI_PHY_5 register**
**(Offset 0x00a5)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| RX_RESERVE | 7-0 | reserve regesiter | R/W | 8'h00 | | | |

**Table 1-136 MIPI_PD_RX register**
**(Offset 0x00b0)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-1 | | -/- | -- | | | |
| PD_RX | 0 | PD signal for RX, 1 for power down, 0 for power up | R/W | 1'b0 | | | |

**Table 1-137 MIPI_PD_TERM register**
**(Offset 0x00b1**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PD_TERM_FORCE | 7-4 | Force the term with PD_TERM_VALUE | R/W | 4'h0 | | | |
| PD_TERM_VALUE | 3-0 | Set the forced value | R/W | 4'h0 | | | |

**Table 1-138 MIPI_PD_HSRX register**

(Offset 0x00b2)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PD_HSRX_FORCE | 7-4 | Force the hsrx with PD_HSRX_VALUE | R/W | 4'h0 | | | |
| PD_HSRX_VALUE | 3-0 | Set the force value | R/W | 4'h0 | | | |

Table 1-139 MIPI_PD_LPTX register

(Offset 0x00b3)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PD_LPTX_FORCE | 7-4 | Force the LPTX with PD_LPTX_VALUE | R/W | 4'h0 | | | |
| PD_LPTX_VALUE | 3-0 | | R/W | 4'hf | | | |

Table 1-140 MIPI_PD_LPRX register

(Offset 0x00b4)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PD_LPRX | 7-4 | Power down the LPRX | R/W | 4'h0 | | | |
| PD_LPCD | 3-0 | Power down the LPCD | R/W | 4'hf | | | |

Table 1-141 MIPI_PD_CK_LANE register

(Offset 0x00b5)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| PD_CK_TERM_FORCE | 7 | Force clock lane TERM with PD_CK_TERM_VALUE | R/W | 1'b0 | | | |
| PD_CK_TERM_VALUE | 6 | Set the force value | R/W | 1'b0 | | | |
| PD_CK_HSRX_FORCE | 5 | Force clock lane HSRX with PD_CK_HSRX_VALUE | R.W | 1'b0 | | | |
| PD_CK_HSRX_VALUE | 4 | Set the force value | R/W | 1'b0 | | | |
| PD_CK_LPRX | 3 | Power down clock lane LPRX | R/W | 1'b0 | | | |
| PD_LPCD_FORCE | 2 | For lane0 | R/W | 1'b0 | | | |
| Reserved | 1-0 | | R/W | 2'b00 | | | |

Table 1-142 MIPI_FORCE_0 register

(Offset 0x00b6)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| LAST_RD_FORCE | 7 | Debug: force last rd type. | R/W | 1'b0 | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| LAST_RD_VALUE | 6 | Debug: force last rd value | R/W | 1'b0 | | | |
| SHUT_DOWN_FORCE | 5 | Dedbug: force shut down | R.W | 1'b0 | | | |
| SHUT_DOWN_VALUE | 4 | Debug: force shut down value | R/W | 1'b0 | | | |
| REVERSE_FIX_LONG | 3 | 1: reverse use long packet only | R/W | 1'b0 | | | |
| Reserved | 2-0 | | -/- | -- | | | |

**Table 1-143 MIPI_RST_CTRL register**
**(Offset 0x00b7)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-3 | | -/- | -- | | | |
| MIPI_RST_200 | 2 | 1: reset mipi rx 200M clock domain | R/W | 1'b0 | | | |
| MIPI_RST_HS_BYTE | 1 | 1: reset mipi rx hs_clk domain | R/W | 1'b0 | | | |
| MIPI_RST_HS_BRIDGE | 0 | 1: reset bridge hs_clk domain | R.W | 1'b0 | | | |

**Table 1-144 MIPI_RST_NUM register**
**(Offset 0x00b8)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| Reserved | 7-4 | | -/- | -- | | | |
| MIPI_HS_RST_NUM | 3-0 | Set the reset time for hs_clk | R/W | 4'ha | | | |

**Table 1-145 MIPI_DBG_SET_0 register**
**(Offset 0x00c0)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| MIPI_REV_DATA_0 | 7-0 | Set the reverse transition value | R/W | 8'h00 | | | |

**Table 1-146 MIPI_DBG_SET_1 register**
**(Offset 0x00c1)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| MIPI_REV_DATA_1 | 7-0 | Set the reverse transition value | R/W | 8'h00 | | | |

**Table 1-147 MIPI_DBG_SET_2 register**
**(Offset 0x00c2)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| MIPI_REV_DATA_2 | 7-0 | Set the reverse transition value | R/W | 8'h00 | | | |

Table 1-148 MIPI_DBG_SET_3 register
(Offset 0x00c3)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| MIPI_REV_DATA_3 | 7-0 | Set the reverse transition value | R/W | 8'h00 | | | |

Table 1-149 MIPI_DBG_SET_4 register
(Offset 0x00c4)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| MIPI_REV_DATA_4 | 7-0 | Set the reverse transition value | R/W | 8'h00 | | | |

Table 1-150 MIPI_DBG_SET_5 register
(Offset 0x00c5)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| MIPI_REV_DATA_5 | 7-0 | Set the reverse transition value | R/W | 8'h00 | | | |

Table 1-151 MIPI_DBG_SET_6 register
(Offset 0x00c6)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| MIPI_REV_DATA_6 | 7-0 | Set the reverse transition value | R/W | 8'h00 | | | |

Table 1-152 MIPI_DBG_SET_7 register
(Offset 0x00c7)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| MIPI_REV_DATA_7 | 7-0 | Set the reverse transition value | R/W | 8'h00 | | | |

Table 1-153 MIPI_DBG_SET_8 register
(Offset 0x00c8)

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| REV_REG_EN | 7 | 1: trnasiton with the register set value | R/W | 1'b0 | | | |
| REG_REG_LENGTH | 6_4 | Set the reverse transition length | R/W | 3'h0 | | | |
| DBG_DI_WC_SEL | 3 | 0: latch all word count<br>1: latch only video word count | R/W | 1'b0 | | | |
| DBG_DI_WC_EN | 2 | 1: enable latch word count | R/W | 1'b0 | | | |
| DBG_PHY_EN | 1 | When 1, latch the front 4 non-zero data. | R/W | 1'b0 | | | |
| DBG_EN | 0 | Only this is set to 1'b1, above debug | R/W | 1'b0 | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | function is enabled. | | | | | |

**Table 1-154 MIPI_DBG_SET_9 register**
**(Offset 0x00c9)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| RX_TEST_EN | 7 | RX PHY test enable | R/W | 1'b0 | | | |
| RX_TEST_SEL | 6_4 | RX PHY test select | R/W | 3'h0 | | | |
| AT_EN | 3 | analog test enable | R/W | 1'b0 | | | |
| ATBUF_BYP | 2 | bypass analog test buffer | R/W | 1'b1 | | | |
| Reserved | 1-0 | | -/- | -- | | | |

**Table 1-155 MIPI_DBG_SEL register**
**(Offset 0x00e0)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| DBG_SEL | 7-0 | Select debug register signals for DBG_DAT | R/W | 8'h00 | | | |

**Table 1-156 MIPI_DBG_DATA register**
**(Offset 0x00e1)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| DBG_DAT | 7-0 | Based on DGB_SEL[0xe0] | RO | 8'h00 | | | |

**Table 1-157 MIPI_ATE_TEST_SEL register**
**(Offset 0x00e2)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| TX_DATA_FORCE | 7 | Ate test | R/W | 1'b0 | | | |
| TX_TEST_DATA | 6-5 | Ate test | R/W | 2'b00 | | | |
| LP_TX_RX_TEST | 4 | Ate test | R/W | 1'b0 | | | |
| HS_TEST_128 | 3 | Ate test | R/W | 1'b1 | | | |
| HS_TEST_SEL | 2 | Ate test | R/W | 1'b0 | | | |
| HS_TEST | 1 | Ate test | R/W | 1'b0 | | | |
| LP_TEST | 0 | Ate test | R/W | 1'b0 | | | |

**Table 1-158 MIPI_ATE_STATUS_0 register**
**(Offset 0x00e3)**

| Name | Bit | Description | R/W | Reset | CM | WM | RM |
|---|---|---|---|---|---|---|---|

| | | | | Value | | | |
|---|---|---|---|---|---|---|---|
| DBG_STATUS_0 | 7-0 | Ate test status | RO | 8'h00 | | | |

**Table 1-159 MIPI_ATE_STATUS_1 register**
**(Offset 0x00e3)**

| Name | Bit | Description | R/W | Reset Value | CM | WM | RM |
|---|---|---|---|---|---|---|---|
| DBG_STATUS_0 | 7-0 | Ate test status | RO | 8'h00 | | | |