

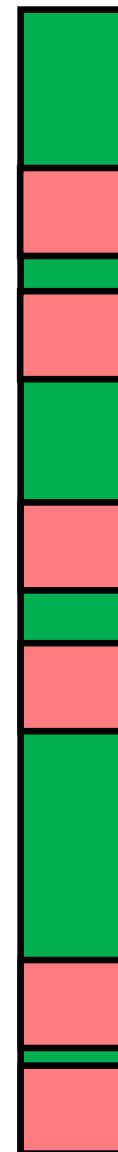
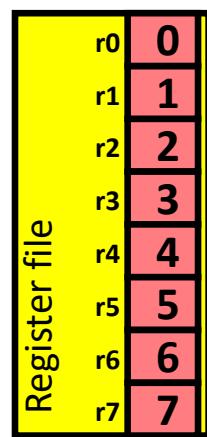
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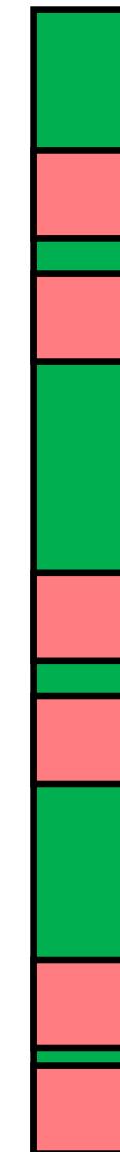
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mem



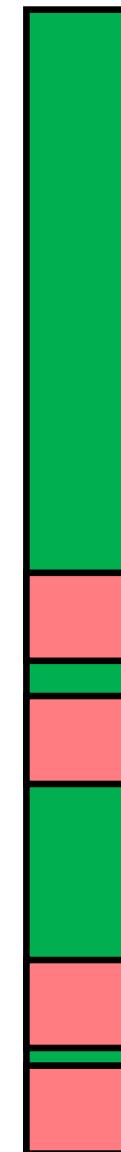
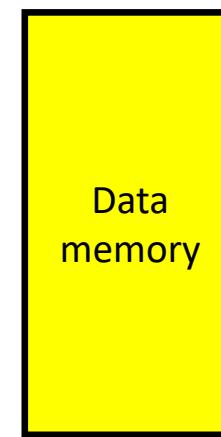
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EX



MEM

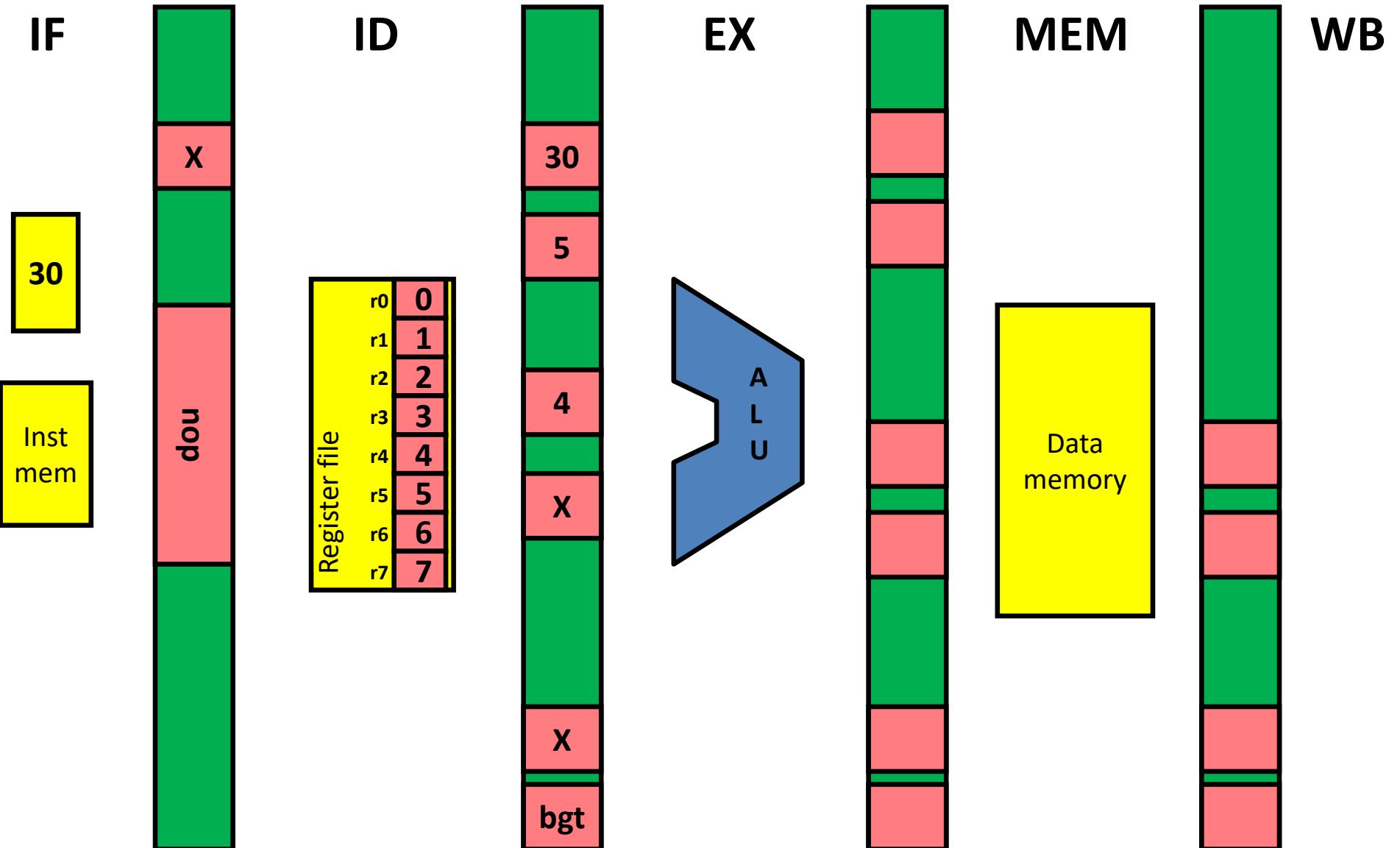


WB

Case 1:
branch is
taken

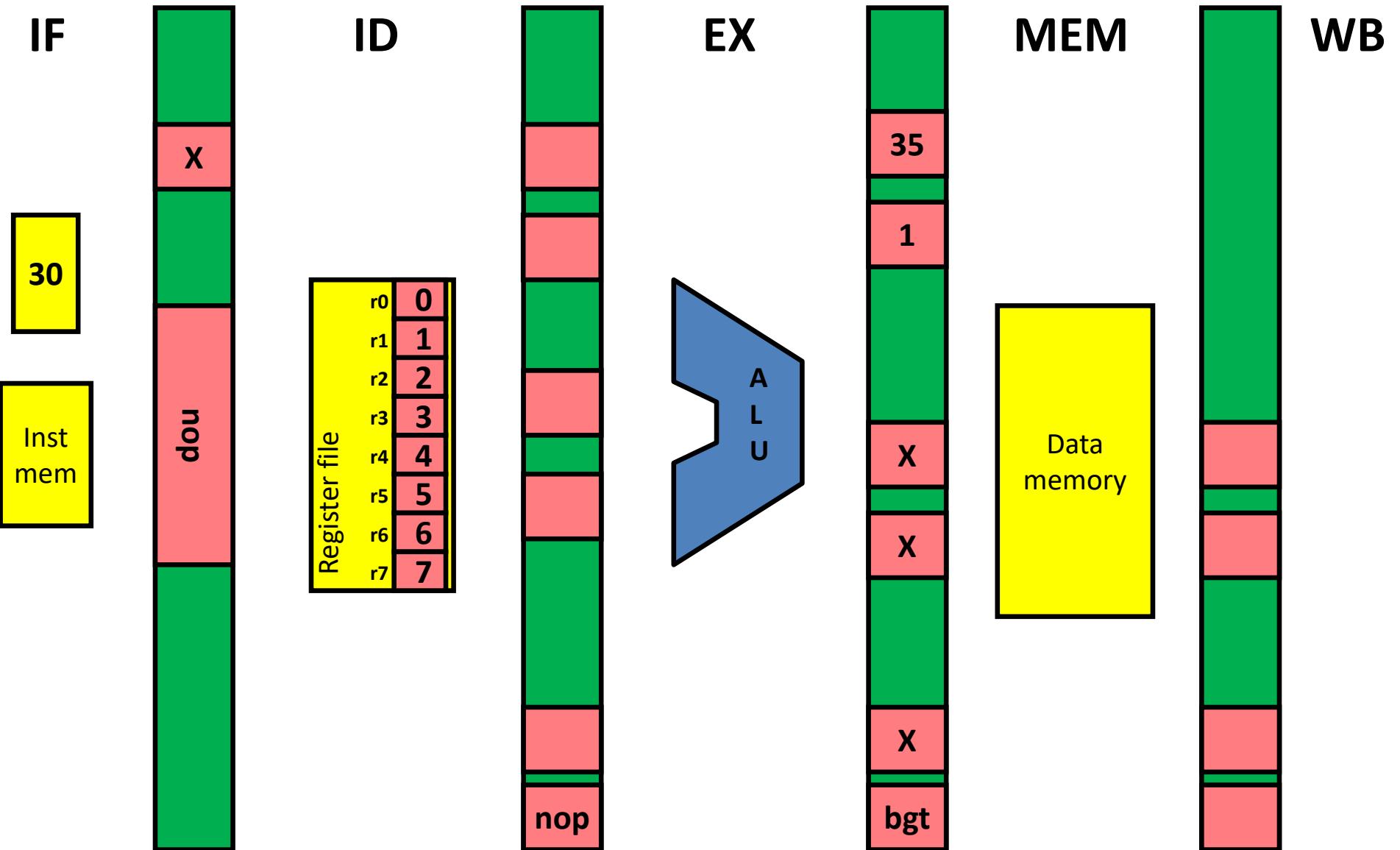
add r1 r2 r3

bgt r4 0x5



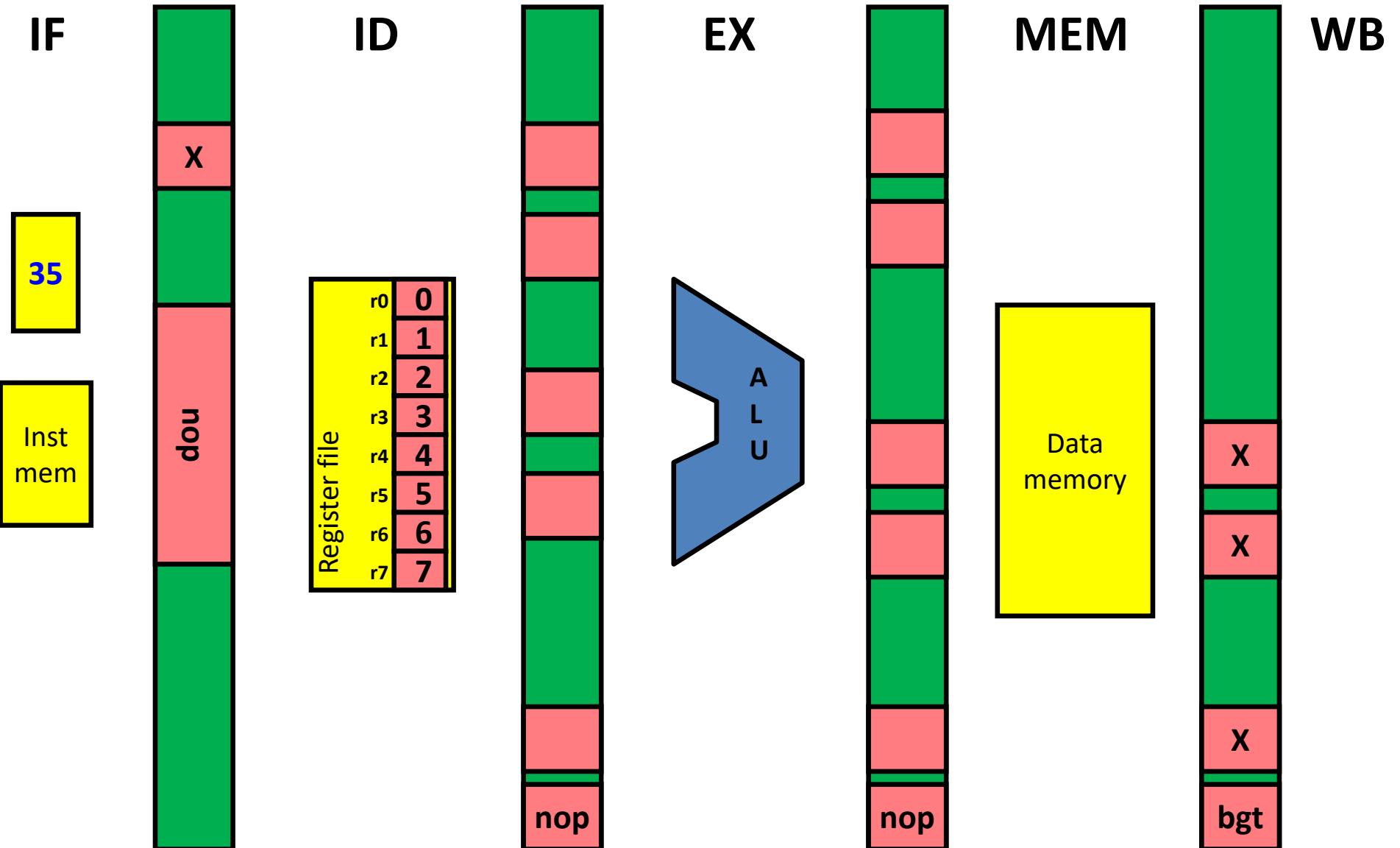
add r1 r2 r3

bgt r4 0x5



add r1 r2 r3

bgt r4 0x5



sw r5 r6 3

bgt r4 0x5

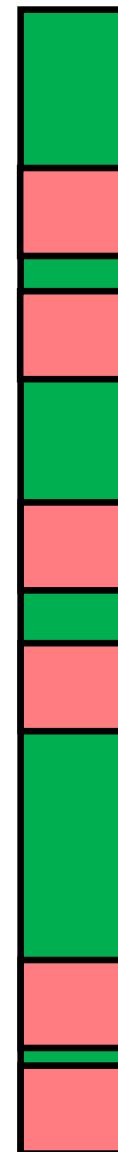
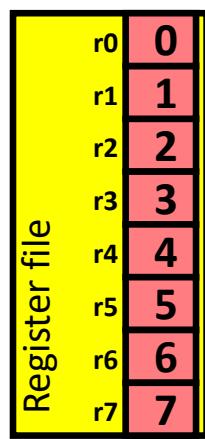
IF

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Inst
mem



ID

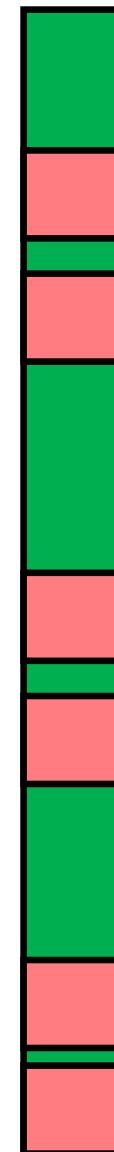


EX



MEM

Data
memory



WB

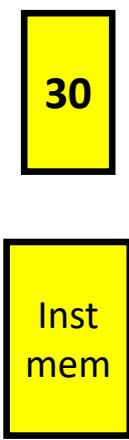


Case 2:
branch is
not taken

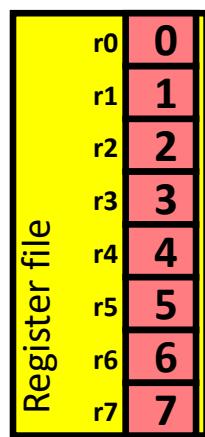
add r1 r2 r3

beq r4 0x5

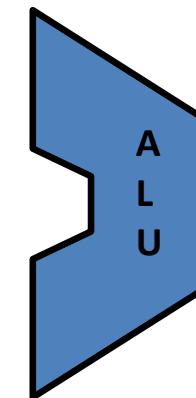
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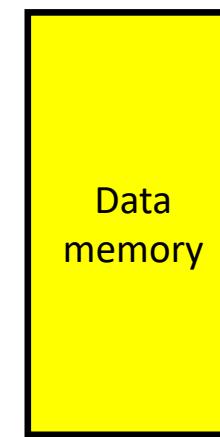
ID



EX



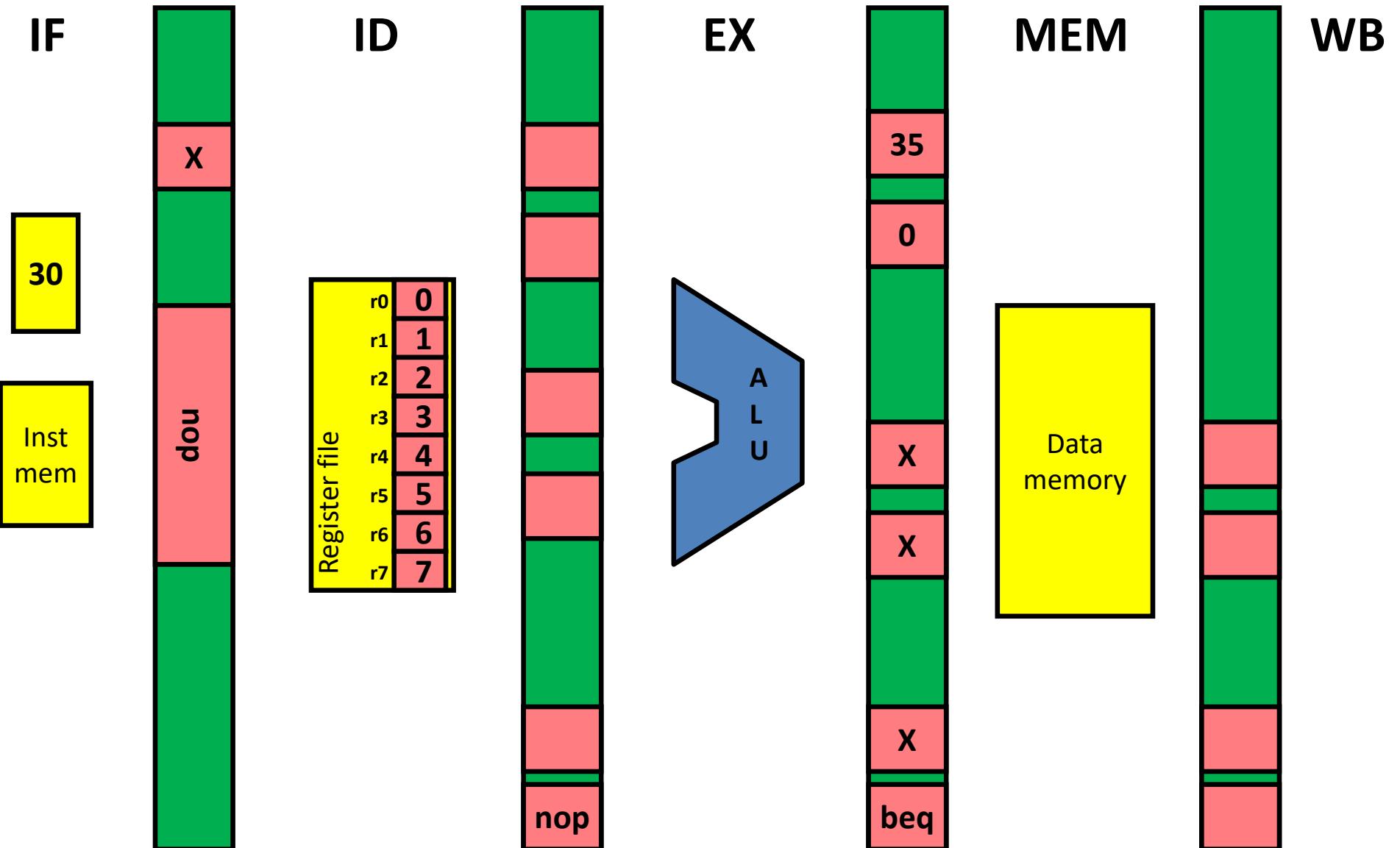
MEM



WB

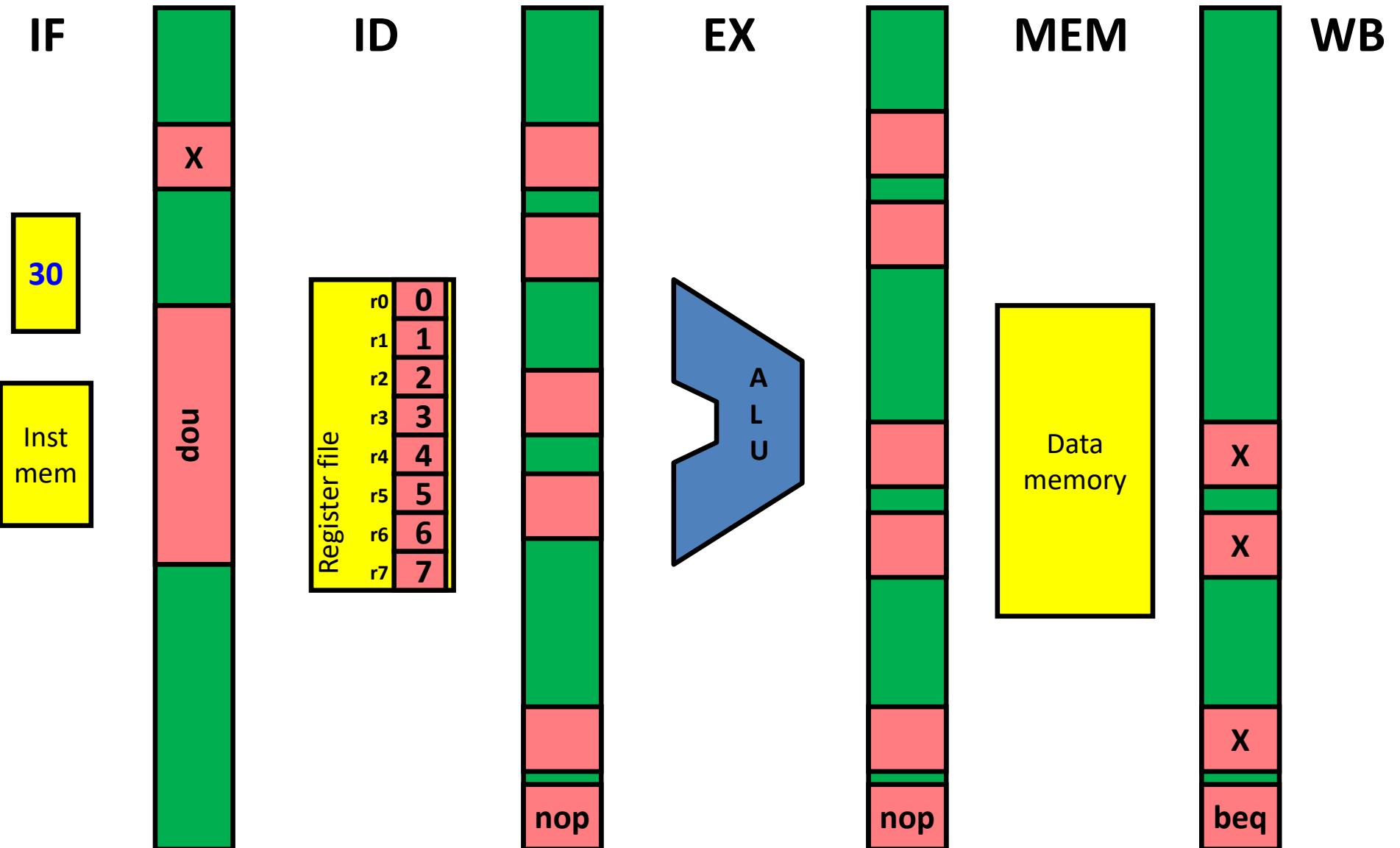
add r1 r2 r3

beq r4 0x5



add r1 r2 r3

beq r4 0x5



add r1 r2 r3

beq r4 0x5