LAB5 Report

B06901160 電機三 翁挺瑋

1. What are the main differences I2C between SMbus (System Management Bus)?

|  |  |
| --- | --- |
| SMBus | I2C |
| Max speed 100kHz | Max speed 400 kHz |
| Min clock speed 10kHz | No minimum clock speed |
| 35ms timeout | No timeout |
| Logic levels are fixed | Logic levels depend on VDD |
| Dynamic address type | General slave address type (7-bit, 10-bit) |
| Different bus protocols | No protocols |

1. What is the I2C address of ADXL 345, if ALT ADDRESS is connected to HIGH?

ADX345 address at 0x53

1. What is the wired-AND logic?

The wired AND connection is a form of AND gate. It uses a pull up resistor and one diode per input to create this function.

1. What are the bus master and the bus slave?

Bus masters are devices on a PCI bus that are allowed to take control of the bus by dominating the clock rate. The slave simply follows the rate.

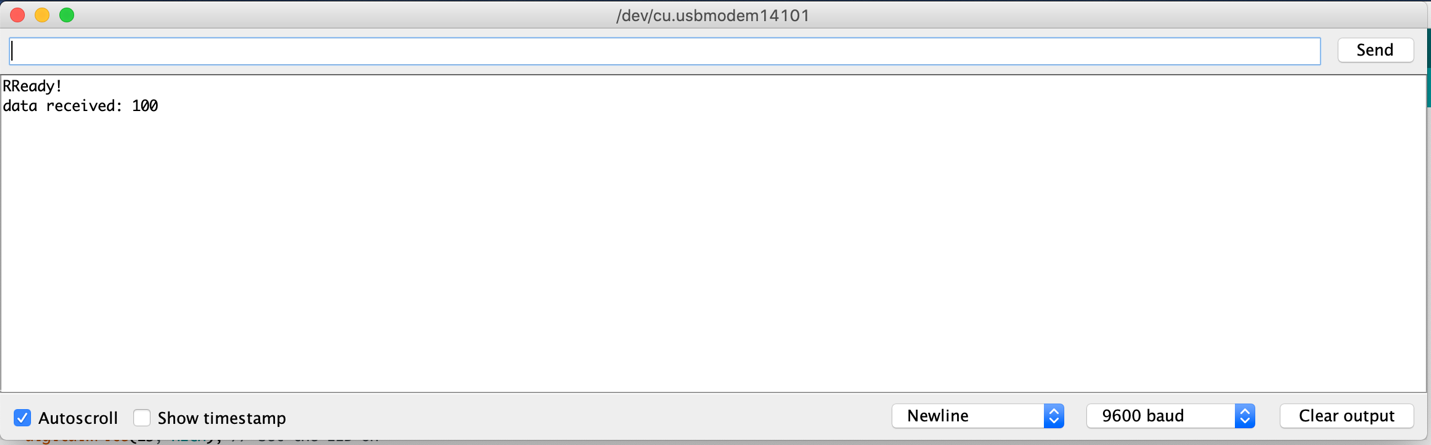
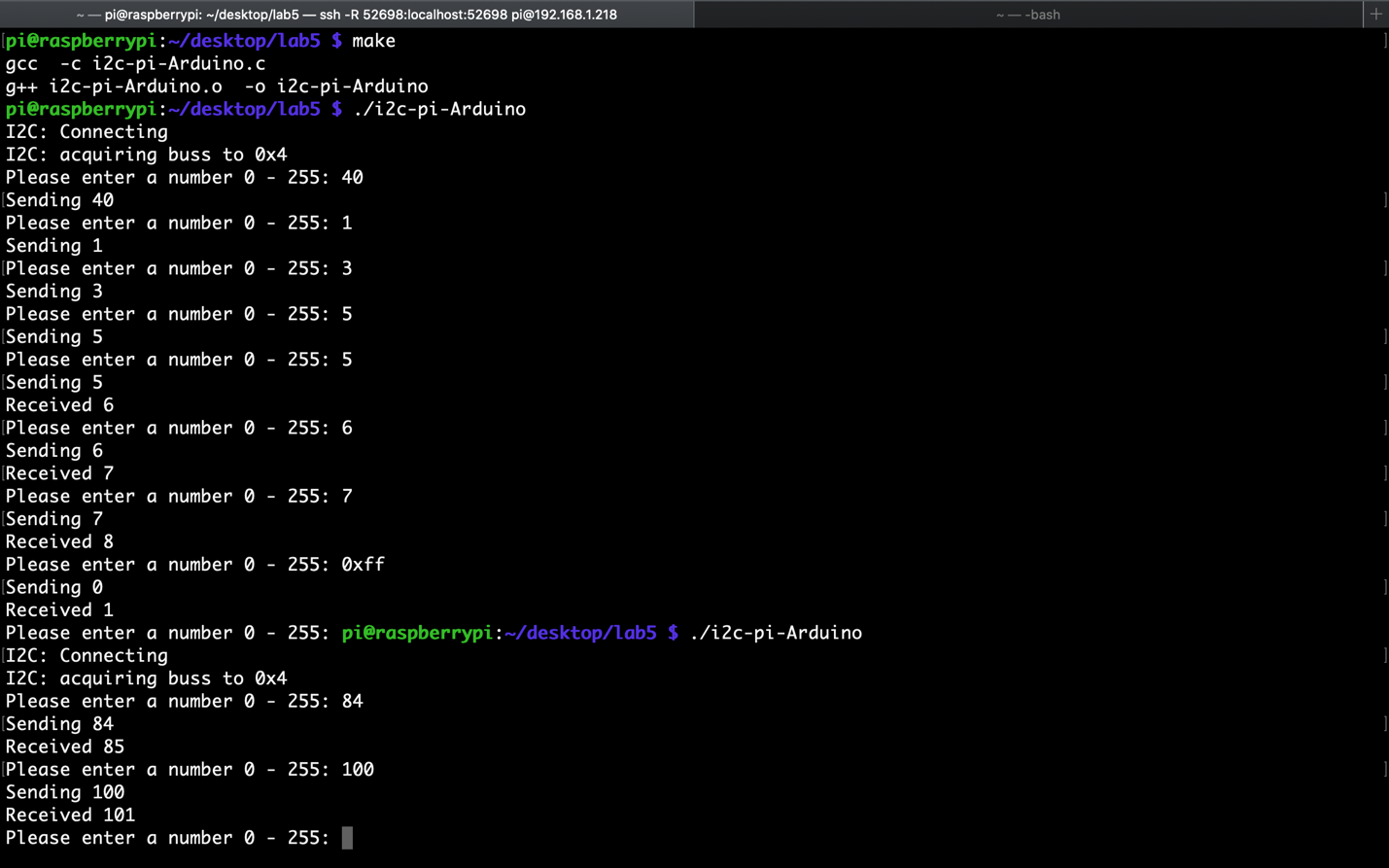
1. How to detect activity/inactivity in ADXL345?

From datasheet of ADXL345

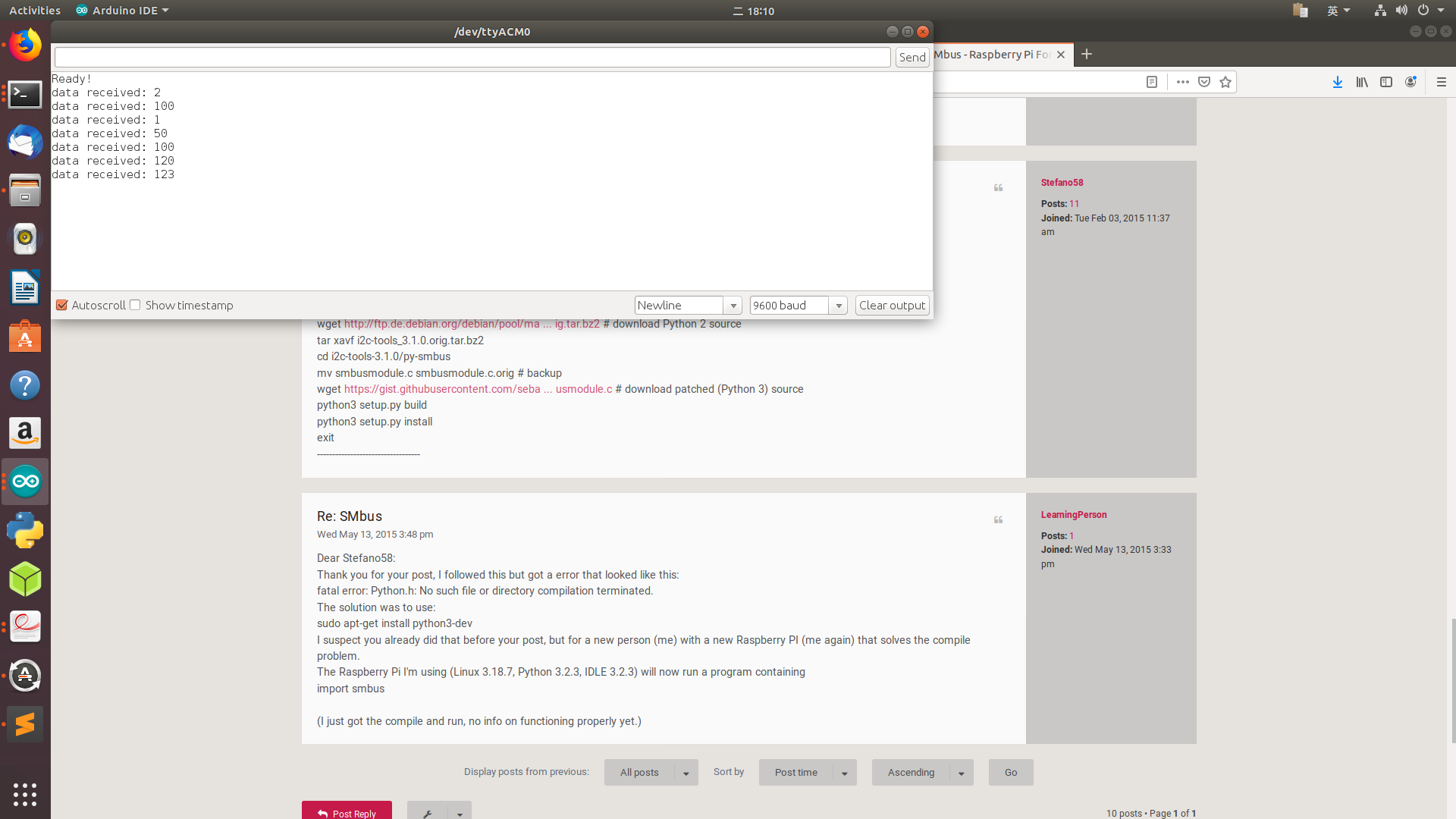
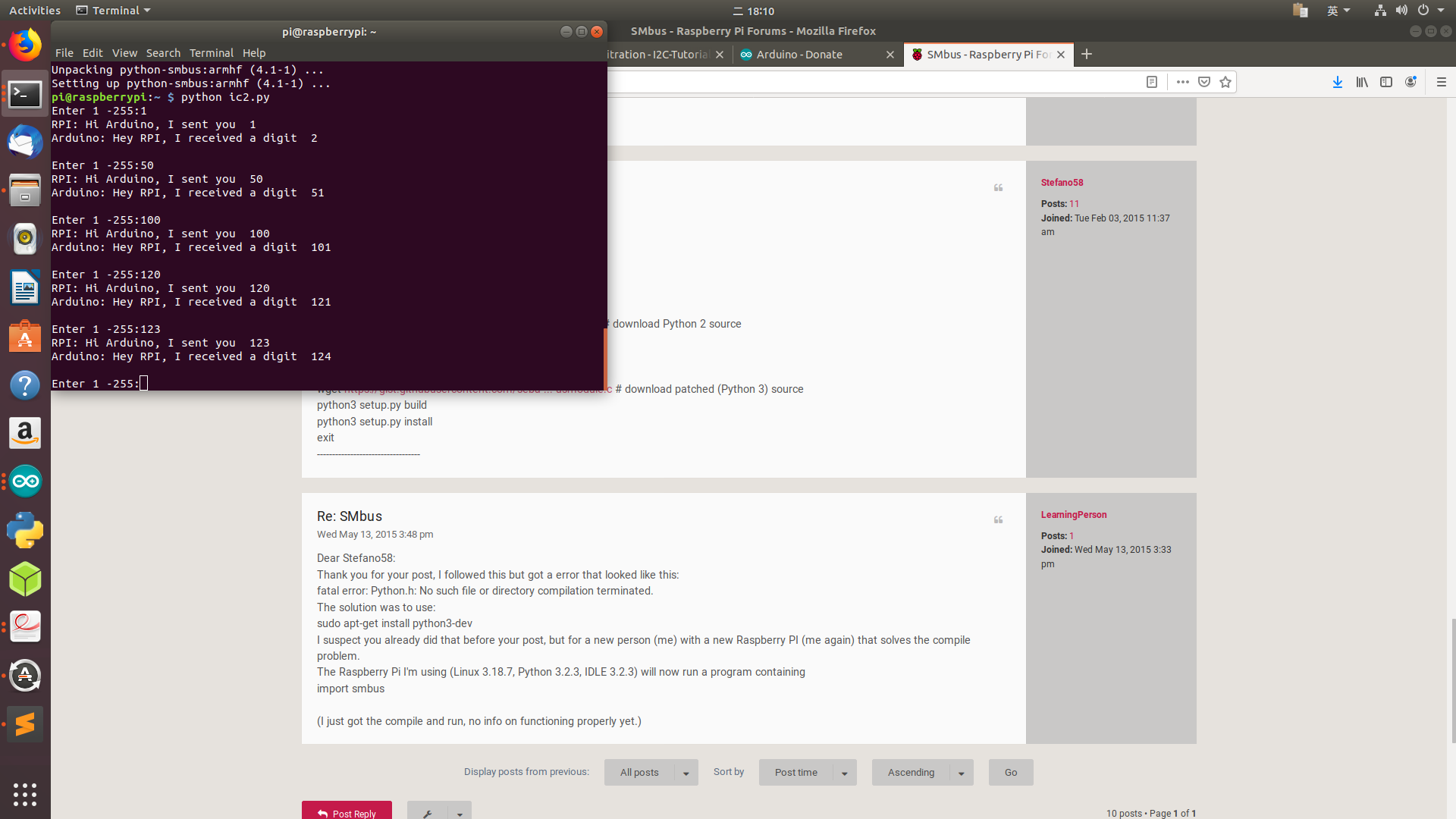
The activity bit is set when acceleration greater than the value stored in the THRESH\_ACT register (Address 0x24) is experienced on any participating axis, set by the ACT\_INACT\_CTL register (Address 0x27).

The inactivity bit is set when acceleration of less than the value stored in the THRESH\_INACT register (Address 0x25) is experienced for more time than is specified in the TIME\_INACT register (Address 0x26) on all participating axes, as set by the ACT\_INACT\_CTL register (Address 0x27). The maximum value for TIME\_INACT is 255 sec.

C FILE



Python File



BONUS File in attachment