Lab Code [5 points]
Filename: chipInterface.sv
AndrewID: xd2

```
`default_nettype none // Required in every sv file
module chipInterface
    (input logic SW [17:0],
    output logic LEDR[17:0]);
    multiplexer DUT (.a(SW[0]),
                     .b(SW[1]),
                     .f(LEDR[15]),
                     .sel(SW[7]));
endmodule: chipInterface
module multiplexer
    (output logic f,
    input logic a, b, sel);
    logic f1, f2, n_sel;
    and #2 g1(f1, a, n_sel),
    g2(f2, b, sel);
    or #2 g3(f, f1, f2);
    not g4(n_sel, sel);
endmodule: multiplexer

    // TODO:
    // - Instantiate your multiplexer module
    // inside this chipInterface
    // - Hook up SW[0], SW[1] and SW[7] to a, b and
    // sel inputs on the mux
    // - Hook up LEDR[15] to the output of your multiplexer
    // - Finish the module (you'll need something else
    // to indicate your module is complete)
```

Lab Code [5 points]
Filename: lab0.sv
AndrewID: xd2

```
1  `default_nettype none // Required in every sv file
2  module multiplexer
3      (output logic f,
4      input logic a, b, sel);
5      logic f1, f2, n_sel;
6      and #2 g1(f1, a, n_sel),
7      g2(f2, b, sel);
8      or #2 g3(f, f1, f2);
9      not g4(n_sel, sel);
10 endmodule: multiplexer
11
12
13
14 module muxTester
15     (output logic a, b, sel,
16     input logic muxOut);
17     initial begin
18         $monitor($time,,
19             "a = %b, b = %b, sel = %b, muxOut = %b",
20             a, b, sel, muxOut);
21             a = 0;
22             b = 0;
23             sel = 0;
24         #10 b = 1;
25         #10 a = 1;
26         #10 b = 0;
27         #10 sel = 1;
28         #10 b = 1;
29         #10 a = 0;
30         #10 b = 0;
31         #10 $finish;
32     end
33 endmodule: muxTester
34
35
36 module system();
37     logic wire_a, wire_b, select, mux_out;
38     multiplexer DUT (.a(wire_a),
39                      .b(wire_b),
40                      .f(mux_out),
41                      .sel(select));
42     muxTester mt (.a(wire_a),
43                   .b(wire_b),
44                   .muxOut(mux_out),
45                   .sel(select));
46 endmodule: system
```