Problem 7: [6 points] Drill problem
Filename: hw1prob7.sv
AndrewID: xd2

```systemverilog
 1 module hw1prob7
 2     (input logic  a,  b,  c,  d,
 3     output logic prime, div3);
 4
 5     logic p2, p3, p5, p7, p11, p13;
 6     logic d0, d3, d6, d9, d12;
 7
 8     assign num1 = b & ~c & d;
 9     assign num2 = ~a & b & d;
10     assign num3 = ~a & ~b & c;
11     assign num4 = ~b & c &  d;
12
13     assign d1 = ~a & ~b & ~c & ~d;
14     assign d2 = ~a & ~b &  c &  d;
15     assign d3 = ~a &  b &  c & ~d;
16     assign d4 =  a & ~b & ~c &  d;
17     assign d5 =  a &  b & ~c & ~d;
18     assign d6 =  a &  b & c & d;
19
20     assign prime = num1 | num2 | num3 | num4;
21     assign div3 = d1 | d2 | d3 | d4 | d5 | d6;
22
23 endmodule : hw1prob7
24
25
26
```

Problem 8: [6 points] Drill problem
Filename: hw1prob8.sv
AndrewID: xd2

```systemverilog
 1  `default_nettype none
 2  module hw1prob7_test;
 3
 4      logic a, b, c, d, prime, div3;
 5
 6      hw1prob7 DUT( .a, .b, .c, .d, .prime, .div3 );
 7
 8      initial begin
 9          $monitor("a=%b, b=%b, c=%b, d=%b, prime=%b, div3=%b",
10                    a, b, c, d, prime, div3);
11
12          for (int i = 0; i < 16; i++) begin
13              {a, b, c, d} = i;
14              #5;
15          end
16
17          #5 $finish;
18      end
19
20  endmodule: hw1prob7_test
21
22
```

Problem 12: [12 points]
AndrewID: xd2

Compilation Errors:

hw1prob12.sv: file does not exist

Problem 12: [12 points]
Filename: hw1prob12.sv
AndrewID: xd2

File hw1prob12.sv was not found