MP4 Progress Report

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**1 Introduction**

This project is mainly about the design of a basic RV32I processor and various improvements we have made on it. This project is an integration of instruction processing (CPU part) and memory access (cache part). To improve the performance of our processor, we enhance the processor from different aspects using the knowledge of computer architecture: splitting CPU into 5-stage and pipelining, solving hazards to avoid stalls, increasing the accuracy of branch prediction, using advanced cache to reduce miss penalty. In Part 2, we will give an overview to the whole design. In part 3, detailed design descriptions are provided to each part of our processor, including designs, testing and performance analysis. Part 4 is a conclusion of the whole project.

**2 Project Overview**

**2.1 Goals and Constraints**

The goal of the project is to make an efficient RV32I processor. Efficient is not only about running test codes in less time, but also less power consumption under the constraint of 100 MHz Fmax. To run test codes in less time, we tried to pipeline the CPU, increase memory hit rate and branch prediction accuracy. To reduce power consumption and Fmax constraint, we minimize the resource utilization and make decisions to strike a balance between different designs. For example, we use a 2-way L1 cache instead of 4-way to avoid long critical path when it is both a L1 and L2 cache miss.

**2.2 Work Distribution**

This project is completely designed and tested by two students from ECE411 as shown in Table 2.2.

|  |  |  |
| --- | --- | --- |
| Functionality | Notes | Work Distribution |
| a 5-stage pipeline CPU which can handle RV32I Instructions | 1. no hazard detection  2. full RV32I Instructions except FENCE\*, ECALL, EBREAK, and CSRR | Zhi: split mp2 CPU into 5 stages, unit test each stage and test the whole CPU with provided tb.  Tingkai: design control\_rom, assign control signals to each stage and connect all stages in datapath. |
| Hazard, static branch prediction | 1. data hazard: forwarding  2. control hazard: static-not-taken branch prediction | Tingkai |
| L1 cache, arbiter | 1. arbiter connected to I-Cache, D-cache and cacheline adaptor  2. no cache coherence | Zhi |
| L2 cache |  | Tingkai |
| 4-way cache | 1. only used in L2 cache | Zhi |
| 2-level Branch predictor |  | Zhi, Tingkai |
| Prefetch | 1. only used in instruction cache | Zhi |

Table 2.2 Work Distribution

**3 Design Description**

**3.1 Overview**

To achieve the goal described in 2.1, we divide the whole project into 3 milestones: (1) basic pipeline, (2) L1 cache and hazards, (3) advanced designs.

**3.2 Milestones**

**3.2.1 Checkpoint 1: RV32I ISA and basic pipelining**

(a) Datapath

Diagram

Description automatically generated

(b) Instruction Analysis

The opcode of basic RV32I ISA instructions includes IMM, REG, LUI, MEM, AUIPC, BR and JAL(R). The Table 3.2.1(b) shows the use of each stage by different types of opcode.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Opcode | IF | ID | EX | MEM | WB | Note |
| IMM | 1 | 1 | 1 | 0 | 1 |  |
| REG | 1 | 1 | 1 | 0 | 1 |  |
| LUI | 1 | 1 | 0 | 0 | 1 | Place u\_imm into register |
| MEM | 1 | 1 | 1 | 1 | 1/0 | Not need to write back for ST |
| AUIPC | 1 | 1 | 1 | 0 | 1 | Add something to PC and place the result into register. |
| BR | 1 | 1 | 1 | 0 | 0 | Conditional branch |
| JAL | 1 | 1 | 1 | 0 | 1 | Unconditional jump. |
| JALR | 1 | 1 | 1 | 0 | 1 | Unconditional jump. |

Table 3.2.1(b) 5-stage utilization of different opcode

(c) Specific Design Description

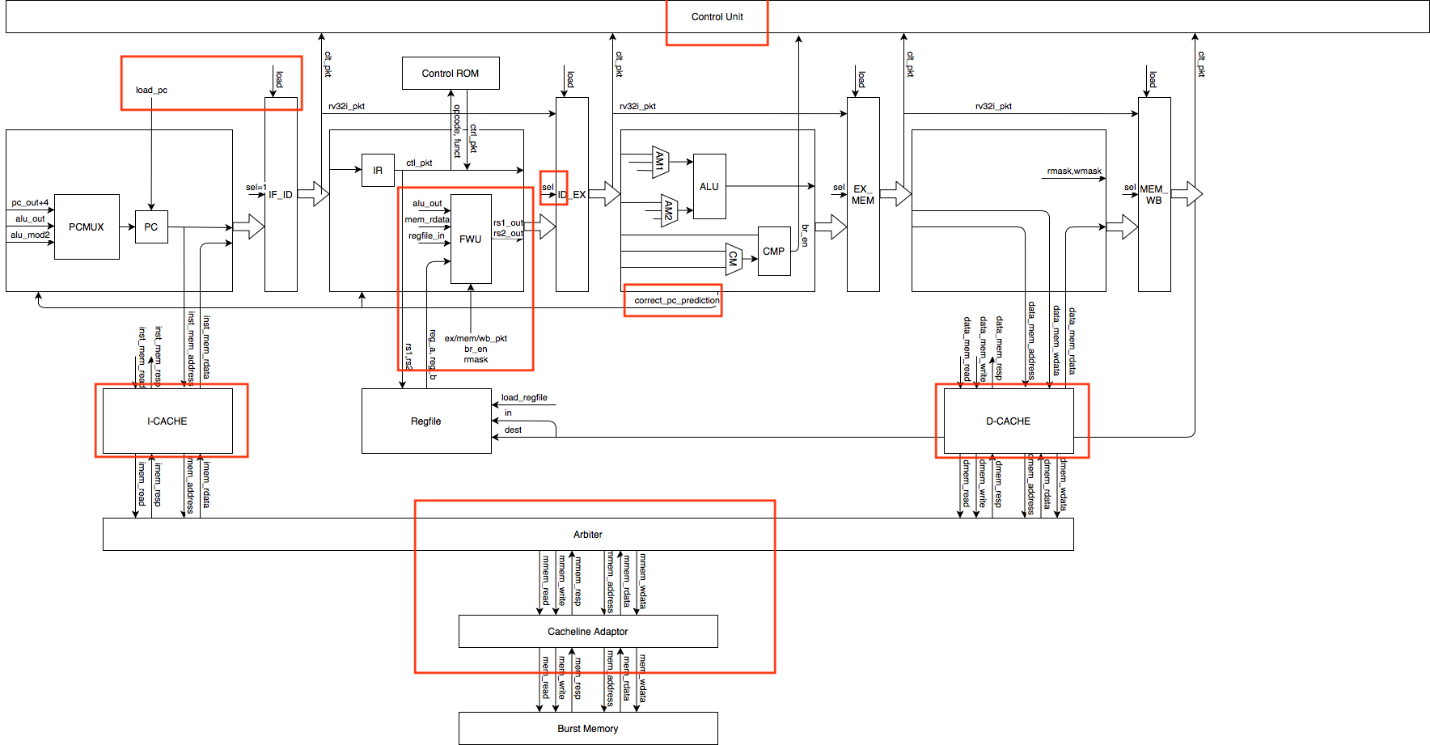
As shown in 3.2.1(a) and 3.2.1(b), we divide a basic processor into 5-stage pipelined processor: IF (fetching instruction), ID (decode), EX (execute), MEM (reading/writing to memory) and WB (write to regfile). To move the pipeline, we wrap the information of each instruction in a packet and pass it down through the pipeline. The packet contains four subsets: valid (indicate if it should be committed), CTRL packet (controls which stages/components are used), INST packet (decode by control rom) and DATA packet (saved data, e.g. pc). There are buffers between the stages to save the former information and signals (load and sel as shown in 3.2.1(a) datapath) to determine if it should be updated or dropped.

(d) Testing

|  |  |
| --- | --- |
| Testing Type | Files |
| Unit test | if\_unit\_test.sv, id\_unit\_test.sv, ex\_unit\_test.sv, wb\_unit\_test.sv |
| Using source code | mp4\_cp1.s |

**3.2.2 Checkpoint 2: L1 caches, hazards and static branch prediction**

(a) Update Datapath



(b) Specific Design Description

(i) Arbiter

Arbiter is connected to data cache and instruction cache. It determines which cache is interacted with memory. Below table shows the state machine design of arbiter.

|  |  |  |  |
| --- | --- | --- | --- |
| State | Description | Next | Output |
| WAIT | Wait until a access request happens from either I-cache or D-cache | If I-cache requests, to I\_MEM.  If D-cache requests, to D\_MEM. I-cache request is check first (Prioritized) | 0 |
| I\_MEM | Access memory according to the signals from I-cache | If mem\_resp, to I\_DONE | Pass signals of I-cache to physical memory |
| I\_DONE | Finish I-cache request, and check whether need to do D-cache request | To WAIT | inst\_mem\_resp = 1 |
| D\_MEM | Access memory according to the signals from D-cache | If mem\_resp, to D\_DONE | Pass signals of D-cache to physical memory |
| I\_DONE | Finish D-cache request, and check whether need to do I-cache request | To WAIT | data\_mem\_resp = 1 |

Table 3.2.2(1) Arbiter state machine design

(ii) Forwarding

At ID stage, when reading the register values, the latest version of register value may not be write-back. As a result, we design the forwarding to be getting the latest value of register at ID stage if necessary, which means instead of connecting forwarded value to EX, MEM, WB, we only forward the value to ID stage and store the forward value in the packet and pass it along the pipeline.

Note that for register dependency happens when the previous instruction is a load instruction, the pipeline need to stall since the next instruction needs the value at EX at the same time MEM is getting the value. The way we solve that is when such cases is detected, the IF, IF\_ID, and ID are stalled by keeping the load to be 0, and an invalid instruction is inserted in ID\_EX and keep ID\_EX, EX, EX\_MEM, MEM, MEM\_WB, WB moving.

(iii) Control Hazard

|  |  |
| --- | --- |
| Opcode | PC |
| BRANCH | PC <- PC + (br\_en? b\_imm : 4) |
| JAL | PC <- PC + j\_imm |
| JALR | PC <- {(rs1\_out + i\_imm) [31:1], 1’b0} |
| Other opcodes | PC <- PC + 4 |

Table 3.2.2(2) PC update table

Mark the mis-fetched instruction to be invalid and stop them from updating memory and registers. Since we are using static no-taken branch prediction, when we see a br/jal/jalr at EX stage calculated the correct branch target which is not pc+4, we will mark the instruction in IF\_ID and ID\_EX to be invalid since they are mis-fetched. After those instructions are marked as invalid, they won’t be able to write to memory or registers.

(c) Testing

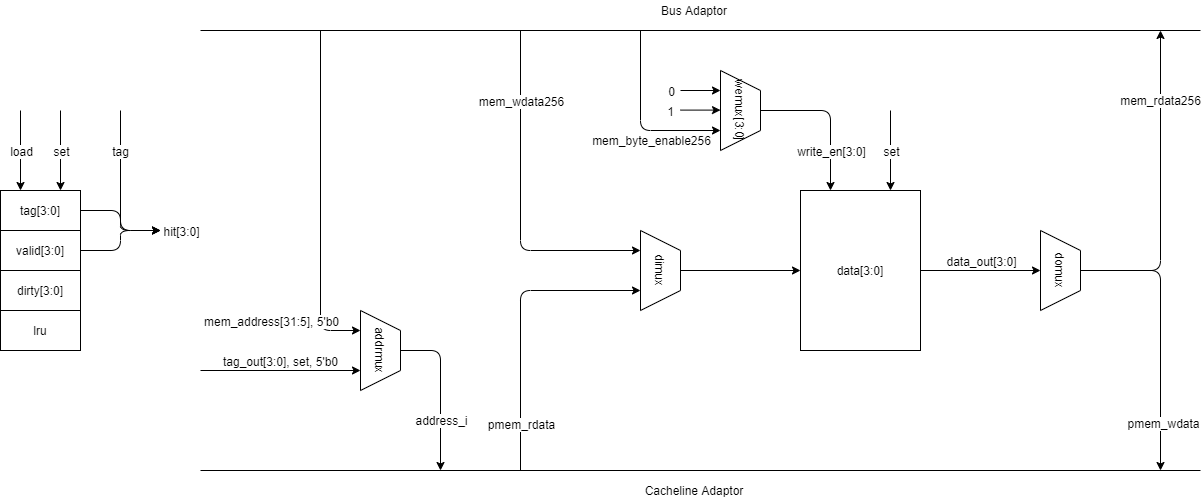
|  |  |
| --- | --- |
| Testing Type | Files |
| Unit test | cache\_unit\_test.sv, arbiter\_unit\_test.sv, cache\_top\_unit\_test.sv |
| Using source code | mp4\_cp2.s, factorial.s, mp4\_cp3.s |

**3.3 Advanced Design Options [11]**

**3.3.1 4-way cache [2]**

(a) Design

(i) Datapath



(ii) Description

After successfully implemented the 2-way cache, by analyzing the performance, we find that it takes (10 + burst delay) cycles for a cache miss without a write back and (19 + 2\*burst delay) for a cache miss with a write back. Thus, it is a great penalty for miss and we can improve the performance by increasing the hit rate by changing the 2-way cache to 4-way cache.

The datapath of the 4-way cache is similar to the 2-way cache, except for the number of ways. As for the control part, we use the pseudo LRU algorithm to determine which way we should replace for a miss. Below are the LRU update table (Table 3.3.1(a)) and LRU replacement table (Table 3.3.1(b)).

|  |  |  |  |
| --- | --- | --- | --- |
| Way hit | L2 | L1 | L0 |
| 1 | x | 0 | 0 |
| 2 | x | 1 | 0 |
| 3 | 0 | x | 1 |
| 4 | 1 | x | 1 |

Table 3.3.1(a) LRU update table

|  |  |  |  |
| --- | --- | --- | --- |
| Way to replace | L2 | L1 | L0 |
| 1 | x | 1 | 1 |
| 2 | x | 0 | 1 |
| 3 | 1 | x | 0 |
| 4 | 0 | x | 0 |

Table 3.3.1(b) LRU replacement table

(b) Testing

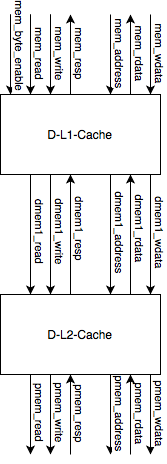
|  |  |
| --- | --- |
| Testing Type | Files |
| Unit test | cache\_unit\_test.sv |
| Using source code | mp4\_cp3.s, comp1.s, comp2.s, comp3.s |

(c) Performance Analysis

**3.3.2 L2 cache [2]**

(a) Design

(i) Datapath



(ii) Description

After finish the 4-way L1 cache, we find that using 4-way L1 cache results in very long critical path. The main reason is that we use combinational logic in array reading in order to response a memory hit in one cycle.

To fix this Fmax problem and further accelerate our compiler, we decide to add a L2 cache. The design of a L2 cache is similar to L1 cache, the only difference is that we don’t need a bus adaptor to covert 32-bit data to a 256-bit cacheline.

(b) Testing

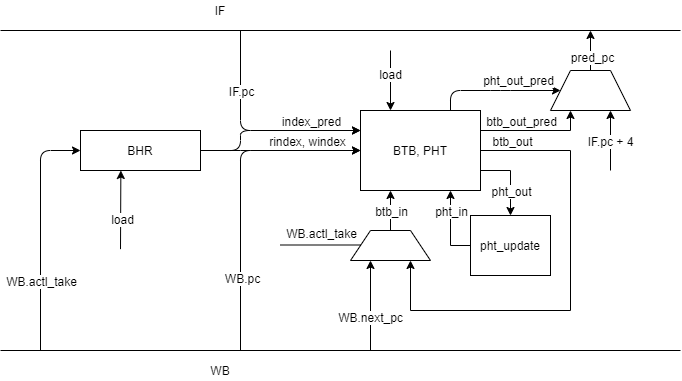
|  |  |
| --- | --- |
| Testing Type | Files |
| Unit test | cache\_unit\_test.sv |
| Using source code | mp4\_cp3.s, comp1.s, comp2.s, comp3.s |

(c) Performance Analysis

**3.3.3 Global 2-level branch predictor [3]**

(a) Design

(i) Datapath



(ii) Description

A wrong branch prediction will cause stalls or waste cycles. Therefore, if we can predict the next pc with higher accuracy, we can save cycles and promote the performance.

A local branch history table use (PC xor BHR) as index to BTB and PHT.

(b) Testing

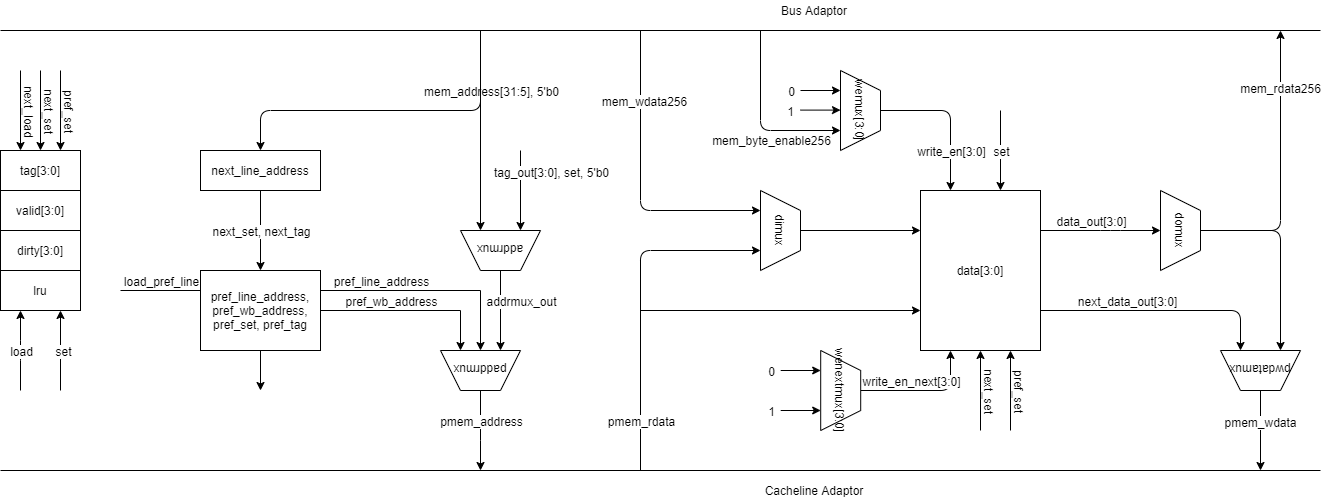
|  |  |
| --- | --- |
| Testing Type | Files |
| Unit test | bp\_unit\_test.sv |
| Using source code | mp4\_cp3.s, comp1.s, comp2.s, comp3.s |

(c) Performance Analysis

**3.3.4 Basic hardware prefetch [4]**

(a) Design

(i) Datapath



(ii) Description

We only use prefetch in instruction cache, because most instructions are sequence accessed. If cacheline k is accessed and it is a hit, but cacheline k+1 is a miss, then the cache will request a read of cacheline k+1.Below table shows the state transition.

|  |  |  |
| --- | --- | --- |
| State | Description | Next |
| HIT CHECK | Serves curr\_line hit and deals with misses. | if curr\_line miss, to WRITE BACK/READ BACK.  if curr\_line hit but next\_line miss, to PREFETCH WB/RB.  if curr\_line hit and next\_line hit, to HIT CHECK. |
| WRITE BACK | Writes the dirty cacheline back to memory. | if (pmem\_resp), to READ BACK |
| READ BACK | Reads curr\_line back to cache. | if (pmem\_resp), to HIT CHECK |
| PREFETCH WB | Writes the dirty cacheline back to memory.  Serves curr\_line hit. | if (pmem\_resp), to PREFETCH RB |
| PREFETCH RB | Reads next\_line back to cache.  Serves curr\_line hit. | if (pmem\_resp), to HIT CHECK |

Table 3.3.4 State machine of prefetch

(b) Testing

|  |  |
| --- | --- |
| Testing Type | Files |
| Using source code | mp4\_cp3.s |

(c) Performance Analysis

Prefetch can only pass mp4\_cp3.s. Since most instructions are cached in L2 and L1 I-cache, it does not accelerate the whole design distinctly.

**4 Additional Observations**

Our group has tried to implement Tomasulo Algorithm but failed.

**5 Conclusion**

In conclusion, this project successfully designs a 5-stage pipelined RV32I processor and improves its performance by using 4-way L2 cache, branch predictor and prefetch method.