**Simulink Design Verifier Demo for Wind Turbine Main Controller**

Generate cumulative coverage data:

1. Open ControlLogic\_Testrig.slx
2. Open Signal Builder Block
3. “Run All” Test Cases (3)
4. Save workspace coverage data through the command:   
   >> cvsave('cvdata\_ControlLogic\_Testrig', cvdata\_ControlLogic\_Testrig)

Find missing test cases:

1. Open ControlLogic\_Ports.slx
2. Analysis -> Design Verifier -> Options -> Select the “Test generation” Mode
3. Analysis -> Design Verifier -> Generate Tests -> Model
4. Highlight analysis results on model and generate test harnesses for missing test cases that will provide 100% model coverage

Find dead logic:

1. Open ControlLogic\_Ports.slx
2. Analysis -> Design Verifier -> Options -> Select the “Design error detection” Mode
3. Navigate to Design Error Detection Properties (on left) -> Check “Dead Logic”
4. Analysis -> Design Verifier -> Detect Design Errors -> Model

Find integer overflows or divide-by-zeros:

1. Open ControlLogic\_Ports.slx
2. Analysis -> Design Verifier -> Options -> Select the “Design error detection” Mode
3. Navigate to Design Error Detection Properties (on left) -> Check “Division overflow” and “Divide by zero”
4. Analysis -> Design Verifier -> Detect Design Errors -> Model